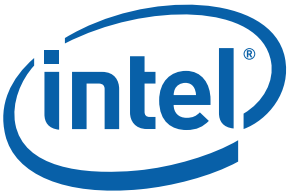
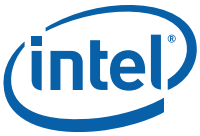


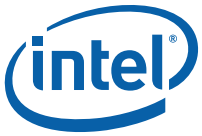
Intel® Pentium® M Processor on 90 nm process with Intel® E7520 Chipset Development Kit

User's Manual

March 2007

Order Number: 308475-002US





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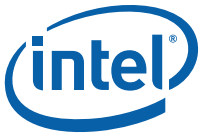


Revision History

Date	Revision	Description
March 2007	002	Updated safety information in Section 3.0, Section 4.1, and Section 4.3.1. Updated power supply requirements in Section 1.2 and Table 5.
July 2005	001	Initial public release of this document

1.0 Overview

The Intel® Pentium® M Processor on 90 nm process with Intel® E7520 Chipset Development Kit consists of an IA-32 Intel® Architecture-based processor platform, which serves as a reference for OEM development platforms. This and other Development Kits from Intel provide a fully working product with a range of performance options that can be modified or used immediately for product development.

1.1 Related Documents

Contact an Intel Sales Representative for access to the following documents.

Table 1. Related Documents

Title
Intel® Pentium® M/Intel® Celeron® M Processor based on 90 nm process technology and Intel® E7520/E7320 Chipset Platform Design Guide
Intel® Pentium® M/Intel® Celeron® M Processor based on 90 nm process technology and Intel® E7520/E7320 Chipset Platform (DDR2-400) Customer Reference Board (CRB) PDF Schematics
Intel® Pentium® M/Intel® Celeron® M Processor based on 90 nm process technology and Intel® E7520/E7320 Chipset Platform (DDR2-400) Customer Reference Board (CRB) Board File
Intel® Pentium® M / Celeron® M (90 nm)
Intel® Pentium® M/Celeron® M on 90 nm Process and E7520/E7320 Chipset Platform Design Guide
Intel® Pentium® M Processor on 90 nm Process with 2 MByte L2 Cache Datasheet
Intel® Pentium® M Processor on 90 nm Process with 2 MByte L2 Cache Specification Update
Intel® Pentium® M Processor on 90 nm Process with 2 MByte L2 Cache for Embedded Applications Thermal Design Guide
Intel® Pentium® M Processor and Intel® Celeron® M Processor for Embedded Applications Thermal Design Guide
RS - Intel® Pentium® M Processor on 90 nm Process with 2 MByte L2 Cache Electrical, Mechanical, and Thermal Spec (EMTS)
RS - Intel® Celeron® M Processor on 90 nm Process Electrical, Mechanical, and Thermal Specification (EMTS)
RS - Intel® Pentium® M Processor 2 MByte L2 Cache and 533 MHz FSB Electrical, Mechanical, & Thermal Specification (EMTS)
Dothan Processor with 400 MHz FSB Thermal Design Power (TDP) Application Study and Power Definitions
Intel® E7520 MCH
Intel® E7520 Memory Controller Hub (MCH) Datasheet
Intel® E7520 Memory Controller Hub (MCH) Spec Update
Intel® E7520 Memory Controller Hub (MCH) External Design Specification (EDS)
Intel® E7520/E7320/E7525 Chipset Memory Controller Hub (MCH) Thermal/Mechanical Design Guidelines
Intel® E7520 and Intel® E7320 MCH Embedded EDS Addendum
eXtended Debug Port: Debug Port Design Guide for Lindenhurst Chipset Platforms
Intel® E7520 Chipset Memory Controller Hub (MCH) and Intel® 6700PXH 64-Bit PCI Hub Thermal Design Guide

1.2 Development Kit Contents

Visually inspect the board and ensure that the Memory Controller Hub (MCH), I/O Controller Hub (ICH), and other components mounted on the board did not shake loose during shipment. If the board has any loose or missing components, contact an Intel representative.

The following hardware is included in the Development Kit:

- One Intel® Pentium® M 760 Processor
- Two sticks of 512 MByte 400MHz DDR2 ECC DIMM
- CPU, Intel® E7520 MCH and Intel® 6700PXH Thermal Solution
- Intel® E7520 and Intel® 6300ESB Chipset mounted on the board
- FWH is also mounted in the socket and flashed with the BIOS
- Cable kit
- 2.5 inch SATA hard drive
- Matrox* G55-MDDE32F video card
- Sparkle Power, Inc. power supply (FSP460-60GLC P)
- Intel Ethernet NIC (EXPI9402PTG2P20PAK1)
- Drivers CD-ROM

1.3 Development Kit Feature List

Table 2 describes the supported processor and chipset pairing.

Table 2. Supported Processor and Chipset Pairing

Processor Brand	Processor Number	Chipset Pairing	Process	Processor Speed	Front Side Bus	Cache
Intel® Pentium® M Processor	760	Intel® E7520	90 nm	2.0GHz	533 MHz	2 MByte L2
	745	Intel® E7520		1.8GHz	400 MHz	2 MByte L2
Intel® Pentium® M Processor Low Voltage	738	Intel® E7520		1.4GHz	400 MHz	2 MByte L2
Intel® Celeron® M Processor	370	Intel® E7520		1.5Ghz	400 MHz	1 MByte L2
Intel® Celeron® M Processor Ultra Low Voltage	373	Intel® E7520		1.0 GHz	400 MHz	512 KB L2

Note: Only the Intel® Pentium® M 760 Processor will be included in the Development Kit.

- Processor Support
  - — On-board processor voltage regulators compatible with RS – IMVP-IV Mobile Processor and Mobile Chipset Voltage Regulation Specification
- Clocking
  - — CK409B clock synthesizer generates all host clock and PCI Express* interface clock for the MCH PHY layer
  - — DB800 generates the PCI Express differential pair clocks to the onboard PCI Express components and dedicated PCI Express slots

- Memory Support
  - — Support for direct connect of two DDR channel interfaces, DDR2-400 technology
  - — Full operational support in single channel mode on either channel interface. Lock-step support only for dual channel operation (logically shared address, independent data).
  - — 144-bit wide with ECC, DDR2-400 memory interface supports x72, ECC, registered DDR2-400 DIMMs (using 256 MByte, 512 MByte, and 1 GByte). Stacked or unstacked DIMM support for registered DDR2-400 technology (up to four single-ranked or two stacked DIMMs per channel).
  - — Support for base DDR clock rates of 200 MHz
  - — Data interface double-pumped to 400 MHz
  - — Data bandwidth per channel of 3.2 GByte/s (DDR2-400)
- I/O Slot Support
  - — One PCI Express x8 slot
  - — One PCI Express x4 slot
  - — One PCI-X 133 MHz slot from PXH
  - — Two PCI-X 100 MHz slot from PXH
  - — Upstream hub interface for access to the MCH
- SATA support
  - — Two-port Serial ATA controller
- IDE support
  - — Two-channel Ultra ATA/100 Bus Master IDE controller
- USB support
  - — One EHCI USB 2.0 host controller and two UHCI USB 1.1 host controllers (expected capabilities for four ports)
- I/O APIC
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC'97 2.2 interface
- PCI-X 1.0 interface
- PCI 2.2 interface
- Two serial I/O ports
- Two-stage watchdog timer
- Back panel I/O
- Two RS232 serial ports from the Intel® 6300ESB ICH
- Two PS/2 connectors for mouse and keyboard
- On-board VGA video ATI Rage Mobility* video controller
- Parallel port
- Miscellaneous (Analog Devices* ADM1023 for system voltages, thermal, and fan speed monitoring and management)

Refer to Table 2 for complete features of the Evaluation Board.

1.4 Block Diagram

Figure 1. Evaluation Board Block Diagram

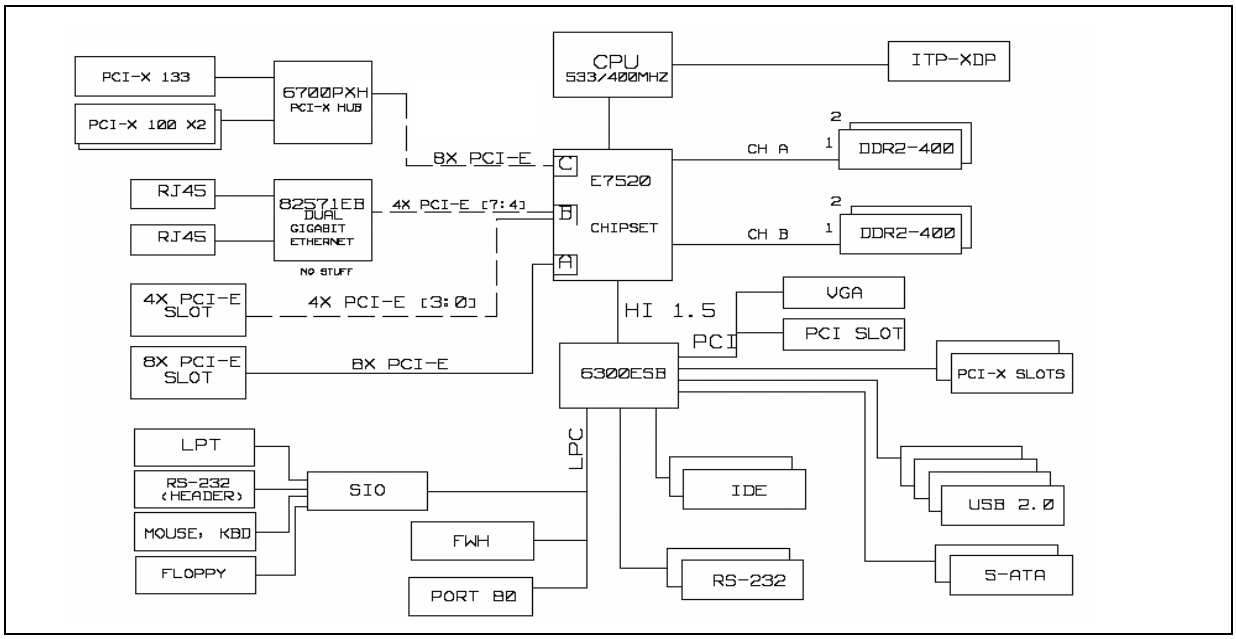
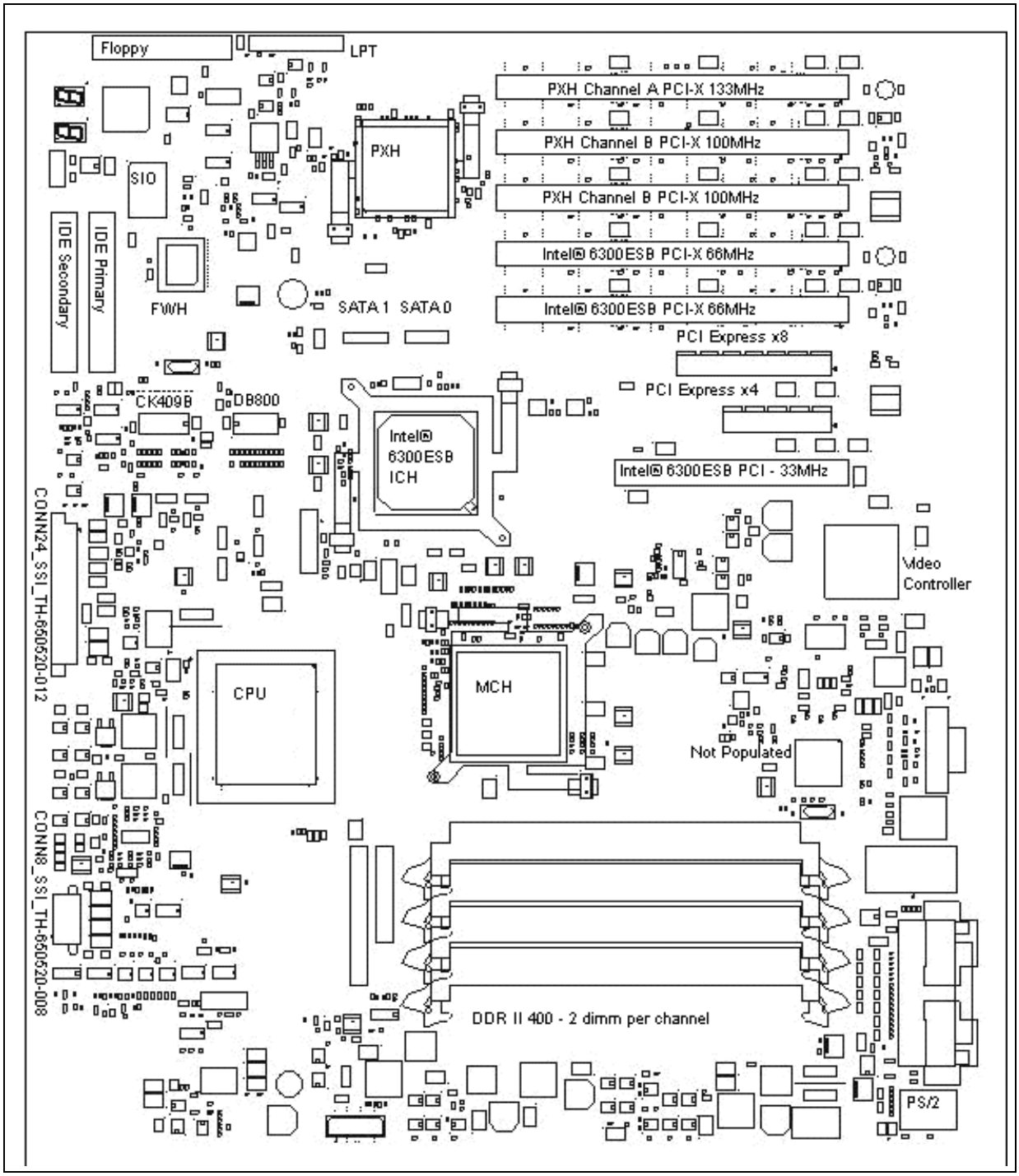
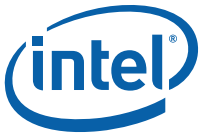


Figure 2. Evaluation Board Placement – Top View





1.4.1 Memory Subsystem

The memory subsystem is designed to support Double Data Rate 2 (DDR2) Synchronous Dynamic Random Access Memory (SDRAM) using the E7520 MCH. The MCH provides two independent DDR channels, which support DDR2-400 DIMMs. The peak bandwidth of each DDR2 branch channel is 3.2 GByte/s (8 bytes x 400 MT/s) with DDR2-400. The two DDR2 channels from the MCH operate in lock step; the effective overall peak bandwidth of the DDR2 memory subsystem is 6.4 GByte/s for DDR2-400. The Evaluation Board supports a maximum of 4 GBytes memory.

Table 3 shows all DIMM technology supported by the Evaluation Board. Other DIMM types are not supported.

Table 3. Supported DIMM Module Types

Technology	Organization	SDRAM Chips/DIMM
256 Mbit	8 MBytes x 8 x 4 banks	8
	16 MBytes x 4 x 4 banks	16
512 Mbit	16 MBytes x 8 x 4 banks	8
	32 MBytes x 4 x 4 banks	16
1 Gbit	32 MBytes x 8 x 4 banks	8
	64 MBytes x 4 x 4 banks	16

1.4.2 DIMM Placement DDR2-400

Table 4. DIMM Placement DDR2-400

DIMM Configuration	DIMM1	DIMM2
1 Single Rank	Empty	Single Rank
1 Dual Rank	Empty	Dual Rank
2 Single Rank	Single Rank	Single Rank
1 Dual Rank, 1 Single Rank	Single Rank	Dual Rank
2 Dual Rank	Dual Rank	Dual Rank

Notes:
1. Populate DIMMs starting with the sockets farthest away from the MCH (DIMM slots A2 and B2).
2. When populating both channels, always place identical DIMMs in sockets that have the same position on channel A and channel B (i.e., DIMM A2 should be identical to DIMM B2).

1.5 Memory Population Rules and Configurations

The system supports two DDR2-400 DIMM slots for Channel A and two DDR2-400 DIMM slots for Channel B. The four slots are interleaved and placed in a row in the following order: A1, B1, A2, B2, with A1 being closest to the MCH. This design supports only registered ECC-enabled DIMMs.

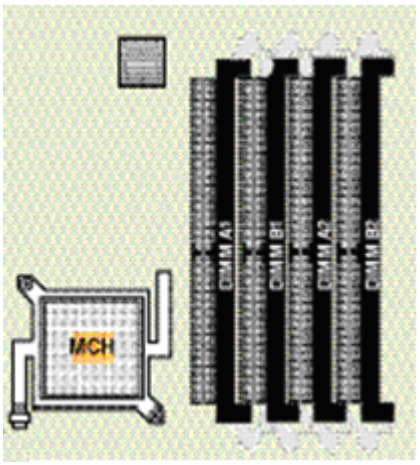
Note: Ensure that the same speed DIMMs are plugged into all slots.

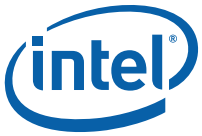
- When populating both channels, always place identical DIMMs in sockets that have the same position on Channel A and Channel B (i.e., DIMM A2 should be identical to DIMM B2).
- In addition, single-rank DIMMs should be populated farthest away from the MCH when a combination of single-rank and double-rank DIMMs are used. This

recommendation is based on the signal integrity requirements of the DDR2 interface.

- Populate DIMMs starting with the sockets farthest away from the MCH (slots A4 and B4).
- When populating two single ranked and one dual ranked DIMMs (per channel), place single ranked DIMMs in sockets A2, A3, B2, B3 and dual ranked DIMMs in sockets A4 and B4.
- When populating one single ranked and one dual ranked DIMMs (per channel), place single ranked DIMMs in sockets A3 and B3 and dual ranked DIMMs in sockets A4 and B4.
- When populating two dual ranked DIMMs (per channel), place the DIMMs in sockets A3, A4, B3, and B4.
- When populating one dual ranked DIMM (per channel), place the DIMMs in sockets A4 and B4.

Figure 3. DDR2-400 Memory – DIMM Ordering





2.0 Platform Management

The following sections describe how the system power management operates and how the different ACPI states are implemented. Platform management involves:

- ACPI implementation specific details.
- System monitoring, control, and response to thermal, voltage, and intrusion events.
- BIOS security.

2.1 Power Button

The system power button is connected to the I/O controller component. When the button is pressed, the I/O controller receives the signal and transitions the system to the proper sleep state as determined by the operating system and software. If the power button is pressed and held for four seconds, the system powers off (S5 state). This feature is called power button override and is particularly helpful in case of system hang and system lock.

2.2 Sleep States Supported

The I/O controller controls the system sleep states. States S1, S3, S4, and S5 are supported. The platform enters sleep states in response to BIOS, operating system, or user actions. Normally the operating system determines which sleep state to transition into. However, a four-second power button override event places the system immediately into S5. When transitioning into a software-invoked sleep state, the I/O controller attempts to gracefully put the system to sleep by first going into the processor C2 state.

2.2.1 S1 State

The S1 sleep state is a low wake latency sleep state. In this state, no system context is lost (CPU or chipset) and hardware maintains all system context. This state is entered via a processor Sleep signal from the ICH (processor C3 state). The system remains fully powered with memory contents intact but no instructions are executed.

2.2.2 S2 State

This state is not supported.

2.2.3 S3 State

The S3 sleep state is a low wake latency sleep state where all system context is lost except system memory. CPU, cache, and chipset context is lost. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor's reset vector after the wake event.

This state is also called Suspend to RAM (STR). Memory is retained, and refreshes continue. All clocks stop except the RTC. S3 is entered when the ICH asserts the SLP_S3# signal to downstream circuitry to control 1.8 V power plane switching. Power must be switched from the normal 1.8 V rail to standby 1.8 V, because the 12V 460 W power supply does not directly supply a standby 1.8 V rail. At time of publication, the Linux kernel 2.4.x series does not support S3 state.

2.2.4 S4 State

The S4 sleep state is the lowest power, longest wake latency sleep state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is maintained. This state is also called Suspend to Disk. Memory contents are written to hard disk before power down. During S4 wake up, the system must power up and fully boot. Boot time to an application is reduced because the platform is returned to the same system state as when the preceding power off occurred.

2.2.5 S5 State

The S5 state is similar to the S4 state except that the OS does not save any context. The system is in the “soft” off state and requires a complete boot when it wakes. Software uses a different state value to distinguish between the S5 state and the S4 state to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

This state is the normal off state whether entered through the power button or soft off. The system remains in the S5 state only while the power supply is plugged into the electrical outlet. If the power supply is unplugged, this is considered a mechanical off or G3.

2.2.6 Wake-up Events

The types of wake-up events and wake-up latencies are related to the actual power rails available to the system in a particular sleep state, as well as to the location in which the system context is stored. Regardless of the sleep state, Wake on the Power Button is always supported except in a mechanical off situation. When in a sleep state, the system complies with the PCI specification by supplying the optional 3.3 V standby voltage to each PCI slot as well as the PME# signal. This enables any compliant PCI card to wake up the system from supported sleep states (except mechanical off).

Note: Wake on USB, Wake on PS/2, and Wake on LAN are not supported.

2.2.7 Wake-up from S1 Sleep State

During S1, the system is fully powered, permitting support for PCI Express Wake and Wake on PCI PME#.

2.2.8 Wake-up from S4 and S5 States

The power button is used to wake from S4 and S5.

2.3 PCI PM Support

This design holds the system reset signal low when in a sleep state. The system supports the PCI PME# signal and provides 3.3 V standby to the PCI and PCI Express slots. This support allows any compliant PCI or PCI Express card to wake up the system

from any sleep state except mechanical off. The user and the operating system must configure the system carefully following the PCI power management interface specification because of the limited amount of power available on 3.3 V standby.

2.4 Platform Management

The ADM1023 monitors the majority of the system voltages. The VID signals from the processor is also monitored by the ADM1023. All voltage levels can be read via the SMBus.

2.5 Processor Thermal Management

The Processor Thermal Management solution contains the following features:

- Monitor CPU temperature

  The Pentium M processor has a thermal diode connected to pins ThermDA and ThermDC. The ADM1023 will use its A/D converter to determine the CPU temperature. When the CPU temperature reaches its threshold, the System Management will react accordingly to lower the overall system temperature.

- Adjust CPU temperature

  The fan can be off or running on 12 V. The fan will spin at maximum speed. The speed is set by BIOS. If the system gets too hot, an alert will be sent to the system management controller. The administrator may then want to turn the system off but keep the fan running to cool the system faster.

- Power failure

  Monitor Power Good to detect power subsystem failure.

- System reset

  The reset button on the front panel can be routed to monitor and control reset to prevent reset from occurring. This can be used for remote management to reset the system.

- Monitor CPU events

  System Management monitors the processor's THERMTRIP#, PROCHOT#, IERR#, VID [5:0], and other signals and takes appropriate actions, which may include logging the event, sending a warning to the administrator, and if necessary shutting the system down.

2.6 System Fan Operation

The system uses the ADM1023 to monitor the temperature. The fan headers are the standard 12V, three-pin type, which includes power, ground, and tachometer. All fan tachometer data can be extracted from the controllers via the SM Bus. The fan control function is not activated for the Evaluation Board and the fan will be switched on all the time at maximum speed.

3.0 Additional Hardware and Software Required

This section describes the additional hardware and software required by the Evaluation Board which may not be included in the development kit unless its inclusion is specifically mentioned.

Warning: Do not install the power supply until all other installation steps have been completed.

Caution: Powering up without all components installed correctly could lead to a power-up failure that could damage the board. Do not power up the board until the source of any loose component is determined and the component has been replaced on the board.

Note: Review the document provided with the Development Kit titled "Important Safety and Regulatory Information". This document contains addition safety warnings and cautions that must be observed when using this development kit.

3.1 Additional Hardware Required

The table below lists additional hardware required by the Development Kit.

Table 5. Additional Hardware for Development Kit

Hardware	Description
VGA monitor	Any standard VGA or greater resolution monitor.
Keyboard	Keyboard with a PS/2 style connector or adapter as well as USB.
Mouse	Mouse with a PS/2 style connector or adapter as well as USB.
Hard drives	Up to two IDE and two SATA devices.
Floppy drive (optional)	A floppy drive can be connected to the evaluation board, but no floppy drives or cables are included in the Development Kit.
Other devices and adapters	The evaluation board behaves much like a standard PC motherboard. Many PC-compatible peripherals can be attached and configured to work with the evaluation board. For example, users may want to install a sound card or additional network adapters. The user is responsible for procuring and installing any drivers required for additional devices.

3.2 Precautions

The following precautions will reduce the chances of damaging the board:

- Ensure that a 460 W 12 V power supply is used to power up the board.
- This platform supports DDR2-400 DIMMs; ensure that the same speed DIMMs are plugged in all slots of the platform.
- Ensure that the processor has heat sinks mounted securely with 4 screws fastened before powering up the board.
- Ensure that the heat sink is mounted securely to the MCH and 6700PXH each before powering up the board. Never attach a heat sink while the board is powered.
- Use Section 5.0 on page 26 to verify that all jumpers are in their default positions.

3.3 Driver and Operating System Requirements

The Development Kit supports these operating systems:

- Red Hat* Advanced Server 2.1
- Red Hat 8.0
- Red Hat Enterprise Linux* v.3 AS
- Microsoft* Windows* Embedded XP
- Microsoft Windows XP
- Microsoft Windows Server 2003
- Listed below are operating systems that are supported by vendors:
- Wind River* VxWorks* (www.windriver.com)

Listed below are operating systems that are not supported (leverage from other programs):

- FreeBSD*
- Red Hat Enterprise Linux v.3 WS

3.3.1 Drivers Included on the CD

The CD contains three packages of drivers. The contents of each package are detailed below.

- Red Hat Advanced Server v3.3 Compatible Drivers Package
- Windows-Compatible Drivers Package 1 (Chipset_inf_7.0.0.1019)
- Windows-Compatible Drivers Package 2 (E7520-esb-windows)

3.3.1.1 Red Hat* AS v3.3-Compatible Drivers Package 1

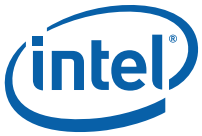
Table 6. Red Hat* AS v3.3-Compatible Drivers Package 1

Files	Description
utils/debug/ks.cfg-XXX	Basic kickstart file to install from FTP to HDA
utils/debug/bldkernel.pl	Script to build/install ESB-enabled kernel sources
utils/debug/bldsrcs.pl	Script to build/install ESB-enabled UP drivers
utils/debug/readme.txt	Describes best method of installing this driver package
sources/kernel/config-2.4.21-20.EL-p4-upapic-i2c	UP Kernel config file
sources/kernel/config-2.4.21-20.EL-p4-smp	SMP Kernel config file
sources/esbwdt/LICENSE	License for Intel watchdog timer driver
sources/esbwdt/esbwdt-doc.txt	esbwdt driver/demoapp release notes
sources/esbwdt/driver/esbwdt.c	esbwdt driver sources
sources/esbwdt/driver/esbwdt.h	esbwdt driver header file
sources/esbwdt/driver/Makefile	esbwdt driver makefile
sources/esbwdt/demoapp/esbwdt-demo.c	esbwdt driver demo app
patches/COPYING	GPL-v2 license for Intel patches
patches/ide-sata/piix.c-hr.patch	Patches to 2.4.21-20.EL IDE driver to enable support for PATA and SATA
patches/smbus/i2c-hr.patch	Enables esb6300 smbus dev in I^2C driver
patches/ioapic/hw_irq.h-hr.patch	Allows error-free kernel compilation

3.3.1.2 Windows*-Compatible Drivers Package 1

The .zip file named InfInst_AUTOL.zip contains the Intel® Chipset Software Installation Utility, which installs Windows INF files to the target system. These files outline to the operating system how to configure the chipset components in order to ensure that these features function properly:

- Core PCI and ISAPNP services
- PCI Express support
- IDE/ATA33/ATA66/ATA100 storage support
- SATA storage support
- USB support
- Identification of Intel chipset components in the Device Manager



3.3.1.3 Windows*-Compatible Drivers Package 2

This driver package is designed to provide driver support for the Intel® 6300ESB ICH Customer Reference Platform using a Windows operating system. This package contains the following drivers, INF files, and documents.

Table 7. Windows*-Compatible Drivers Package 2

Files	Description
ESB_windows_relnotes.txt	Release notes for Windows-compatible drivers
ESB_windows_gold.exe	Self-extracting .zip file containing all project-related files
smb_license.txt	Generic Beta license
SMB.SYS	SMBUS driver
SMB.INF	Install file for SDMBUS driver
smb.cat	SMB driver security catalog file
WDTDRVR.SYS	Watchdog timer driver
WDTDRVR.INF	Install file for watchdog timer
WDT_LICENSE.TXT	Generic Alpha license for watchdog timer components
WDTDEMO.EXE	Demo program for exercising watchdog timer features
mfc42.dll	Microsoft C++ runtime library
mfco42.dll	Microsoft C++ runtime library
msvcrtd.dll	Microsoft C++ runtime library
wdtdemoAppSpec.pdf	WdtDemo App user documentation
wdtdriverspec.pdf	Overview of watchdog timer driver
Intelwdtapi.pdf	Watchdog timer driver interface API document
IWDTLIB.DLL	Watchdog timer interface dynamic link library
CWESB.slx	eXP configuration file
CWESB.log	Log of OS build for eXP
eXP-README.DOC	Readme for eXP build
infinst_enu.exe	Intel® INF Update Utility

3.3.1.4 Third Party Drivers

Software compatible with the ATI Rage* Mobility M Graphics Accelerator is found on the CD-ROM in the file named 021112a-006561C-ATI.zip.

3.3.1.5 Device Driver Download

The table below maps supported features for Intel chipsets with the locations to download support available for each operating system.

Note: Each X in the table is a hyperlink to a web site where more information can be found. The column headings are also hyperlinks to general information on the device types.

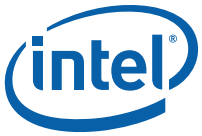
Note: This list is provided as a convenience. Some of these links lead off Intel's web site. Intel does not control the content on other company's web sites or endorse other companies supplying products or services.

Table 8. Device Driver Downloads

Operating System	3x USB 1.1 3x USB 2.0	2x IDE ATA/ 100	Watchdog Timer	Serial ATA	Integrated LAN	AC'97 2.2	Chipset Install Utility
Microsoft Windows 2000	X [1]	X	X	X	X	X	X
Microsoft Windows 2000 Server	X [1]	X	X	X	X	X	X
Microsoft Windows 2000 Advanced Server	X [1]	X	X	X	X	X	X
Microsoft Windows 2003	X [1]	X	X	X	X	X	X
Microsoft Windows XP	X [2]	X	X	X	X	X	X
Microsoft Windows XP Embedded	X [2]	X	X	X	X	X	X [4]
Red Hat Linux 3.0 Advanced Server	X [3]	X	X	X	X	X	X [4]
Wind River VxWorks 5.x	X	X	X	X	X	X [4]	X [4]

Notes:

1. USB support available in a Microsoft Windows 2000 Service Pack release.
2. USB support available in a Microsoft Windows XP Service Pack release.
3. Linux 2.4.19 kernel or newer is needed for USB 2.0 support.
4. Driver support available separately from third party vendors.



4.0 Getting Started

This section identifies key components, features and specifications of the Development Kit. It also describes how to set up the board for operation.

Note: This manual assumes the user is familiar with basic concepts involved with installing and configuring hardware for a PC or server system.

4.1 Overview

The Development Kit contains a baseboard with Intel® Pentium M Processor (760 2.0GHz), Intel® E7520 Chipset, Intel® 6300ESB ICH, and other system board components and peripheral connectors. Various software and documentation are also included in the kit.

Note: The evaluation board is shipped as an open system with stand-offs allowing for maximum flexibility in changing hardware configuration and peripherals in a lab environment. Since the board is not in a protective chassis, the user is required to take safety precaution in handling and operating the system. Some assembly is required before use.

Note: Review the document provided with the Development Kit titled “Important Safety and Regulatory Information”. This document contains addition safety warnings and cautions that must be observed when using this development kit.

4.2 Software Key Features

This section describes the software tools included in the kit. The software was chosen to facilitate development of real-time applications based on the components used in the evaluation board.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in the Development Kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using tools that work with other third party products must have licensed those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third party vendors.

4.3 Setting up the Evaluation Board

After gathering the hardware described in the previous section, follow the steps below to set up the Development Kit. This manual assumes familiarity with basic concepts involved with installing and configuring hardware for a PC or server system.

4.3.1 Safety

Ensure a safe work environment. Measures must be taken to protect the unused DC connectors of the power supply from accidental contact to objects in the work area. Ensure a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge, which may cause product failure or unpredictable operation.

Warning: Do not install the power supply until all other installation steps have been completed.

Caution: Connecting the wrong cable or reversing a cable may damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

4.3.2 Package Contents

Verify kit contents. Inspect the contents of the kit, and please refer to Section 3.1, "Additional Hardware Required" on page 16 for list of hardware that comes with the kit. Check for damage that may have occurred during shipment. Contact an sales representative if any items are missing or damaged.

Check jumper settings. Verify that the jumpers are set in their default state. Refer to Section 5.1 for detailed descriptions of all jumpers and their default settings.

4.3.3 Installed Hardware

Visually inspect components on the board. Make sure the following hardware is populated on the Evaluation Board without noticeable physical defect:

- Intel® Pentium® M Processor
- BIOS FWH
- Battery in holder
- Intel® E7520 MCH
- Intel® 6300ESB ICH

Note: The E7520 MCH and 6300ICH have been mounted to the board at the factory. If it is not mounted correctly, DO NOT power on the board. Ensure that the processor is firmly seated on the socket and its knob fully tightened. If there is a possibility that any of the kit components have been damaged, contact an Intel field sales representative or local distributor for assistance.

4.3.4 Installing the Heat Sinks for CPU

Make certain that the processor is firmly seated in the socket, and the package is secured using a flat head screwdriver to turn the knob.

Figure 4. Processor Seated in Socket

Please refer to Section 8.1 for complete heat sink installation instructions.

4.3.5 Installing Memory

The kit includes two 512 MByte 400 MHz DDR2 ECC DIMMs. To install, ensure the tabs on the slot are open, or rotated outward from the slot. Line up the DIMM above the slot (the DIMM is keyed so that it only fits in the slot in one orientation). Firmly, but carefully, insert the DIMM into the slot until the tabs close. Repeat for all other DIMMs and slots.

Note: When populating both channels, always place identical DIMMs in sockets that have the same position on channel A and channel B (i.e., DIMM A1 should be identical to DIMM B1).Populate DIMMs starting with the sockets farthest away from the MCH (DIMM slots A2 and B2).

Caution: DO NOT bend the board when installing memory. There are a large number of components near the memory slots and excessive board flex can lead to solder joint failure.

4.3.6 Installing Storage Devices

There is one IDE connector on the evaluation board. For a correct boot-up of the system, ensure that a hard drive is installed as the primary master. (Master/slave settings are determined by a jumper on each IDE device. Consult the device label or documentation to verify that the jumper is set correctly for the chosen configuration.) A CD-ROM drive or additional hard drive may be installed as a primary slave device. To install a hard drive on the evaluation board:

1. Verify that the jumper on the hard drive is set correct for single or master, depending on the system configuration.
2. Install the hard drive. This can be done using either the IDE or SATA.

Install IDE device:

a. Connect the short end of the IDE cable to the IDE connector J2K2 on the board. Ensure that the red line, pin one on the cable, is aligned with pin one of the connector indicated by an arrow.

b. Connect the middle connector of the cable to the hard drive. Again, ensure that the red line, pin one on the cable, is aligned with pin one on the hard drive.

Note: Failure to properly align the IDE cable may damage the evaluation board and/or the hard drive.

Install SATA device:

a. Connect one end of SATA cable to hard drive connection. Connect other end to SATA 0 or SATA1 connector J3F2 or J3F1, respectively, on board.

b. Connect a power connector from the power supply to the hard drive.

3. Install the CD-ROM drive (optional). A CD-ROM drive is not included in the kit and is not required, but it may be useful in loading additional software. To install it on the evaluation board:

   a. Verify that the jumper on the CD-ROM drive is set for slave.

   b. Connect the unused end of the IDE cable to the CD-ROM drive. Ensure that the red line, pin one on the cable, is aligned with pin one of the CD-ROM drive connector, as indicated by an arrow.

   c. Connect a large 4-pin power connector from the power supply to the CD-ROM drive.

4. Install the floppy drive (optional). A floppy disk drive is not included in the kit and is not required, but it may be useful in loading additional software. To install a floppy drive on the evaluation board:

   a. Connect the floppy cable to the floppy connector J1J1. Ensure that the red line, pin one on the cable, is aligned with pin one of the connector, as indicated by an arrow.

   b. Connect the other end of the floppy cable to the floppy drive.

   c. Connect a power cable to the floppy drive. Ensure that the red line, pin one on the cable, is aligned with pin one on the floppy drive.

Note: Only an IDE hard drive is included in the Development Kit.

4.3.7 Connect the Monitor Cable

Connect the monitor cable to J6A1 on the Evaluation Board.

Note: Monitor is not included in this Development Kit.

4.3.8 Connect the Keyboard and Mouse

Connect a PS/2 mouse and keyboard to the stacked PS/2 connector on the evaluation board. The bottom connector (often purple) is the keyboard connector and the top (often green) is the mouse connector. Alternatively, plug a USB keyboard and a USB mouse into the USB connectors on the evaluation board.

Note: Keyboard and mouse are not included in this Development Kit.

4.3.9 Connect the Power Supply

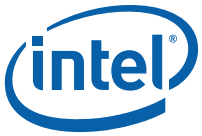
Make sure the power supply is turned off and unplugged. Connect the two SSI power supply cables to connectors J5K1 and J8K1 on the evaluation board. Next, plug the power cord into the power supply and the wall.

4.3.10 Power up the System

Turn on the monitor and then turn on the evaluation board.

Note: Do not turn power on until the CPU thermal solution has been installed.

Caution: Ensure that the fan heat sink on the processor is operating. If not, turn off the power immediately and verify that the fan heat sink is connected to the board correctly (see



Section 4.3.4). If the fan heat sink is not operating, contact an Intel field sales representative or local distributor.

4.4 Configuring the BIOS

An AMI BIOS is pre-loaded on the evaluation board. Changes to the BIOS may be necessary to enable hard disks, floppy disks, and other supported features. Use the setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface.

On first boot-up of the system, consider using the BIOS setup program to verify the date/time and boot device. To enter into the BIOS setup program, press the Delete key during boot.

BIOS updates may be updated periodically. Please contact an field sales representative for BIOS updates.

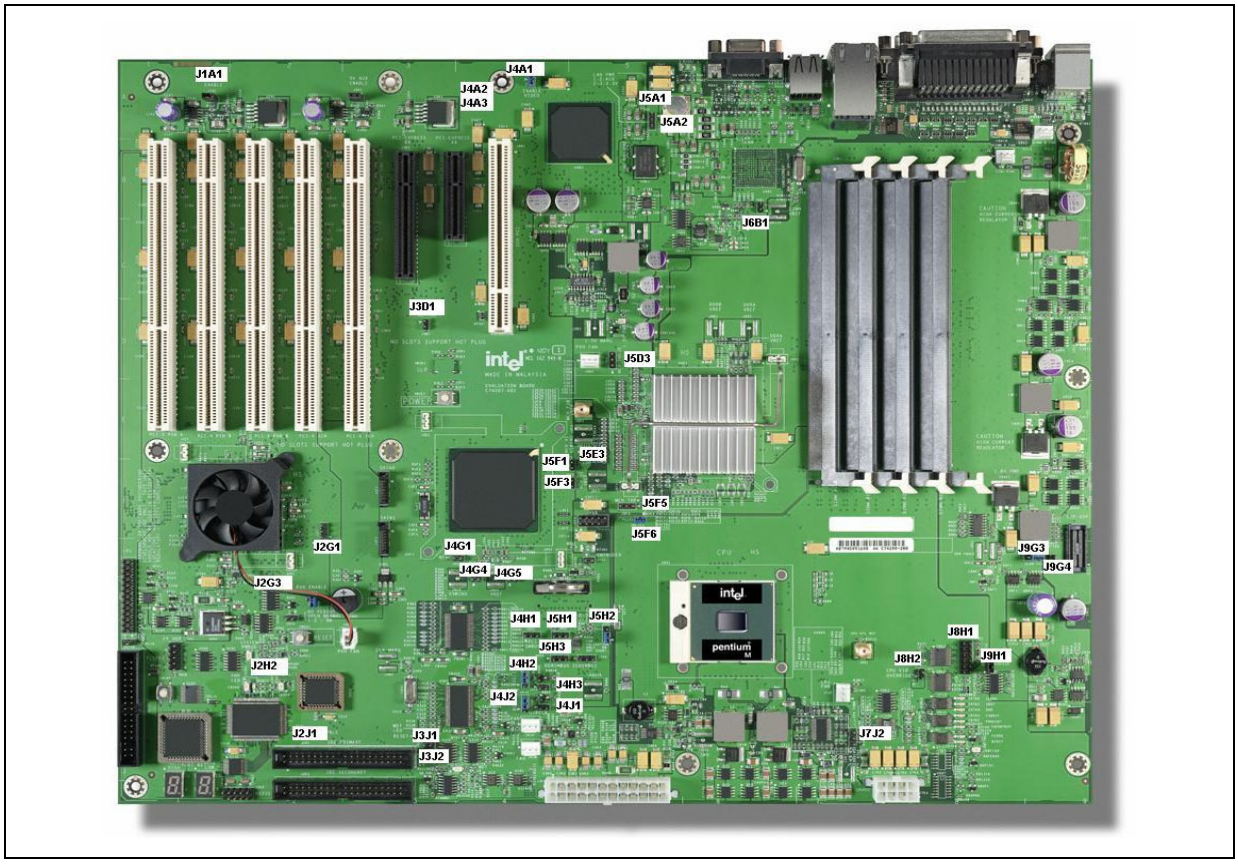
5.0 Jumpers and Headers

This section describes the platform component placement as well as configuration, test, and debug features of the Intel® Pentium® M Processor on 90 nm process with Intel® E7520 Chipset Development Kit board.

5.1 Jumpers

Figure 5 depicts all jumpers on the Evaluation Board. Table 9 illustrates the settings and usage of the jumpers. Review Figure 5 and Table 9 before changing default setting of the jumpers on the board.

Figure 5. Evaluation Board Headers and Jumpers



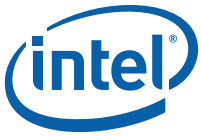


Table 9. Jumper Settings (Sheet 1 of 2)

Jumper Name	Ref Des	Description / Settings	Default Position
Enable PXH	J2G3	Enable on PXH 1-2: Enable Open: Disable	1-2
CPU Detect	J2H2	CPU socket occupy signal routing Short : CPU present Open : CPU not present	1-2
Enable Super I/O Chip	J2J1	Enable on SIO 1-2: Enable Open: Disable	1-2
CMOS Clear	J5H2	Clears CMOS 1-2: Normal 2-3: Configure	1-2
CPU VID Override	J8H2	Manual VID select 1-2: Manual select Open: CPU select	Open
CPU VID	J8H1	VID[5] / VID[4] / VID[3] / VID[2] / VID[1] / VID[0] 11–12 / 1-2 / 3-4 / 5-6 / 7-8 / 9-10	(1.212V) 1-2 Open 3-4 Open 5-6 Open 7-8 Open 9-10 Open 11-12 Short
Enable Video	J4A1	Enables on-board video 1-2: Enable Open: Disable	1-2
Freq FSB Clock Override (Host Clock Jumper)	BSEL1 / BSEL0	BSEL1 / BSEL0 / SPEED 2-3 / 1-2 / CPU Original Fused Speed	BSEL1: 2-3 BSEL0: 1-2
	J4H2 / J4J2	2-3 / 2-3 / 100 MHz 2-3 / OPEN / 133 MHz	
DIMM Speed Configuration	FREQ_SEL1 / FREQ_SEL0	FREQ_SEL1 / FREQ_SEL0 / FSB Frequency OPEN / SHORT / 533 MHz	J5E3(1-2)
	J5F6 / J5E3	SHORT / OPEN / 400 MHz	
ITP CPU Access	J9G4 / J9G3	J9G4 / J9G3 1-2 / Open / CPU Access Only 2-3 / 1-2 / Chain Test	J9G3 (1-2)
3.3V AUX SWITCH @ 1.7A	J1A1	Install jumper to enable AUX voltage 1-2: Enable Open: Disable	1-2
Speaker Pull-up	J2H1	Pulls up speaker routing 1-2: Enable Open: Disable	Open
5V AUX SWITCH @ 1.7A	J3A1	Install jumper to enable AUX voltage supply 1-2: Enable Open: Disable	1-2
PXH_TDC and PXH_TDA	J2G1	Check for PXH temperature (for validation) Open: (For external access only)	Open
Front Panel Sleep Button	J3D1	For validation only	Open
ICH Watchdog Test Out	J3J1	For validation only	Open
Watchdog Control	J3J2	For validation only	Open

Table 9. Jumper Settings (Sheet 2 of 2)

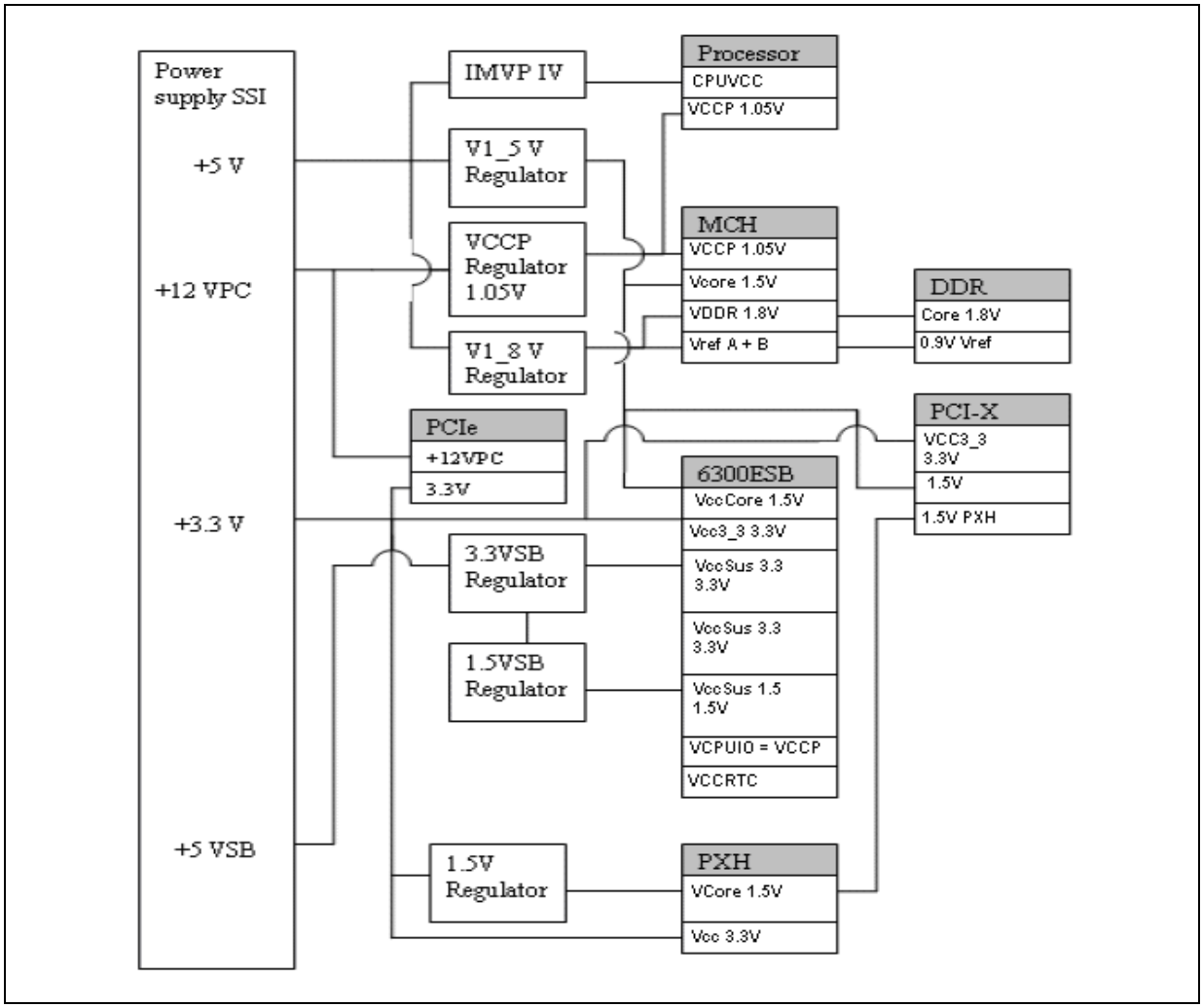
Jumper Name	Ref Des	Description/Settings	Default Position
ICH HI_RCOMP Control	J4G1	For validation only	Open
ICH VSWING Control	J4G4	For validation only	Open
ICH VREF Control	J4G5	For validation only	Open
PCI_SMBus Clock and PCI_SMBus DATA Ground Option	J4H1	Grounds PCI_SMB Clock & SM Bus Data 1-2: SMBData Grounded 3-2: SMBCLK Grounded Open: Idle	Open
LAN SMBus Clock and LAN SMBus DATA Ground Option	J5H1	Grounds LAN SMB Clock & SM Bus Data 1-2: SMBData Grounded 3-2: SMBCLK Grounded Open: Idle	Open
DIMM SMBus Clock and DIMM SMBus DATA Ground Option	J5H3	Grounds DIMM SMB Clock & SM Bus Data 1-2: SMBData Grounded 3-2: SMBCLK Grounded Open: Idle	Open
System Management Interrupt Control	J4H3	Enables external interrupt to SMI pin (validation use only) Open: Disable	Open
Enable ICH Stop Clock Control from External Control	J4J1	For validation only	Open
LAN_AUXPWR_ STRAP	J5A1	Manually controls LAN AUX power strap either pulled up to 3.3V or down to ground 1-2 Disable 2-3 Enable Open IDLE	Open
To Pull MCH_SMBCLK and MCH_SMBDAT to Ground	J5D3	Grounds MCH SMB Clock & SM Bus Data 1-2: SMBData grounded 3-2: SMBCLK grounded Open: IDLE	Open
Enable A16 ICH SWAP OVERRIDE	J5F1	Short : Top swap Open : Normal (default)	Open
Enable ICH Run at Safe Mode	J5F3	Short : Safe mode Open : Normal (default)	Open
Enable MCH THERMAL DIODE Access	J5F5	For validation only	Open
LAN Wake On Control	3.3V Supply / LAN_ AUXPWR_ STRAP / ICH_ Wake	J5A1 / J5A2 / J6B1 / LAN Wake On Status	Open
	J5A1 / J5A2 / J6B1	1-2 / 1-2 / 1-2 / Wake On	
		2-3 / 2-3 / Open / No Wake On	
DDR S3 ENABLE BCKFD_CT_LTCH	J9H1	Short : Enable DIMM S3 Open : Disable DIMM S3	1-2
CPU ThermDA and ThermDC External Connection	J7J2	1 : Thermal DC connection 2: Thermal DA connection 3: Ground External Access Only	Open

6.0 System Overview

6.1 Power Diagrams

Figure 6 shows the power distribution for the Evaluation Board. For details on power distribution logic, refer to the Customer Reference Board Schematics listed in Table 1 on page 6.

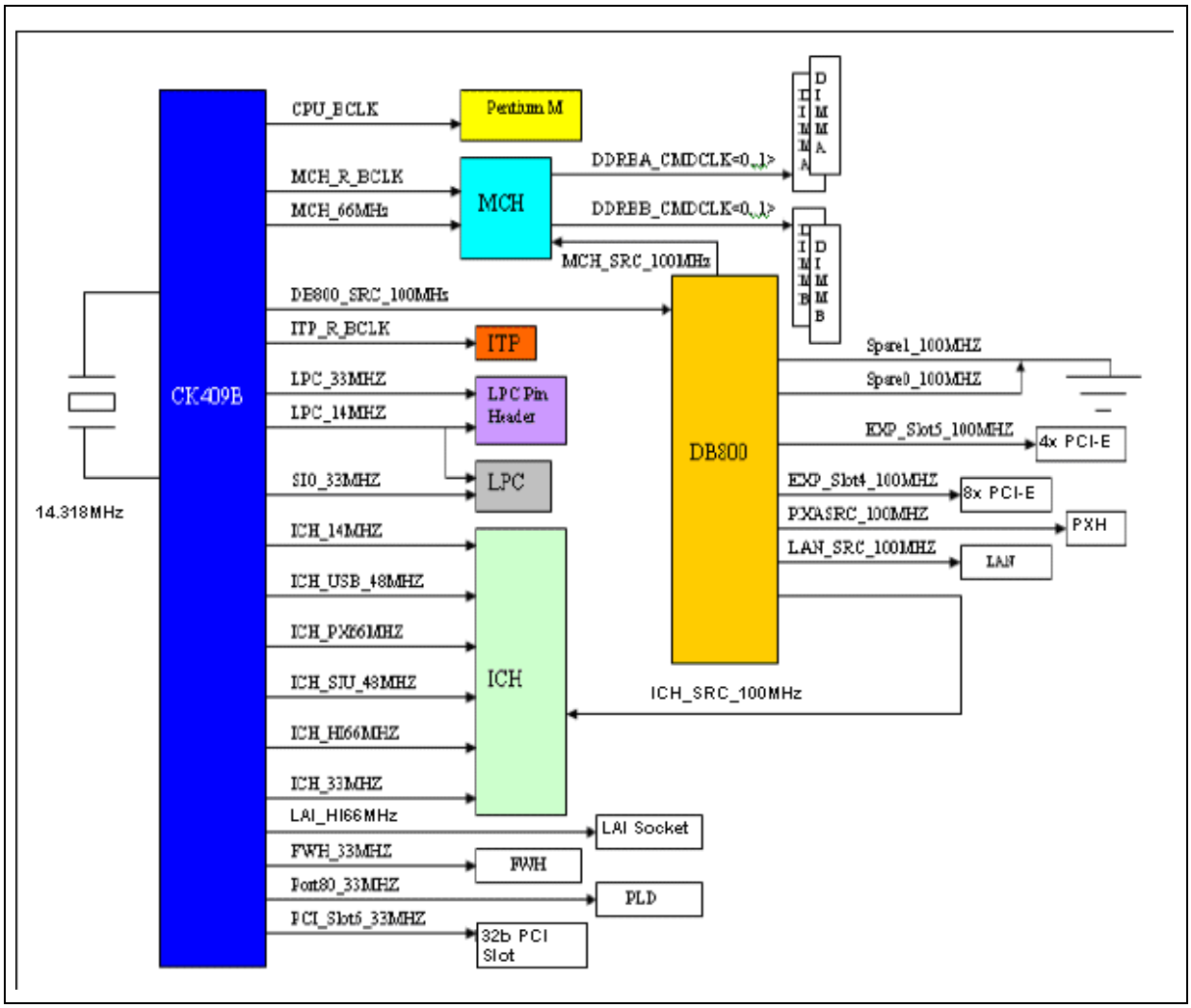
Figure 6. Power Distribution Block Diagram



6.2 Platform Clocking

The board uses one CK409B Clock Synthesizer to generate the host differential pair clocks and the 100 MHz differential clock to the DB800. The DB800 then generates the 100 MHz differential pair clock for the PCI Express devices. Figure 7 shows the board clocking configuration.

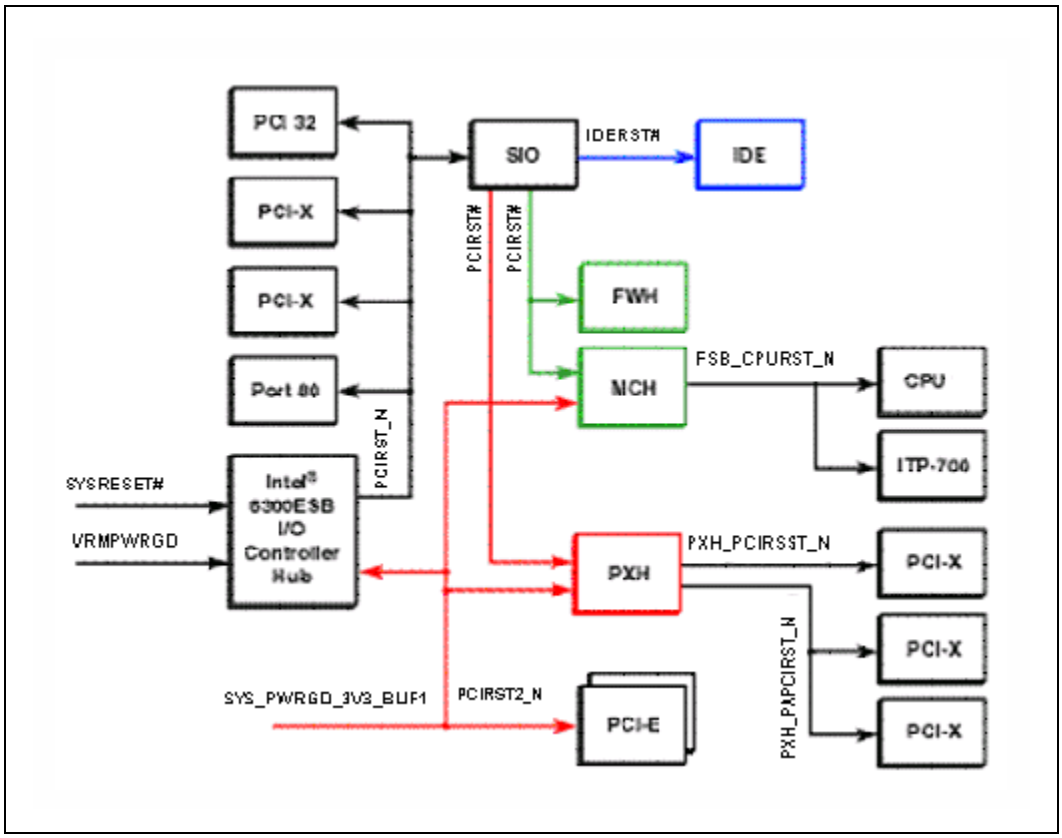
Figure 7. Clock Block Diagram



6.3 Platform Resets

Figure 8 depicts the reset logic for the Evaluation Board. The Intel® 6300ESB I/O Controller Hub (ICH) provides most of the reset following assertion of power good and system reset. However, the glue logic within the SIO is also used to buffer reset to PXH, MCH, FWH, and IDE.

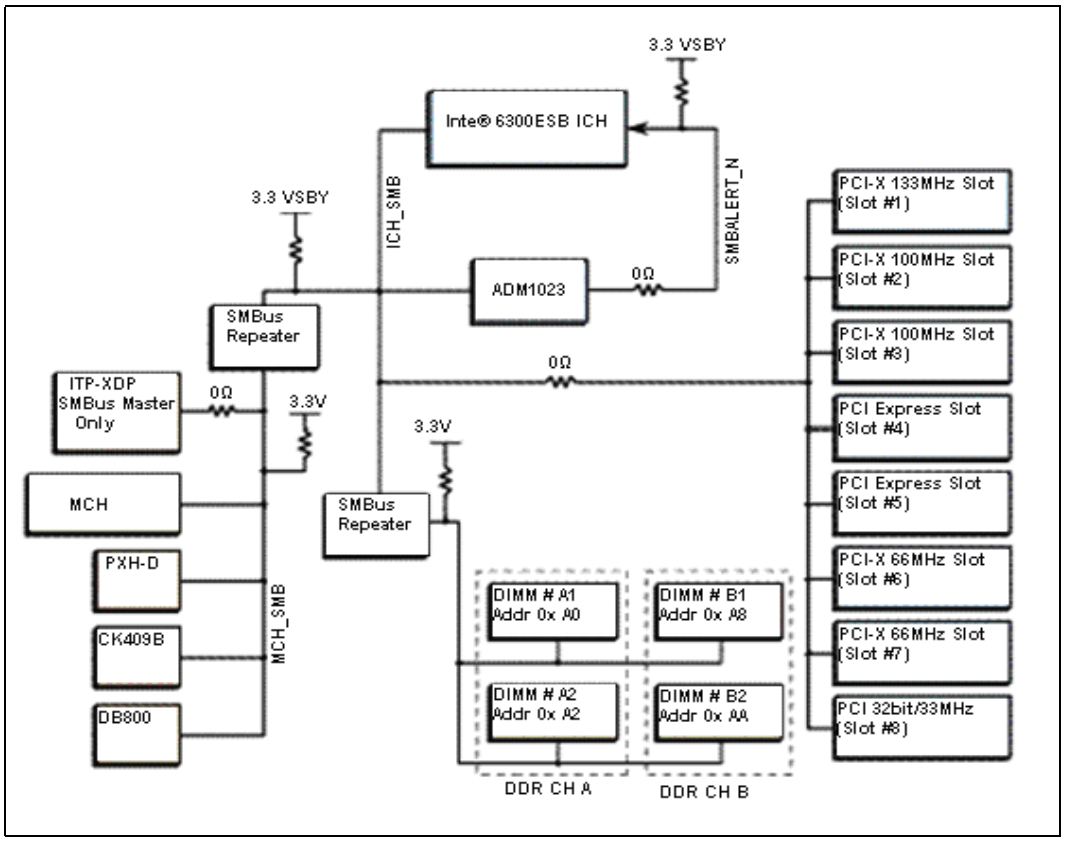
Figure 8. Platform Reset Diagram



6.4 SMBus

Figure 9 below illustrates the routing of the SMBus signal among the components.

Figure 9. SMBus Block Diagram



6.5 VRD VID Headers

The Development Kit provides for manual control of the processor core voltage regulator output level(s). Normally, the processor should be run at its default VID (voltage identification) value as set during manufacturing. However, in the event that the user needs to set a different VID value from the default value, it can be accomplished through a jumper block found on the board. Note that these headers are not populated by default.

The CPU VID header is located at J8H2. Table 10 provides the VID settings available via the VID headers.

Table 10. VID vs. $V_{CC\text{-}CORE}$ Voltage (Sheet 1 of 2)

VID						$V_{CC\text{-}CORE}$ (V)
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692

VID						$V_{CC\text{-}CORE}$ (V)
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.18

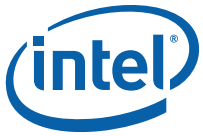


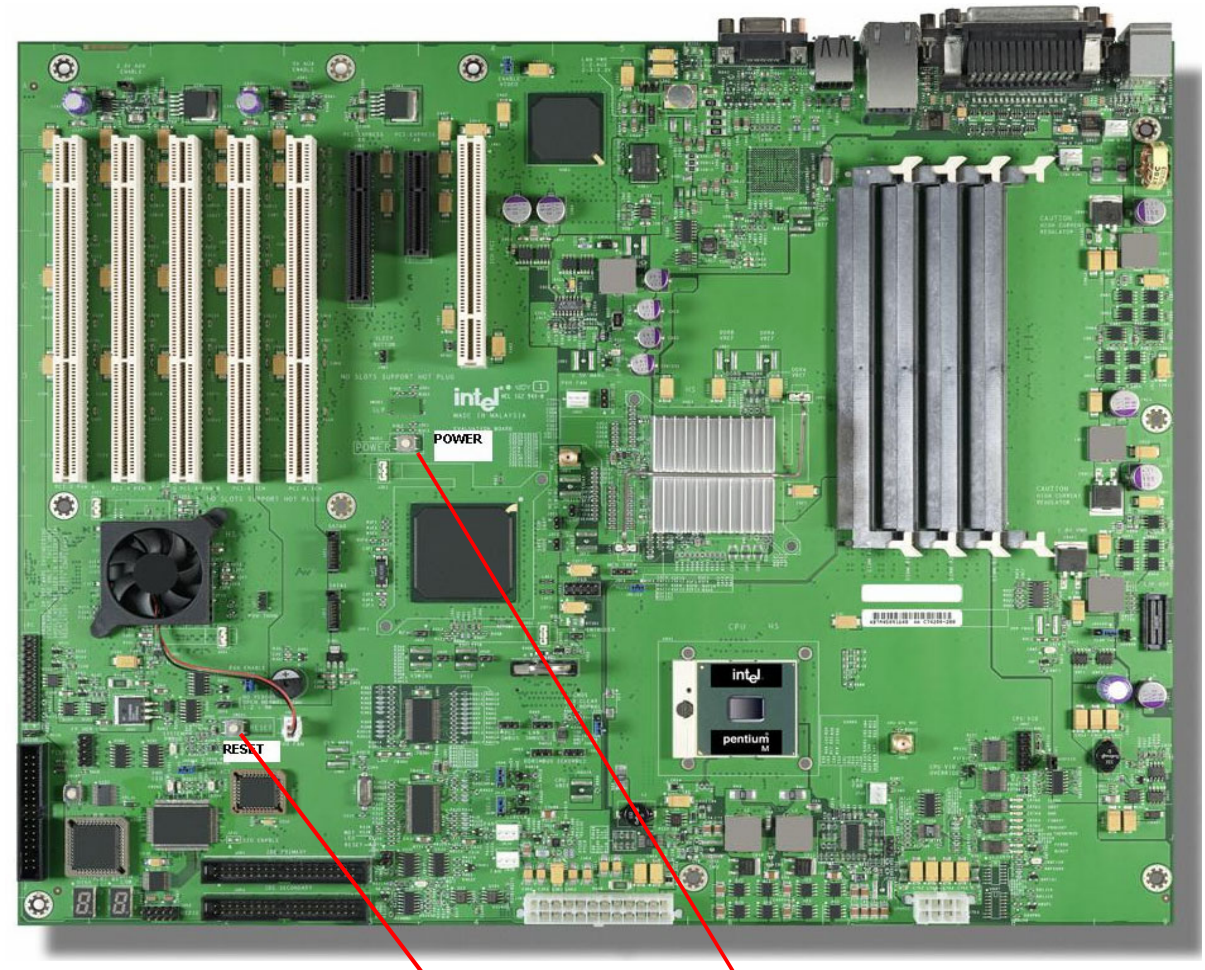
Table 10. VID vs. $V_{CC-CORE}$ Voltage (Sheet 2 of 2)

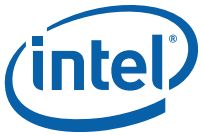
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.66	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.1
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.58	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.02
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.5	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.94
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.42	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.86
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.34	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.78
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.26	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.7

6.6 Miscellaneous Buttons

Figure 10 below shows the location of the power buttons within the platform.

Figure 10. Power Buttons





7.0 Debug Procedure

The debug procedures in this section are used to determine baseline functionality for the Development Kit board. This is a cursory set of tests designed to provide a level of confidence in the platform operation.

7.1 Level 1 Debug (Port 80/BIOS)

Refer to the steps in Table 11 when debugging a board that does not boot.

Table 11. Level 1 Debug (Port 80/BIOS)

Item	Test	Pass/Fail Criteria	Cause of Failure
1	Verify "SYSTEM PWRGD" LED	CR2H1: green	Power sequence failure—go immediately to Level 2 debug
2	Is PCI RESET LED (decimal on DS1J2) illuminated?	Decimal on Port 80 display red	PCI reset stuck—go to Level 3 debug
3	Verify CPURST LED is off	Off	CPU reset stuck—go to Level 3 debug
4	Verify Port 80 posting	Port 80 LEDs are posting boot codes and stopping	System hang—Check BIOS go to level 3 debug. Refer to AMI* BIOS documentation for details.
5	Check BIOS revision	Latest BIOS installed	Contact an Intel representative for the latest BIOS image.
6	Verify default jumper settings	See default settings	Improper jumper settings

7.2 Level 2 Debug (Power Sequence)

Check the items in Table 12 below if "SYSTEM PWRGD" is not illuminated.

Table 12. Level 2 Debug (Power Sequence) (Sheet 1 of 2)

Item	Test	Pass/Fail Criteria	Cause of Failure
1	Primary power supply voltages	Measure voltage across: C3K2: 3.3 V J5K1.14 (-12VPC) : -12 V J5K1.14 (12VPC) :12 V J8K1.5 (P12V0): 12 V J8K1.8 (P12V1): 12 V	External power supply failure
2	P1V8_DDR	Q9G1.3: 1.8 V	DDR2 power supply failure
3	1.5 V	R5C5.2: 1.5 V	MCH/PXH/ICH core power supply failure
4	P1_8DDR_STBY	Q9G1.8: 1.8 V	DDR2 standby power supply failure
5	VCCP	CR6H1.1: 1.05 V	VCCP power supply failure

Table 12. Level 2 Debug (Power Sequence) (Sheet 2 of 2)

6	VCCA	C7J4: 1.8 V	VCCA power supply failure
7	CPUVCC	Check VID fused in CPU	CPU VRD failure
8	Verify SYSTEM PWRGD LED	CR2H1: green	Power sequence failure

7.3 Level 3 Debug (Voltage References)

Table 13 includes instructions to help with debug.

Table 13. Level 3 Debug (Voltage References)

Item	Test	Pass/Fail Criteria	Cause of Failure
1	MCH DDR2 Channel A V_{REF}	R2M4.1: 0.9 V	V_{REF} incorrect: check resistor values
2	MCH DDR2 Channel B V_{REF}	R2M3.1: 0.9 V	V_{REF} incorrect: check resistor values
3	MCH Hublink V_{REF}	R5F5.1: 0.354 V	V_{REF} incorrect: check resistor values
4	MCH Hublink V_{SWING}	R6F12.1: 0.804 V	V_{SWING} incorrect: check resistor values
5	ICH Hublink V_{REF}	R4G7.1: 0.347 V	V_{REF} incorrect: check resistor values
6	ICH Hublink V_{SWING}	R4G6.1: 0.696 V	V_{SWING} incorrect: check resistor values
7	CPU VCCP V_{REF} (back of board)	R3V4.1: 0.7 V	V_{REF} incorrect: check resistor values
9	MCH VCCP V_{REF}	R6F14.1: 0.68 V	V_{REF} incorrect: check resistor values

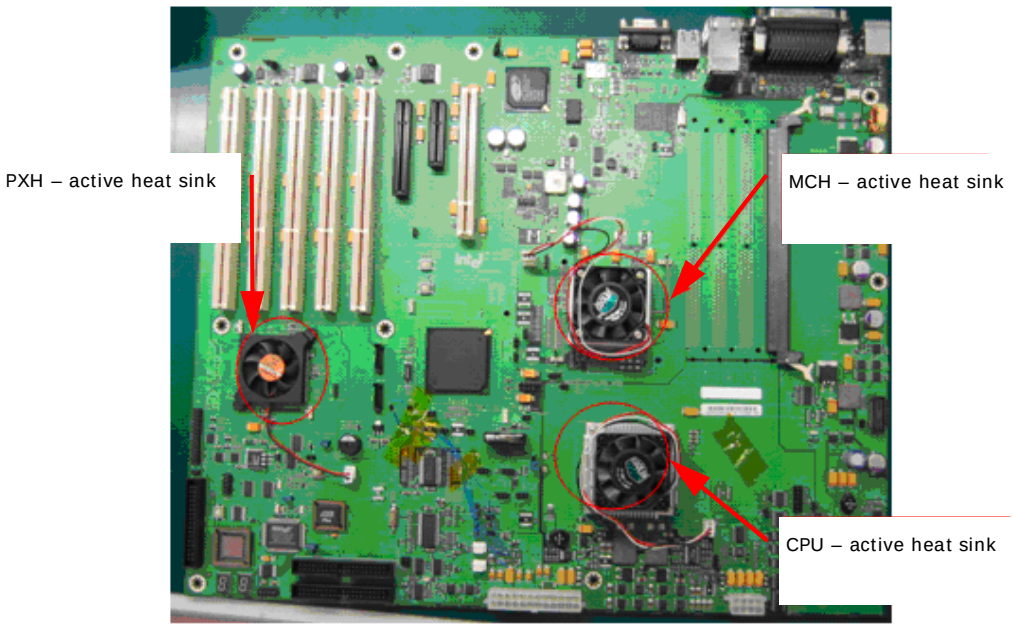
8.0 Heat Sink Assembly

This section provides heat sink assembly instructions for the Evaluation Board. Components requiring heat sink are listed in Table 14. Please note that the thermal solutions listed below are provided by third party vendors.

Table 14. Components Requiring Heat Sink Assembly

Component	Quantity	Manufacturer	Part Number	Comments
CPU	1 per board	Cooler Master*	EEB-N41ES-02	Active heat sink and backplate
MCH	1 per board	Cooler Master	ECB-000208-01	Active heat sink
PXH	1 per board	Sunon*	GC123506BHDA.05.N.B515/ 2026	Active heat sink

Figure 11. Heat Sink Placement



8.1 Processor Heat Sink Installation Instructions

Note: Tools needed include one Phillips screwdriver and one flat head screw driver. Consumable items needed include disposable towels, thermal interface material (TIM), and isopropyl alcohol.

Table 15. Heat Sink Installation Instructions (Sheet 1 of 3)

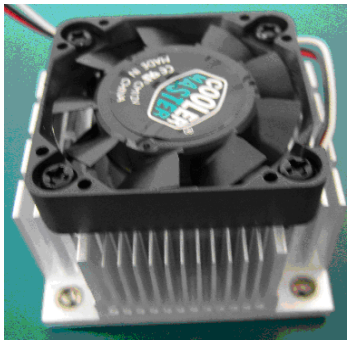
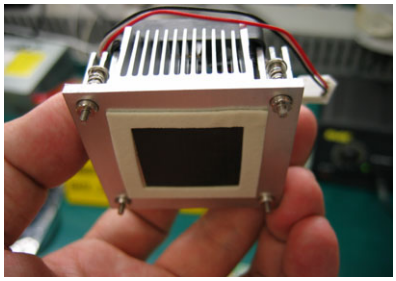
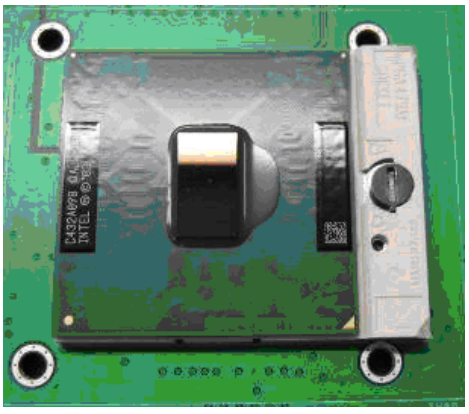
Instructions	Illustration
1. Ensure the heat sink gasket is sitting flat and balanced on the package substrate.	 Heat sink top view  Heat sink bottom view ***Note:*** Scrape off scratched TIM with plastic ruler and replace with new TIM.
2. Make certain that the processor is firmly seated in the socket, and the package is secured using a flat head screwdriver to tighten the knob.	

Table 15. Heat Sink Installation Instructions (Sheet 2 of 3)

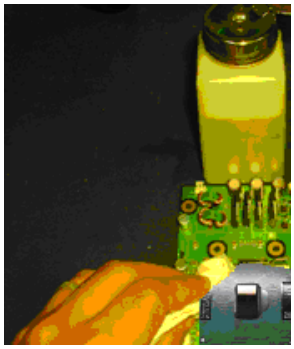
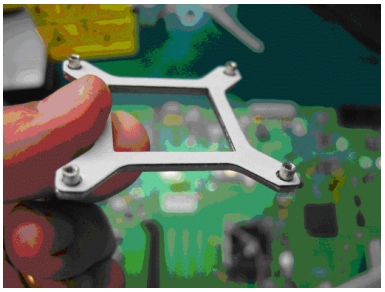
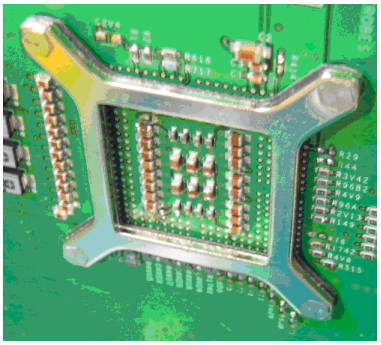
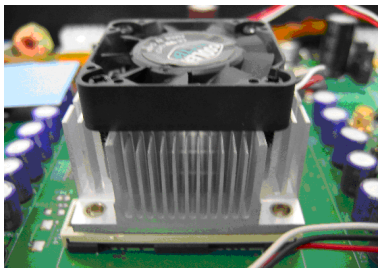
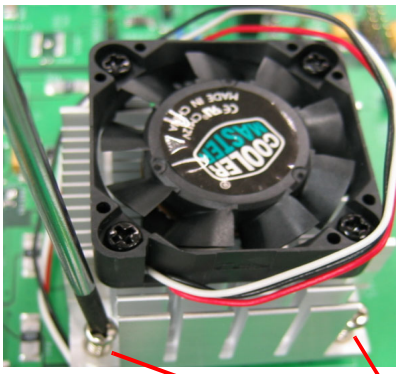
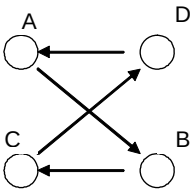
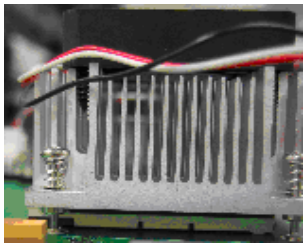
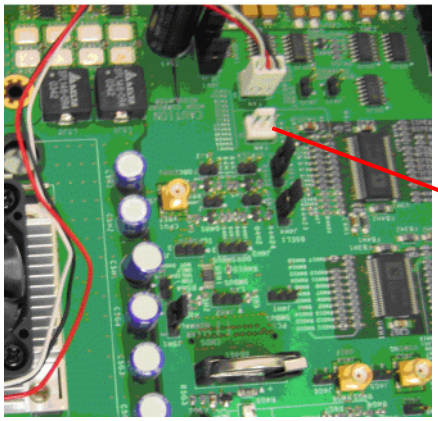
3. Clean the top surface of the processor package with a clean towel and isopropyl alcohol.	
4. Mount the backplate for the CPU heat sink on the bottom surface of the board / PCB at the CPU location. Insert the four stand-offs on the backplate into the bottom side of the board. **Caution:** The backplate may fall down when the board is oriented horizontally. Use a finger to hold the backplate in place while turning the board.	 Backplate stand-offs  Backplate mounted on board
5. Mount the heat sink on the PCB with gasket on the heat sink bottom surface touching the package substrate. ***Note:*** The thermal interface material must make contact with the silicon die.	

Table 15. Heat Sink Installation Instructions (Sheet 3 of 3)

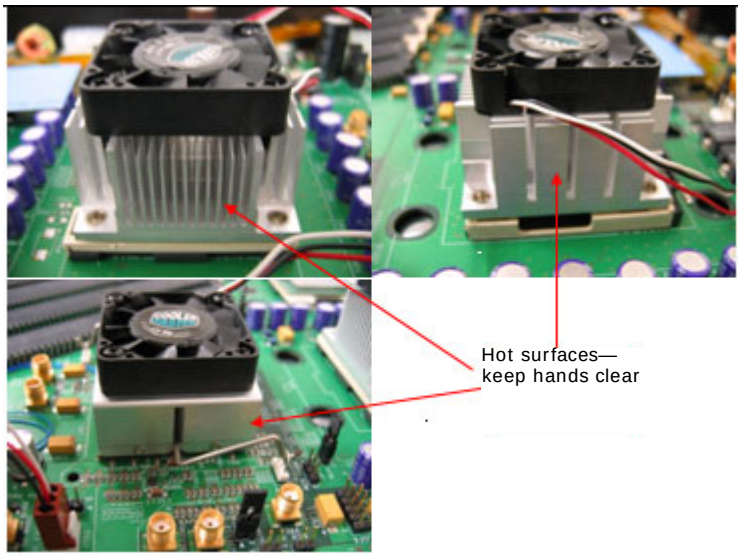
6. Align the screws (one at each of the four corners) so they can slide into the threaded holes of the backplate stand-offs. 7. Holding the heat sink fins at the sides, tighten the four retaining screws using a Phillips head screwdriver. **Caution:** To to prevent silicon die cracking, observe the following procedure when tightening the heat sink retaining screws. 8. Tighten the screws in three stages: • Tightening each screw to half of the screw travel length, proceeding from A to D as shown in the diagram at right. • Repeat the sequence, tightening each screw a further one-quarter of the screw length. • Repeat the sequence, tightening each screw until firm resistance is met. Do not overtighten.	 Retaining screws  Screw tightening sequence
9. Ensure the heat sink base is fully seated and flat with respect to the board surface. If not, remove reverse the screws by reversing the procedure outlines in Step 5-8 above. Then re-tighten the heat sink, again following the instructions above.	
10. Plug the fan connector to the fan pin header on the board.	 Fan pin header

8.2 Mechanical, Thermal, and Electrical Precautions

Keep fingers clear of the fan blades while they are in operation.

Keep hands away from the hot metal surfaces on the sides of the heat sinks, as shown in Figure 12.

Figure 12. Elevated Temperature on Heat Sink Fin Surface



The fan must always be securely connected to the 3-pin header provider(s) on the board, labeled “Fan” next to the pin header. Figure 13 shows the locations of the heat sink fan connectors.

Figure 13. Heat Sink Fan Connector