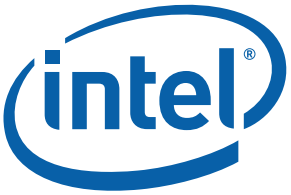

Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit

User Manual

January 2012

Document Number: 324213-002

Contents

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Revision History

Revision	Description	Revision Date
002	Updated Windows* XP OS installation instructions and removed outdated installation instructions for other OS. Updated description of included panel display.	January 2012
001	First release of development kit.	October 2010

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1.0 Introduction

This manual describes the typical hardware set-up procedures, features, and usage of the Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit. This document is written for evaluation by OEMs, system integrators, and embedded system developers. The document defines all jumpers, headers, LED functions, and their locations on the development platform along with subsystem features. The document assumes basic familiarity in the fundamental concepts involved with installing and configuring hardware for a personal computer system.

Note: Read this document in its entirety prior to applying power to the reference platform.

Intel recommends having the schematic files and development kit boards present while reading this document. The references in this document correlate to reference designators and board properties of the Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit.

Chapter 6.0 provides quick start procedures.

1.1 About the Development Kit

The development kit includes the following:

- COM Express* Module with Intel® Atom™ Processor E660, 1GB DDR2 soldered down memory, system management CPLD and SPI Flash.
- Carrier board with the Intel® Platform Controller Hub EG20T and other system components and peripheral connectors for PCIe*, PCI, SDVO, SATA, USB, LAN, LVDS, SD/SDIO/MMC, UART and audio interfaces.
- Timesys Fedora* Remix Linux operating system (pre-installed on the hard drive included in the kit)
- Software CD with user's guide, reference design materials, drivers and utilities
- SATA Gen2 hard drive
- USB floppy drive
- Power supply
- LVDS cable

The kit contents may be prepared with additional equipment (depending on options made available to you at the time of purchase):

- LVDS panel
- VGA SDVO ADD2N card and display (instead of the LVDS display and LVDS cable)
- DVD-ROM drive
- Keyboard and mouse with PS/2 or USB interface (BIOS setting dependent)
- Chassis with ATX power supply (or AC adapter)

1.2 Terminology

Table 1. Conventions and Terminology (Sheet 1 of 2)

Term	Definition
AC	Audio Codec
ACPI	Advanced Configuration Power Interface
ADD2	Advanced Digital Display 2 card
ADD2-N	Advanced Digital Display 2 card with PCIe* graphics lane in normal orientation
ANV	Analog Validation
ATA	Advanced Technology Attachment
BGA	Ball Grid Array
BIOS	Basic Input / Output System
CAN	Controller Area Network
CRB	Customer Reference Board
CTS	Clear To Send
DCD	Data Carrier Detect
DCE	Data Circuit-Terminating Equipment
DMA	Direct Memory Access
DFM	Design For Manufacturing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
DVI	Digital Video Interface
EBL	Extended Battery Life
EFI	Extensible Firmware Interface
EBL	Extended Battery Life
EHCI	Enhanced Host Controller Interface
EM	Electromagnetic
EMI	Electromagnetic Interface
ESR	Equivalent Series Resistance
EV	Electrical Validation
FAE	Field Application Engineer
FWH	Firmware Hub
GbE	Gigabit Ethernet
GE	General Embedded
GMAC	Gigabit Ethernet Media Access Controller
GND	Ground (Signal Ground)
GPIO	General Purpose Input Output
Intel® HD Audioβ	Intel® High Definition Audioβ
ICG	Integrated Clock Generator
Intel® EMGD	Intel® Embedded Media & Graphics Driver
IVI	In-Vehicle Infotainment
KBC	Keyboard Controller
LAN	Local Area Network
LED	Light Emitting Diode
LPC	Low Pin Count
LVDS	Low Voltage Differential Signaling
MMC	Multi Media Card

Table 1. Conventions and Terminology (Sheet 2 of 2)

Term	Definition
MP	Media Phone
OHCI	Open Host Controller Interface
PCB	Printed Circuit Board
PCH	Platform Controller Hub
PCI*	Peripheral Component Interconnect
PCIe*	PCI Express*
PEG	PCI Express* Graphics
PLL	Phase Lock Loop
PS/2	(IBM) Personal System/2
POST	Power On Self Test
RGMII	Reduced Gigabit Media Independent Interface
RI	Ring Indicator
RS232C	Recommended Standard 232 (Standard: EIA-232-D/E)
RS485	Recommended Standard 485 (Standard: EIA-485)
RTC	Real Time Clock
RTS	Request To Send
RX	Receiver or Receive (in reference to PCI Express* differential signal pairs)
RXD	Receive Data
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDVO	Serial Digital Video Output
SIO	Super Input Output
SIV	System Integrity Validation
SJR	Solder Joint Reliability
SKU	Stock Keeping Unit
SLI	Second Level Interconnect. Describes the connection between the package and the main PCB
SLIC	Standard Linear Integrated Circuit
SMbus	System Management Bus. A two-wire interface through which various system components can communicate
SMC	System Management Controller
SMV	System Marginality Validation
Intel® TPM[ε]	Intel® Trusted Platform Module[ε]
TX	Transmitter or Transmit (in reference to PCI Express* differential signal pairs)
TXD	Transmit Data
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VR	Voltage Regulator

Table 2. Component Names

Component	Name Used in this Document
COM Express* Module equipped with Intel® Atom™ Processor E660	Little Bay
Platform with COM Express* Module equipped with Intel® Atom™ Processor E660 and carrier board equipped with Intel® Platform Controller Hub EG20T	Crown Bay
Carrier board equipped with Intel® Platform Controller Hub EG20T	Shell Bay

Note: Shell Bay is available as a customer reference board for developing applications with the Intel® Platform Controller Hub EG20T.

1.3 Technical Support

Support Services for your hardware and software are provided through the secure Intel® Premier Support Web site at https://premier.intel.com. After you log on, you can obtain technical support, review "What's New," and download any items required to maintain the platform.

1.3.1 Additional Technical Support

If you require additional technical support, please contact your field sales representative or local distributor.

1.4 Product Literature

You can order product literature from the following Intel literature centers.

Table 3. Intel Literature Centers

U.S and Canada	1-800-548-4275
U.S. (from overseas)	708-296-9333
Europe (U.K.)	44(0)1793-431155
Germany	44(0)1793-421333
France	44(0)1793-421777
Japan (fax only)	81(0)120-47-88-32

1.5 Reference Documents

Table 4 is a partial list of the available collateral. For the complete list, contact your local Intel representative.

Table 4. Reference Documents (Sheet 1 of 2)

Document	Document No./Location
Little Bay – Bill of Materials (BOM) / Parts List	425970
Little Bay – Customer Reference Board File	425969
Little Bay Schematic	433299
Intel® Atom™ Processor E6xx Series Datasheet	324208
Intel® Atom™ Processor E6xx Series-based – Platform Design Guide	433311
Intel® Atom™ Processor E6xx Series – Sightings Report (SR)	433308; Note 1
Intel® Atom™ Processor E6xx Series Thermal and Mechanical Design Guidelines	324210
Shell Bay – Bill of Materials (BOM) / Parts List	439439
Shell Bay – Customer Reference Board File	431138
Shell Bay – Customer Reference Board Schematic	432866
Intel® Platform Controller Hub EG20T Datasheet	324211
Intel® Platform Controller Hub EG20T – Platform Design Guide	433342
Intel® PCH EG20T – Boundary Scan Description Language (BSDL) File	426985
Intel® PCH EG20T – I/O Buffer Information Specification (IBIS) Models	426984
Intel® PCH EG20T – Cadence* Allegro* OrCAD* and Concept* Schematic Symbol Files	432874
Intel® Platform Controller Hub EG20T – Sightings Report	438312; Note 1
Intel® Embedded Media and Graphics Driver, EFI Video Driver, and Video BIOS v1.5 for Windows XP and Linux* Specification Update*	445348
Specifications	
Advanced Configuration and Power Interface, Version 3.0 (ACPI)	http://www.acpi.info/spec.htm
Alert Standard Format Specification, Version 1.03	http://www.dmtf.org/standards/asf
AP-728 ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	http://www.intel.com/Assets/PDF/appnote/292276.pdf
ATX12V Power Supply Design Guide, Version 1.1	http://www.formfactors.org/
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 0.96 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
ExpressCard* Standard Release 1.0	http://www.expresscard.org
Intel® High Definition Audio Specification	http://www.intel.com/standards/hdaudio
RS - Intel® Serial Digital Video Out (SDVO) Port External Design Specification (EDS)	Note 2

Notes:
1. Sightings Reports will only be available when there are sightings to report.
2. Contact your Intel Field Representative for the latest version of this document.

Table 4. Reference Documents (Sheet 2 of 2)

Document	Document No./Location
Low Pin Count Interface Specification, Revision 1.1 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
PCI Express* Card Electromechanical Specification Revision 1.0	http://www.pcisig.com/specifications
PCI Express* Base Specification, Revision 1.0a	http://www.pcisig.com/specifications
PCI Local Bus Specification, Revision 2.3 (PCI)	http://www.pcisig.com/specifications
PCI Mobile Design Guide, Revision 1.1	http://www.pcisig.com/specifications
PCI Standard Hot Plug Controller and Subsystem Specification Revision 1.0	http://www.pcisig.com/specifications
PICMG® COM Express* Module Base Specification	http://www.picmg.org/
PICMG® COM Express* Carrier Design Guide, Revision 1.0	http://www.picmg.org/
SD Host Controller Standard Specification Ver1.0	http://www.sdcard.org/
System Management Bus Specification, Version 2.0 (SMBus)	http://www.smbus.org/specs/
Serial ATA Specification, Version 2.6	http://www.serialata.org/
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
BOSCH CAN Specification Version 2.0	http://www.semiconductors.bosch.de/pdf/can2spec.pdf

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1. Sightings Reports will only be available when there are sightings to report.
2. Contact your Intel Field Representative for the latest version of this document.

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2.0 Getting Started

This section identifies the key components, features and specifications of the development kit. It also describes how to set up the boards for operation.

Note: This manual assumes a familiarity with basic concepts involved with installing and configuring hardware for a PC.

Figure 1. Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit

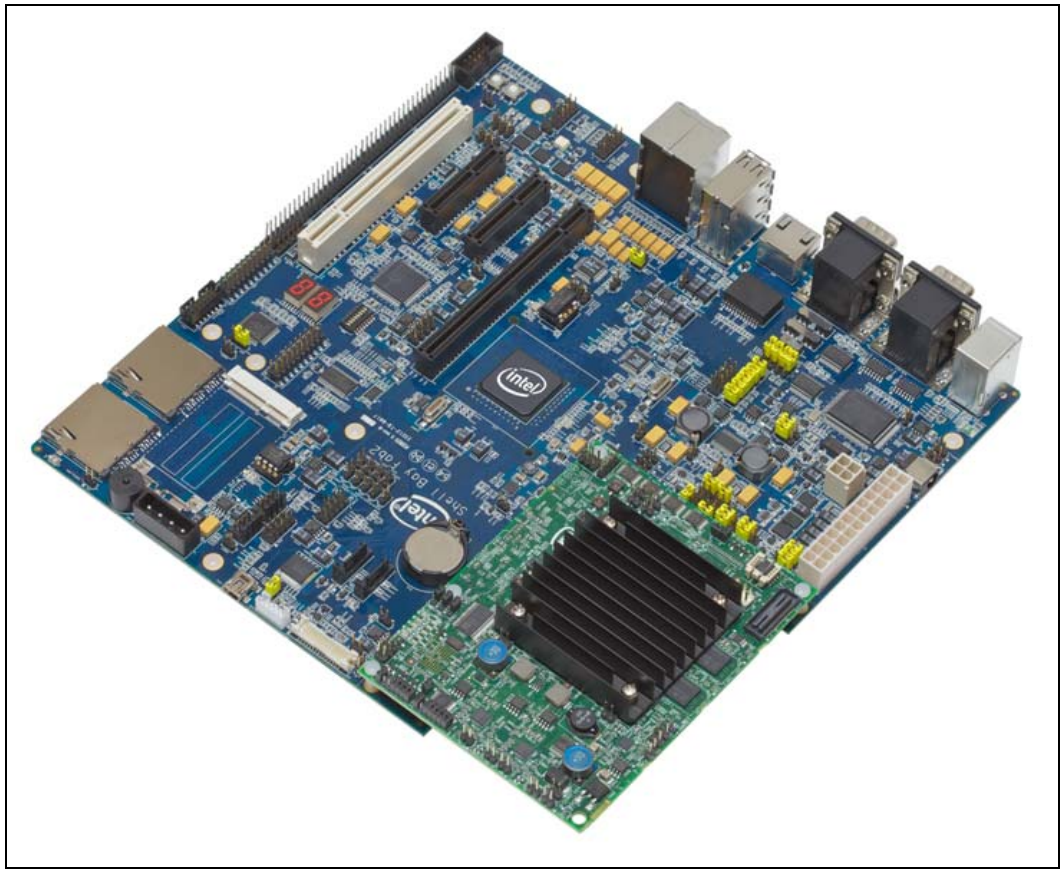
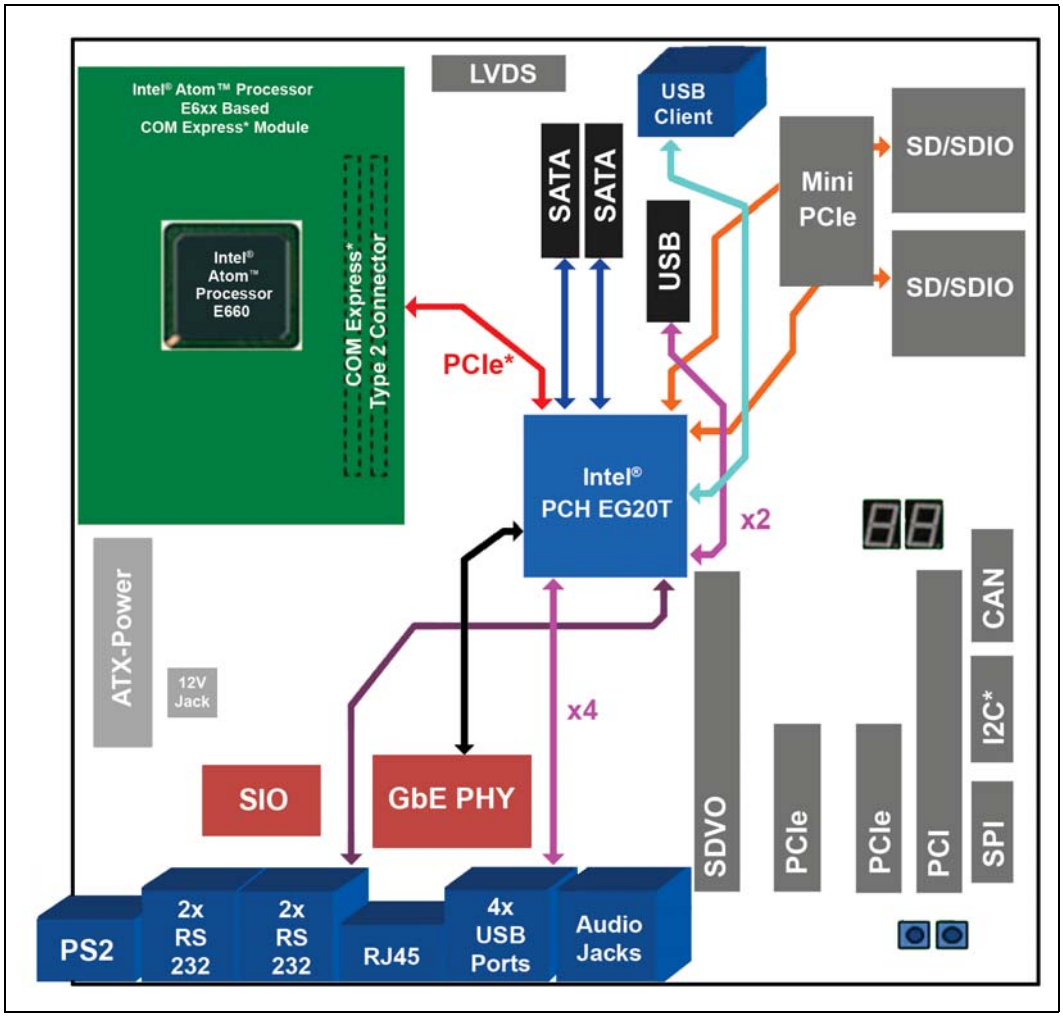


Figure 2. Block Diagram



Note: PCIe* x4 slots only have x1 connection.

2.1 Overview

The development kit contains the Intel® Atom™ Processor E660 (populated on the COM Express* module), other system board components and peripheral connectors and a carrier board with the Intel® Platform Controller Hub EG20T.

Note: The Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit is shipped as an open system, allowing maximum flexibility in changing hardware configuration and peripherals. Since the boards are not in a protective chassis, extra precaution is required when handling and operating the system. Review the document provided with the reference boards titled *Important Safety and Regulatory Information*. This document contains additional safety warnings and cautions.

2.2 Major Features

Table 5 lists the major features of the development kit.

Table 5. Development Kit Feature Set Summary (Sheet 1 of 2)

Feature	Board Implementation	Comments
Processor	Intel® Atom™ Processor E660 with 512KB L2 cache	Supports 0.6 GHz (Ultra Low Power SKU), 1.0 GHz (Entry SKU), 1.3 GHz (Mainstream SKU) or 1.6 GHz (Premium SKU) Intel® Atom™ Processor E660. 22 X 22 mm FCBGA package with 0.8 mm diagonal ball pitch and 676 pins.
CPU Voltage Regulator	Intel® Mobile Voltage Positioning 6 (Intel® MVP 6)	Single phase voltage regulators (U5C1, U5B2) on the COM Express module.
Board Size	Little Bay: 4.92 x 3.74 inch (125 x 95 mm) Shell Bay: 9.6 x 8 inch (243.84 x 203.2 mm)	Doubled-sided placement.
Memory	Single-channel DDR2, dual ranks, memory down on PCB, 800 MT/s data rate	Supports up to 2-GB of system memory, eight SDRAM devices max (4 on top and 4 on bottom), JEDEC standard DDR2, soldered down memory only
Main Clock	IDT* ICS9LPRS436 CK505 compliant clock	U4D1 on the COM Express module, TSSOP, 48-pin package
SPI	16Mbit SPI serial flash (SST25VF016B) on the COM Express module for storing boot code	2x4 header (J1A2) on the COM Express module for DediProg SF100* programmer
ITP Support	Extended Debug Port (XDP)	J1A1 XDP connector
Platform Controller Hub	Intel® PCH EG20T x1	Connects to the COM Express* Module by PCIe* x1
COM Express*	COM Express* (Type-2) Connector	Interface to the COM Express* module
LVDS	1 connector (from COM Express* connector) (30pin)	Single 18/24-bit LVDS interface; Back Light Inverter (BLI) and LED backlight support.
SDVO	1 slot of PCIe* x16 height vertical edge card connector (PCIe* Graphics) (from COM Express* connector)	Supports ADD2-N cards
PCIe* slot	2 slots of PCIe* x4 height vertical edge card connector via Pericom PI2PCIE212-D signal switch	Each slot is assigned PCIe* x1 signals (Not using x4 signals)
PCIe* Signal Switch	1	Pericom PI2PCIE212-D
PCIe* Mini Card	1 slot (alternate with a PCIe* slot) via Pericom PI2PCIE212-D signal switch	
PCIe*-PCI Bridge	1	Pericom PI7C9X111SL
PCI slot	1 slot via PCIe*-PCI Bridge	
SATA	2 ports from PCH	
USB 2.0 Host	4 ports of Type A receptacle from PCH, 2 headers from PCH	SMI pin of PCH is connected to COM Express* pin C63 for legacy USB support.
USB 2.0 Client	1 port from PCH	Connector: Mini-B receptacle
GbE	1 port from PCH, GMAC interface: RGMII	PHY chip: 1 Realtek RTL8211CL
SD/SDIO/MMC	2x SD Card slots with MMC (8bit) support	
UART	3xRS232C by DB-9 (1 of them from SIO), 1xRS485/RS232C selectable by DB-9 and header with flow control, via RS transceiver, 1 port by header from PCH directly	RS-232C Transceiver: MAXIM MAX3245ECAI+ RS-485 Transceiver: MAXIM MAX3076EESD+
SIO	1	SMSC LPC47M172

Table 5. Development Kit Feature Set Summary (Sheet 2 of 2)

Feature	Board Implementation	Comments
PS/2 KB	1 port from SIO	
PS/2 Mouse	1 port from SIO	
CPLD	Altera EPM570 MAXII system management CPLD on the COM Express module and POST code display CPLD (Port 80h decode) on the carrier board	POST code display CPLD: Xilinx XC9572XL
7-segment LED	2 digits from CPLD	From COM Express* connector
Buzzer	1	
LPC	1 header (20-pin); for SIO and CPLD	From COM Express* connector
Intel® TPM$^{\varepsilon}$	1 header (20-pin)	From COM Express* connector
Validation Header	1 header (40-pin)	From COM Express* connector
GPIO	1 header (12-pin)	From PCH
Intel® HD Audio$^{\beta}$	1 header (10-pin) from Audio Codec	1 Realtek ALC888 CODEC
7.1 Audio Jacks	1 port (Stereo Jack x 6) from Audio Codec	
I^2C*	1 header (4-pin) from PCH	
SPI	1 header (10-pin) from PCH	
CAN	1 header (4-pin) from PCH via CAN transceiver	Transceiver: NXP TJA1040T
JTAG Port	2 headers (PCH (6-pin), CPLD(14-pin))	
Serial ROM	DIP 8-pin socket x 1 to store SATA Option ROM & Ethernet MAC Address	SPI EEPROM: Microchip 25LC512-I/P
Clocks for PCH	Crystal Oscillator: 3 CLK Buffer: 1 (for PCIe*) CLK Generator: 1 (for SATA)	SYSCLK: Osc (25MHz) USBCLK: Osc (48MHz) UARTCLK: Osc (1.8432MHz) SATACLK: CLK Gen (75MHz) PCIeCLK: CLK Buff (100MHz)
Push buttons	Power x 1, Reset x 1	
PCB Specification	8 layers, thickness: 63 mils (1.6mm), Halogen Free Multilayer Material	All components are RoHS compliant
Temperature	Operation: 0 to 40°C Storage: -20 to 85°C	
Humidity	Operation: 20 to 80% Storage: 5 to 95%	
Power Supply	ATX connector x1 12V ATX connector x1 DC Jack: for AC Adapter (+12V, 5A)x1 CMOS Battery (CR2032) x1	Power indicated LED and header
Power management (ACPI)	ACPI Compliant	S0 – Power On S3 – Suspend to RAM (S4 – Suspend to Disk) S5 – Soft Off

2.3 Processor Support

The COM Express* module comes with 1.3 GHz Intel® Atom™ Processor E660 with 512-KB cache in a 676 pins, FCBGA package.

Note: A heatsink is required for the 1.0 GHz or above processor SKU during room temperature ambient operation.

2.3.1 Processor Voltage Regulators

The COM Express* module uses an onboard Intel® MVP6 single-phase regulator for the processor core supply. The I/O voltage is 1.05 V.

2.4 COM Express* Module Support

The carrier board supports the COM Express* module with the Intel® Atom™ Processor E660. A heatsink is required for the 1.0 GHz or above processor SKUs during room temperature ambient operation.

2.5 Subsystem Descriptions

Subsystem features refer to the component, slot and connector locations on the carrier board. Component, slot and connector locations are labeled with a letter-number combination. Refer to the silkscreen labeling on the carrier board for location details. Refer to Chapter 4.0 for more information.

2.5.1 Intel® Atom™ Processor E660

- Single channel 32-bit DDR2 memory interface running at 800 MT/s
- Four PCI Express* ports, x1
- Intel® HD Audio$^{\beta}$
- One channel 18- or 24-bit LVDS
- One channel SDVO
- SPI bus

2.5.2 COM Express* Connector

The carrier board contains a COM Express* interface connector for stacking the COM Express* module. This connector is based on the Type 2 pinout, which is defined in the COM Express* specification by PICMG*.

However, the carrier board does not support several functions in this pinout. Table 6 lists the COM Express* interface functions supported on the carrier board.

Table 6. COM Express* Interface Implemented Signals (Sheet 1 of 2)

COM Express* Function	Type 2 Description	Carrier Board
LVDS	A&B ch, dedicated I^2C*	A channel only
VGA	1ch, Analog RGB, dedicated DDC	No support[1]
TV-Out	1ch, Composite Video, S-Video, Component Video	No support[1]
LAN	1 port, Gigabit or 100/10 Base	No support[1]
SATA	4 ports, SATA 150-300	No support[1]

Table 6. COM Express* Interface Implemented Signals (Sheet 2 of 2)

COM Express* Function	Type 2 Description	Carrier Board
ExpressCard*	2 ports, Tx/Rx is shared with PCI Express*	No support[1]
PCI Express*	6 ports, PCIe* REFCLK	4 ports
USB 2.0	8 ports, Over Current detection	No support[1]
LPC	1 port, Low Pin Count Interface	Super I/O (PS2), CPLD (POST Indication), Pin Header
AC'97/ Intel® HD Audio$^{\beta}$	1 port, Audio Codec '97, Intel® High Definition Audio$^{\beta}$ Interface	Audio Codec IC
I^2C*	1ch, Inter-Integrated Circuit	Option EEPROM for PCI Bridge IC
SMB	1ch, System Management Bus	PCIe*/miniPCIe/SDVO/ PCI/SIO/PCIe* CLK Buff/PCI Bridge IC
PCI	1 port, PCI Bus 32bit 33/66MHz	No support[1]
PATA	1 port, Parallel ATA100	No support[1]
PCI Express* Graphics (SDVO)	1 port, Share with SDVO dedicated I^2C* and PCI Express* Graphics x16	SDVO (PEG) slot

Notes:
1. The associated signals are not connected.

2.5.3 Intel® Platform Controller Hub EG20T

The Intel® PCH EG20T was developed for IO extension of the processor. The features of the Intel® PCH EG20T provide the functionality necessary for storage and connectivity as well as functionality normally associated with handheld devices such as SDIO/MMC and USB device.The Intel® PCH EG20T has several functions as follows:

- Interface to processor of PCI Express* x1 lane (Gen1)
- One GMAC interface for Gigabit Ethernet
- Two SATA ports, Gen2
- Six USB 2.0HS Host compatible ports
- One USB 2.0HS Client compatible port
- Two SDIO/MMC interfaces
- Four UART interfaces
- One CAN interface
- One Serial Peripheral Interface (SPI)
- One I^2C* interface
- One 12-bit GPIO interface
- One SPI Serial ROM interface

Note: For details, see the *Intel® Platform Controller Hub EG20T Datasheet*.

2.5.4 System Memory

- Supports DDR2 soldered down memory.
- Supports 800 MHz memory bus frequencies.

2.5.5 Display

The carrier board has two options for display as follows. Refer to Figure 11 for the location.

- LVDS – location is X4
- SDVO – location is X9

Note: The Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit supports single channel LVDS only. Table 7 lists the displays that have been tested with the kit.

Table 7. Supported LVDS Displays

Manufacturer	Size	Resolution	Back Light	Aspect Ratio	Part#
LG Display (18-bit color)	13 inch (330.2 mm)	1366 x 768	LED	16:9	LP140WH1-TLA1
AUO Display (24-bit color)	8.4 inch (213.4 mm)	800 x 600	LED	4:3	G084SN05 V8

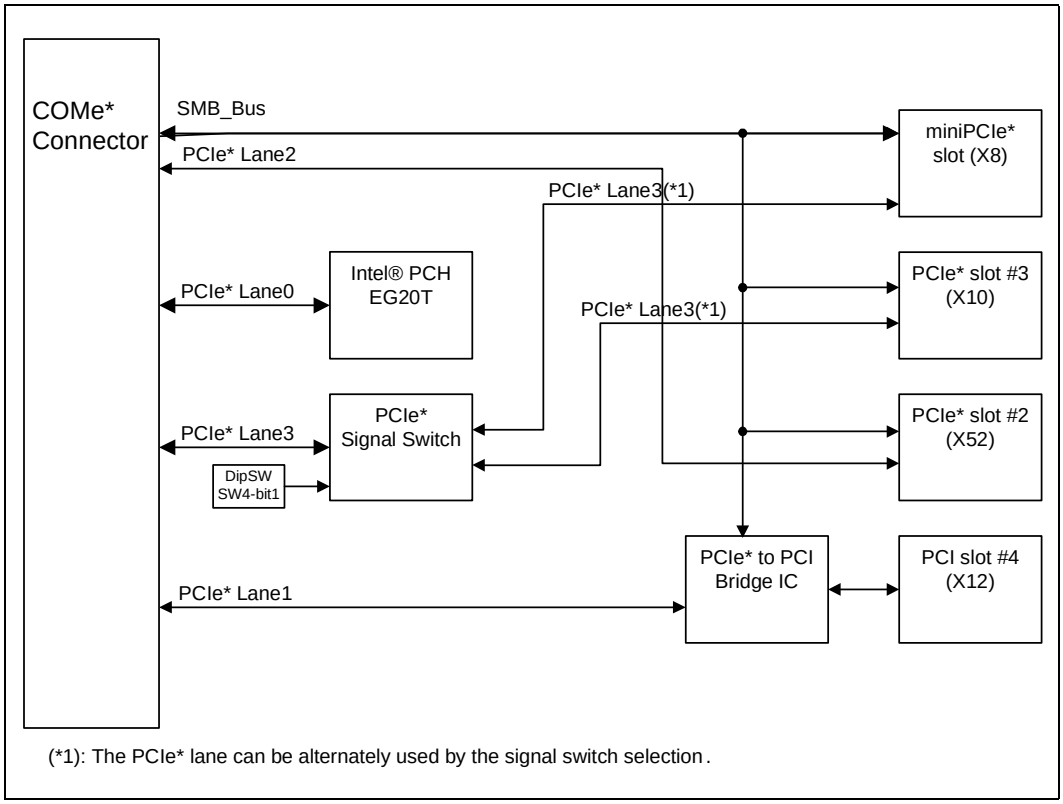
Notes:
1. The protective tape on top of the LVDS connector must be removed prior to installing an LVDS cable.
2. VGA output is not directly supported. Customers can use PCI Express*-based x1 discrete external 3D graphics cards, or a third-party component available on an ADD2-N card through the SDVO interface.

2.5.6 PCI Express* Slots/ PCI* Slots

- Two PCIe* x1 ports connect to x4 PCIe* slots (X10, X52) for add-in cards. The X10 slot is alternately used with a PCIe* mini card slot (X8).
- One PCIe* mini card slot (X8) for mini PCIe* card module. This slot is alternately used with PCIe* slot (X10).
- One PCI slot (X12) for PCI add-in card
- One PCIe* signal switch is used to alternate between the connected devices
- The PCIe* bus complies with the PCI Express* Rev. 1.0a specification.

Figure 3 describes the carrier board PCIe* connection.

Figure 3. PCI Express* Block Diagram of the Carrier Board



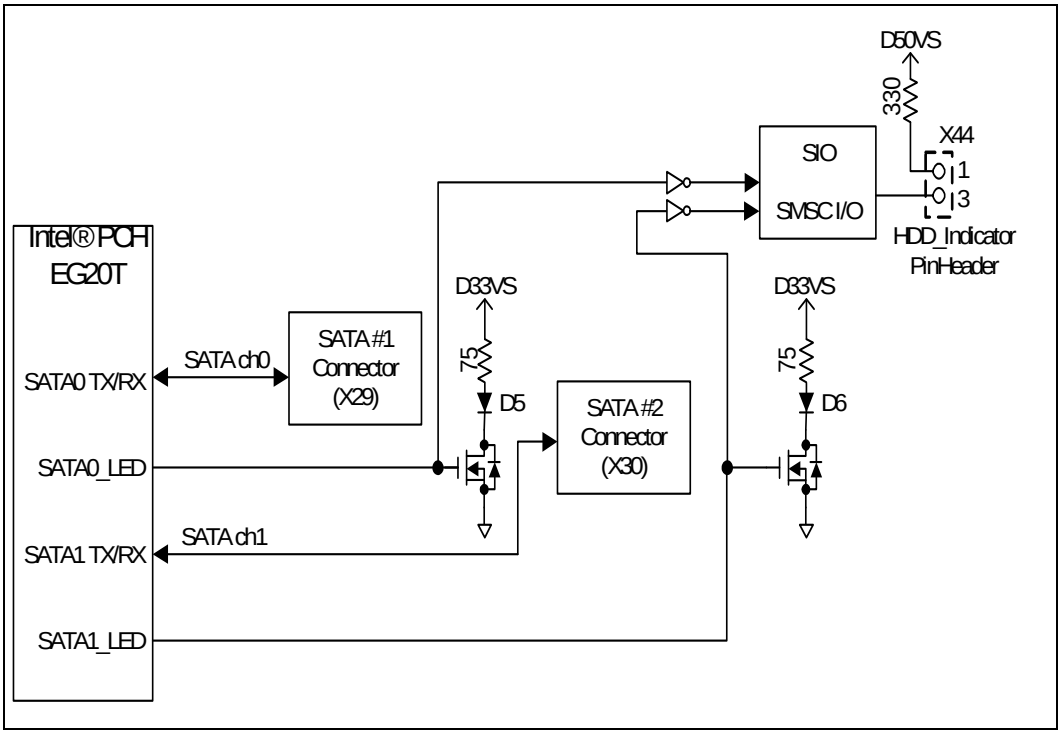
2.5.7 SATA Connectors

The carrier board provides two SATA connectors. These connectors (X29, X30) are connected to the Intel® PCH EG20T for SATA Gen 1 or Gen2 compliance devices.

There is one peripheral power connector (X48) provided for the purpose of powering external devices such as a SATA drive.

Figure 4 describes the carrier board SATA interface connection.

Figure 4. SATA Block Diagram in the Carrier Board



2.5.8 USB Connectors

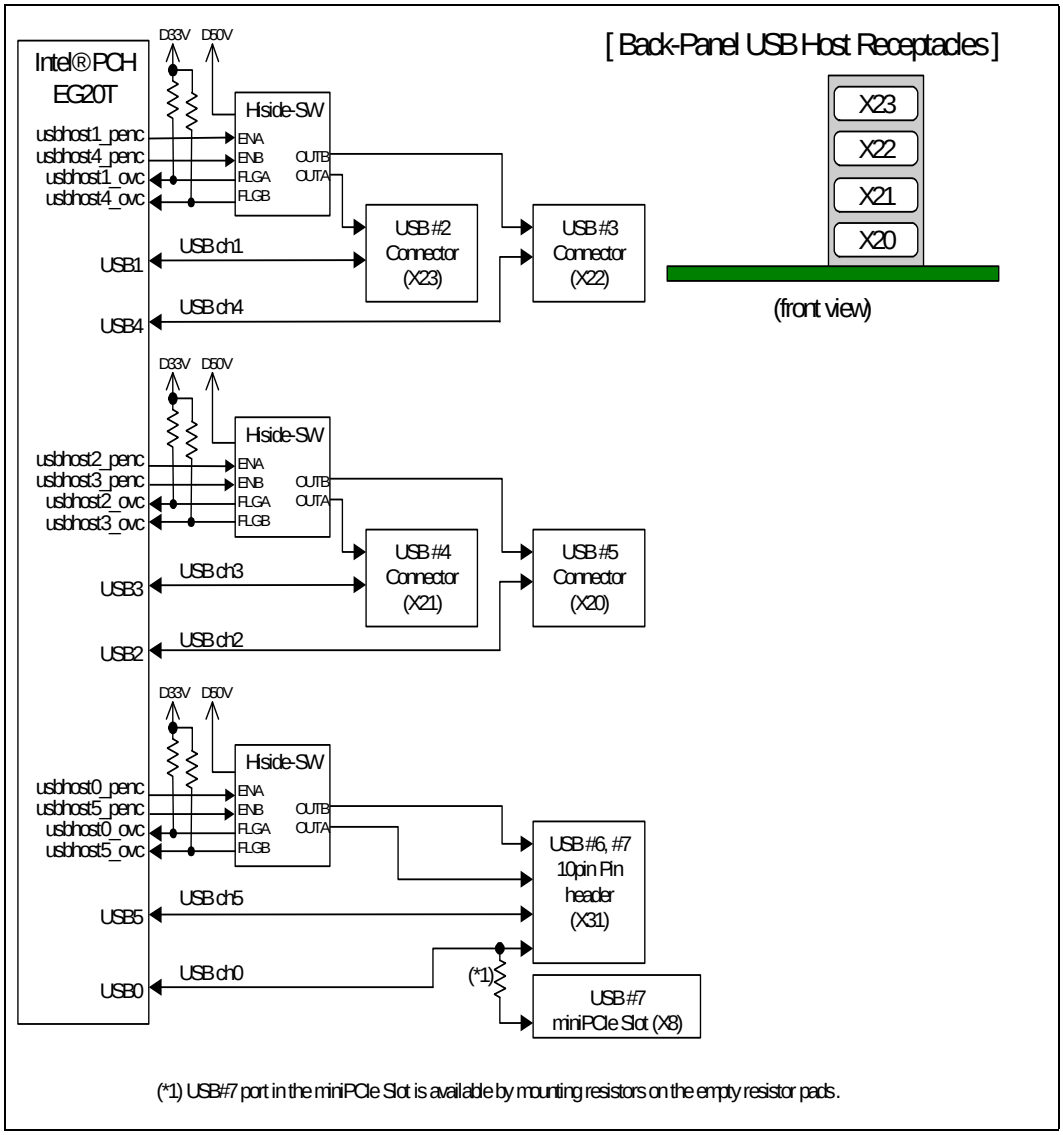
The carrier board has six USB Host ports with stackable standard Type-A receptacles (X20 – X23) for rear panel, two USB Host ports with 10 pin header (X31) for front panel and one USB client port with mini B receptacle (X45) for front panel. The functionality of these ports are provided by the Intel® PCH EG20T.

Note: The two USB Host ports that are routed to the front panel side's pin header (X31) from the Intel® PCH EG20T can be connected to the mini PCIe* slot. The mini PCIe* slot USB port is enabled by stuffing resistors on R409 and R410 and removing resistors on R407 and R408.

Each USB Host port on the carrier board has a USB high side switch that is a low current output type (ROHM BD2052AFJ* Continuous current load: 0.50A by a port) in the VBUS output for the purpose of validating the Intel® PCH EG20T. Therefore, additional power supply may be necessary depending on the USB device to connect.

Figure 5 describes the carrier board USB-Host interface connection.

Figure 5. USB-Host Block Diagram in the Carrier Board



2.5.9 Gigabit Ethernet Connector

The carrier board provides one Gigabit Ethernet interface from the Intel® PCH EG20T via a Realtek RTL8211CL* Gigabit Ethernet PHY transceiver. The Gigabit Ethernet port (X26) is routed to the rear I/O panel's stacked receptacle.

2.5.10 SD/SDIO/MMC

The carrier board provides two SD/SDIO/MMC ports (X5, X6) with the following features:

- All ports are SD rev1.1 specification compliant and MMC rev4.0 specification compliant.
- All ports operate to 48 MHz and support 8-bit operation.

2.5.11 UART

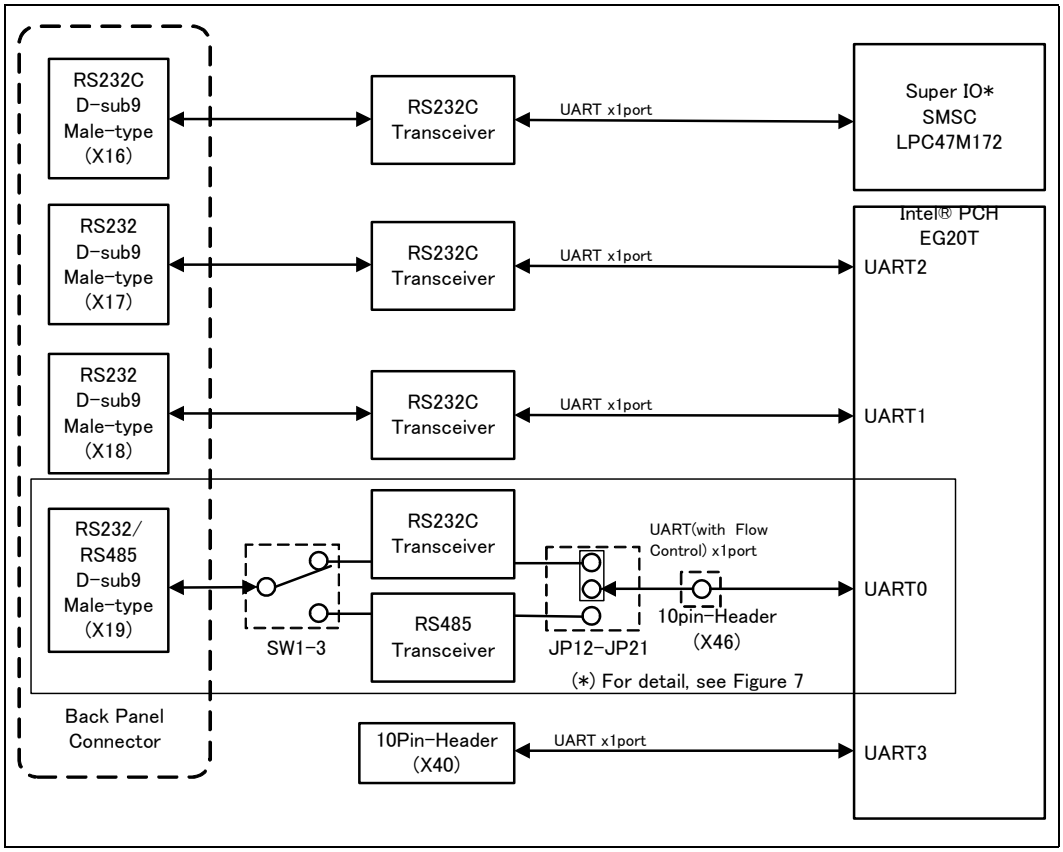
The carrier board provides five UART ports for use in the system.

Four UART ports are provided from the Intel® PCH EG20T and one UART interface is provided from the SIO (SMSC LPC47M172*). The features of these ports are as follows:

- Intel® PCH EG20T UART feature:
  - UART port 0:
    - Assigned rear I/O panel's D-Sub 9pin stacked connector (X19) via a RS-232C transceiver MAXIM MAX3245ECAI+* or via two RS485 transceivers MAXIM MAX3076EESD*. The alternate selection is done by switches (SW1-SW3) and jumpers (J16-J21) on the board. UART0 is connected to a 2x5 2.54mm pin header (X46) directly.
    - Standard 16550 Compatible UART with Send/Receive 256-Byte FIFOs
    - The receive FIFO generates 3-bit error data per byte
    - Supports 300k and 4Mbps Baud Rate but X19 port supports up to 1Mbps following RS-232C transceiver's specification.
    - Programmable Baud Rate Generator
    - Enables auto hardware flow control of the Intel® PCH EG20T
  - UART port 1-3:
    - Assigned rear I/O panel's D-Sub 9pin stacked connectors (X17; UART2, X18; UART1) via a RS-232C transceiver MAXIM MAX3245ECAI+*. UART3 is connected to a 2x5 2.54mm pin header (X40) directly.
    - Standard 16550 Compatible UART with Send/Receive 64-Byte FIFOs
    - The receive FIFO generates 3-bit error data per byte
    - Supports 300k and 1Mbps Baud Rate
    - Programmable Baud Rate Generator
  - SIO (SMSC LPC47M172*)'s UART feature:
    - Assigned rear I/O panel's D-Sub 9pin stacked connector (X16) via a RS-232C transceiver MAXIM MAX3245ECAI+*.
    - High Speed 16C550A Compatible UART with Send/Receive 16-Byte FIFOs
    - Supports 230k and 460k Baud Rate
    - Programmable Baud Rate Generator

Figure 6 and Figure 7 describe the carrier board UART interface connection.

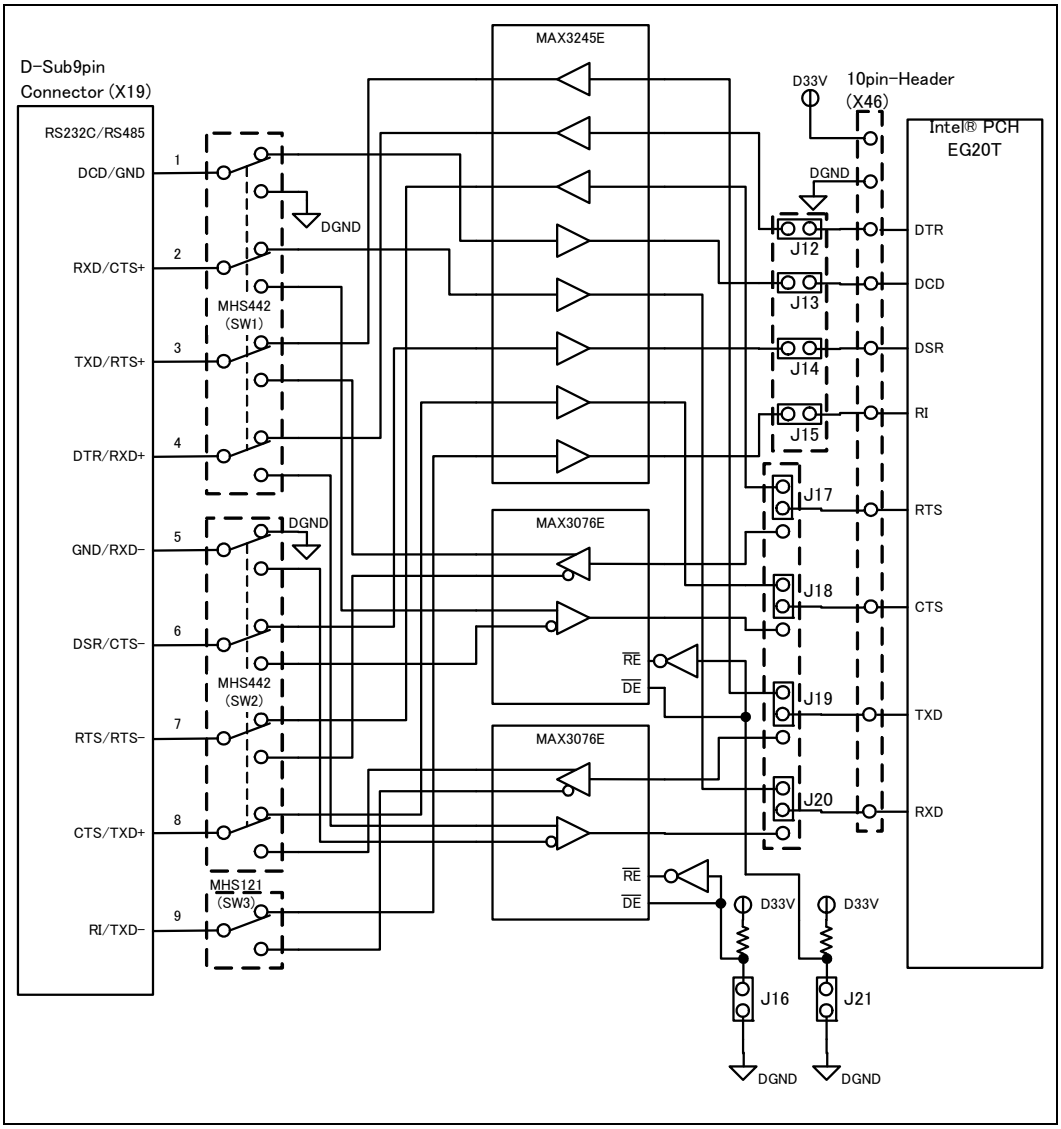
Figure 6. UART Block Diagram in the Carrier Board



Note: For UART0 port, it is necessary to configure switches and jumpers for RS transceiver selection. See Section 4.3.1 for details.

Caution: Do not change the setting after powering on the system. Be careful to configure proper setting if the intention is to change the setting. A fault in the setting could damage the platform, the interconnecting cable, or the attached external device.

Figure 7. Intel® Platform Controller Hub EG20T UART Port0 Connection Diagram in the Carrier Board



Note: For the UART0 port, it is necessary to configure switches and jumpers for RS transceiver selection. See Section 4.3.1 for details.

Caution: Do not change the setting after powering on the system. Be careful to configure proper setting if the intention is to change the setting. A fault in the setting could damage the platform, the interconnecting cable, or the attached external device.

2.5.12 I²C*

The carrier board provides one I²C* port from the Intel® PCH EG20T that conforms to the typical I²C* bus specification. It operates as a master or slave device and supports a multi-master bus. The Intel® PCH EG20T I²C* port is connected to the 1x4 2.54mm pin header (X37) and 2x5 2.54mm pin header (X38) directly.

2.5.13 SPI

SPI serial flash device (P/N# SST25VF016B) on the COM Express module stores the boot code. The boot firmware can be programmed through an in-system programming tool from Dediprog. A 2x4 2.54 mm pin header is provided on board for use to program the SPI flash. Refer to Chapter 5.0 for more information.

The carrier board provides one serial peripheral interface (SPI) from the Intel® PCH EG20T for use in the system. The Intel® PCH EG20T SPI is connected to the 2x5 2.54mm pin header (X38) directly.

This port can be used to connect the protocol analyzer of Total Phase Beagle* I²C*/SPI/MDIO.

2.5.14 CAN

The carrier board provides a CAN interface from the Intel® PCH EG20T for use in the system. This CAN controller performs communication in accordance with BOSCH CAN Protocol Version 2.0B Active[1] (standard format and extended format). The bit rate can be programmed to a maximum of 1Mbit/s based on the technology used. The Intel® PCH EG20T CAN bus is connected to the 1x4 2.54mm pin header (X39) via CAN transceiver NXP TJA1040T*.

When communicating in a CAN network, individual message objects (see the CAN Message Objects section in the Message RAM section of the Intel® PCH EG20T datasheet) are configured. The message objects and identifier masks for the receive filter for the received messages are stored in the message RAM.

2.5.15 Serial ROM

The Intel® PCH EG20T provides Serial ROM interface for use of Option ROM data loading through SPI. This Serial ROM interface has the following two roles.

- Initialization with hardware for Ethernet function and PCI configuration (Packet Write mode).
  - — Initialization of MAC-address of Gigabit Ethernet
  - — Initialization of “Subsystem ID” or “Subsystem Vendor ID” of each PCI device in the Intel® PCH EG20T
- Access to Option ROM space for SATA AHCI function (ROM mode).
  It is used to support a single SPI compatible EEPROM device with 8pin DIP socket (X32). This SPI EEPROM device has some limitations. The following are requirements for selecting connectable SPI EEPROM:
  - — Supporting 5 MHz Read and Write
  - — Supporting Page Write Mode more than 4 bytes
  - — Memory size is up to 512 Kbit from 8 Kbit

Microchip 25LC512-I/P* meets the requirements mentioned above and is installed on the SPI EEPROM Socket (X32) on the carrier board.

Note: Please use the following utilities for programming the Serial EEPROM for MAC address or SATA AHCI Option ROM
(link: http://sourceforge.net/projects/generalembedded/files/)

- — phub_util_orom.tar.bz2
- — phub_util_mac.tar.bz2

1. Defined by ISO 11519, ISO 11898, and SAEJ2411.

2.5.16 LPC Bus

The LPC bus connects to these devices on the carrier board:

- SMSC LPC47M172 Super I/O*
- Xilinx XC9572XL* POST code display CPLD
- Intel® TPMε header (X35)
- LPC debug header for LPC testing (X34)

Note: LPC DMA is not supported by the processor on the Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit.

2.5.16.1 Super IO (SIO)

The LPC47M172 serves as legacy PS/2* keyboard and mouse controller on the carrier board. The LPC47M172 Super I/O supports:

- LPC interface
- One UART serial port at the rear I/O panel (see Section 2.4.10)
- Two PS/2 ports located at the rear I/O panel

2.5.16.2 POST Code Display CPLD

I/O writes to port 80h on LPC bus are decoded by the Xilinx XC9572XL* device on the carrier board and displayed on two 7-segment LEDs.

2.5.16.3 Intel® Trusted Platform Moduleε (Intel® TPMε) Header

The carrier board implements a header (X35) that supports Intel® TPMε 1.2 specification compliant devices.

2.5.17 Intel® High Definition Audioβ (Intel® HD Audioβ)

The Intel® HD Audioβ is enabled through the Realtek ALC888* CODEC. Six port Intel® HD Audioβ jack (X27) is provided on the rear I/O panel. No SPDIF receptacle is provided on the carrier board. For the front panel, only a 2x5 header (X36) is provided.

2.5.18 Clocks

The COM Express* Module uses a CK-505 clock solution. The BSEL [2:1] signals driven by the processor are used by the CK-505 to configure the processor external reference clock.

The carrier board uses several clocks. Figure 8 describes the clock circuit connections in the carrier board. Figure 9 describes the change required to connect the Intel® PCH EG20T clock circuit in the carrier board when using the custom CK505 clock generator on the COM Express module.

Figure 8. Clock Circuit Diagram in the Carrier Board

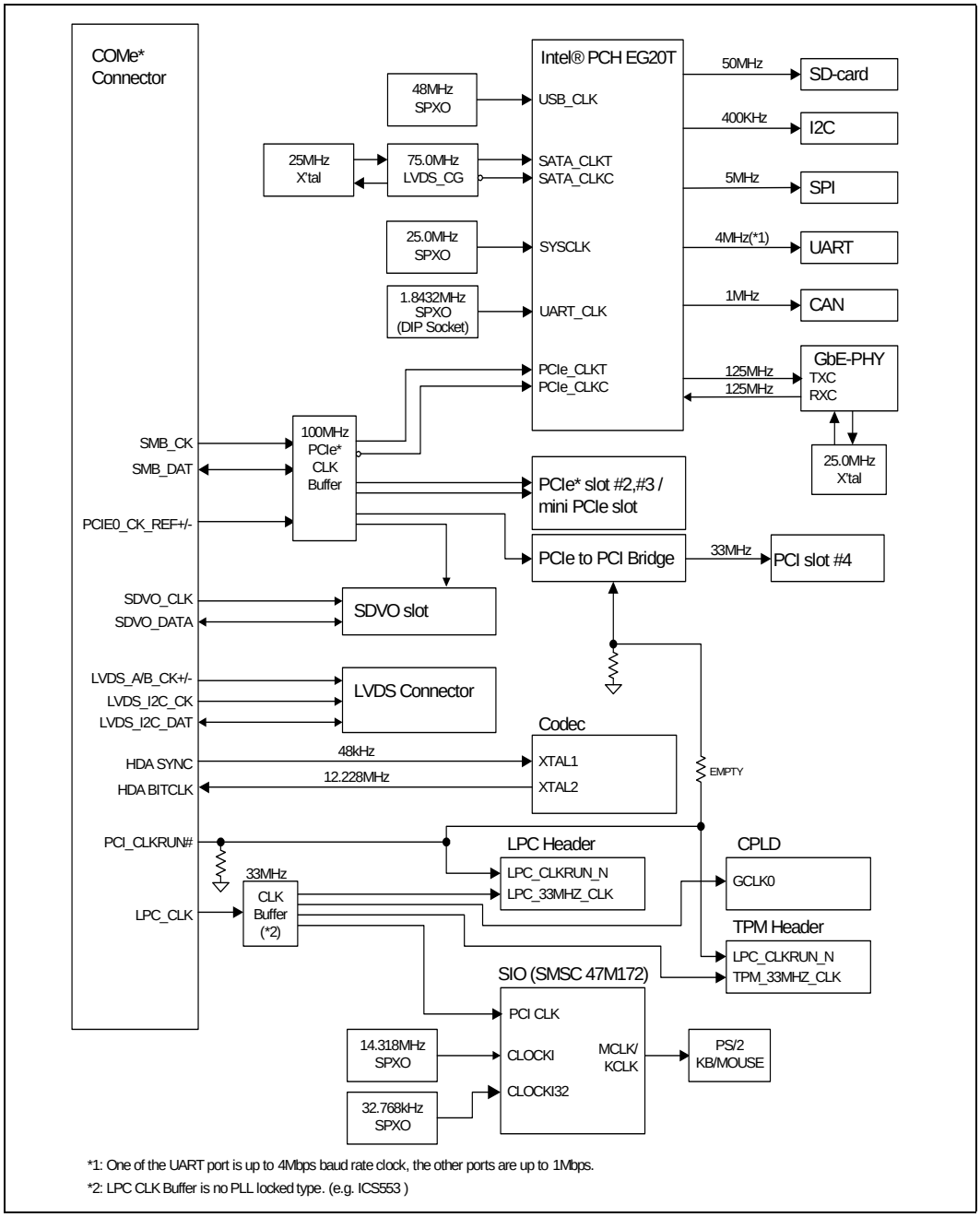
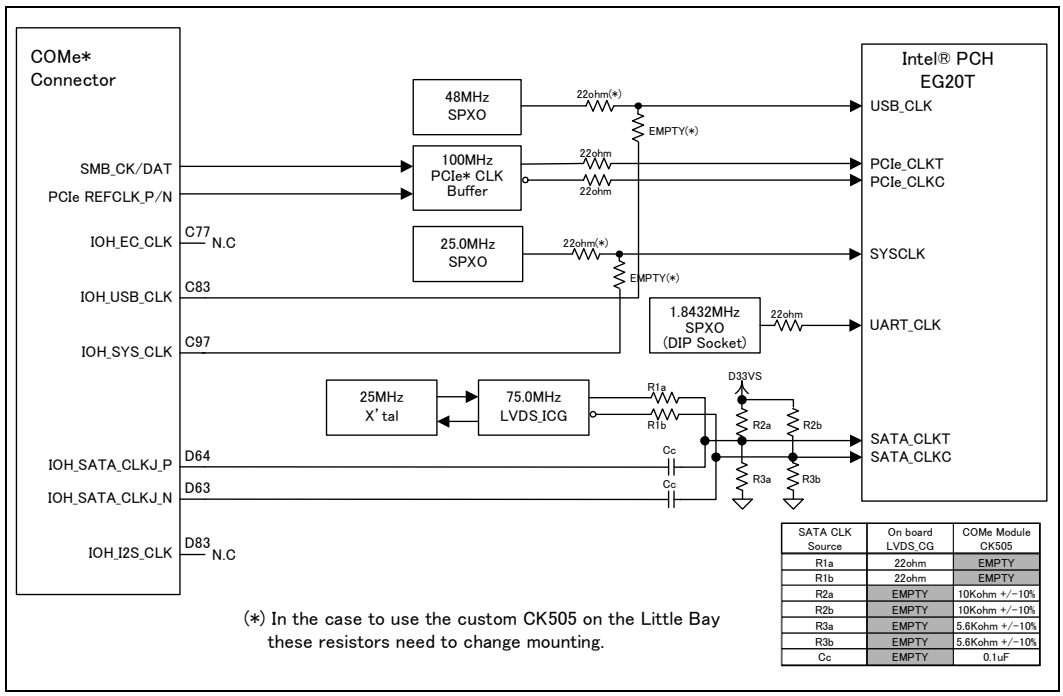


Figure 9. Clock Changing Circuit Diagram for the Intel® Platform Controller Hub EG20T in the Carrier Board



2.5.19 Real Time Clock

An on-board battery on the carrier board maintains power to the real time clock (RTC) on the COM Express module when in mechanical off state (G3 state).

2.5.20 In-Target Probe (ITP) and Debug Support

The development kit provides on-board ITP support with an XDP connector on the COM Express* Module. You can debug from the reset vector without EFI or OS dependency (up to OS functionality). Ports 80-83 are provided as a troubleshooting tool to monitor POST output during EFI execution.

ITP requires that the CMC be loaded to configure the Intel® Atom™ Processor E660 before register accesses can be made. The CMC code resides in the SPI flash on the COM Express* module. The SPI flash must be programmed to use ITP.

2.5.21 Power Supply Solution

The development kit can be powered from an ATX power supply (desktop solution) that contains all of the voltage regulators necessary to power the system up. Additionally, battery or AC adapter support is provided through +12VDC input.

The characteristic of using AC adapter or battery pack is slightly different from using an ATX power supply:

- Due to the low current rating of the AC adapter, the carrier board does not support a full load of extension slots (SDVO, 2 PCIe* and PCI slots). When using these extension slots, please use an ATX power supply.
- In the case of using the AC adapter, it is recommended that the carrier board be connected to the LVDS LCD module and an external 2.5" hard disk only. When using AC adapter, please supply power to the hard disk using the power supply connector (X48) on the carrier board. If using the X48 connector, the customer must prepare a hard disk power cable that converts to the adaptive connector.
- Using the AC adapter is allowed as long as the total of the system current consumption is not beyond the rating output of the used AC adapter. Please use available AC adapter that has the rating output of 6.5A or less.

Note: Use an UL94V-1 minimum compliant AC adapter that provides 80 Watts of continuous output power. For example, the Sinpro Electronics Model No. SPU80-105* meets this requirement.

Use an ATX12V 1.1 specification compliant power supply regardless of maker or wattage level (an ATX12V rating means V5 min current =0.1 A vs. an ATX V5 min current = 1.0 A, among other differences). For example, the Sparkle* Model No. FSP300-60BTV meets this requirement and is an ATX12V 1.1 specification compliant power supply.

If the power switch on the ATX power supply is used to shut down the system, wait at least 5 seconds before turning the system on again.

The recommended way to shut down the board is through software or by pressing and holding the power button switch (SW5) for 5 seconds until the power supply turns off.

Using the power supply switch or pulling the plug out of the wall is not recommended.

2.5.22 Board Size

The form factor of the carrier board follows Micro ATX 9.6 x 8 inch (243.84mm x 203.2mm) specification. The back panel jacks may not conform to ATX specifications.

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3.0 Power Management

3.1 Power Measurement Support

The development kit has power measurement for each IO circuit and device validation. Power measurement resistors are provided to measure the power on many of the subsystems. Table 8 lists the measurement resistors.

Table 8. Power Measurement Resistors

Feature	Resistor-1	Resistor-2	Resistor-3
Tolerance	1%	1%	5%
Value	10 mΩ	10 mΩ	2 mΩ
Watt	0.5W	0.75W	2W
Package Size (inch)	0805	1206	2512

Note: Intel recommends that larger (~10 mΩ) resistors be stuffed for greater accuracy.

Power on a particular subsystem is calculated using the following formula:

Equation 1. $P = V^2/R$

R = value of the sense resistor (typically 0.01 Ω)

V = the voltage difference measured across the sense resistor.

Use a high precision digital multi-meter tool such as the Agilent 34401A digital multi-meter.

Refer to Table 9 for a comparison of a high-precision, digital multi-meter (Agilent 34401A) versus a precision, digital multi-meter (Fluke 79).

Table 9. Digital Multi-Meter Comparison

Example System	
Sense Resistor Value	0.01 Ohm
Voltage Difference Across Resistor	1.492 mV (149.2 mA)
Calculated Power	0.223 mW

Digital Multimeter	Agilent 34401A ($6\frac{1}{2}$ digit display)	Fluke 79 (3 digit display)
Specification	(+/- 0.0030% of reading) + (+/- 0.0030% of range)	0.09% +/- 2 digits
Min voltage displayed Calculated power	1.49193 mV 0.22258 mW	1.47 mV 0.216 m
Max voltage displayed Calculated power	1.49206 mV 0.22624 mW	1.51 mV 0.228 mW
Error in power	+/- 0.009%	+/- 0.3%

Note: The precision achieved by using a high precision digital multi-meter versus a normal digital multi-meter is ~33 times more accurate.

Table 10 summarizes all the power measurement sense resistors located on the carrier board. All sense resistors are 0.01 Ω unless otherwise noted.

Table 10. Carrier Board Voltage Rails (Sheet 1 of 3)

Schem Page	Target Component	Voltage	Supply Power Rail	Rail	Ref Des	Resistor Spec
13	PCIe* Slot #2	12V	D120Vslot	D120VSlot_PCIE_SLOT2	R35	Resistor-2
13	PCIe* Slot #2	3.3V	D33VSlot	D33VSlot_PCIE_SLOT2	R37	Resistor-2
13	PCIe* Slot #2	3.3V	D33V	D33V_PCIE_SLOT2	R38	Resistor-1
13	PCIe* mini Card	1.5V	D15VS	D15VS_EXCD_MINI	R40	Resistor-1
13	PCIe* mini Card	3.3V	D33V	D33V_EXCD_MINI	R42	Resistor-1
14	PEG Slot #1 SDVO	12V	D120VSlot	D120VSlot_SDVO	R48	Resistor-2
14	PEG Slot #1 SDVO	3.3V	D33VSlot	D33VSlot_SDVO	R49	Resistor-2
15	PCIe* Slot #3	12V	D120VSlot	D120VSlot_PCIE_SLOT3	R391	Resistor-2
15	PCIe* Slot #3	3.3V	D33VSlot	D33VSlot_PCIE_SLOT3	R392	Resistor-2
15	PCIe* Slot #3	3.3V	D33V	D33V_PCIE_SLOT3	R390	Resistor-1
19	LVDS	12V	D120VS	D12VS(1pin: VDD_BLI)	R269	Resistor-1
19	LVDS	5.0V	D50VS	D50VS(4pin: VDD_DBC)	R270	Resistor-1
19	LVDS	3.3V	D33VS	D33VS(18pin: VDD_VCL)	R274	Resistor-1
19	LVDS	3.3V	D33VS	D33VS_LVDS_VDDVDL (16,17pin: VDD_VDL1,2)	R275	Resistor-1
22	SATA_HDD	5.0V	D50VS_HDD	D50VS for HDD_POW	R405	Resistor-2
23	SD Slot 1(X5)	3.3V	D33VS	D33VS_SD_SLOT0	R299	Resistor-1
23	SD Slot 2(X6)	3.3V	D33VS	D33_VS_SD_SLOT1	R395	Resistor-1
26	Hiside SW for D50V_D50VS_USB_Port2,3	5.0V	D50V_D50VS_USB2_5	Hiside SW Pow for D50V_D50VS_USB_Port2, 3	R151	Resistor-1

Table 10. Carrier Board Voltage Rails (Sheet 2 of 3)

Schem Page	Target Component	Voltage	Supply Power Rail	Rail	Ref Des	Resistor Spec
26	Hiside SW for D50V_D50VS_USB_Port4,5	5.0V	D50V_D50VS_USB2_5	Hiside SW Pow for D50V_D50VS_USB_Port4,5	R158	Resistor-1
27	Hiside SW for D50V_D50VS_USB_Port0,1	5.0V	D50V_D50VS_USB_SIO	Hiside SW Pow for D50V_D50VS_USB_Port0,1	R155	Resistor-1
28	Hiside SW for D50V_D50VS_USB_Port6,7	5.0V	D50V_D50VS_USB6_7	Hiside SW Pow for D50V_D50VS_USB_Port6,7	R163	Resistor-1
35	Intel® TPMε Header	5.0V	D50VS	D50VS for Intel® TPMε Header(6pin)	R278	Resistor-1
35	Intel® TPMε Header	3.3V	D33VS	D33VS for Intel® TPMε Header (9pin)	R279	Resistor-1
35	Intel® TPMε Header	3.3V	D33VA	D33VA for Intel® TPMε Header (15pin)	R283	Resistor-1
36	AUX Pow Supply	12V	AUX_+12V	ATX_+12V	R402	Resistor-3
37	P-ch MOSFET(Q19) for D50VA and +5VB_D50VA	5.0V	D120VA	D50VA via Power SW Reg	R396	Resistor-3
37	P-ch MOSFET(Q26) for D33VA	3.3V	D120VA	D33VA via Power SW Reg	R397	Resistor-3
37	Power Switch for D50V, D50VS, D50DS_HDD, D50V_D50VS_USB2_5, D50V_D50VS_USB6_7 and D50V_D50VS_USB_SIO, Validation Header (X33),FP Header (X44), COM Express* Conn (XAB)	5.0V	D120VA	+5VB_D50VA and D50VA	R398	Resistor-3
37	Reset IC for D33VA_D33V,D25VA DLY, Reset IC for D33V_D33VS,D50V_D50VS DLY, Reset IC for D33VS DLY, Switching Regulator for D12VA, FET-SW for D33VA_D33V, LDO Regulator for D25VA, FET-SW for D33VA_D33VS, FET-SW for D33VS, FET-SW for D12V, FET-SW for D33V, LDO Regulator for D18VS,LDO Regulator for D10V, LDO Regulator for D15VS, FET-SW for D10VS, FET-SW for D12VS, Intel® TPMε Header, POW LED(D1), PCI Bridge EEPROM Sel, CK505 for PCH	3.3V	D120VA	D33VA	R399	Resistor-3
38	PWR_OK Circuit,D50VA FET Circuit (Q19, Q20),D33VA FET Circuit (Q26, Q25),D120VS FET Circuit (Q11),D120VSlot FET Circuit (Q21),Switching Regulator for D50VA,D33VA (U61)	12V	ATX_+12V or DC_+12V	D120VA	R294	Resistor-3
43	25MHz OSC for PCH, GbE PHY, GbE LED,PCH(PLA), GbE Reset IC	3.3V	D33VA	D33VA_D33V	R435	Resistor-1
43	PCH UART CLK, PCH(PLB),LPC CLK Buf, SIO,32.768kHz OSC for SIO,RS232C Drv, RS485 Drv	3.3V	D33VA	D33V_D33VS	R536	Resistor-1
43	PCH(PLA), GbE-PHY	2.5V	D33VA	D25VA	R535	Resistor-1

Table 10. Carrier Board Voltage Rails (Sheet 3 of 3)

Schem Page	Target Component	Voltage	Supply Power Rail	Rail	Ref Des	Resistor Spec
43	FET-SW for D12V,FET-SW for D12VS,PCH(PLA),Reset IC for PCH IOVDDA	1.2V	D33VA	D12VA	R537	Resistor-1
43	PCH(PLB), Reset IC for PCH IOVDDB	1.2V	D12VA	D12V	R538	Resistor-1
44	PCIe* Slot #2, PCIe* mini Card, PEG Slot #1 SDVO, PCIe* Slot #3, PCIe* to PCI Bridge, PCI Slot #4, Power_LED(D2)	3.3V	D33VA	D33V	R306	Resistor-2
44	LVDS, SIO, Audio Codec, CAN Driver, SPI Header, Intel® TPM$^{\varepsilon}$ Header, Validation Header, FP Header, Speaker	5.0V	D50VA	D50VS	R309	Resistor-2
44	COM Express* (PU), SATA_CLK_Gen, PCH(PLC), PCIe_CLK_Buf, PCIe* Slot #2, PCIe* mini Card LED, PCIe* Slot #3, SW4_PU, PCIe* to PCI Bridge, EEPROM, LVDS, SATA_LED, SD_Conn, SIO, LPC_CLK_Buf, Audio_Codec, HAD_Header, RS232C_Driver, RS485_Driver, I^2C* Header, SPI Header, CPLD, Intel® TPM$^{\varepsilon}$ Header, PCH Internal Monitor Header, Power_LED	3.3V	D33VA	D33VS	R310	Resistor-2
44	COM Express* Conn (XAB, XCD), LVDS, SATA_POW, PWOK_Gen	12V	D120VA	D120VS	R311	Resistor-3
44	PCIe* Signal SW	1.8V	D33VA	D18VS	R318	Resistor-1
44	COM Express* CARD Power SW, PCIe* mini Card	1.5V	D33VA	D15VS	R319	Resistor-2
44	PCIe* to PCI Bridge, FET-SW for D10VS	1.0V	D33VA	D10V	R357	Resistor-1
44	PCH(PLC), Reset IC for PCH IOVDDC	1.2V	D12VA	D12VS	R539	Resistor-1
44	PCIe* to PCI Bridge	1.0V	D10V	D10VS	R540	Resistor-1

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4.0 Reference Board Summary

4.1 Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit Features

Figure 10. COM Express* Module Components (Top View)

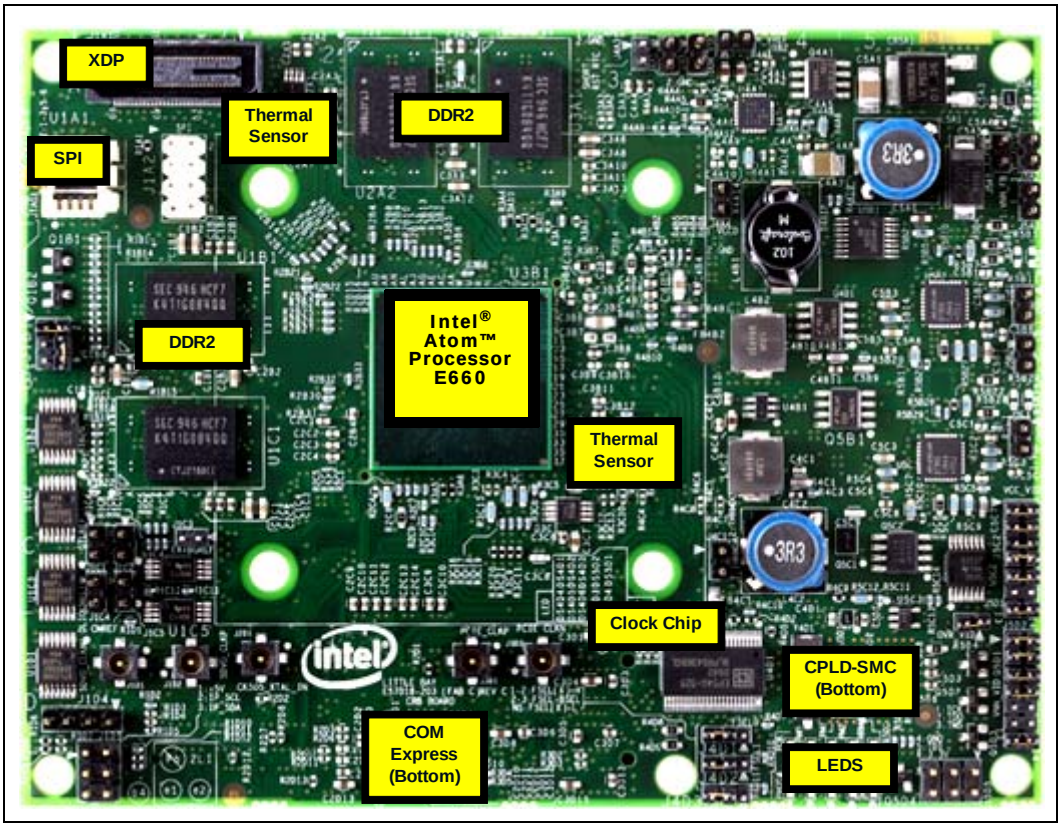
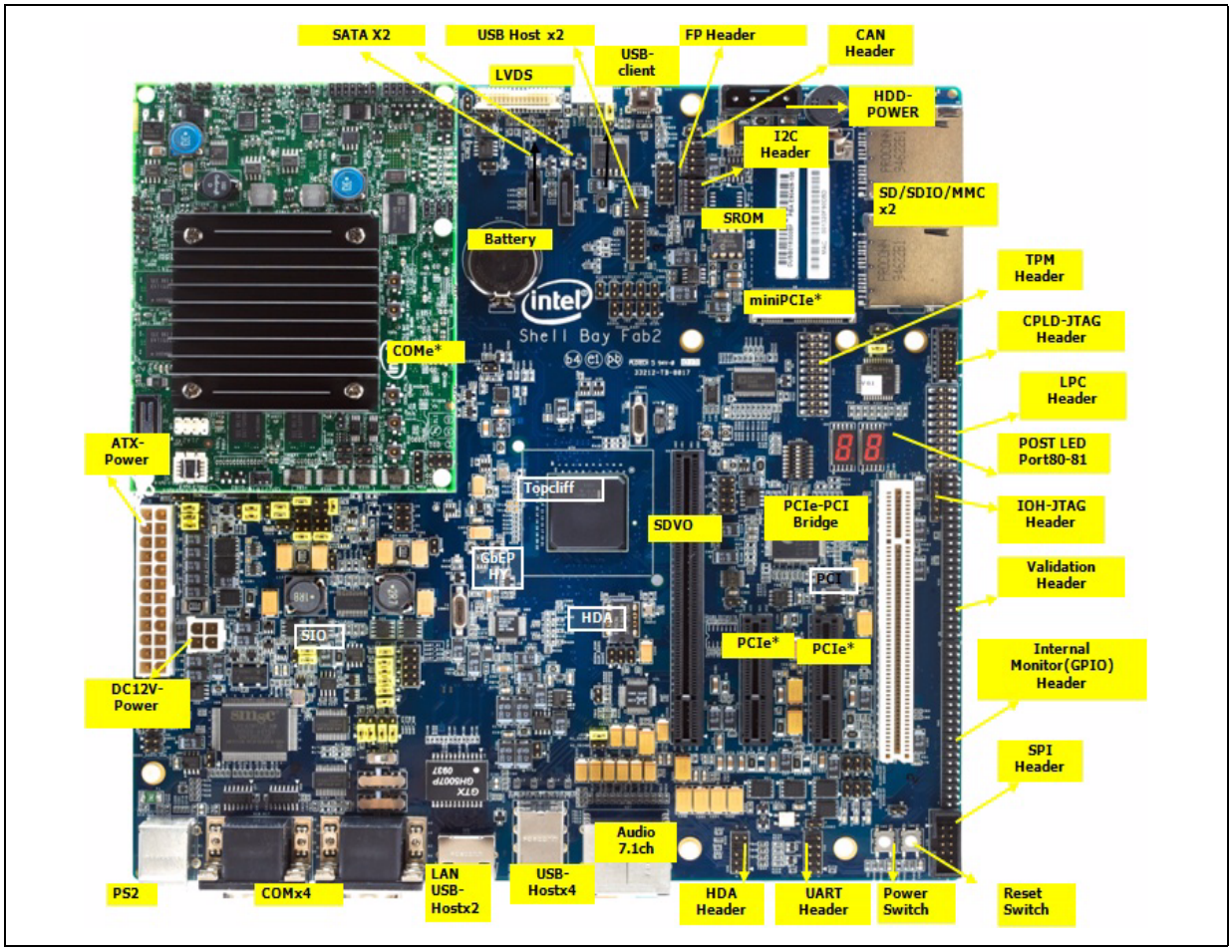


Figure 11. Carrier Board Feature Placement



4.2 Connectors

This section describes the board's connectors. Figure 12 shows the location number of the connectors (including back panel side) on the board. Table 11 lists connectors' labels and names.

Caution: Most of these connectors are not over-current protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could damage the computer, the interconnecting cable, or the attached external device.

Figure 12. Carrier Board Connectors

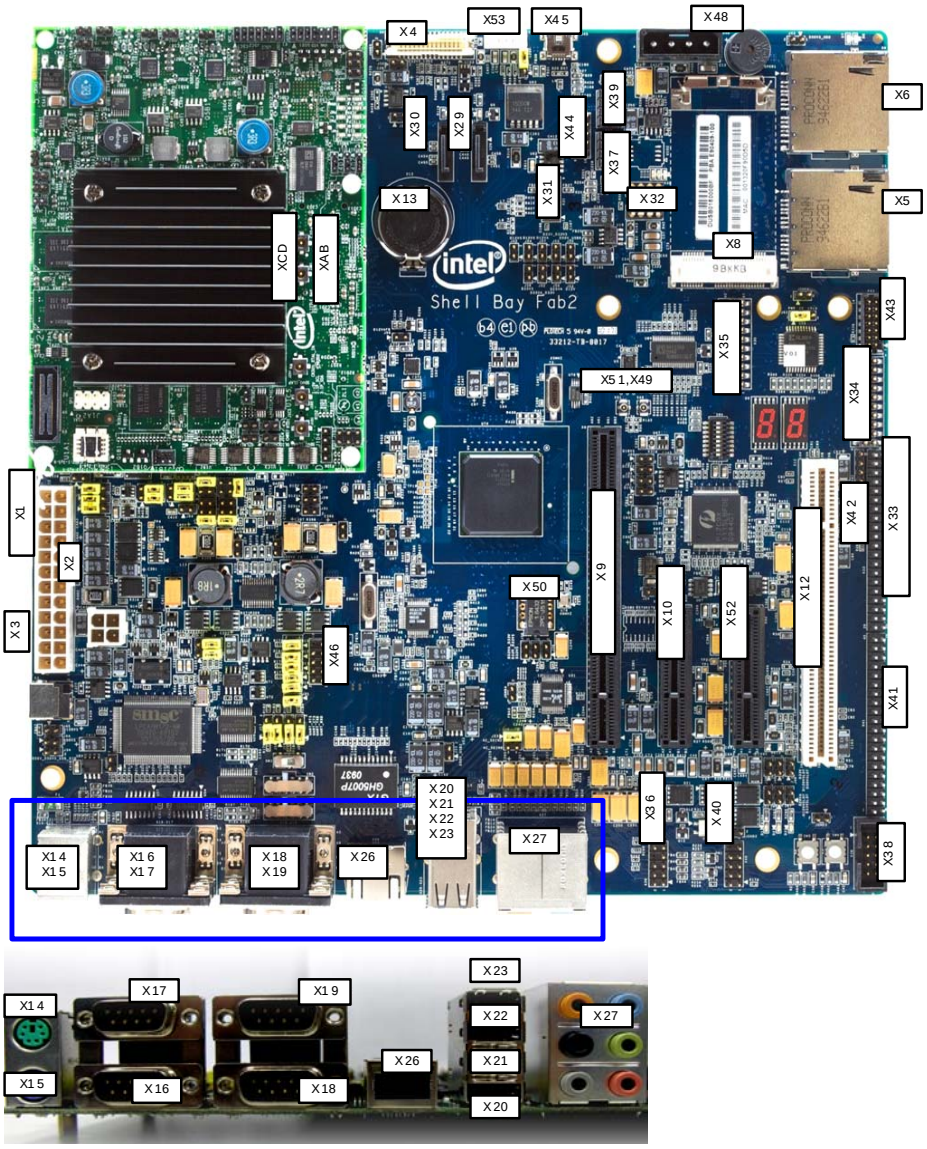


Table 11. Carrier Board Connectors

Label	Connector Name	Label	Connector Name
XAB	COM Express*-Module (Type-2;AB)	X31	USB-Host6,7
XCD	COM Express*-Module (Type-2;CD)	X32	SPI-ROM Socket
X1	ATX Power	X33	Validation Header
X2	AUX Power	X34	LPC Header
X3	12V DC-Jack	X35	Intel® TPMε Header
X4	LVDS	X36	Intel® HD Audioβ Header
X5	SD slot1	X37	I^2C*
X6	SD slot2	X38	SPI
X8	miniPCIe* slot	X39	CAN
X9	PCI Express* Graphic (SDVO); Slot#1	X40	UART (from PCH)
X10	PCI Express* x4; Slot#3	X41	PCH Validation Header
X12	PCI; Slot#4	X42	JTAG from PCH
X13	Battery Holder	X43	JTAG from CPLD
X14	PS/2 Mouse	X44	Front Panel Header
X15	PS/2 Keyboard	X45	USB-Client
X16	Serial COM1 (from SIO)	X46	UART with flow control (from PCH)
X17	Serial COM2 (from PCH)	X48	HDD Power
X18	Serial COM3 (from PCH)	X49	SMA Connector for PCIe* CLKN
X19	Serial COM4 (from PCH; RS232C/RS485 selectable)	X50	UART CLK Socket
X20	USB-Host 5 (from PCH)	X51	SMA Connector for PCIe* CLKP
X21	USB-Host 4 (from PCH)	X52	PCI Express* x4; Slot#2
X22	USB-Host 3 (from PCH)	X53	Connector for LVDS back light
X23	USB-Host 2 (from PCH)		
X26	Gigabit Ethernet		
X27	7.1ch Audio		
X29	SATA1 (from PCH)		
X30	SATA2 (from PCH)		

4.3 Configuration Settings

4.3.1 Configuration Jumpers/Switches

Caution: Do not move jumpers when the power is on. Switches may be moved while power is on. Always turn off the power and unplug the power cord from the computer before changing jumper settings. Otherwise, damage to the board could occur.

Figure 13. COM Express* Module Configuration Jumpers/Switches

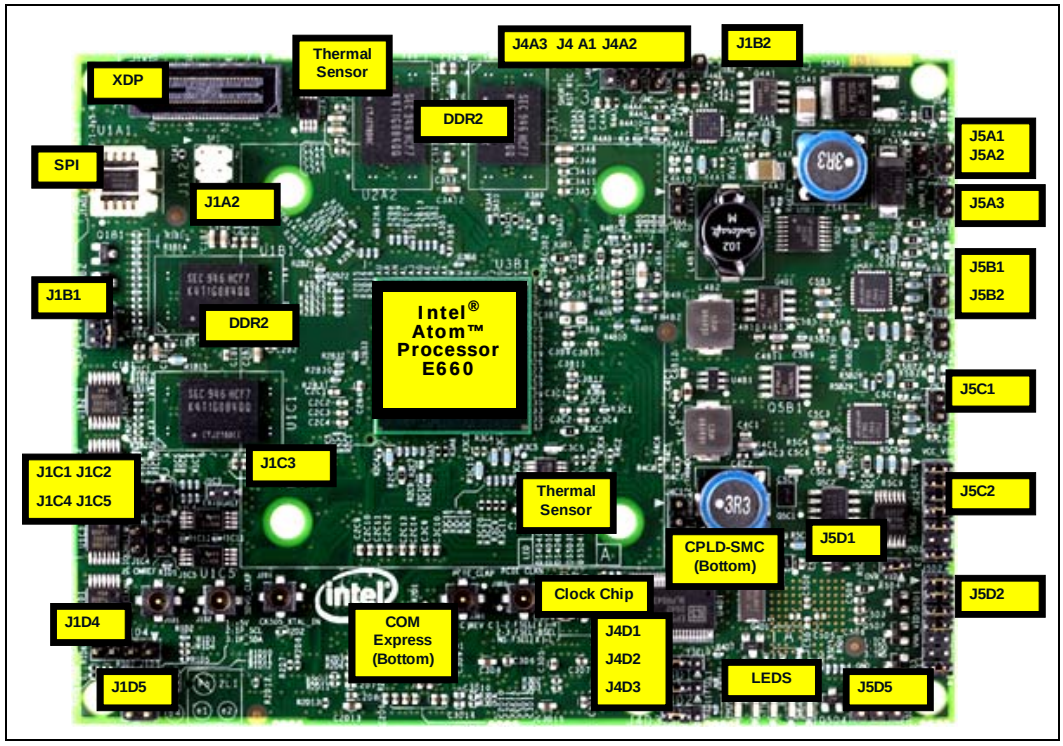


Figure 13 and Figure 14 show the locations of the major configuration jumpers and switches on the COM Express* module and the carrier board. Table 12, Table 13, Table 14, and Table 15 summarize the jumpers and switches and give their default and optional settings.

The development kit is shipped with the jumpers and switches shunted in the default locations.

Figure 14. Carrier Board Configuration Jumpers/Switches

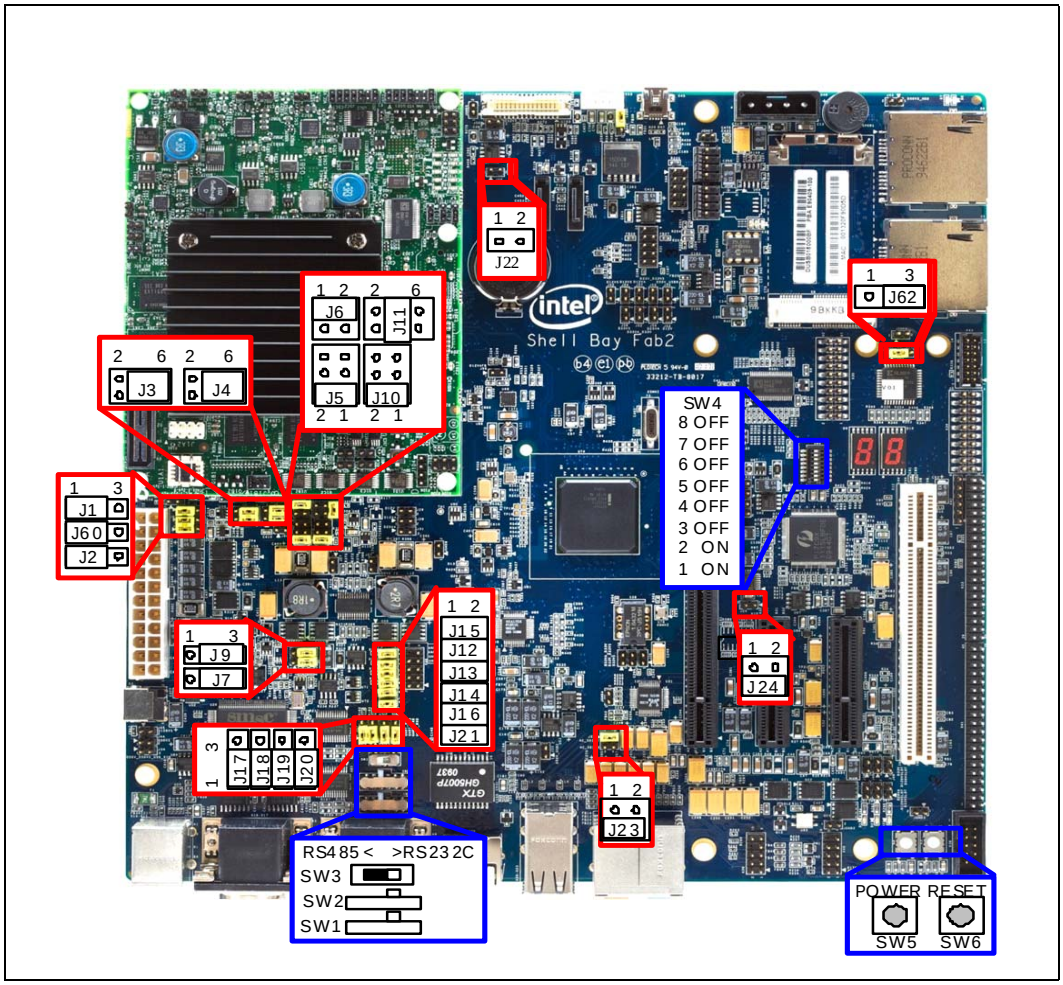


Table 12. Configuration Jumpers/Switches Setting on the COM Express* Module

Board	Description	Default Setting[1]	Optional Setting	Reference Designator
COM Express* module	RTC Reset header	Open	1-2 to clear CMOS.	J4A3
	Override BSEL0 header	2-3	See Table 15.	J4D1
	Override BSEL1 header	2-3	See Table 15.	J4D2
	Override BSEL2 header	2-3	See Table 15.	J4D3
	OVR_ALL_VID_N header	Open	1-2 to enable override with J5C2 and J5D2. Refer to Section 4.3.3.	J5D1
	VCC_VID Override	Open	Refer to Section 4.3.3.	J5C2
	VNN_VID Override	Open	Refer to Section 4.3.3.	J5D2

Note: A jumper consists of two or more pins mounted on the board. When a jumper cap is placed over two pins, it is designated as IN. When there are more than two pins on the jumper, the pins to be shorted are indicated as 1-2 (to short pin 1 to pin 2), 2-3 (to short pin 2 to pin 3), etc. When no jumper cap is to be placed on the jumper, it is designated as OPEN or OUT.

Table 13. Configuration Jumper Settings on Carrier Board (Sheet 1 of 3)

Label	Jumper Name	Setting Context	Initial Setting (AC Adapter Use Case)	Initial Setting (ATX-Power Use Case)
J1	PWOK select	PWROK signal to IOH and SIO select 1-2 short: Internal signal by D33VS and SUS_S3# 2-3 short: external signal by ATX-POW	1-2 short	1-2 short
J2	PSON select	PSON# signal to ATX-POW control select 1-2 short: ATX-POW using by ATX-mode 2-3 short: ATX-POW using by AT-mode (This case main power of ATX-POW is rised by ATX-POW switch on timing.)	2-3 short	1-2 short
J3	5V power select	+5V power rail (D50VA) source select 1-3, 2-4 short: using ATX-POW 5V 3-5, 4-6 short: using on board DC-DC converter 5V output	3-5, 4-6 short (for DC-DC converter pow validation)	3-5, 4-6 short (for DC-DC converter pow validation)
J4	3.3V power select	+3.3V power rail (D33VA) source select 1-3, 2-4 short: using ATX-POW 3.3V 3-5, 4-6 short: using on board DC-DC converter 3.3V output	3-5, 4-6 short (for DC-DC converter pow validation)	3-5, 4-6 short (for DC-DC converter pow validation)
J5	IOH PLA Power select	+1.2V power rail (D12VA) control signal select 1-2 short: using D33VA and it is enabled S5 state in IOH_PLA 3-4 short: using SUS_S5# and it is enabled S3 state in IOH PLA 5-6 short: using J6 select signal (this case is same state enable in IOH_PLA and PLB)	1-2 short (IOH_PLA is S5 state enabled)	1-2 short (IOH_PLA is S5 state enabled)
J6	IOH PLB Power select	+1.2V power rail (D12V) control signal select 1-2 short: using SUS_S5# and it is enabled S3 state in IOH_PLB 3-4 short: using SUS_S3# and it is enabled S0 state in IOH PLB	1-2 short (IOH_PLB is S3 state enabled)	1-2 short (IOH_PLB is S3 state enabled)
J7	PS_ON# to ATXPOW select	PSON# signal Suspend signal select in ATX-POW node 1-2 short: SUS_S5# select 2-3 short: SUS_S3# select	2-3 short	2-3 short
J9	ATXPOW UP Control Select	PSON# signal source select 1-2 short: SIO output signal (SIO_PSON#) select 2-3 short: Suspend signal from COMe module select (in this case, using suspend signal is depend on the J7 selection)	2-3 short	2-3 short
J10	IOH PLA Reset Select	IOH_PLA Reset input select 1-2 short: reset assert by D33VA_D33V (IOPLA) Powerup 3-4 short: reset assert by SIO RSMRST# 5-6 short: reset assert by CB_RESET# This jumper setting is linked with the IOH_PLA power selection by J5.	1-2 short (it is same as J5 setting)	1-2 short (it is same as J5 setting)
J11	IOH PLB Reset Select	IOH_PLB Reset input select 1-2 short: reset assert by SIO RSMRST# 3-4 short: reset assert by SIO KBDRST# 5-6 short: reset assert by CB_RESET# This jumper setting is limited by the IOH_PLB power selection by J6.	3-4 short	3-4 short
J12	UART0 port DTR connection	connection select between UART0 DTR port of IOH to RS232C driver 1-2 short: connect to RS232C driver open: no connection (if the case of using UART0 port in baud rate up 4Mbps, it is necessary to be set open.)	1-2 short	1-2 short

Note: A jumper consists of two or more pins mounted on the board. When a jumper cap is placed over two pins, it is designated as SHORT. When there are more than two pins on the jumper, the pins to be shorted are indicated as 1–2 (to short pin 1 to pin 2), 2–3 (to short pin 2 to pin 3), etc. When no jumper cap is to be placed on the jumper, it is designated as OPEN.

Table 13. Configuration Jumper Settings on Carrier Board (Sheet 2 of 3)

Label	Jumper Name	Setting Context	Initial Setting (AC Adapter Use Case)	Initial Setting (ATX-Power Use Case)
J13	UART0 port DCD connection	connection select between UART0 DSR port of IOH to RS232C driver 1-2 short: connect to RS232C driver open: no connection (if the case of using UART0 port in baud rate up 4Mbps, it is necessary to be set open.)	1-2 short	1-2 short
J14	UART0 port DSR connection	connection select between UART0 DSR port of IOH to RS232C driver 1-2 short: connect to RS232C driver open: no connection (if the case of using UART0 port in baud rate up 4Mbps, it is necessary to be set open.)	1-2 short	1-2 short
J15	UART0 port RI connection	connection select between UART0 RI port of IOH to RS232C driver 1-2 short: connect to RS232C driver open: no connection (if the case of using UART0 port in baud rate up 4Mbps, it is necessary to be set open.)	1-2 short	1-2 short
J16	RS485DRV TX/RX Enable select	RS485DRV (TX/RX) enable select 1-2 short: Disable open: Enable	1-2 short	1-2 short
J17	UART0 port RTS select	connection select between UART0 RTS port of IOH to RS232C driver or RS485 driver 1-2 short: connect to RS232C driver 2-3 short: connect to RS485 driver open: no connection	1-2 short	1-2 short
J18	UART0 port CTS select	connection select between UART0 CTS port of IOH to RS232C driver or RS485 driver 1-2 short: connect to RS232C driver 2-3 short: connect to RS485 driver open: no connection	1-2 short	1-2 short
J19	UART0 port TXD select	connection select between UART0 TXD port of IOH to RS232C driver or RS485 driver 1-2 short: connect to RS232C driver 2-3 short: connect to RS485 driver open: no connection	1-2 short	1-2 short
J20	UART0 port RXD select	connection select between UART0 RXD port of IOH to RS232C driver or RS485 driver 1-2 short: connect to RS232C driver 2-3 short: connect to RS485 driver open: no connection	1-2 short	1-2 short
J21	RS485DRV CTS/RTS Enable select	RS485DRV (CTS/RTS) enable select 1-2 short: Disable open: Enable	1-2 short	1-2 short
J22	BIOS Disable/Enable select	BIOS on COMe module Enable select 1-2 short: Disable open: Enable (this case of BIOS using on COMe Module)	open	open
J23	Audio Codec SDATA IN select	Audio codec (Realtek ALC888-GR) "SDATA-IN" connection select 1-2 short: connect to AC_SDIN2 of COMe connector 3-4 short: connect to AC_SDIN0 of COMe connector	3-4 short	3-4 short
J24	I2C-EEPROM connection select	I2C-EEPROM of PCIe to PCI Bridge IC(PI7C9X111) connect mode select 1-2 short: I2C port on COMe is connected to EEPROM open: I2C port on PI7C9X111 is connected to EEPROM (This EEPROM is no use by default.)	open	open

Note: A jumper consists of two or more pins mounted on the board. When a jumper cap is placed over two pins, it is designated as SHORT. When there are more than two pins on the jumper, the pins to be shorted are indicated as 1–2 (to short pin 1 to pin 2), 2–3 (to short pin 2 to pin 3), etc. When no jumper cap is to be placed on the jumper, it is designated as OPEN.

Table 13. Configuration Jumper Settings on Carrier Board (Sheet 3 of 3)

Label	Jumper Name	Setting Context	Initial Setting (AC Adapter Use Case)	Initial Setting (ATX-Power Use Case)
J60	COMe ATXPOWUP control select	PWROK signal to COMe Module select 1-2 short: Internal signal by D33VS and SUS_S3# 2-3 short: external signal by ATX-POW	1-2 short	1-2 short
J61	LVDS power select	Onboard 5V or 12V supply select for LVDS backlight power 1-2 short: 5V supply at X53 2-3 short: 12V supply at X53	2-3 short	2-3 short
J62	Power SW to COMe Select	Power SW signal to COMe module select 1-2 short: SW5 signal connect to COMe module directly 2-3 short: SW5 and Intel® PCH EG20T wake_out_n signal merged signal connect to COMe module via CPLD If the case to use the Wake On LAN in S5 state, it needs to set 2-3 short	2-3 short	2-3 short

Note: A jumper consists of two or more pins mounted on the board. When a jumper cap is placed over two pins, it is designated as SHORT. When there are more than two pins on the jumper, the pins to be shorted are indicated as 1–2 (to short pin 1 to pin 2), 2–3 (to short pin 2 to pin 3), etc. When no jumper cap is to be placed on the jumper, it is designated as OPEN.

Table 14. Configuration Switch Settings on Carrier Board

Label	Switch Name	Setting Context	Initial Setting (AC Adapter Use Case)	Initial Setting (ATX-Power Use Case)
SW1	RS-232C/485 select1	DB9 port (X19) is selected between RS232C and RS485. 1-2, 4-5, 7-8, 10-11 short: RS232C 2-3, 5-6, 8-9, 11-12 short: RS485	1-2, 4-5, 7-8, 10-11 short (for RS232C setting)	1-2, 4-5, 7-8, 10-11 short (for RS232C setting)
SW2	RS-232C/485 select2	DB9 port (X19) is selected between RS232C and RS485. 1-2, 4-5, 7-8, 10-11 short: RS232C 2-3, 5-6, 8-9, 11-12 short: RS485	1-2, 4-5, 7-8, 10-11 short (for RS232C setting)	1-2, 4-5, 7-8, 10-11 short (for RS232C setting)
SW3	RS-232C/485 select3	DB9 port (X19) is selected between RS232C and RS485. 1-2 short: RS232C 2-3 short: RS485	1-2 short (for RS232C setting)	1-2 short (for RS232C setting)
SW4	bit1: PCIe-signal select dip switch	bit 1: PCIe* Lane 3 connection on signal switch (U3) select ON: PCI Express* Slot (X10) connection OFF: PCI Express* Mini Card (X8) connection	bit 1: ON (for PCI Express* Slot X10)	bit 1: ON (for PCI Express Slot* X10)
	bit3-8: Not used	bit3-5: No assign on the board bit6-8: it is connected to CPLD, but it is not used	bit 3-8: OFF	bit 3-8: OFF
SW5	POWER push switch	Non Lock push button (Push to ON) ON: PWRBTN# to COMe Module is asserted. OFF: PWRBTN# to COMe Module is de-asserted.	OFF	OFF
SW6	RESET push switch	Non Lock push button (Push to ON) ON: FPRST# to SIO is asserted. OFF: FPRST# to SIO is de-asserted.	OFF	OFF

Notes:
1. When a switch is designated as 1–2, the switch slide is positioned such that pins 1 and 2 are shorted together.

4.3.2 BSEL Jumper Settings

The jumper settings in Table 15 are provided to accommodate frequency selection for the processor. The custom CK-505 clock chip (ICS9LPRS436BGLFT*) receives BSEL signals from the Intel® Atom™ Processor E660 for frequency selection.

Table 15. BSEL Jumper Settings

		Processor	Override
Processor External Reference Clock Frequency (MHz)	Processor driven (default)	J4D1: 2-3 J4D2: 2-3 J4D3: 2-3	No Override
	0.6 GHz (Ultra Low Power) or 1.0 GHz (Entry SKU) or 1.3 GHz (Mainstream SKU) or 1.6 GHz (Premium SKU) BCLK = 100 MHz	J4D1: Open J4D2: Open J4D3: Open	CPU BSEL 0=0 CPU BSEL 1=0 CPU BSEL 2=0

4.3.3 Manual VID Support for CPU

The COM Express* module supports manual VID operation for the processor and graphics core VRs. Headers J5C2 (VCC_VID override) and J5D1 (OVR_ALL_VID_N) are provided to incorporate “VCC VID override”, and J5D2 (VNN_VID override) and J5D1 (OVR_ALL_VID_N) are provided to incorporate “VNN VID override”. See Figure 13. VID override allows for overriding the VID outputs to the VCC_S and VNN_S VR. The intent of the “VID override” circuit is to enable debugging and testing. See Table 16 for the VID code table.

Table 16. VID vs. $V_{CC-CORE}$ Voltage

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc-core	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc-core
0	0	0	0	0	0	0	1.5000V	1	0	0	0	0	0	0	0.7000V
0	0	0	0	0	0	1	1.4875V	1	0	0	0	0	0	1	0.6875V
0	0	0	0	0	1	0	1.4750V	1	0	0	0	0	1	0	0.6750V
0	0	0	0	0	1	1	1.4625V	1	0	0	0	0	1	1	0.6625V
0	0	0	0	1	0	0	1.4500V	1	0	0	0	1	0	0	0.6500V
0	0	0	0	1	0	1	1.4375V	1	0	0	0	1	0	1	0.6375V
0	0	0	0	1	1	0	1.4250V	1	0	0	0	1	1	0	0.6250V
0	0	0	0	1	1	1	1.4125V	1	0	0	0	1	1	1	0.6125V
0	0	0	1	0	0	0	1.4000V	1	0	0	1	0	0	0	0.6000V
0	0	0	1	0	0	1	1.3875V	1	0	0	1	0	0	1	0.5875V
0	0	0	1	0	1	0	1.3750V	1	0	0	1	0	1	0	0.5750V
0	0	0	1	0	1	1	1.3625V	1	0	0	1	0	1	1	0.5625V
0	0	0	1	1	0	0	1.3500V	1	0	0	1	1	0	0	0.5500V
0	0	0	1	1	0	1	1.3375V	1	0	0	1	1	0	1	0.5375V
0	0	0	1	1	1	0	1.3250V	1	0	0	1	1	1	0	0.5250V
0	0	0	1	1	1	1	1.3125V	1	0	0	1	1	1	1	0.5125V
0	0	1	0	0	0	0	1.3000V	1	0	1	0	0	0	0	0.5000V
0	0	1	0	0	0	1	1.2875V	1	0	1	0	0	0	1	0.4875V
0	0	1	0	0	1	0	1.2750V	1	0	1	0	0	1	0	0.4750V
0	0	1	0	0	1	1	1.2625V	1	0	1	0	0	1	1	0.4625V
0	0	1	0	1	0	0	1.2500V	1	0	1	0	1	0	0	0.4500V
0	0	1	0	1	0	1	1.2375V	1	0	1	0	1	0	1	0.4375V
0	0	1	0	1	1	0	1.2250V	1	0	1	0	1	1	0	0.4250V
0	0	1	0	1	1	1	1.2125V	1	0	1	0	1	1	1	0.4125V
0	0	1	1	0	0	0	1.2000V	1	0	1	1	0	0	0	0.4000V
0	0	1	1	0	0	1	1.1875V	1	0	1	1	0	0	1	0.3875V
0	0	1	1	0	1	0	1.1750V	1	0	1	1	0	1	0	0.3750V
0	0	1	1	0	1	1	1.1625V	1	0	1	1	0	1	1	0.3625V
0	0	1	1	1	0	0	1.1500V	1	0	1	1	1	0	0	0.3500V
0	0	1	1	1	0	1	1.1375V	1	0	1	1	1	0	1	0.3375V
0	0	1	1	1	1	0	1.1250V	1	0	1	1	1	1	0	0.3250V
0	0	1	1	1	1	1	1.1125V	1	0	1	1	1	1	1	0.3125V
0	1	0	0	0	0	0	1.1000V	1	1	0	0	0	0	0	0.3000V
0	1	0	0	0	0	1	1.0875V	1	1	0	0	0	0	1	0.2875V
0	1	0	0	0	1	0	1.0750V	1	1	0	0	0	1	0	0.2750V
0	1	0	0	0	1	1	1.0625V	1	1	0	0	0	1	1	0.2625V
0	1	0	0	1	0	0	1.0500V	1	1	0	0	1	0	0	0.2500V
0	1	0	0	1	0	1	1.0375V	1	1	0	0	1	0	1	0.2375V
0	1	0	0	1	1	0	1.0250V	1	1	0	0	1	1	0	0.2250V
0	1	0	0	1	1	1	1.0125V	1	1	0	0	1	1	1	0.2125V
0	1	0	1	0	0	0	1.0000V	1	1	0	1	0	0	0	0.2000V
0	1	0	1	0	0	1	0.9875V	1	1	0	1	0	0	1	0.1875V
0	1	0	1	0	1	0	0.9750V	1	1	0	1	0	1	0	0.1750V
0	1	0	1	0	1	1	0.9625V	1	1	0	1	0	1	1	0.1625V
0	1	0	1	1	0	0	0.9500V	1	1	0	1	1	0	0	0.1500V
0	1	0	1	1	0	1	0.9375V	1	1	0	1	1	0	1	0.1375V
0	1	0	1	1	1	0	0.9250V	1	1	0	1	1	1	0	0.1250V
0	1	0	1	1	1	1	0.9125V	1	1	0	1	1	1	1	0.1125V
0	1	1	0	0	0	0	0.9000V	1	1	1	0	0	0	0	0.1000V
0	1	1	0	0	0	1	0.8875V	1	1	1	0	0	0	1	0.0875V
0	1	1	0	0	1	0	0.8750V	1	1	1	0	0	1	0	0.0750V
0	1	1	0	0	1	1	0.8625V	1	1	1	0	0	1	1	0.0625V
0	1	1	0	1	0	0	0.8500V	1	1	1	0	1	0	0	0.0500V
0	1	1	0	1	0	1	0.8375V	1	1	1	0	1	0	1	0.0375V
0	1	1	0	1	1	0	0.8250V	1	1	1	0	1	1	0	0.0250V
0	1	1	0	1	1	1	0.8125V	1	1	1	0	1	1	1	0.0125V
0	1	1	1	0	0	0	0.8000V	1	1	1	1	0	0	0	0.0000V
0	1	1	1	0	0	1	0.7875V	1	1	1	1	0	0	1	0.0000V
0	1	1	1	0	1	0	0.7750V	1	1	1	1	0	1	0	0.0000V
0	1	1	1	0	1	1	0.7625V	1	1	1	1	0	1	1	0.0000V
0	1	1	1	1	0	0	0.7500V	1	1	1	1	1	0	0	0.0000V
0	1	1	1	1	0	1	0.7375V	1	1	1	1	1	0	1	0.0000V
0	1	1	1	1	1	0	0.7250V	1	1	1	1	1	1	0	0.0000V
0	1	1	1	1	1	1	0.7125V	1	1	1	1	1	1	1	0.0000V

Note: When manually overriding the VID outputs, an open jumper position will result in logic '1' on the corresponding VID signal. Closing the jumper position will result in logic '0' on the corresponding VID signal.

4.4 Power On and Reset Push Buttons

The carrier board has two push buttons, POWER and RESET. The POWER button releases power to the entire board causing the board to boot. The RESET button forces all systems to warm reset.

The two buttons are located near the PCI slot in the backside area. The POWER button is located at SW5 and the RESET button is located at SW6. See Figure 11.

4.5 LEDs

Figure 15 provides the location of the LEDs and Table 17 describes the functions of the LEDs and their reference designators.

Figure 15. Carrier Board LEDs

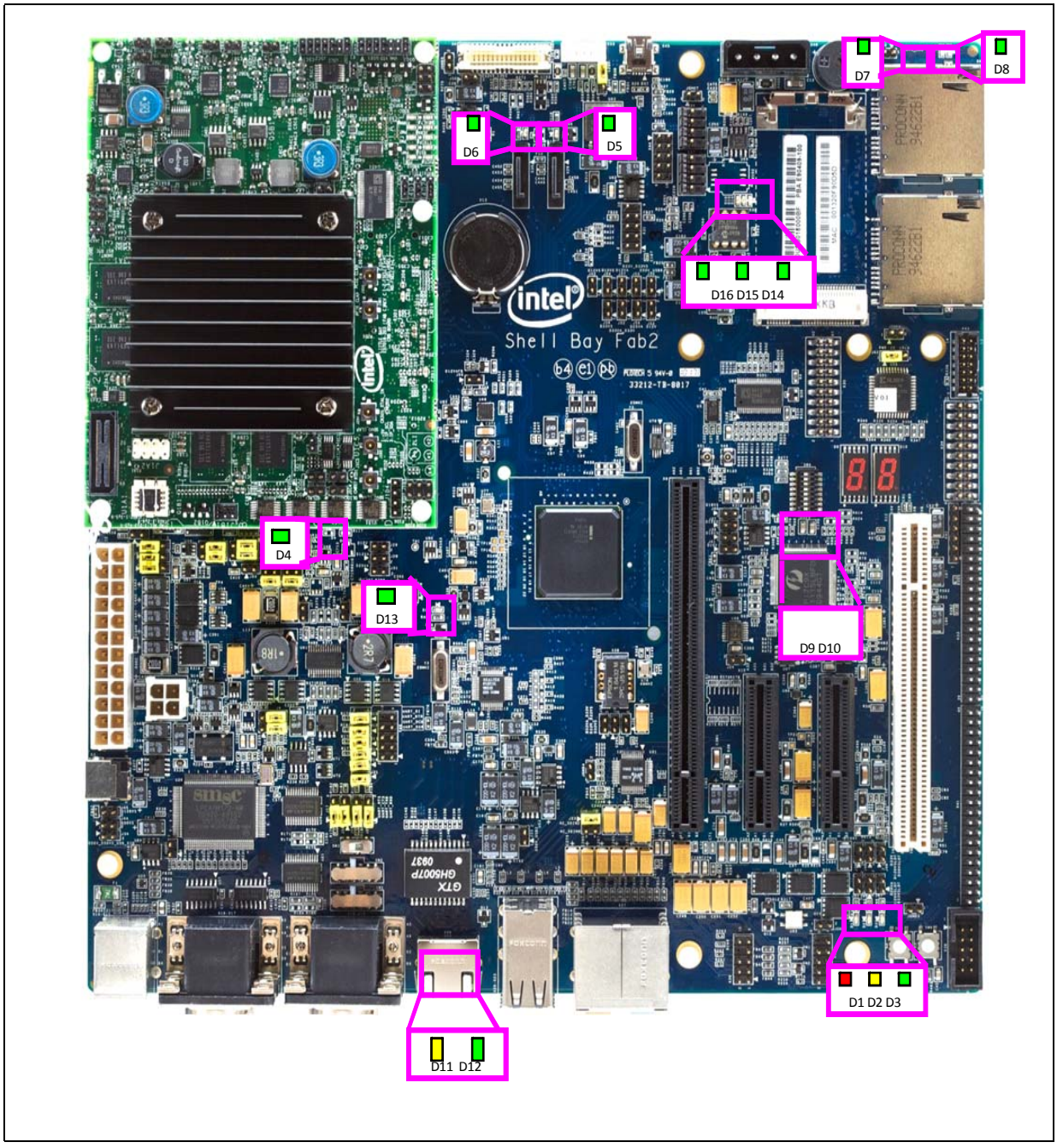


Table 17. Carrier Board LEDs

Target	LED			FP-Header (X44)(*4)	
	Silk	Status Indication	Color	No.	Status Indication
Power	D1	S5 Indication(*1)	red	2	S0 Indication (LED_GRN)
	D2	S3 Indication(*1)	yellow	4	-
	D3	S0 Indication(*1)	green	-	-
HDD	D4	COMe_HDD	green	3	COMe_HDD/ SATA0/SATA1(*2)
	D5	SATA0	green	3	-
	D6	SATA1	green	-	-
SDIO	D7	SDIO0	green	-	-
	D8	SDIO1	green	-	-
POST Code	D9	POST Code Port80h (HIGHNIBBLE) (7 segments)	red	-	-
	D10	POST Code Port80h (LOW NIBBLE) (7 segments)	red	-	-
LAN Port(*3)	D11	LED0 (ACT)	yellow	-	-
	D12	LED1 (LINK)	green	-	-
	D13	LED2	green	-	-
PCIe* miniCard	D14	WWAN	green	-	-
	D15	WLAN	green	-	-
	D16	WPAN	green	-	-

Notes:
1. D3-D1 are power status indicator; if the power status is S5, then D1 LED is on; if the power status is S3, then D1 and D2 LED are on; if the power status is S0, then D1 to D3 LED are on.
2. HDD LED of the front panel is status indication of HDD access. These signals are controlled from SIO.
3. LAN ACT(D13), LINK(D14) LEDs are indicated by the build-in LED in the LAN connector.
4. X44 other pins assigned are omitted.

4.6 PCI Express* Routing

4.6.1 PCI Express* x1 Port0

This is the first PCIe* port from the COM Express* module. It connects to the Intel® PCH EG20T.

4.6.2 PCI Express* x1 Port1

This is the second PCIe* port from the COM Express* module. The PCI Express* port 1 link connects to a PCIe*-PCI bridge (Pericom PI7C9X111SL*) which provides one PCI slot (X12).

4.6.3 PCI Express* x1 Port2

This is the third PCIe* port from the COM Express* module. It connects to a x4 PCIe* slot (X52).

4.6.4 PCI Express* x1 Port3

The PCI Express* port 3 link can connect to either two end points via a signal switch (Pericom PI2PCIE212-D*). The first target device is a x4 PCIe* slot (X10); the second target device is a PCI Express* Mini Card connector (X8).

This PCIe* signal switch is controlled by slide switch (SW4 - bit 1), see Figure 3, Figure 14 and Table 14.

4.7 JTAG Headers

The JTAG headers are used primarily for the microcontroller firmware upgrade and boundary scan testing.

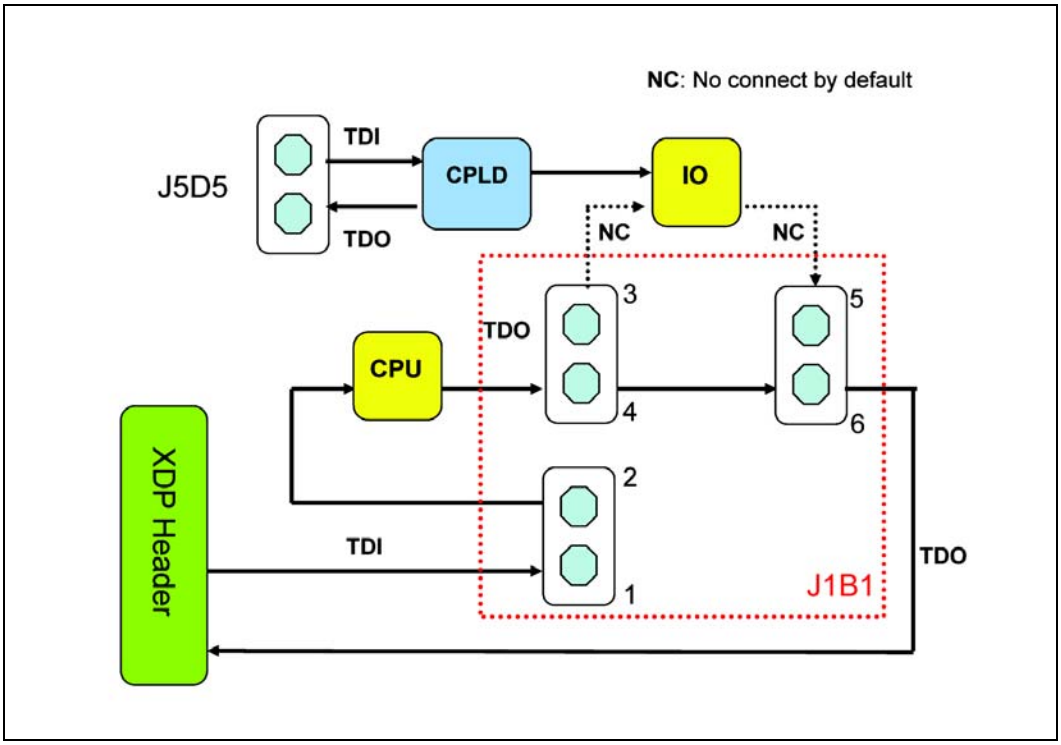
The Intel® Atom™ Processor E660 JTAG chains are daisy chained onto the XDP JTAG port (J1A1) on the COM Express* module. Jumper (J1B1) allows you to bypass the CPU or I/O chain, see Figure 13.

Table 18. JTAG Chain Jumper Options on the COM Express* Module

JTAG Chain	J1B1 Options
CPU and I/O JTAG	1-2, 3-4, 5-6
CPU JTAG only (default)	1-2, 4-6
I/O JTAG only	1-3, 5-6

The System Management CPLD can be accessed in-system via the JTAG header (J5D5) on the COM Express* module. Figure 16 shows the JTAG chain on the COM Express* Module.

Figure 16. JTAG Chain on the COM Express* Module



The carrier board has two JTAG headers. One is used for the Intel® PCH EG20T internal boundary scan testing and signal monitoring in validation. The other is used the CPLD's firmware programming. These JTAG interfaces are not chained and each header is different.

The Intel® PCH EG20T JTAG header is 1x6 2.54mm pin header (X42), and the CPLD's JTAG header is 2x7 2.00mm pin header (X43). See Figure 11 for header location.

The CPLD's JTAG header is only used to connect Xilinx JTAG download cable.

§ §

5.0 Software

5.1 Overview of Software Availability for the Development Kit

Table 19. Software Availability Overview

		Dev Kit	Where to Get Drivers
OS	Drivers for Windows* XP SP3	Yes	Intel (http://edc.intel.com/Platforms/Atom-E6xx/#software) or Native in OS
	Drivers for Windows ES 2009*	Yes	Intel (http://edc.intel.com/Platforms/Atom-E6xx/#software) or Native in OS
	Drivers for Windows Embedded POSReady* 2009	Yes	Intel (http://edc.intel.com/Platforms/Atom-E6xx/#software) or Native in OS
	Linux drivers		http://sourceforge.net/projects/generalembedded/files/ or kernel.org
	Linux: MeeGo*	Yes	http://meego.com
	Linux: Timesys Fedora* Remix	Yes	https://linuxlink.timesys.com/intel/linux
	WinCE 6.0 R3 BSP	Yes	BSP vendors
BIOS	AMI	Enabled	AMI
	Insyde	Enabled	Insyde
	Phoenix	Enabled	Phoenix
	ByoSoft	Enabled	ByoSoft
Intel® Embedded Graphic Driver	All supported OS as above	Yes	Intel (http://edc.intel.com/Platforms/Atom-E6xx/#software)
VMM Software	Tenasys	Yes	Tenasys

5.2 Platform Drivers for the Development Kit

The following are the required drivers for the development kit for both Linux and Windows* XP. The drivers can be obtained from the location listed in Table 20.

Table 20. Platform Drivers for the Intel® Atom™ Processor E660 with Intel® Platform Controller Hub EG20T Development Kit

Component	Linux* Drivers	Windows* XP Driver
CAN (Intel® PCH EG20T)	http://sourceforge.net/projects/generalembedded/files/ or kernel.org	http://edc.intel.com/Platforms/Atom-E6xx/#software
DMA Controller (Intel® PCH EG20T)		
Gigabit Ethernet (Intel® PCH EG20T)		
GPIO (Intel® PCH EG20T)		
I²C* (Intel® PCH EG20T)		
IEEE 1588 (Intel® PCH EG20T)		
Packet Hub (Intel® PCH EG20T)		
UART (Intel® PCH EG20T)		
SPI (Intel® PCH EG20T)		
USB Device (Intel® PCH EG20T		
SATAII (Intel® PCH EG20T)	Native	
SD/SDIO/MMC (Intel® PCH EG20T))		Native
USB Host (Intel® PCH EG20T)		
Intel® High Definition Audio[β] (ALC888*)		http://www.realtek.com.tw/downloads/downloadsView.aspx?Langid=1&PNid=24&PFid=24&Level=4&Conn=3&DownTypeID=3&GetDown=false (Note: There are 2 pieces of drivers along with the package, Microsoft UAA a.k.a KB888111 and codec driver)

Notes:
1. Windows XP includes Windows XP SP3, Windows Embedded Standard 2009 and Windows Embedded POSReady 2009.
2. Chipset INF files can be obtained http://edc.intel.com/Platforms/Atom-E6xx/#software.

5.3 EFI Firmware

The development kit EFI firmware is an AMI Aptio* based reference BIOS. It is stored on a 16 Mbit SPI part on the COM Express module. The EFI setup utility for changing the date, enabling/disabling peripherals and boot order is accessed during POST by pressing the <del> or <F2> key.

5.3.1 EFI Firmware Features

- Supports Intel® Hyper-Threading Technology[α] by default
- Supports Intel® Virtualization Technology for IA-32 and Intel® Architecture[δ] (Intel® VT-x[δ]) in hardware and can be enabled through the Intel® VT[δ] option in the BIOS setup menu
- Supports Digital Thermal Sensor
- Supports Thermal Management (TM) and Thermal Management 2 (TM2) and can be enabled/disabled in the BIOS setup option menu
- Supports processor power states C0, C1, C2, C4 and C6. The default max C state is C6 and this can be changed manually in the BIOS setup menu.
- Supports S0 (G0), S3, S4 (G1) and S5 (G2)

- Supports Enhanced Intel SpeedStep® Technology$^{\theta}$
- Supports boot from USB

Note: Please check BIOS release notes for latest updates and features. Also check the latest Specification Updates or Sightings Reports (if available) before implementing any of the above features.

5.3.2 Where to Download

The EFI firmware is available at http://edc.intel.com/Platforms/Atom-E6xx/#software.

5.3.3 BIOS/EFI Firmware Update Tool

The development kit EFI firmware can be upgraded/reflashed using either of two methods:

- A standalone SPI programmer
- AMI Firmware Update (AFU) utilities
  - afuwin
  - afudos
  - afulnx
  - afuefi

These utilities are free tools available on AMI's web site at http://www.ami.com/support/product.cfm

Go to the "Product Support" page, select "Aptio" in the AMIBIOS drop down box and click "Submit".

A Readme file on how to use the tools can be found on the download page.

Note: The BIOS installed on the development platform is an EFI-based BIOS hence only the EFI version of the reflash tool can be used to update the BIOS.

5.3.4 EFI Firmware/BIOS Status Code

If the board does not power up completely, the Port 80 code may provide insight into the issue. A complete list of Port 80 checkpoint definitions can be found in http://www.ami.com/support/doc/AMI_Aptio_4.x_Status_Codes_PUB.pdf

For processor Memory Reference Code (MRC) status code, it is denoted as below:

- A0: Memory initialization starts
- A1: Read memory strap information
- A2: Program memory controller
- A3: Perform DDR2 initialization sequence
- A4: Clear FIFO in memory controller
- A5: Enable refresh
- A6: Memory initialization ends
- EF: Invalid frequency
- EE: No memory

Note: The default MRC status code overlaps with the AMI's status code hence it requires proper debugging steps and tracing to isolate the real problem.

5.3.5 Links to Vendors Providing a BIOS Solution for the Intel® Atom™ Processor E660

A custom EFI Firmware is installed on the board included with this development kit.

This BIOS is specific to this board and is not applicable for customer designs. It is recommended that customer work with one of the following vendors directly to implement a solution for their design. These BIOS vendors can help provide the right solution:

- American Megatrends, Inc. (http://www.ami.com)
- Phoenix Technologies (http://www.phoenix.com)
- Insyde Software (http://www.insydesw.com)
- Byosoft Co., Ltd (http://byosoft.com.cn/en/index.asp)

5.4 WinCE BSP Vendors

Below are the links to WinCE OS vendors who support the Intel® Atom™ Processor E660 and Intel® PCH EG20T for Embedded platform:

Adeneo - http://www.adeneo-embedded.com/srt/en/document/show?location.id:=1360

bSQUARE - http://www.bsquare.com/partners/siliconvendors/intel.asp

Wipro - http://www.wipro.com/pes/alliances/ica/wincebsp.htm

5.5 Intel® Embedded and Media Graphic Driver

The Intel® Embedded and Media Graphic Driver that is validated on the development platform can be downloaded from http://edc.intel.com/Platforms/Atom-E6xx/#software.

Note: Please also see *Intel® Embedded Media and Graphics Driver, EFI Video Driver, and Video BIOS v1.5 for Windows* XP and Linux* Specification Update*.

5.6 Virtual Machine Monitor Software (VMM Software)

For customers that want to include an Intel® VT$^{\delta}$ solution in their platform, please work with the following vendor directly to implement a solution for their design and usage.

- Tenasys (www.tenasys.com)

5.7 CPLD Firmware Update

5.7.1 CPLD Firmware Update on the COM Express* Module

To update the CPLD firmware on the module, please refer to Altera's USB-Blaster Download Cable User Guide at: http://www.altera.com/literature/ug/ug_usb_blstr.pdf

The CPLD firmware can be downloaded from http://edc.intel.com/Platforms/Atom-E6xx/#software.

Note: A modification is required before you can use the 10-pin female plug on the module. Please refer to the *Intel® Atom™ Processor E6xx Series-based – Platform Design Guide* and USB-Blaster Download Cable User Guide for information on how to make the changes.

5.7.2 CPLD Firmware Update on the Carrier Board

To update the CPLD firmware on the carrier board, please refer to Xilinx's USB-platform download cable datasheet at:
http://www.xilinx.com/support/documentation/data_sheets/ds593.pdf

The CPLD firmware for the carrier board can be downloaded from http://edc.intel.com/Platforms/Atom-E6xx/#software.

5.8 Software Included in the Development Kit

1. The hard disk that is included in the development kit is preloaded with:
   - Timesys Fedora* Remix OS which includes all the Intel PCH Drivers.
   - For the latest Intel PCH drivers, you may obtain from http://sourceforge.net/projects/generalembedded/files/
   - Intel® Embedded Graphics Driver package
   - Mplayer-vaapi-20100713-FULL.tar.bz2
2. The following is the user information that has been set in the hard disk.

   For root user:

   Username: root

   Password: fedora

   or

   Username: user

   Password: fedora
3. The EFI BIOS is specific to this board, and is not applicable for customer designs. Please check the BIOS information in the BIOS menu (when <F2> or <del> is pressed when prompted during the system boot up) for the BIOS version used on the board. It is recommended that customers work with one of the following vendors directly to implement a solution for their design. Most of these vendors provide both legacy and EFI solutions for this platform. The BIOS vendors listed below can help provide the right solution.

- American Megatrends, Inc. (http://www.ami.com)
- Phoenix Technologies (http://www.phoenix.com)

- Insyde Software (http://www.insydesw.com)
- Byosoft Co., Ltd (http://byosoft.com.cn/en/index.asp)

5.9 Operating System Installation

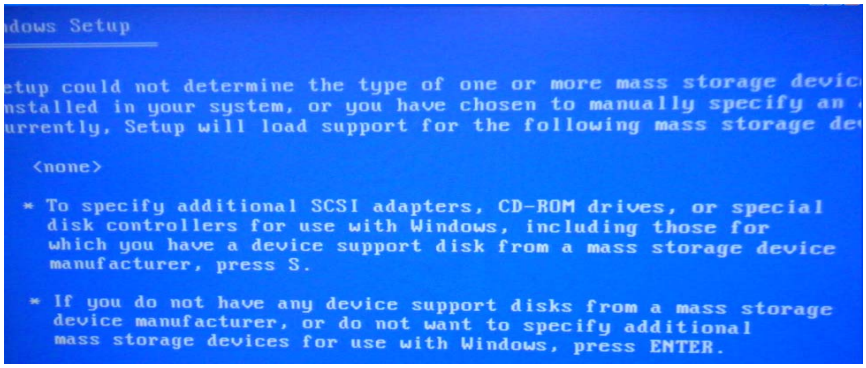
5.9.1 Windows* XP SP3

The Intel® PCH EG20T SATA does not support an IDE interface that is compatible with legacy drivers and Windows* XP SP3 does not contain the required SATA AHCI driver natively. Use the following instructions to install the Intel® PCH EG20T SATA AHCI driver during the installation of Windows XP SP3.

Note: During the installation of Windows XP, only single USB device (the USB floppy disk) is allowed to be connected to the system at USB port x23 else Windows XP installation will not be successful. This is due to USB issue in the Intel® PCH EG20T A0 and A1 silicon. Refer to the *Intel® Platform Controller Hub EG20T – Sightings Report* for more information. Some USB floppy drivers are not supported during F6 installation. See details at http://support.microsoft.com/kb/916196.

1. Copy the files in 'FD_Inst_WinXP' in the SATA driver package to the root of a floppy disk. The SATA driver package can be obtained from http://edc.intel.com/Platforms/Atom-E6xx/#software.
   - iohsata.cat
   - iohsata.inf
   - iohsata.sys
   - txtsetup.oem
2. Make sure that the target computer has a compatible floppy drive.
3. Insert the floppy disk prepared in step 1 into the floppy drive.
4. Insert the Windows XP SP3 installer into the CD-ROM and boot from the CD-ROM to start the Windows XP SP3 installation.
5. Press <F6> to add further SCSI/RAID drivers when prompted during the very early stage of the Windows installation. (Figure 17)

Figure 17. Installing the Intel® PCH EG20T SATA Driver - press F6



6. Press <S> to add an additional SCSI device. Select the correct driver (Intel® PCH EG20T SATA AHCI Controller for Windows XP) and press <ENTER> to continue the

installation. This will install the Intel® PCH EG20T SATA AHCI controller driver (Figure 18).

Figure 18. Selecting the SCSI Adapter

Note: Slipstreaming the Intel® PCH EG20T SATA AHCI controller driver onto the Windows XP SP3 installer will not work.

7. During the installation, the message box below may appear:

At this time, any low/full speed USB devices (for example the keyboard and mouse) that are connected to USB port 1 (Device2:Function0), USB port 3 (Device2:Function1) and USB Port 5 (Device2:Function2) will not function for a brief period during installation. This may appear due to an OHCI driver issue for USB Host controller #1 (Device 2: Function 0-2). These USB ports will resume working once you can dismiss the above message box by clicking Yes. Figure 19 indicates the internal USB port connections.

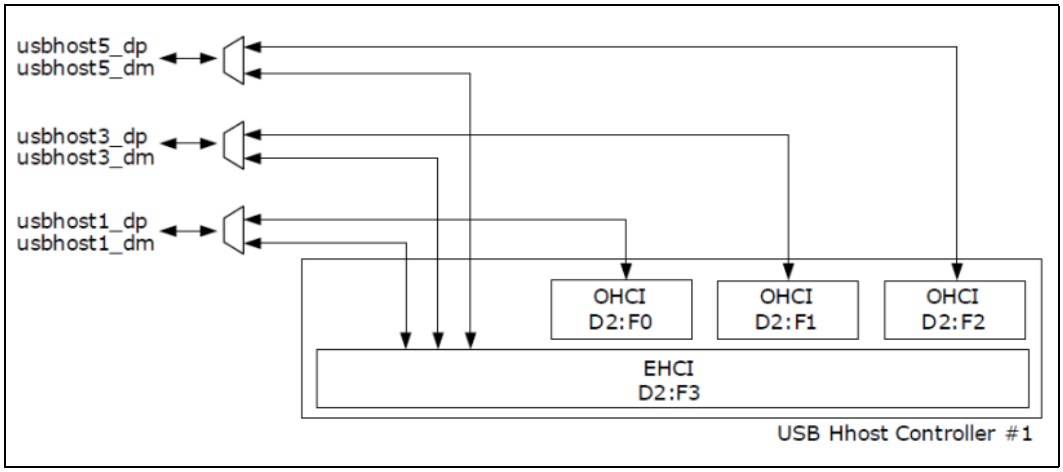
The proposed workarounds for this issue are:

— For a customer design that has PS2 ports, please use a PS2 mouse and keyboard to facilitate the installation.

— For a customer design that has USB port 0/2/4 (USB Host controller #0 Device 8:Function 0-2), use those ports for the USB mouse and keyboard connection to facilitate the installation.

— For a customer design that has only ports 1/3/5 (USB Host controller #1 Device 2: Function 0-2), please connect a USB mouse and keyboard through the USB high speed hub.

Figure 19. USB Host Controller #1 Port Connection



8. Finish the Windows XP installation according to your needs.

5.9.2 MeeGo*

You can obtain the latest MeeGo OS image from:

https://www.meego.com/

Download the version for In-Vehicle Infotainment (IVI) applications and follow the installation instructions provided.

To use the embedded graphics drivers, refer to the EMGD site:

http://www.intel.com/p/en_US/embedded/hwsw/software/emgd

Follow the download and installation instructions provided in the *Intel® Embedded Media and Graphics Driver v1.10 for Windows* XP, Windows* Embedded Compact 7 and Linux* User Guide*.

5.9.3 Timesys Fedora* Remix

You can obtain the latest OS image from:

https://linuxlink.timesys.com/intel/login

Download OS installer and follow the installation instructions provided. Note that you will have to register to obtain the free image.

To use the embedded graphics drivers, refer to the EMGD site:

http://www.intel.com/p/en_US/embedded/hwsw/software/emgd

Follow the download and installation instructions provided in the *Intel® Embedded Media and Graphics Driver v1.10 for Windows* XP, Windows* Embedded Compact 7 and Linux* User Guide*.

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6.0 Quick Start

The development kit is shipped as an open system allowing maximum flexibility in changing hardware configuration and peripherals. Use caution when configuring the hardware and observe proper safety cautions and warnings. The following sections summarize the necessary hardware and power-on instructions.

Note: Always turn off the power and unplug the power cord before changing hardware configuration and peripherals. The user is required to observe extra precautions when handling and operating the system.

Review the document provided with the reference board titled *Important Safety and Regulatory Information*. This document contains additional safety warnings and cautions.

6.1 Required Peripherals

- ATX power supply
- Keyboard and mouse
- SATA hard drive preloaded with OS
- DVD-ROM (optional if OS is preloaded on hard drive)
- SATA cable
- LVDS panel and backlight inverter (if required)
- Associated cables

Note: PCIe* and ADD2-N (VGA output provided) graphics card “Quick Start” is not included in this document.

6.2 Display Assembly (LVDS Panel)

Figure 20. AUO 8.4 inch Panel

Figure 21. LVDS Cable Connected to the Carrier Board

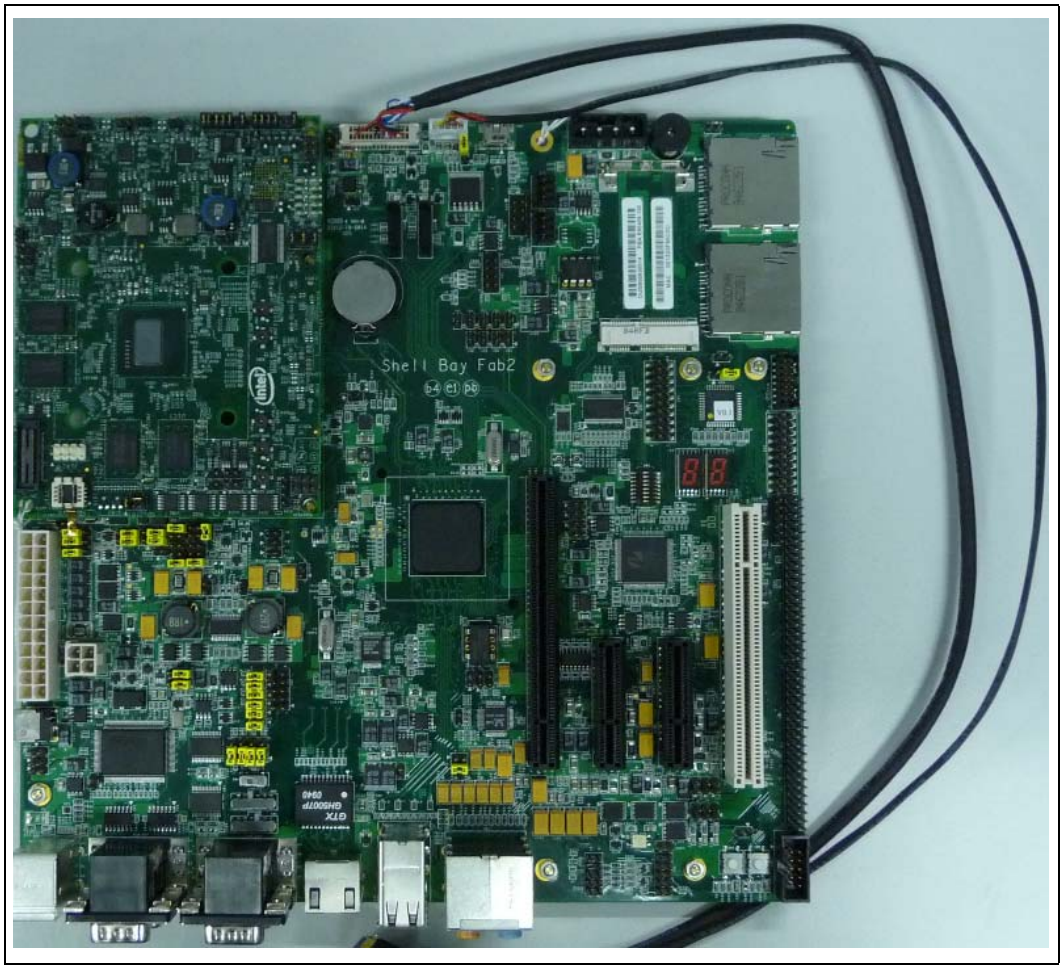
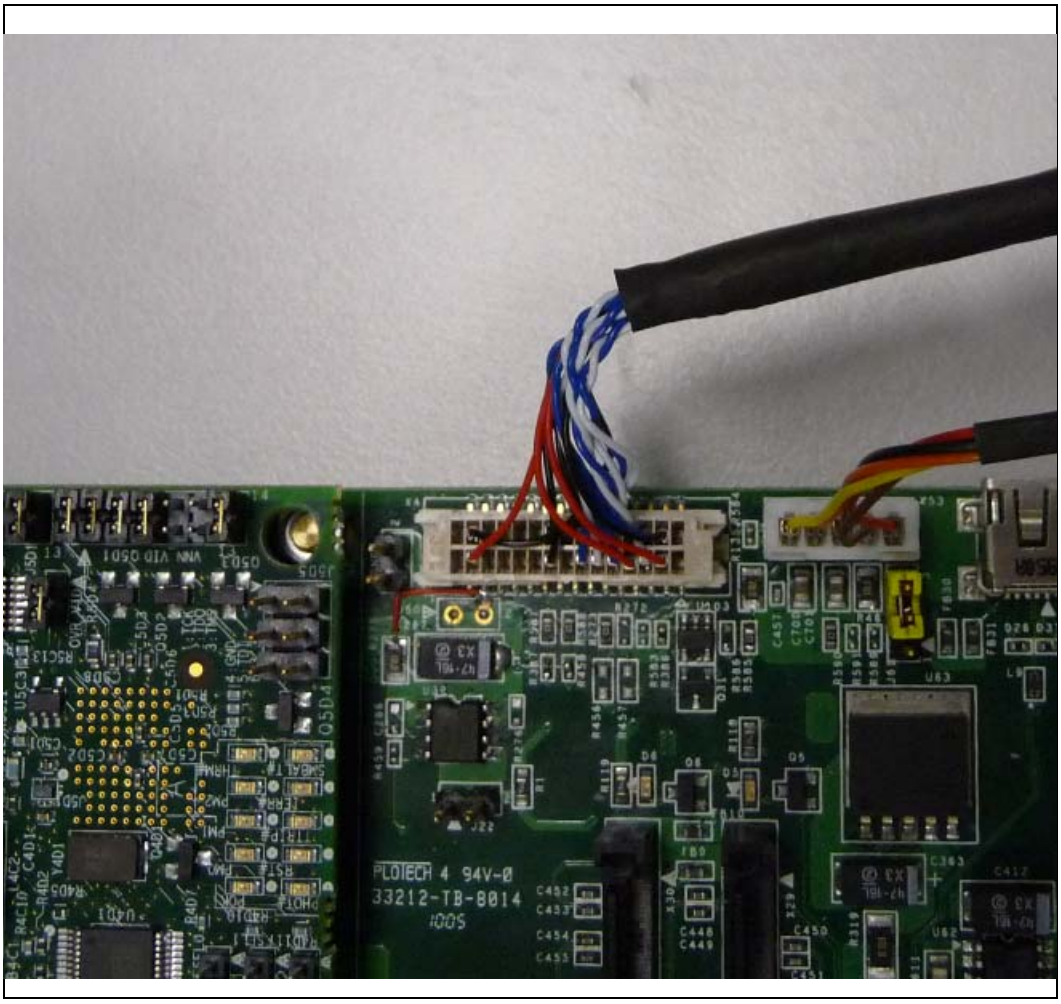


Figure 22. LVDS Connector and Cable



Complete the following steps to operate the reference board with the AUO 8.4 inch (213.4 mm), 800x 600 (G084SN05 V8) panel. These steps will change if using different displays.

1. Attach the LVDS cable to the AUO panel and carrier board as shown in Figure 20, Figure 21 and Figure 22.
2. Attach the additional +12V built onto the LVDS cable for LED backlight to onboard 12V supply at X53.

6.3 Heat Sink Installation

All Intel® Atom™ Processor E6xx series (except the 0.6 GHz, 2.7 W devices) require a thermal solution. This section describes how to attach the processor heat sink included in your development kit.

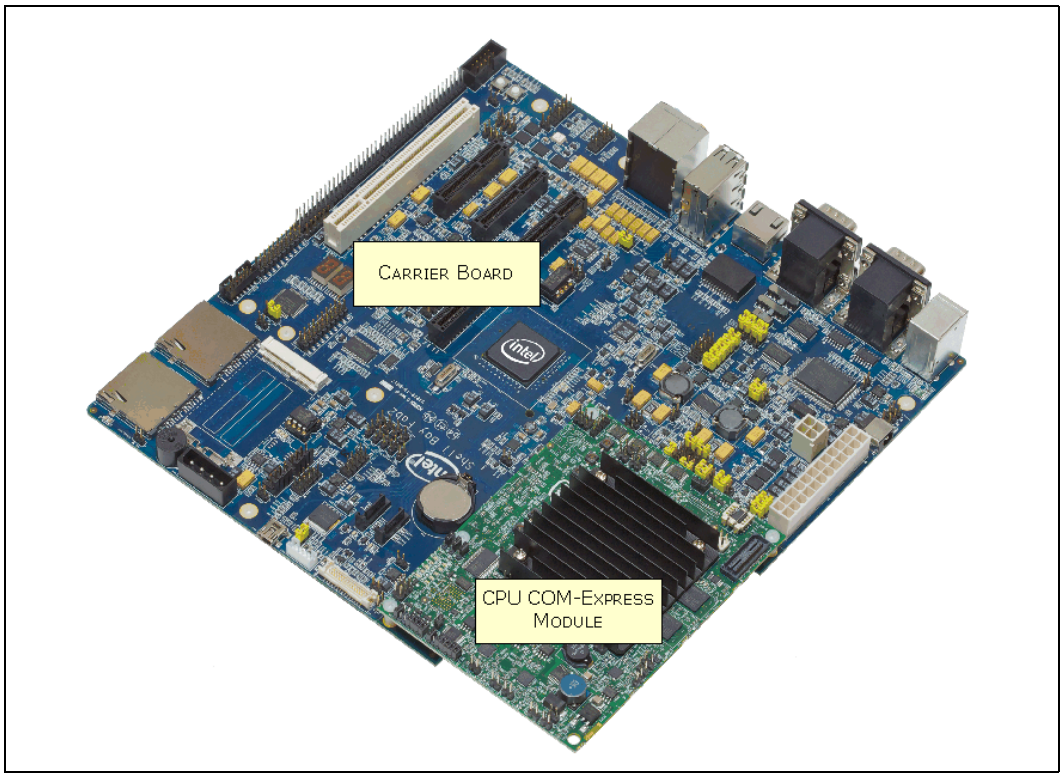
You will need:

- Flat-head and Phillips-head screwdriver
- Linen free cloth
- Isopropyl alcohol (IPA)

If you are reinstalling the heat sink after removing it, you may also need thermal interface material (TIM).

6.3.1 COM Express* Module and Carrier Board

Figure 23. COM Express* Module and Carrier Board

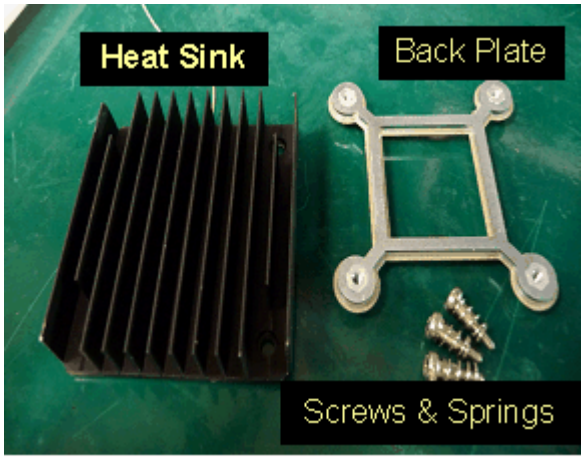


6.3.2 Heat Sink Installation

Note: All SKU except ULP (0.6GHz, 2.7W) parts require heat sink as cooling solutions.

1. Check heat sink and back plate for any visual defects prior to assembly.

Figure 24. Heat Sink Components

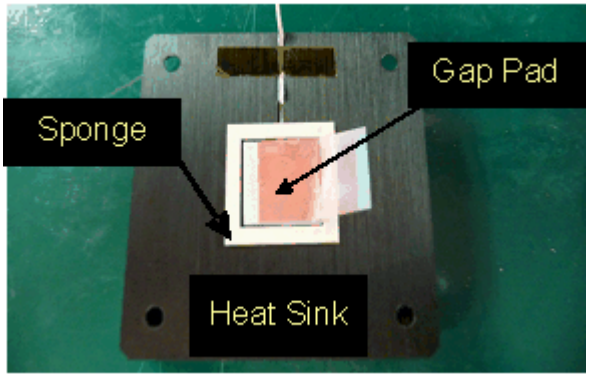


2. Remove double sided tape sticker from back-plate. Attach the back plate onto the bottom side of the PCB. Back-plate pins should be aligned to PCB holes.
3. A gap pad and sponge is provided with the heat sink assembly.

Note: Thermal grease (TIM) is only needed when heat sink has been removed and reinstalled or when the gap pad has been damaged.

4. Attach the gap pad and sponge to the center of the heat sink as shown in Figure 25.

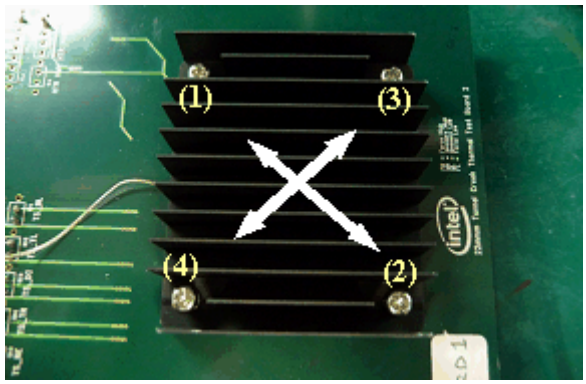
Figure 25. Back Side of the Heat Sink



5. Clean package top surface with a clean towel and isopropyl alcohol.
6. Gently place heat sink on top of processor with heat sink mounting holes aligning with the pins on the back plate.
7. Insert springs onto all screws; fasten the screws diagonally, following the similar sequence as shown in Figure 26.

Caution: Do not apply external downward pressure onto heat sink during installation.

Figure 26. Sequence to Fasten the Screws



6.4 Power On

Complete the following steps to operate the reference board:

1. Install or verify the configuration jumpers as shown in Section 4.3.1.
2. Verify the presence of an RTC battery at X13.
3. Plug in an ATX power supply into connector X1. The connector is keyed and will only fit in one position.
4. Connect a SATA hard drive to onboard SATA receptacle X29 or X30 (see Figure 12) and ATX power to hard drive via a SATA power cable.
5. Connect a PS/2 keyboard to connector X15 (bottom) (shown in Figure 12).
6. Connect a PS/2 mouse to connector X14 (top) (shown in Figure 12).
7. Follow steps in Section 6.2 to complete the display assembly. If an alternative to the integrated graphics is desired, plug a PCIe* x1 Graphics card in the PCIe* slot.

Note: If PCIe* Slot X10 is used, make sure SW4-1 is ON to connect PCIe* Port 3 link to PCIe* Slot X10 and disable Mini PCIe* Slot (X8). Refer to Figure 3 and Section 4.6 for more details.

6.4.1 Power Up

1. Ensure power supply is plugged in and press the power button located at SW5.
2. As the system boots, press F2 or the Delete button on the keyboard to enter the BIOS setup screen.
3. Check time, date and configuration settings. For most users the default setting should be sufficient for the initial bring-up.
4. Press F10 to save and quit the BIOS setup.

5. The system reboots and is ready for use.

Note: If the board does not power up completely, the port 80 code on the 7-segment displays (D9 and D10) may provide insight into the issue. Refer to Section 5.3.4 for more detail.

6.4.2 Power Down

1. Use OS controlled shutdown mechanism (Windows Start menu or equivalent).
2. If the system is hung, it is possible to asynchronously shut the system down by holding the power button (SW5) down continuously for at least 3 seconds.

Note: Intel does not recommend powering down the board by shutting off power at the ATX power supply.

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