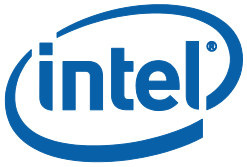

White Paper

**David Hibler Jr**
Platform Solutions Engineer
Intel Corporation

# Considerations for designing an Embedded IA System with DDR3 ECC SO-DIMMs

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# Executive Summary

*What are ECC SO-DIMMs? How do I design with them in my platform?* If these are some of the questions you have when the term "ECC SO-DIMM" comes up, then this paper may be for you. Since the ECC SO-DIMM form factor is an alternative solution that is often considered in the Embedded market this paper will look at all the aspects of preparing for and designing an Embedded system with ECC SO-DIMMs instead of using the traditional DDR3 UDIMM or SO-DIMM memory. Each level of a system design will be addressed in this paper.

*The ECC SO-DIMM form factor is an alternative solution often considered in the embedded market…*

The levels of a system design that will be covered include:

- Product Planning
- Board Design
- Software Considerations

The goal of this paper is to provide an a starting place for the creation of an Intel Architecture system with ECC SO-DIMM and to help alleviate early questions that system designers may have.

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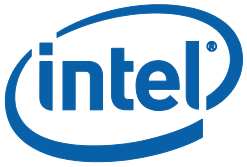


# Background

The term "ECC SO-DIMM" is used to describe a newer memory form factor module available on the market. ECC stands for *Error Correcting Code* while SO-DIMM stands for *Small Outline Dual Inline Memory Module*. The ECC SO-DIMM is capable of handling a 72-bit data interface. This form factor adds ECC capability to the current SO-DIMM specs and keeps a similar form factor (with changes in pinout).

The ECC SO-DIMM form factor is an alternative solution that is often considered in the embedded market due to the variety of constraints and usage models embedded customers require. The ECC SO-DIMM form factor may help ease or conform to the design constraints that are faced by many embedded applications.

**Table 1: ECC SO-DIMM Product Family Attributes:**

| | |
|---|---|
| DIMM Organization | X72 ECC |
| DIMM dimensions: height (nom.) x width (nom.) x thickness (max.) / MO-number, Variation | 30.0 mm x 67.6 mm x 3.80 mm / MO-268, Variation xA |
| Pin Count | 204 |
| SDRAMs supported | 512 Mb, 1 Gb, 2 Gb, 4 Gb, 8 Gb |
| Ranks supported per DIMM | 1, 2 ,4 |
| Capacity | 256 MB, 512 MB, 1 GB, 2 GB, 4 GB, 8 GB, 16 GB, 32 GB |
| Serial PD | Consistent with JC 45 |
| Voltage options | 1.5 volt (VDD), 3.3 volt (VDDSPD) |
| Interface | 1.5 volt signal switching based on reference voltage at VDD/2. See DRAM specification for more detail. |

This paper will go over all items that need to be considered when looking into designing an embedded system with DDR3 ECC SO-DIMMS instead of using the traditional DDR3 UDIMM or standard SO-DIMM memory. Different aspects of system design will be addressed in this paper including background on ECC SO-DIMMS, and checklists to aid in determining if ECC SO-DIMM is the right solution for your application. The goal of this paper is to provide a starting place for the creation of an Intel® Architecture system with ECC SO-DIMM and to help alleviate early questions that system designers may have.

This paper is based on the JEDEC base spec revision for DDR3 SDRAM 72b-ECC SO-DIMM at 0.5 with several RAW cards Annex revisions at 1.0.

# *Planning*

Before building an actual system, there are several considerations that need to be looked at in determining if ECC SO-DIMMs are right for your design.

## Is ECC SO-DIMM the right memory form factor for my system?

When determining if ECC SO-DIMM is the right application for your system the following checklist is meant to help with the decision making process:

**Systems which would benefit from ECC SO-DIMMs**

- ✓ The system may be subject to internal data corruption and system memory errors are a crucial point for the system design (i.e used in financial or scientific computing)
    - Since ECC SO-DIMMs have the capability to detect and/or correct errors for data in memory they would be a good fit for these types of systems
- ✓ The design needs to have the option of ECC capability
    - Since ECC SO-DIMMs and SO-DIMMS are not pinout compatible, if a designer wishes to have a more flexible design, going with ECC SO-DIMM as a base provides this option
- ✓ The size of the DIMM form factor is important
    - Due to its smaller size ECC SO-DIMMs would be a good fit over systems that have tight board space compared to using traditional UDIMMs.
- ✓ Connector varieties and orientation to the main board is an important factor
    - Since the ECC SO-DIMM is based on the standard SO-DIMM form factor, there are many connector designs to choose from including 180 degree or 90 degree orientations.

**Systems which may not benefit from ECC SO-DIMMs**

- ✓ The design does not require ECC capability
    - While it is possible to use ECC SO-DIMMs in these system since this feature would not be used designers would most likely want to choose the standard SO-DIMM as it more widely used in the market.
- ✓ System BOM cost is a high priority

- Since ECC SO-DIMM is a new player in the market, the costs may be slightly higher than traditional UDIMM or standard SO-DIMMs currently available. For more details on this please contact your memory provider.

Once it is determined whether ECC SO-DIMM is right for your system you can move forward with confidence and start looking into more details.

**Figure 1: General layout of an ECC SO-DIMM module**


# Board Design

When designing the PCB, a few points need to be considered when utilizing an ECC SO-DIMM implementation. Let's walk through each step of the board design going through schematics and layout.

## Key differences between standard SO-DIMMs and ECC SO-DIMMs

If designers have used standard SO-DIMMs in the past there are some details that need to be considered. While very similar in design, standard SO-DIMMs and ECC SO-DIMMs do differ.

The major difference in these form factors is the pinout. The following diagrams show pin outs for each form factor.

**Figure 2: Standard SO-DIMM Pinout**

| Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Vref/DQ | 2 | GND | 53 | DQ19 | 54 | GND | 105 | VDD | 106 | VDD | 157 | DQ42 | 158 | DQ46 |
| 3 | GND | 4 | DQ4 | 55 | GND | 56 | DQ28 | 107 | A10/AP | 108 | BA1/BA0[3] | 159 | DQ43 | 160 | DQ47 |
| 5 | DQ0 | 6 | DQ5 | 57 | DQ24 | 58 | DQ29 | 109 | BA0/BA1[3] | 110 | $\overline{RAS}$ | 161 | GND | 162 | GND |
| 7 | DQ1 | 8 | GND | 59 | DQ25 | 60 | GND | 111 | VDD | 112 | VDD | 163 | DQ48 | 164 | DQ52 |
| 9 | GND | 10 | $\overline{DQS0}$ | 61 | GND | 62 | $\overline{DQS3}$ | 113 | $\overline{WE}$ | 114 | $\overline{S0}$ | 165 | DQ49 | 166 | DQ53 |
| 11 | DM0 | 12 | DQS0 | 63 | DM3 | 64 | DQS3 | 115 | $\overline{CAS}$ | 116 | ODT0 | 167 | GND | 168 | GND |
| 13 | GND | 14 | GND | 65 | GND | 66 | GND | 117 | VDD | 118 | VDD | 169 | $\overline{DQS6}$ | 170 | DM6 |
| 15 | DQ2 | 16 | DQ6 | 67 | DQ26 | 68 | DQ30 | 119 | A13[4] | 120 | ODT1 | 171 | DQS6 | 172 | GND |
| 17 | DQ3 | 18 | DQ7 | 69 | DQ27 | 70 | DQ31 | 121 | $\overline{S1}$ | 122 | NC | 173 | GND | 174 | DQ54 |
| 19 | GND | 20 | GND | 71 | GND | 72 | GND | 123 | VDD | 124 | VDD | 175 | DQ50 | 176 | DQ55 |
| 21 | DQ8 | 22 | DQ12 | 73 | CKE0 | 74 | CKE1 | 125 | TEST | 126 | VrefCA | 177 | DQ51 | 178 | GND |
| 23 | DQ9 | 24 | DQ13 | 75 | VDD | 76 | VDD | 127 | GND | 128 | GND | 179 | GND | 180 | DQ60 |
| 25 | GND | 26 | GND | 77 | NC | 78 | A15/BA3[4] | 129 | DQ32 | 130 | DQ36 | 181 | DQ56 | 182 | DQ61 |
| 27 | $\overline{DQS1}$ | 28 | DM1 | 79 | BA2 | 80 | A14[4] | 131 | DQ33 | 132 | DQ37 | 183 | DQ57 | 184 | GND |
| 29 | DQS1 | 30 | $\overline{RST}$ | 81 | VDD | 82 | VDD | 133 | GND | 134 | GND | 185 | GND | 186 | $\overline{DQS7}$ |
| 31 | GND | 32 | GND | 83 | A12/$\overline{BC}$ | 84 | A11 | 135 | $\overline{DQS4}$ | 136 | DM4 | 187 | DM7 | 188 | DQS7 |
| 33 | DQ10 | 34 | DQ14 | 85 | A9 | 86 | A7/A8[3] | 137 | DQS4 | 138 | GND | 189 | GND | 190 | GND |
| 35 | DQ11 | 36 | DQ15 | 87 | VDD | 88 | VDD | 139 | GND | 140 | DQ38 | 191 | DQ58 | 192 | DQ62 |
| 37 | GND | 38 | GND | 89 | A8/A7[3] | 90 | A6/A5[3] | 141 | DQ34 | 142 | DQ39 | 193 | DQ59 | 194 | DQ63 |
| 39 | DQ16 | 40 | DQ20 | 91 | A5/A6[3] | 92 | A4/A3[3] | 143 | DQ35 | 144 | GND | 195 | GND | 196 | GND |
| 41 | DQ17 | 42 | DQ21 | 93 | VDD | 94 | VDD | 145 | GND | 146 | DQ44 | 197 | SA0 | 198 | $\overline{EVENT}$ |
| 43 | GND | 44 | GND | 95 | A3/A4[3] | 96 | A2 | 147 | DQ40 | 148 | DQ45 | 199 | $VDD_{SPD}$ | 200 | SDA |
| 45 | $\overline{DQS2}$ | 46 | DM2 | 97 | A1 | 98 | A0 | 149 | DQ41 | 150 | GND | 201 | SA1 | 202 | SCL |
| 47 | DQS2 | 48 | GND | 99 | VDD | 100 | VDD | 151 | GND | 152 | $\overline{DQS5}$ | 203 | VTT | 204 | VTT |
| 49 | GND | 50 | DQ22 | 101 | CK0 | 102 | $\overline{CK1}$ | 153 | DM5 | 154 | DQS5 | | | | |
| 51 | DQ18 | 52 | DQ23 | 103 | $\overline{CK0}$ | 104 | CK1 | 155 | GND | 156 | GND | | | | |

1. NC = No Connect, NU = Not Useable, RFU = Reserved Future Use
2. TEST(pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
3. DRAM of Rank 1 are connected to the first, DRAMs of rank 2 are connected to the second. E.g. If $\overline{S0}$ is active, pin 86 has the function of A7, If $\overline{S1}$ is active pin 86 has the function of A8
4. This address might be connected to NC balls of the DRAMs (depending on density); eitherway they will be connected to the termination resistor.

**Figure 3: ECC SO-DIMM Pinout**

| Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREFDQ | 2 | VSS | 53 | VSS | 54 | DQ28 | 103 | A3 | 104 | A4 | 155 | VSS | 156 | DQS5_t |
| 3 | VSS | 4 | DQ4 | 55 | DQ24 | 56 | DQ29 | 105 | A1 | 106 | A2 | 157 | DM5 | 158 | VSS |
| 5 | DQ0 | 6 | DQ5 | 57 | DQ25 | 58 | VSS | 107 | A0 | 108 | BA1 | 159 | DQ42 | 160 | DQ46 |
| 7 | DQ1 | 8 | VSS | 59 | DM3 | 60 | DQS3_c | 109 | VDD | 110 | VDD | 161 | DQ43 | 162 | DQ47 |
| 9 | VSS | 10 | DQS0_c | 61 | VSS | 62 | DQS3_t | 111 | CK0_t | 112 | Par_In, NC, CK1_t | 163 | VSS | 164 | VSS |
| 11 | DM0 | 12 | DQS0_t | 63 | DQ26 | 64 | VSS | 113 | CK0_c | 114 | Err_Out_n, NC, CK1_c | 165 | DQ48 | 166 | DQ52 |
| 13 | DQ2 | 14 | VSS | 65 | DQ27 | 66 | DQ30 | 115 | VDD | 116 | VDD | 167 | DQ49 | 168 | DQ53 |
| 15 | DQ3 | 16 | DQ6 | 67 | VSS | 68 | DQ31 | 117 | A10/AP | 118 | S3_n | 169 | VSS | 170 | VSS |
| 17 | VSS | 18 | DQ7 | 69 | CB0 | 70 | VSS | 119 | BA0 | 120 | S2_n | 171 | DQS6_c | 172 | DM6 |
| 19 | DQ8 | 20 | VSS | 71 | CB1 | 72 | CB4 | 121 | WE_n | 122 | RAS_n | 173 | DQS6_t | 174 | DQ54 |
| 21 | DQ9 | 22 | DQ12 | Key | | | | 123 | VDD | 124 | VDD | 175 | VSS | 176 | DQ55 |
| 23 | VSS | 24 | DQ13 | 73 | VSS | 74 | CB5 | 125 | CAS_n | 126 | ODT0 | 177 | DQ50 | 178 | VSS |
| 25 | DQS1_c | 26 | VSS | 75 | DQS8_c | 76 | DM8 | 127 | S0_n | 128 | ODT1 | 179 | DQ51 | 180 | DQ60 |
| 27 | DQS1_t | 28 | DM1 | 77 | DQS8_t | 78 | VSS | 129 | S1_n | 130 | A13 | 181 | VSS | 182 | DQ61 |
| 29 | VSS | 30 | RESET_n | 79 | VSS | 80 | CB6 | 131 | VDD | 132 | VDD | 183 | DQ56 | 184 | VSS |
| 31 | DQ10 | 32 | VSS | 81 | CB2 | 82 | CB7 | 133 | DQ32 | 134 | DQ36 | 185 | DQ57 | 186 | DQS7_c |
| 33 | DQ11 | 34 | DQ14 | 83 | CB3 | 84 | VREFCA | 135 | DQ33 | 136 | DQ37 | 187 | VSS | 188 | DQS7_t |
| 35 | VSS | 36 | DQ15 | 85 | VDD | 86 | VDD | 137 | VSS | 138 | VSS | 189 | DM7 | 190 | VSS |
| 37 | DQ16 | 38 | VSS | 87 | CKE0 | 88 | A15 | 139 | DQS4_c | 140 | DM4 | 191 | DQ58 | 192 | DQ62 |
| 39 | DQ17 | 40 | DQ20 | 89 | CKE1 | 90 | A14 | 141 | DQS4_t | 142 | DQ38 | 193 | DQ59 | 194 | DQ63 |
| 41 | VSS | 42 | DQ21 | 91 | BA2 | 92 | A9 | 143 | VSS | 144 | DQ39 | 195 | VSS | 196 | VSS |
| 43 | DQS2_c | 44 | DM2 | 93 | VDD | 94 | VDD | 145 | DQ34 | 146 | VSS | 197 | SA0 | 198 | EVENT_n |
| 45 | DQS2_t | 46 | VSS | 95 | A12/BC_n | 96 | A11 | 147 | DQ35 | 148 | DQ44 | 199 | VDDSPD | 200 | SDA |
| 47 | VSS | 48 | DQ22 | 97 | A8 | 98 | A7 | 149 | VSS | 150 | DQ45 | 201 | SA1 | 202 | SCL |
| 49 | DQ18 | 50 | DQ23 | 99 | A5 | 100 | A6 | 151 | DQ40 | 152 | VSS | 203 | VTT | 204 | VTT |
| 51 | DQ19 | 52 | VSS | 101 | VDD | 102 | VDD | 153 | DQ41 | 154 | DQS5_c | | | | |

Terminology:
* Active low signals are indicated by the suffix "_n"
* Positive line of differential pairs are indicated by the suffix "_t"
* Complementary inputs of differential pairs are indicated by the suffix "_c"

Note that the mechanical key for ECC SO-DIMMs and Standard SO-DIMMs is the same, so care needs to be taken to note that in a design to ensure the correct type of memory is used in the system. (i.e. Standard SO-DIMMs will not function in a system designed for ECC SO-DIMMs)

Table 2 lists the pin differences by specific pin number, which as can be seen is quite substantial.

**Table 2: ECC SO-DIMM and Standard SO-DIMM Pinout Differences**

| Pin # | ECC SO-DIMM | Standard SO-DIMM | Pin # | ECC SO-DIMM | Standard SO-DIMM |
|---|---|---|---|---|---|
| 13 | DQ2 | GND | 105 | A1 | VDD |
| 15 | DQ3 | DQ2 | 106 | A2 | VDD |
| 17 | GND | DQ3 | 107 | A0 | A10/AP |
| 19 | DQ8 | GND | 108 | BA1 | BA1/BA0 |
| 21 | DQ9 | DQ8 | 109 | VDD | BA0/BA1 |
| 23 | GND | DQ9 | 110 | VDD | RAS_n |
| 25 | DQS1_c | GND | 111 | CK0 | VDD |

| Pin # | ECC SO-DIMM | Standard SO-DIMM | Pin # | ECC SO-DIMM | Standard SO-DIMM |
|---|---|---|---|---|---|
| 27 | DQS1 | DQS1_c | 112 | Par_in, NC, CK1 | VDD |
| 29 | GND | DQS1 | 113 | CK0_c | WE_n |
| 31 | DQ10 | GND | 114 | Err_out_n, NC, CK1_c | S0_c |
| 33 | DQ11 | DQ10 | 115 | VDD | CAS_n |
| 35 | GND | DQ11 | 116 | VDD | ODT0 |
| 37 | DQ16 | GND | 117 | A10/AP | VDD |
| 39 | DQ17 | DQ16 | 118 | S3_n | VDD |
| 41 | GND | DQ17 | 119 | BA0 | A13 |
| 43 | DQS2_c | GND | 120 | S2_n | ODT1 |
| 44 | DM2 | GND | 121 | WE_n | S1_n |
| 45 | DQS2 | DQS2_c | 122 | RAS_n | NC |
| 46 | GND | DM2 | 125 | CAS_n | TEST |
| 47 | GND | DQS2 | 126 | ODT0 | VrefCA |
| 48 | DQ22 | GND | 127 | SO_n | GND |
| 49 | DQ18 | GND | 128 | ODT1 | GND |
| 50 | DQ23 | DQ22 | 129 | S1_n | DQ32 |
| 51 | DQ19 | DQ18 | 130 | A13 | DQ36 |
| 52 | GND | DQ23 | 131 | VDD | DQ33 |
| 53 | GND | DQ19 | 132 | VDD | DQ37 |
| 54 | DQ28 | GND | 133 | DQ32 | GND |
| 55 | DQ24 | GND | 134 | DQ36 | GND |
| 56 | DQ29 | DQ28 | 135 | DQ33 | DQS4_n |
| 57 | DQ25 | DQ24 | 136 | DQ37 | DM4 |
| 58 | GND | DQ29 | 137 | GND | DQS4 |
| 59 | DM3 | DQ25 | 139 | DQS4_c | GND |
| 60 | DQS3_c | GND | 140 | DM4 | DQ38 |
| 62 | DQS3 | DQS3_c | 141 | DQS4 | DQ34 |
| 63 | DQ26 | DM3 | 142 | DQ38 | DQ39 |
| 64 | GND | DQS3 | 143 | GND | DQ39 |
| 65 | DQ27 | DQ26 | 144 | DQ39 | GND |
| 66 | DQ30 | GND | 145 | DQ34 | GND |

| Pin # | ECC SO-DIMM | Standard SO-DIMM | Pin # | ECC SO-DIMM | Standard SO-DIMM |
|---|---|---|---|---|---|
| 67 | GND | DQ26 | 146 | GND | DQ44 |
| 68 | DQ31 | DQ30 | 147 | DQ35 | DQ40 |
| 69 | CB0 | DQ27 | 148 | DQ44 | DQ45 |
| 70 | GND | DQ31 | 149 | GND | DQ41 |
| 71 | CB1 | GND | 150 | DQ45 | GND |
| 72 | CB4 | GND | 151 | DQ40 | GND |
| 73 | GND | CKE0 | 152 | GND | DQS5_c |
| 74 | CB5 | CKE1 | 153 | DQ41 | DM5 |
| 75 | DQS8_c | VDD | 154 | DQS5_c | DQS5 |
| 76 | DM8 | VDD | 156 | DQS5 | GND |
| 77 | DQS8 | NC | 157 | DM5 | DQ42 |
| 78 | GND | A15/BA3 | 158 | GND | DQ46 |
| 79 | GND | BA2 | 159 | DQ42 | DQ43 |
| 80 | CB6 | A14 | 160 | DQ46 | DQ47 |
| 81 | CB2 | VDD | 161 | DQ43 | GND |
| 82 | CB7 | VDD | 162 | DQ47 | GND |
| 83 | CB3 | A12/BC_c | 163 | GND | DQ48 |
| 84 | VREFCA | A11 | 164 | GND | DQ52 |
| 85 | VDD | A9 | 165 | DQ48 | DQ49 |
| 86 | VDD | A7/A8 | 166 | DQ52 | DQ53 |
| 87 | CKE0 | VDD | 167 | DQ49 | GND |
| 88 | A15 | VDD | 168 | DQ53 | GND |
| 89 | CKE1 | A8/A7 | 169 | GND | DQS6_c |
| 90 | A14 | A6/A5 | 170 | GND | DM6 |
| 91 | BA2 | A5/A6 | 171 | DQS6_c | DQS6 |
| 92 | A9 | A4/A3 | 172 | DM6 | GND |
| 95 | A12/BC_n | A3/A4 | 173 | DQS6 | GND |
| 96 | A11 | A2 | 175 | GND | DQ50 |
| 97 | A8 | A1 | 177 | DQ50 | DQ51 |
| 98 | A7 | A0 | 179 | DQ51 | GND |
| 99 | A5 | VDD | 181 | GND | DQ56 |
| 100 | A7 | VDD | 183 | DQ56 | DQ57 |
| 101 | VDD | CK0 | 185 | DQ57 | GND |
| 102 | VDD | CK1 | 187 | GND | DM7 |

| Pin # | ECC SO-DIMM | Standard SO-DIMM | Pin # | ECC SO-DIMM | Standard SO-DIMM |
|---|---|---|---|---|---|
| 103 | A3 | CK0_n | 189 | DM7 | GND |
| 104 | A4 | CK1_n | | | |
| -VSS and GND are used interchangeably<br>-Active low signals are indicated by the suffix "_n"<br>-Complementary inputs of differential pairs are indicated by the suffix "_c" | | | | | |

# Schematics

When designing the platform schematics, ensure that the symbols being designed in the schematics use the ECC SO-DIMM pinout.

The following examples are for DDR3 ECC SO-DIMM designs:

**Figure 4: Typical ECC SO-DIMM symbol for Schematics Design**

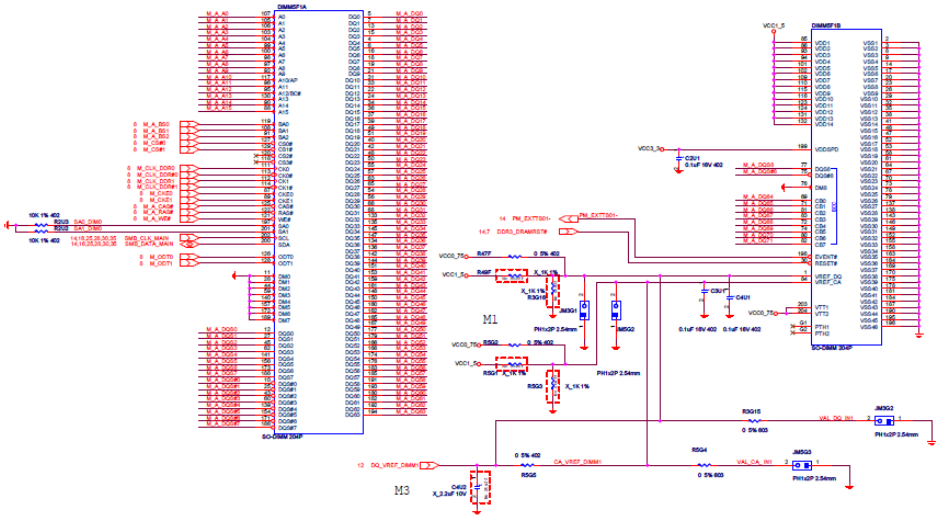
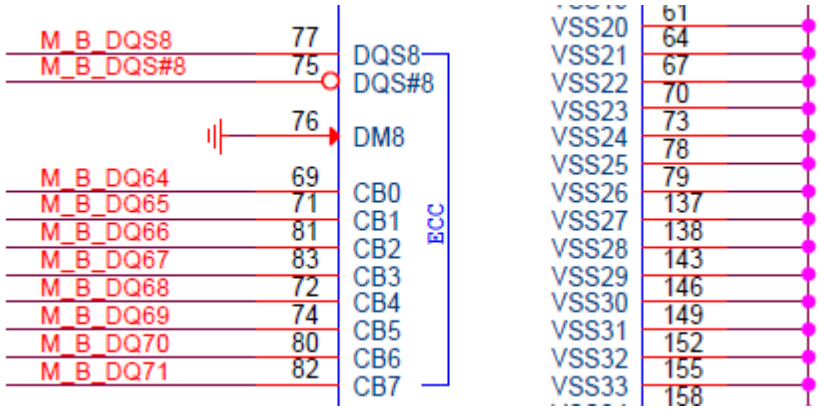


**Figure 5: Zoom view of ECC signals on the ECC SO-DIMM symbol**




# Layout

While there are many ways to route memory implementations the following sections provide an example to reference.

## Length Considerations and Routing Strategy

There are two levels of length constraints placed on each signal group within the interface.

- Absolute length constraints
  - The absolute length constraints are provided in the constraint tables for each signal group. These constraints define the length range over which signals meet signal integrity rules. A subset of this solution space is then defined via a set of clock length matching formulas, defined to ensure the clock relative AC timing margins. These two sets of overlapping length constraints then determine the final routing solution space for a particular platform design.
  - Perform a preliminary test route to establish the natural bounds on all signal groups. Once established, the target lengths for each channel clock group can then be defined such that an acceptable solution space is available when length matching formulas are applied.
- Clock length matching requirements
  - The clock target length is typically constrained on the low end by the control to clock length matching rules, and constrained on the high end by the strobe to clock rules, and the need to minimize data and strobe serpentine. The recommended approach consists of two steps:
    1. Determine the length of the longest control signal for each ECC SO-DIMM in the test route and define the clock target length for each ECC SO-DIMM as short as possible while ensuring the control trace lengths meet the control to clock length matching rule.
    2. Allow the command bus to be routed easily within the more relaxed command to clock length matching rules, and provide the least amount of DQ/DQS serpentine requirements. Check the clock target length a to make sure the longest DQ/DQS byte lanes fall within the resulting length formulas. Additionally, DQ to DQS length matching constraints should be met.

- For optimal timing margins, all clocks to a particular ECC SO-DIMM connector should be length tuned to the target length for that ECC SO-DIMM. Once defined these target lengths should be fed into the Trace Length Calculator to solve for the platform specific routing constraints for each signal group.
- The trace length calculator facilitates trace length matching on the DDR3 memory interface. For each DDR3 trace, segment-wise lengths can be entered and validated.As one motherboard may support multiple package skus, the processor packages are length matched either with same length or with some fixed length offsets between or among them.

## DDR3 Design Topologies

Since DDR3 is a popular type of memory used in the latest generation for embedded platforms, this section contains information and details on the DDR3 topologies. A topology example is provided for each corresponding signal group. While these may change for each type of platform it gives the general idea on what needs to be considered for ECC SO-DIMM designs.

Throughout these examples:

Design topologies are for a single ECC SO-DIMM per channel capable memory controller

Processor/Memory Controller are on the same BGA package

Lx (ie L1, L3)= A given trace length

PKG =Processor Package

### DDR3 Source-Synchronous Signals - DQ[63:0], DQS_{P/N}[8:0], ECC[7:0], DM[8:0]

The data signals are source-synchronous signals that include the 64-bit wide data bus, 8 ECC check bits and 18 data strobe signals.

**Figure 6: Data Group DQ Signal Topology**

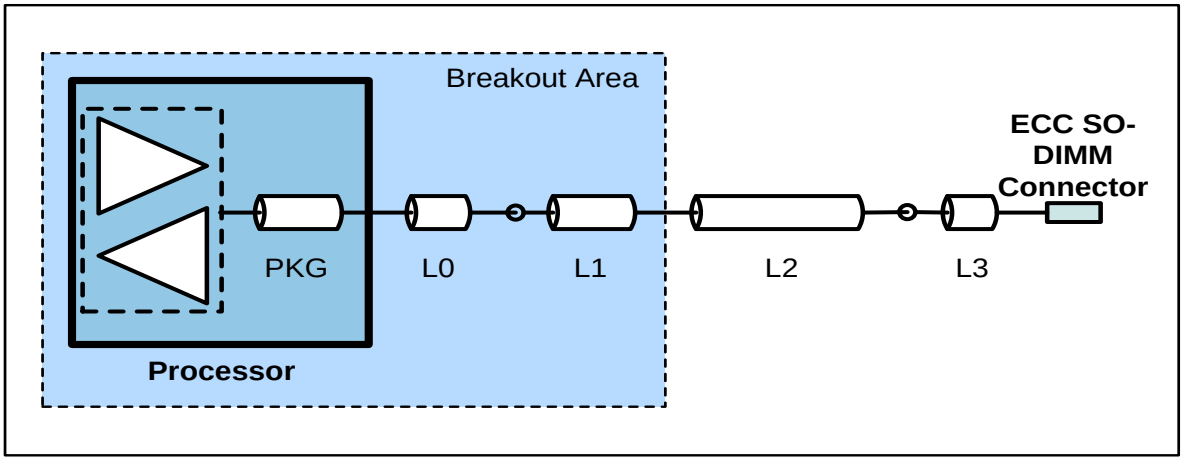
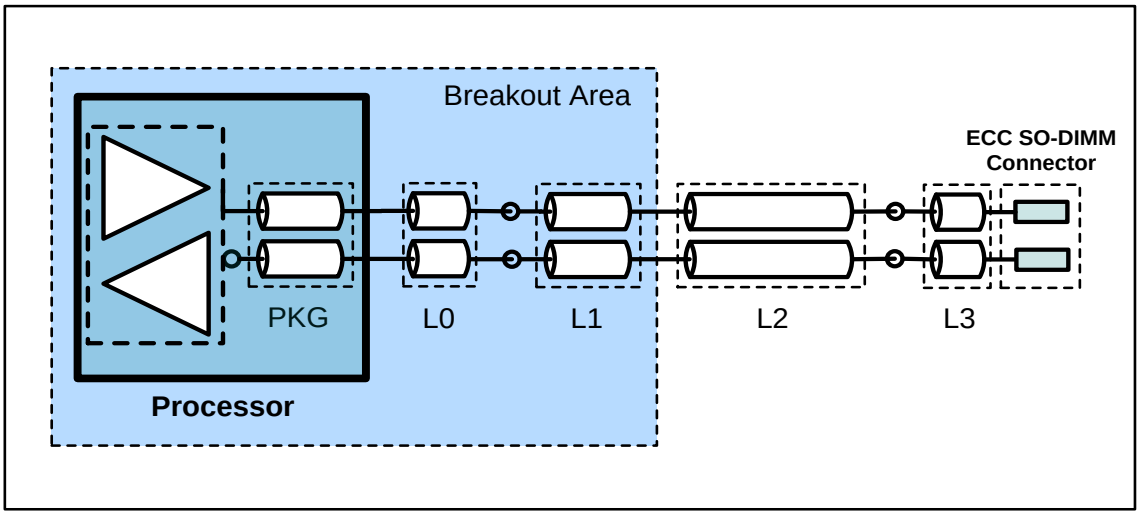


**Figure 7: Data Group DQS/DQS# Signal Topology**



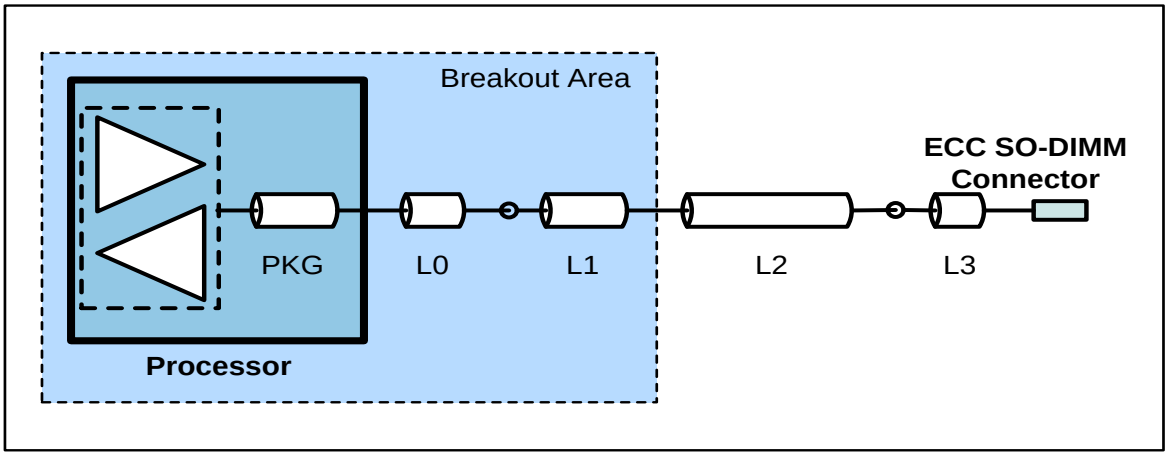

## DDR3 Control Group Source Clocked Signals - CS[1:0]#, ODT[1:0], and CKE[1:0]

The processor provides two chip select (CS#) signals, two ODT signals, and two CKE signals for each channel. These signals are "clocked" into the ECC SO-DIMMs using the positive edge of the differential clock signals.

These signals need to be routed with power referencing as they are power referenced on the processor and on the ECC SO-DIMMs. A 1.5V power island will need to be cut into the ground plane between the processor and the ECC SO-DIMMs to allow continuous power referencing for these signals.

All of these signals are routed point-to-point for the one ECC SO-DIMM slot per channel topology.

**Figure 8: Point-to-Point Control Signal Topology Diagram**

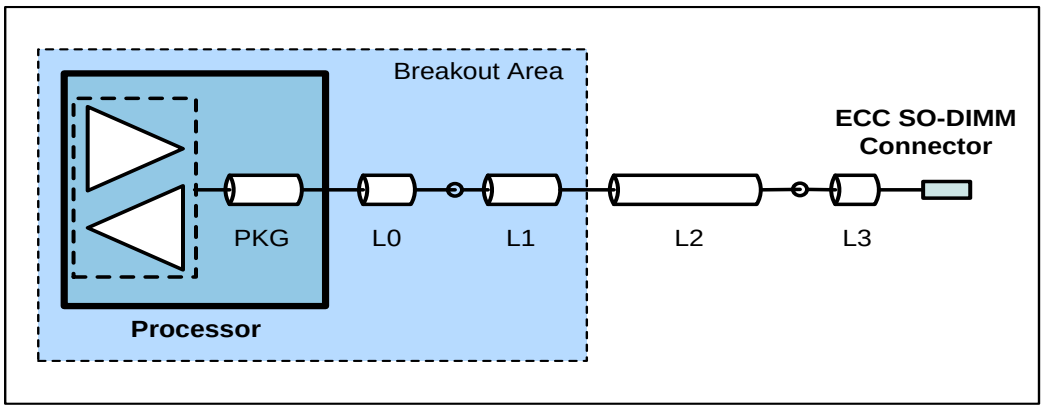


## DDR3 Address/Command Group Source Clocked Signals - MA[15:0], BA[2:0], RAS_N, CAS_N, and WE_N

The processor address/command signals are source-clocked output signals that include 16 system memory address signals (MA[15:0]), 3 bank addresses (BA[2:0]), row address select (RAS_N), column address select (CAS_N), and write enable (WE_N) for each channel. The address/command signals are "clocked" into the ECC SO-DIMMs using the positive edge of the differential clock signals. The processor drives the address/command and clock signals together. Each signal will be connected to one ECC SO-DIMM and needs to be tuned and length matched to its corresponding clock.

These signals need to be routed with power referencing as they are power referenced on the processor and on the ECC SO-DIMMs. A 1.5V power island will need to be cut into the ground plane between the processor and the ECC SO-DIMMs to allow continuous power referencing for these signals.

**Figure 9: Source Clocked Address/Command Group Signal Daisy Chain Topology Diagram**



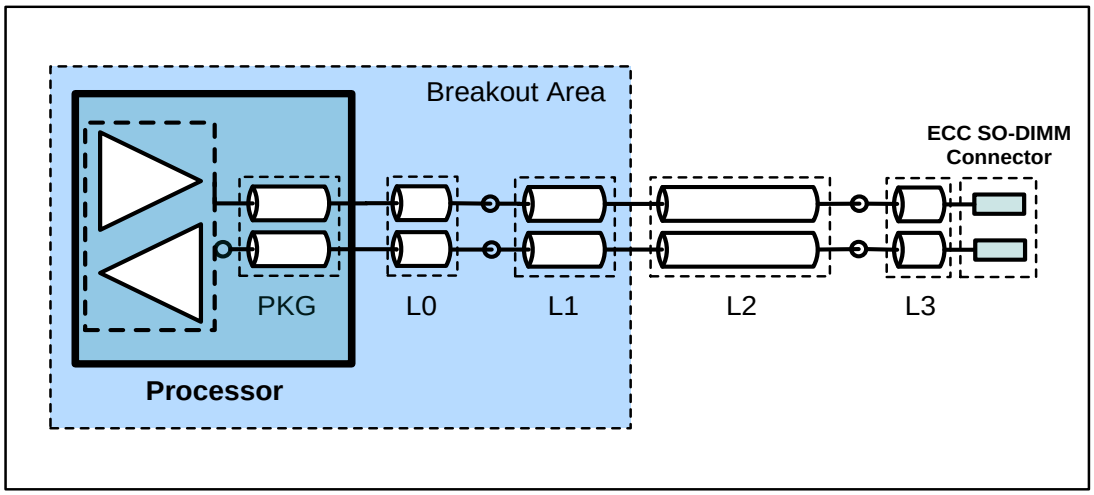

## DDR3 Clock Signals - CLK_{P/N}[1:0]

The processor provides two differential clock pairs (CLK_{P/N}[1:0]). The processor generates and drives these differential clock signals required by the DDR3 interface. As a result, no external clock driver is required. The differential clock pairs are routed to each ECC SO-DIMM connector. The differential clock pairs must be routed differentially from the processor balls to their associated ECC SO-DIMM pins and must maintain the correct isolation spacing from other signals. When the signals serpentine, it is important to maintain the minimum spacing to other DDR3 signals. While serpentining, the differential clock pair must maintain correct spacing to remain differential as well.

The clock signals need to be routed with power referencing as they are power referenced on the processor and on the ECC SO-DIMMs. A 1.5V power island will

need to be cut into the ground plane between the processor and the ECC SO-DIMMs to allow continuous power referencing for the clock signals.

**Figure 10: Point-to-Point Clock Signal Topology**




## Layout examples

The following examples are of a 8-layer board in the Mini-ITX form factor, which has two channels of DDR3 ECC SO-DIMMs.

**Figure 11: Board example (Top)**

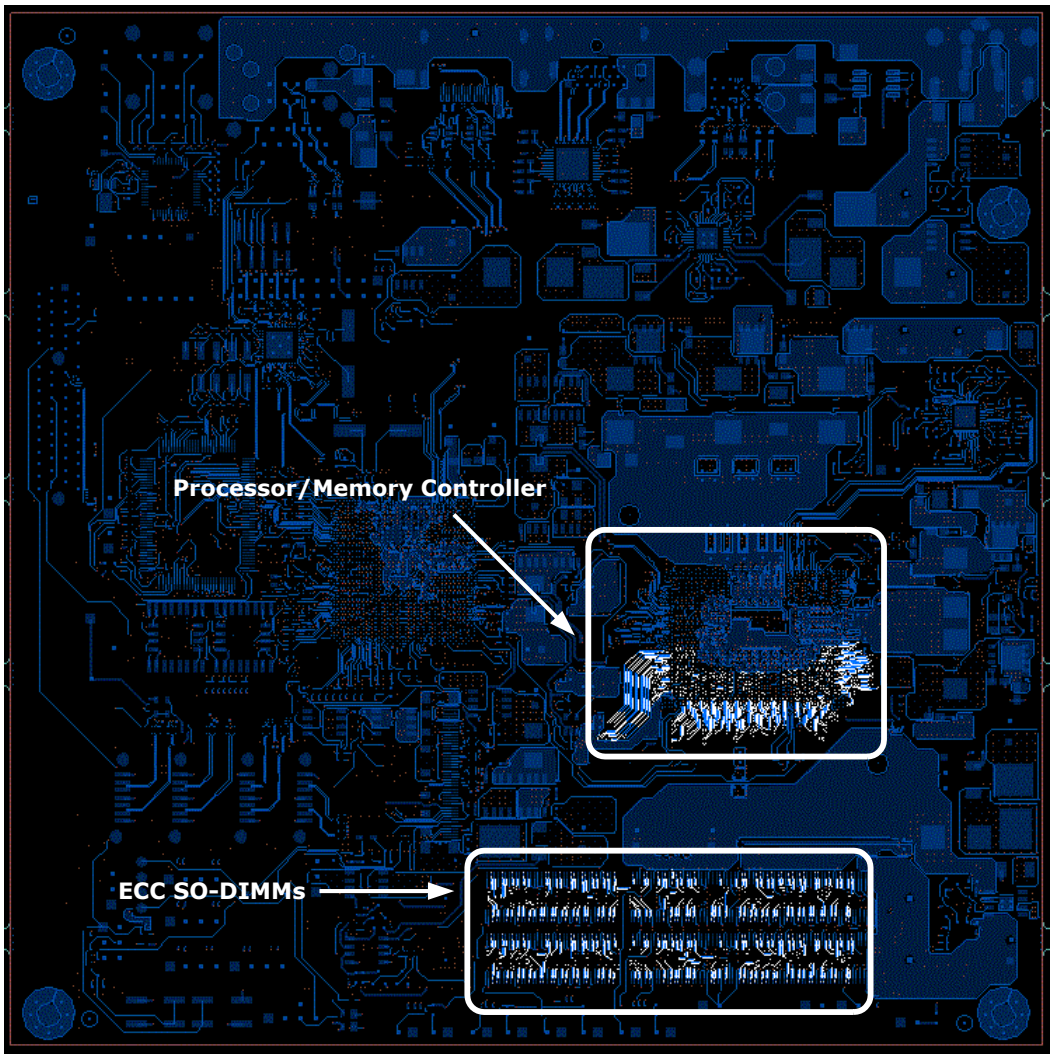


**Figure 12: Board example (Bottom)**

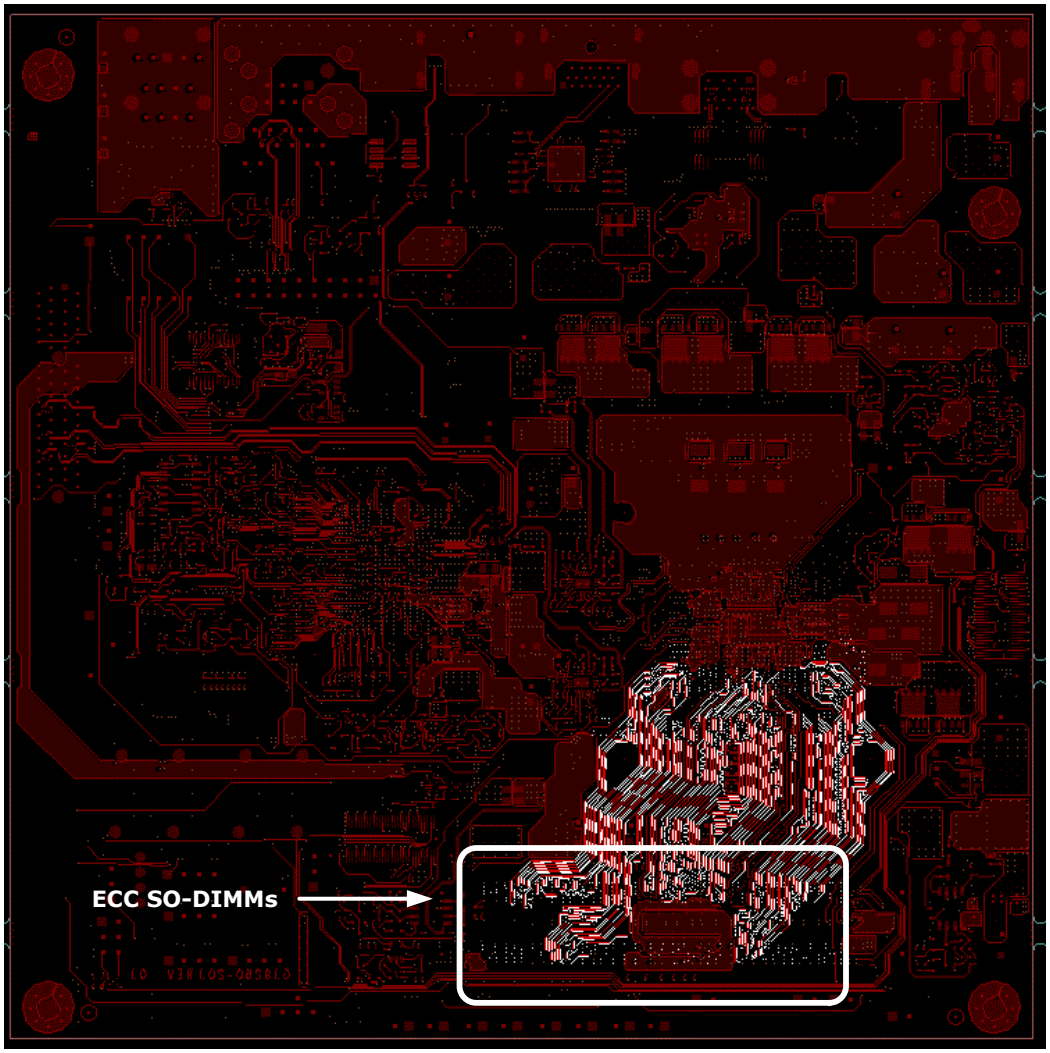


**Figure 13: Layer 3 routing example**

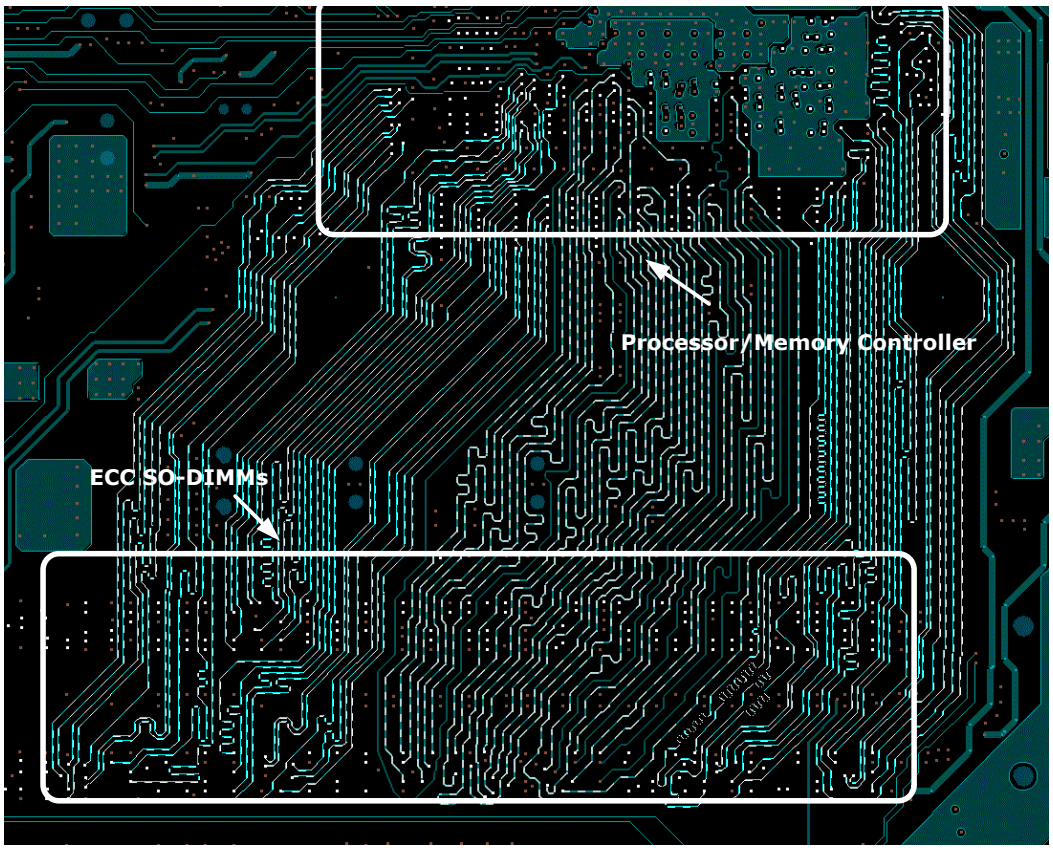


**Figure 14: Layer 6 routing example**

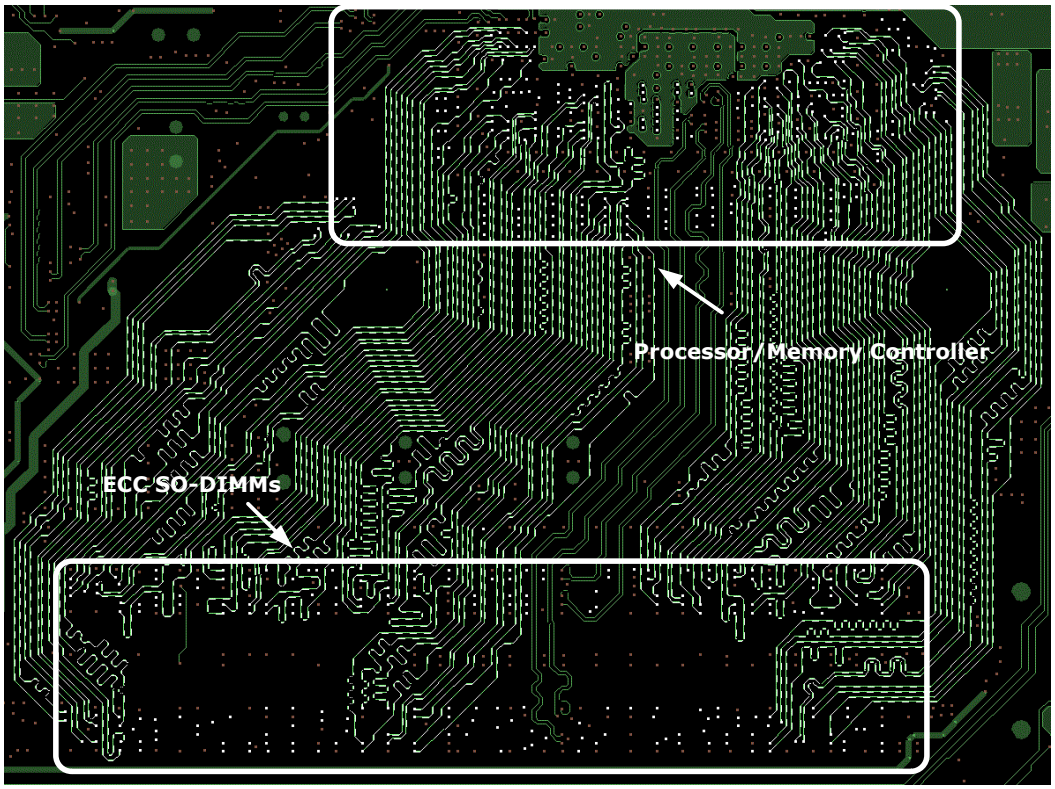
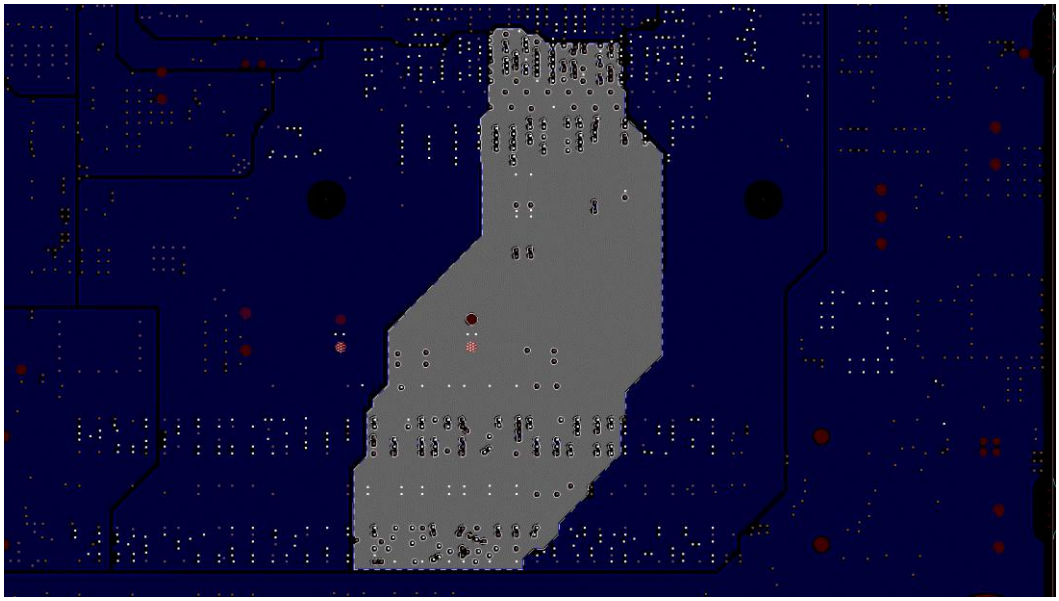


**Figure 15: Power Layer routing examples**



### Silk Screen Considerations

Since the mechanical key for an ECC SO-DIMM and a Standard SO-DIMM is identical, it is possible to plug a Standard SO-DIMM into a slot designed for an ECC SO-DIMM. If this occurs it will cause system malfunction.

To avoid any user error the board designers should place a silk screen note stating "ECC SO-DIMMs Only" near the slot locations on the board.

# Software Considerations

### Memory Reference Code (MRC)

The MRC is responsible for initializing the memory as part of the POST process at power-on. Intel provides support in the MRC for all fully validated memory configurations. For information on whether ECC SO-DIMMs are a fully validated memory configuration for the platform you are using, please contact your local Intel technical support representative. For non-validated configurations, a system designer should work with their BIOS vendor to produce a working MRC solution.

### Serial Presence Detect (SPD) EEPROM

The MRC in the system BIOS needs to know the specification of the attached system memory. Most of this information should be contained in the ECC SO-DIMM SPD, which comes from the ECC SO-DIMM vendor.

# Closing Thoughts

The goal of this paper was to answer some of the basic questions that come to mind when designing an Embedded IA product using system ECC SO-DIMMs.

For more information on specific memory devices please check with your memory vendor for availability and detailed specs.

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## Authors

David Hibler Jr is a Platform Solutions Engineer with the Intelligent Systems Group (Embedded IA) at Intel Corporation.


## Acronyms

BGA- Ball Grid Array

DDR3- Dual Data Rate Three (third generation of DDR memory)

DRAM – Dynamic Random Access Memory

ECC - Error Correcting Code

MRC – Memory Reference Code

SDRAM- Synchronous DRAM

SO-DIMM - Small Outline Dual Inline Memory Module

SPD- Serial Presence Detect

UDIMM – Unbuffered Dual Inline Memory Module

# References


1. *DDR3 SDRAM 72b-ECC SO-DIMM Design Specification (JEDEC 204-pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification)*
2. *DDR3 Unbuffered SO-DIMM reference Design Specification (JEDEC EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SODIMM Design Specification)*
3. *JEDEC 79-3 B DDR3 SDRAM Specification*
4. *JEDEC PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification*

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