Implementing the J1850 Protocol

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INTRODUCTION

This paper introduces the SAE J1850 Communications Standard utilized in On- and Off-Road Land-Based Vehicles. Attributes of the J1850 protocol include an open architecture, low cost, master-less, single-level bus topology. The SAE J1850 Standard supports two main alternatives, a 41.6 Kb/s PWM approach, and a 10.4Kb/s VPW approach. To keep a reasonable depth of subject matter within the confines of this paper, the focus will be on the 10.4Kb/s VPW approach. This paper will explore the positioning of the J1850 Standard, VPW modulation, J1850 arbitration, J1850 message frames, J1850 symbol definitions, In-Frame Responses, the J1850 physical layer, and supporting J1850 documentation.

The SAE J1850 Standard had been a recommended practice for seven years before being officially adopted by the Society of Automotive Engineers, (SAE), as the standard protocol for Class B in-vehicle networks on February 1, of 1994. Today, J1850 is implemented in a variety of production vehicles for diagnostics and data sharing purposes. This wide spread integration of low cost J1850 in-vehicle networks can be found in engine, transmission, ABS, and instrumentation applications.

SAE CLASSIFICATIONS

SAE has defined three distinct protocol Classifications, Class A, Class B, and Class C. Class A is the first SAE classification and maintains the lowest data rate, a rate that peaks as high as 10Kb/s. Class A devices typically support convenience operations like actuators and "smart" sensors. The implementation of Class A has significantly reduced the bulk of automotive wiring harnesses. At the time of this printing, the concerned implementor could assume an approximate cost of $4.00 per node.

The second SAE classification is the Class B protocol. Class B supports data rates as high as 100Kb/s and typically supports intermodule, non-real time control and communications. The utilization of Class B can eliminate redundant sensors and other system elements by providing a means to transfer data (e.g. parametric data values) between nodes. At the time of this printing, one could expect Class B nodes to cost about $5.00 per node. The SAE J1850 Standard is a Class B protocol. Current industry developers are realistically working to drive J1850 implementation costs to as low as $2.00 per node by the end of this decade.

Class C is the last of these three classifications. Performance as high as 1Mb/s is readily supported under the guise of Class C. Because of this level of performance Class C is typically used for critical, real-time control. Class C facilitates distributed control via high data rate signals typically associated with real-time control systems. Typical expectations of Class C utilization at the time of this printing should run in the $10.00 per node range. However, the upper end to Class C utilization invites expensive media, like fiber optics, that can push node costs much higher than estimated. The most predominant in-vehicle networking standard for Class C is CAN, (Controller Area Network). Higher performance communication classifications from 1Mb/s to 10Mb/s are expected in the future. Classifications like Class D can be expected as bandwidth and performance needs push forward.

SAE J1850 CLASS B

The utilization of the Class B J1850 protocol can be drawn from two different alternatives. One is a high speed, 41.6 Kb/s Pulse Width Modulation, (PWM), two wire differential approach. The other J1850 alternative is the 10.4 Kb/s Variable Pulse Width, (VPW), single wire approach. The 10.4Kb/s VPW protocol supports both General Motors, (GM), and Chrysler versions of J1850. A preliferia of solutions are available on the street for the 10.4 Kb/s VPW approach. This paper will focus on the 10.4 Kb/s VPW alternative.

J1850 is an intermodule data communication network for the sharing of parametric information passed in frames (messages) between all vehicle electronic modules connected to the Class B bus. Digital signals between electronic components can be communicated utilizing the concept of multiplexing. Two multiplexing types exist. Frequency division multiplexing and time division multiplexing. Frequency division multiplexing simultaneously transmits two or more messages on a single channel. Time division multiplexing interleaves two or more signals on the same channel for either a fixed or a variable length of time. Our 10.4Kb/s VPW approach utilizes variable time length and time division multiplexing.

VARIABLE PULSE WIDTH MODULATION

VPW is the encoding scheme of choice for all 10.4Kb/s J1850 implementations. Automotive environments place hard demands for low radiated emissions. VPW offers one of the lowest radiated emissions encoding schemes possible due to the minimization of bus transitions per data bit. Some of the key attributes of VPW are its ability to compensate for clock mismatch and ground offsets, fixed transition and sample points, the low number of transitions per bit, and the fact that it is well suited for arbitration. However, VPW does not offer fixed data rates and initially can be a bit confusing.

VPW communicates via time dependent symbols. For example, a "one" bit is not necessarily a high potential on the bus. With VPW, a "one" bit is a symbol denoted by a transition on the bus that lasts for some fixed amount of time, say 64μs. The bus can transition from a low potential to a high potential, or visa-versa; but it is the amount of time that the bus stays in its high or low potential that determines what a particular bus symbol is. In this case, if the bus remains in its high potential for 64μs, then we would consider the symbol to be a "one" bit. VPW J1850 protocol defines a high potential bus driven for 64μs as a "dominant one" bit. The reason it is dominant is due to the J1850 bus drive circuitry.

PASSIVE VERSUS DOMINANT SYMBOLS

The VPW J1850 bus is weakly pulled low, and driven high by a strong pull-up transistor at each node. This means that when no activity is present on the J1850 bus, it is weakly drawn to ground. Whenever a node wants to talk on the J1850 bus, it can either let the weakly drawn bus settle to its low potential at ground, or it can drive the bus to a high potential of approximately 7.5 Volts with its strong pull-up transistor. According to the J1850 VPW standard, a high potential can be anything from 4.25 Volts to 20 Volts. A low potential can be anything from a noisy ground to 3.5 Volts. With this given hardware configuration, any node driving the J1850 bus to a high potential will over-drive any other node wishing to allow the J1850 bus to settle down to a low potential or ground. For this reason, any symbols present on the J1850 bus utilizing a low potential state are considered passive. And conversely, any symbols present on the J1850 bus in the high potential state are considered dominant.

ARBITRATION

The SAE J1850 Standard gives network allocation to each user node based upon the concept of arbitration. Arbitration is a process of determining which of two or more nodes can continue to transmit when both or all network nodes begin transmission simultaneously. The J1850 bus is an asynchronous, master-less, peer-to-peer protocol that offers equal network access for every node. An important attribute of the J1850 bus is that a transmitting node broadcasts its message. This means that not only do all other nodes receive the transmitted message, but the transmitting node sees its own message echoed back as well. All J1850 messages are asynchronous by nature. Being asynchronous forces any message sending devices to determine when a message transmission can begin, and to do so with no pre-defined timing between messages.
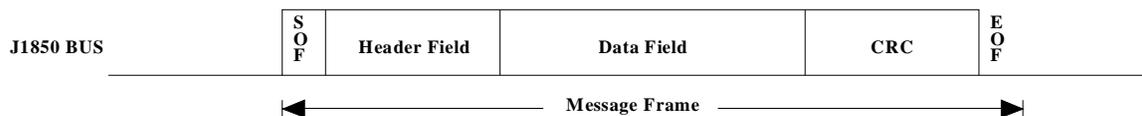
J1850 BUS	S O F	Header Field	Data Field	CRC	E O F

$\longleftarrow$ **Message Frame** $\longrightarrow$

Figure 1. SAE J1850 Message

The J1850 protocol supports CSMA/CR arbitration. CSMA/CR arbitration is a "non-colliding" scheme that supports master-less links. Before any node attempts a transmission, it first "listens" to the J1850 bus for a pre-set amount of time. If the J1850 bus is busy, then the "listening" node waits until the current message is complete before trying again. This process of "listening" before transmitting is called "Carrier Sense" (CS). Because the J1850 protocol is peer-to-peer, offering equal network access to every node, "Multiple Access" (MA) capability is supported. "Multiple Access" means more than one node may begin transmission at the same time. "Collision Resolution" (CR) allows multiple transmitting nodes to all talk at the same time, and resolves the issue of who ultimately controls the bus through the utilization of message prioritization. Message prioritization is accomplished by allowing an active symbol to win over a passive symbol.

When a transmitting node(s) transmits a passive symbol but sees an active symbol, the transmitting node(s) knows that some other node of higher prioritization is transmitting too, (the node driving the active symbol). Any node that transmits a passive symbol on the J1850 bus but sees an active symbol has "lost arbitration". Once arbitration is lost, the losing node(s) then stops transmitting and continues to function as a receiver. The node(s) that "won arbitration" continue to transmit... checking each bit of the current message and dropping out when necessary until just one node is left. Checking is done for every bit and we refer to this process as bit-by-bit arbitration.
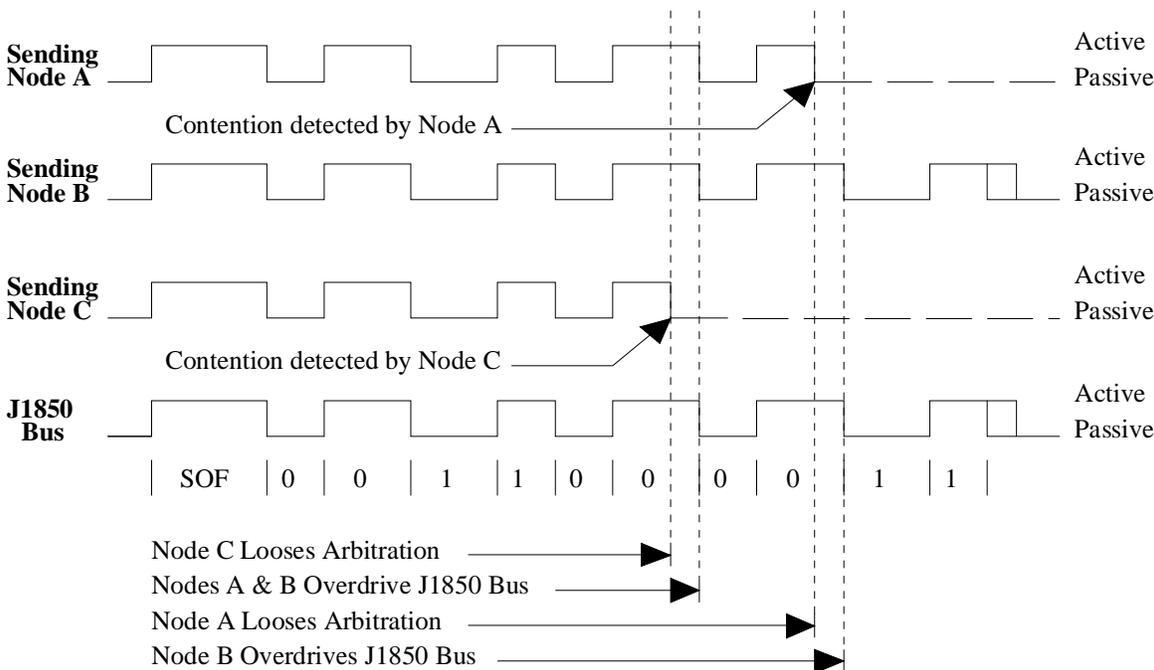

Figure 2. Bit-by-bit Arbitration

Because the lone surviving node has always overdriven the bus with active symbols, when all other loosing nodes transmitted passive symbols, message integrity of the last surviving node remains intact. All of the nodes that "lost arbitration" for this message can try transmission again after the current message is done... again, arbitrating for control of the bus. Higher priority messages are those messages with more active symbols in the beginning of their message content than passive symbols. An inherent issue with CSMA/CR is that it is not possible to have fixed latencies between differing message frames. None the less, this method of non-corruption collision resolution, or CSMA/CR, lies at the heart of the J1850 protocol.
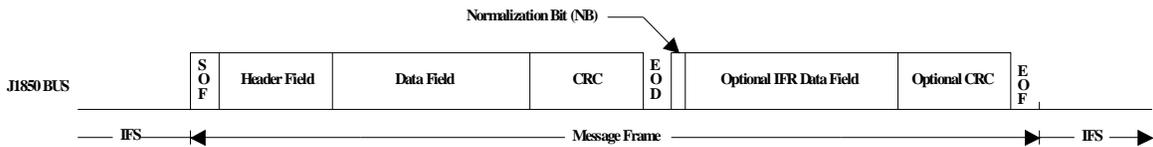

Figure 3. SAE J1850 Message with IFR

START OF FRAME (SOF)

Recall that an idle J1850 bus is weakly pulled to ground. The beginning of any message frame begins with the pre-defined period called a Start Of Frame (SOF). The SOF period is crucial for carrier sense and arbitration purposes. A SOF symbol is defined as a "high potential" J1850 bus for a nominal period of 200µs. After the SOF symbol, bit symbols representing data bytes are transmitted. Anywhere from one byte to eleven bytes can be transmitted.

HEADER FIELD

The first byte is designated as the header field. However, the header field can be modified to be either one or three bytes in length. The header field contains crucial information about what a receiving node should expect in the proceeding message frame. For example, how many bytes make up the header field and how many data bytes the particular message frame contains. The data bytes are referred to as the data field. The dynamic VPW J1850 message frame can contain one to eleven bytes of data. Both the header field and the data field must be contained within the one to eleven byte limit of a VPW J1850 message frame.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P_2	P_1	P_0	H-bit	K-bit	Y-bit	Z_1	Z_0

Figure 4. SAE J1850 Header Byte

Bit	Meaning	Value	Meaning
PPP	Message Priority	000 111	Highest Priority Lowest Priority
H	Header Type	0 1	Three Byte Header Single Byte Header
K	In-Frame Response (IFR)	0 1	IFR Required IFR Not Allowed
Y	Addressing Mode	0 1	Functional Addressing Physical Addressing
ZZ	Specific Message Type	00 01 10 11	The meaning for these values are dependent on K & Y above. Refer to SAE J2178/1 document for more details.

Table 1. Header Byte Bit Definition

The entire byte is utilized as a message identifier with a single byte header field. The first three most significant bits of the header field are priority bits. These three bits are capable of designating eight levels of priority with a binary 000 being highest and a binary 111 being the lowest in priority. These first three bits readily serve the arbitration process without having to influence any other header bit designations.

Following the priority bits is the header bit, or H-bit. This bit conveys whether or not this particular message is going to have a single byte header, or a three byte header. If the H-bit is set to "zero", then a three byte header should be expected. If the H-bit is set to a "one", then only a single byte header should be expected.

The next header bit designates whether an In-Frame Response, (IFR), is requested or not. This bit is known as the K-bit. If the K-bit is set to "zero", then an IFR is requested. If the K-bit is set to a "one", then no IFR is requested. There will be more on IFRs in a moment.

Following the K-bit is a bit utilized to designate an addressing type. This bit is called the Y-bit. Two types of addressing are accommodated with this J1850 protocol. One is a functional type of addressing, the other is a physical type of addressing. How the rest of the message is interpreted is dependent upon how this bit is set. If the Y-bit is set to "zero", then functional addressing is to be used. If the Y-bit is set to a "one", then physical addressing is to be used. Functional addressing has a higher priority than does physical addressing, providing all preceding bits are the same.

Functional addressing is an addressing scheme that labels messages based upon their operation code or content. Physical addressing is an addressing scheme that labels messages based upon the physical address location of their source and/or destination(s).

Physical addressing is independent upon the geographic location, connector pin, and/or wire identification assignments. More details on Functional/Physical addressing can be found with the SAE J2178, Step 1 through 4 documents.

The last two bits of the single byte header are the message type bits, or ZZ-bits. These two bits tell any receiving node(s) what format the rest of the message is going to take. These two bits, combined with the Y-bit and the K-bit, offer up to sixteen different message types that can be transmitted via the single byte header. The Z1-bit helps to designate whether or not this message uses extended addressing. If the Z1-bit is set to a "one", then a receiving node(s) knows that the fifth byte of this message is the extended address of this function. The Z0-bit indicates whether or not data is contained in this message. If the Z0-bit is set to a "zero", then data should be expected with this message. If the Z0-bit is set to a "one", then no data is contained within this message.

A three byte header is fairly the same. With a three byte header, the H-bit is set to a "zero" to indicate that this is a three byte header. All other bits within the first byte operate pretty much the same. The second byte of a three byte header contains a target address. The target address can be either functionally addressed or physically addressed. The third and last byte of a three byte header contains the physical address of the source of this message. Because the source address must always be unique, arbitration is always resolved by the end of the third byte whenever three byte headers are utilized.

DATA BITS

The data bits that make up the header and data fields consist of "ones" and "zeros" represented by symbols. A passive one bit symbol is a 128μs long low potential on the J1850 bus. A dominant one bit symbol is a 64μs long high potential on the J1850 bus. Conversely, a passive zero bit symbol is a 64μs long low potential on the J1850 bus and a dominant zero is a 128μs long high potential on the J1850 bus. These symbols require only one transition per bit, and one can mix the combinations indefinitely.
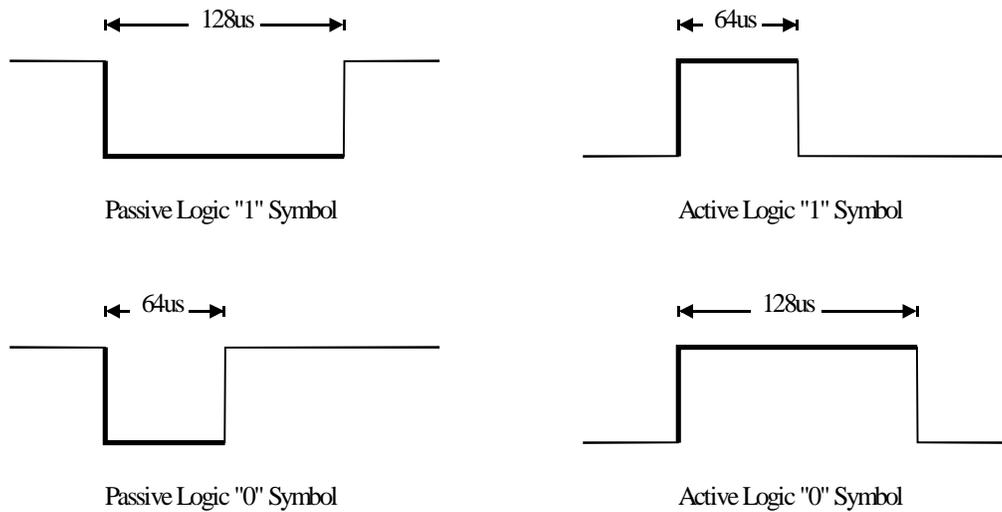
Figure 5. SAE J1850 Bit Symbol Timings

CYCLICAL REDUNDANCY CHECK (CRC)

Appended to the end of every VPW J1850 message is an error handling Cyclical Redundancy Check (CRC) byte. This, coupled with up to eleven data bits, makes the maximum message frame length twelve bytes in length. One of the most effective error protection schemes in the SAE J1850 Standard is its CRC. The entire message frame, not including the SOF symbol, is treated like "one big word". This "one big word" is divided by a special "polynomial". The 1's complement of the "polynomial" calculation is appended to the end of the associated message as a byte, and transmitted out. All receiving nodes do a similar "polynomial" calculation to received message frames, including the inverted CRC. If no errors have occurred, then the receivers resultant CRC calculation will always equate to a certain value, (C4 hex). Details of the CRC process can be found in the SAE J1850 REV. MAY94 document, starting on page 15.

END OF DATA (EOD)

Immediately after the CRC byte has been transmitted, an End Of Data (EOD) symbol is transmitted. The EOD symbol consists of a 200μs long low potential on the J1850 bus. Directly after the EOD symbol, receiving node(s) can opt to immediately respond to the message. This response is called an In-Frame Response (IFR) and contributes to the suite of error handling options that the J1850 protocol supports. If, however, no IFR is desired, then the EOD symbol is allowed to elapse into an End Of Frame (EOF) symbol. EOF symbols are nothing more than EOD symbols that have elapsed from 200μs to 280μs in length. The EOF symbol denotes the end of this particular message frame.
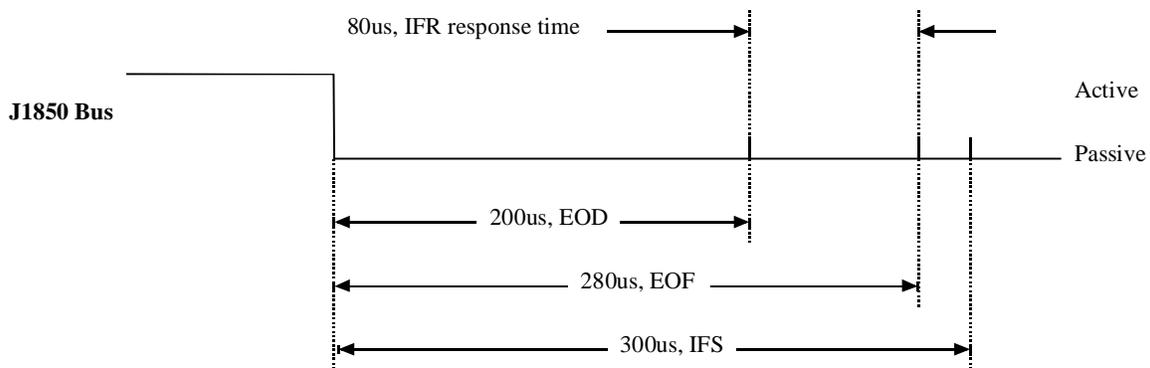

Figure 6. End Of Data Symbol versus an End Of Frame Symbol

IN-FRAME RESPONSE (IFR)

An IFR provides a platform for remote receiving nodes to actively acknowledge a transmission. Receiving node(s) append a reply to the end of the transmitting nodes original message frame. IFRs allow for increased efficiency in transmitting messages since a receiving node may respond within the same message frame that the request originated. A transmitting node request for an IFR is denoted by the K-bit in the transmitting nodes header field. All receiving nodes are required to check the K-bit and respond accordingly. This response must come within the elapse time between an EOD symbol and an EOF symbol, which is approximately 80μs.
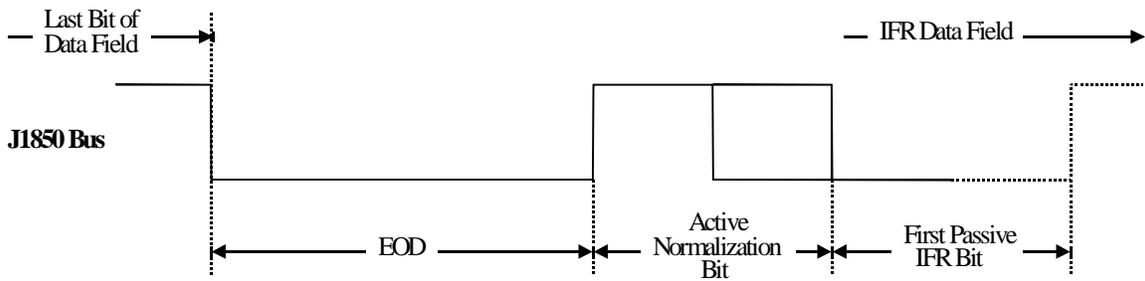
Figure 7. In-Frame Response and Normalization Bit Symbol

The beginning of an IFR response is denoted by the receiving node(s) transmission of a Normalization Bit (NB). The NB provides an active separation between the passive EOD symbol and the first data bit of the IFR response. The NB can take one of two forms. Each form denotes whether or not the IFR includes its own CRC. The interpretation of the NB is dependent upon what industry standard you want to accommodate. For GM compliance, a "dominant zero" NB symbol denotes that the IFR does not include a CRC. A "dominant one" NB symbol denotes that the IFR includes a CRC. However, it is believed that GM will not require IFRs for any J1850 implementations. Chrysler compliance is exactly the opposite of GM, and is the configuration of choice for most systems utilizing IFR.

	GM (NB=1)	**Chrysler NB=0)**
IFR does not include CRC	active long NB	active short NB
IFR includes CRC	active short NB	active long NB

Table 2. Normalization Bit Configurations

In-Frame Responses can take on one of four distinct forms labeled as Type 0, Type 1, Type 2, and Type 3 IFRs. A Type 0 IFR is defined as requiring no response at all. A Type 1 IFR consists of a single byte response from a single responder. Type 2 IFRs are single byte responses from multiple responders. Each responder's arbitrating for its chance to respond. The IFR is not completed until all applicable responders have had a chance to respond. A Type 3 IFR is a response that contains multiple bytes from a single responder, and a CRC is appended to the end.

After the EOF symbol, a grace period of idle bus time is given before other nodes can begin new transmissions. This time is called an Inter Frame Separation (IFS) and is denoted as a "low potential" time of 300µs following an EOF symbol. And, an IFS can be drawn out indefinitely in time so long as the J1850 bus is idle.

One other symbol of interest is the Break (BRK) symbol. The BRK symbol is denoted by a "high potential" on the J1850 bus lasting at least 768µs in length. The

maximum length of a BRK symbol is approximately 5ms. The BRK symbol can be immediately transmitted onto the J1850 bus at any time. The BRK symbols causes any or all other transmitting node(s) to loose arbitration and cease transmission. Completion of the BRK symbol leaves all other nodes in a "ready-to-receive" state. The BRK symbol is usually reserved for diagnostic and scan tools.
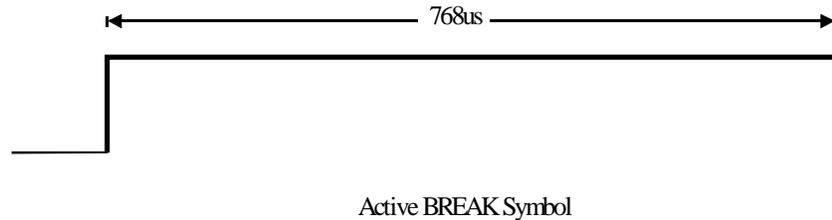

Active BREAK Symbol

Figure 8. SAE J1850 Break Symbol

The goal of the SAE J1850 Standard is fault tolerance. Any glitch or disturbance less than 8µs in length is digitally filtered out as unwanted noise. Though 8µs digital filtering forces a fixed delay to all incoming data, a large portion of noise is eliminated from the J1850 network.

PHYSICAL LAYER

The 10.4Kb/s VPW physical layer consists of a single, voltage driven wire randomly laid with no routing restrictions. Refer to SAE J1211 for help on specifying your multiplexing system, and SAE J1879 for help on specifying components.

The on-vehicle network length is 35 meters. An off-vehicle network length can only be 5 meters long. This means that the total vehicle network length is 40 meters. The maximum number of standard unit loads, including off-vehicle equipment, is 32 nodes. This is assuming that a node averages out to be one unit load. A unit load consists of 10.6 KΩs and 470 pF. Off-vehicle load measurements are measured on the SAE J1962 diagnostic connector. The minimum off-vehicle load resistance is 10.6 KΩs. The off-vehicle capacitance should not exceed 500 pF. The capacitance reading is between the bus wire to signal or chassis ground.

The J1850 application layer requires that a "zero" bit symbol always dominates over a "one" bit symbol. Adherence to the VPW J1850 10.4Kb/s symbol definitions ensures that this happens. As stated earlier, the maximum number of message bytes, (excluding the frame delimiters SOF, EOD, EOF, and IFS), is 12. The VPW timing requirements given below are drawn from the SAE J1850 REV MAY94 document, page 35. Included are the VPW DC parameters as well.

Symbol	T_xMin	$T_x$nom	$T_x$max	$R_x$min	$R_x$max	units
Passive "0" Active "1"	≥ 49	64	≤ 79	> 34	≤ 96	µs
Passive "1" Active "0"	≥ 112	128	≤ 145	> 96	≤ 163	µs
Active "SOF"	≥ 182	200	≤ 218	> 163	≤ 239	µs
Passive "EOD"	≥ 182	200	≤ 218	> 163	≤ 239	µs
Passive "EOF"	≥ 261	280	N/A	> 239	N/A	µs
Passive "IFS"	≥ 280	300	N/A	> 280	N/A	µs
Active "BREAK"	≥ 280µs	300µs	≤ 5ms	> 239µs	≤ 1.0 s	N/A

Table 3. VPW Pulse Width Times (µs)

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage	V_{ih}	4.25	—	20.00	Volts
Input Low Voltage	V_{il}	—	—	3.5	Volts
Output High Voltage	V_{oh}	6.25	—	8.0	Volts
Output Low Voltage	V_{ol}	0.00	—	1.5	Volts
Absolute Ground Offset Voltage	V_{go}	0.00	—	2.00	Volts
Network Resistance	R_{load}	315	—	1,575	ohms
Network Capacitance	C_{load}	2,470	—	16,544	pF
Network Time Constant	T_{load}	—	—	5.2	µs
Signal Transition Time	T_t	—	—	18.0	µs
Node Resistance (unit load)	R_{ul}	—	10,600	—	ohms
Node Capacitance (unit load)	C_{ul}	—	470	—	pF
Node Leakage Current	I_{leak}	—	—	10	µA

Table 4. VPW DC Parameters

The 10.4Kb/s VPW physical description is robust enough to survive several catastrophic system faults, and do so damage free with the ability to recover to normal operation automatically upon fault removal. Fault tolerance for open circuits, direct shorts to ground, direct shorts to power, or direct shorts to any other voltage between ground and power, are all survivable and automatically recoverable.   Interference to communication is not hindered in any way if any one node fails while on the J1850 network.

All pulses on the 10.4Kb/s J1850 network are wave shaped. Wave shaping rounds off the sharp corners of bus transitions, removing unwanted high frequency signal components.   Transmitted pulse widths are affected by individual node oscillator tolerances, and variations in the transmission delay through a nodes source driver as well as the bus medium. These things must be taken into consideration when designing a J1850 node.

Figure 9. SAE J1850 VPW Waveform

Value	Value Description
Voh,min	Minimum output high voltage. This is the highest trip point with 2V receiver noise.
Vih,min	Minimum input high voltage. This is the highest trip point with no offset noise.
Vt	Ideal receiver trip point.
Vil,max	Maximum input high voltage. This is the lowest trip point with no offset noise.
Vol,max	Maximum output low voltage. This is the highest trip point with 2V source noise.
Tt,max	Maximum signal transition time.

Table 5. SAE J1850 VPW Voltage Levels and Trip Points

FORWARD

There are several sources to turn to for further consideration of the SAE J1850 Standard. Given are several documents provided by the Society of Automotive Engineers (S.A.E.). SAE is an industry group that provides a wide range of specifications. They provide guidelines for standards and recommended practices for the automotive world. Some guidelines and standard examples include things like lubrication, corrosion, fasteners, electronics and emissions. Referring to these documents should aid with further SAE J1850 Standard exploration.

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Warrendale, PA 15096-0001 U.S.A.
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FAX (412) 776-5760

SAE J1850 documents of interest:

      SAE J1850: Specifies requirements for a vehicle data communications network. Compliance committee recently formed (J1699)

      SAE J2178: Specifies non-diagnostic messages.
            Part 1 - Message header formats and physical node addresses
            Part 2 - Message parametric data
            Part 3 - Message assignments for the single byte header format
            Part 4 - Message assignments for the three byte header format

      SAE J1962: Diagnostic Connector (under dash). New 16-pin standard.

      SAE J2012: Diagnostic Codes

      SAE J2190: Specifies diagnostic and malfunction messages (to "fix" vehicles)

      SAE J2008: Recommended Organization of Vehicle Service Information

      SAE J1978: OBD - II Scan Tool (On Board Diagnostics)

      SAE J2205: Expanded Diagnostic Protocol for OBD-II Scan Tools

      SAE J2300: Conformance Test Procedures for OBD-II Scan Tools

      SAE J1979: Specifies CARB/EPA functions and messages.

      SAE J1699: Compliance Tests and Test Methods for SAE J1850

      SAE J1113: Electromagnetic Susceptibility Measurement Procedures for Vehicle Components

      SAE J1547: Electromagnetic Susceptibility Measurement Procedures for Common Mode Injection

      SAE J1211: Electronic Equipment Design Recommended Procedure

      SAE J1879: General Qualification and Production Acceptance Criteria for Integrated Circuits in Automotive Applications

      SAE J1930: Electrical/Electronic Systems Diagnostic Terms, Definitions, Abbreviation, and Acronyms

      SAE J1213: Glossary of terms for vehicle networks

CONCLUSION

The SAE J1850 10.4Kb/s standard fulfills mid-range Class B classification protocol requirements. Variable Pulse Width modulation is utilized to facilitate a single wire transmitting medium for harsh automotive environments. Arbitration, CRC, and acknowledgment capability all contribute to a low cost, master-less, efficient network that can be utilized in a multitude of applications.

REFERENCES

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[7] Intel Corporation, 8XC196LB Target Specification, October 18,1995

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[9] Christopher A. Lupini, "Introduction to Vehicle Multiplexing", University Consortium for Continuing Education (UCCE), November 1-3, 1995 Training Program