Modular Reference Design
System Electronics Board

History

Changes made to Revision E.

1. Removed CS_B#[5:0]. Tied CS_Bn# to CS_An# at DIMM connectors.
2. Changed WE_B#, SCAS_B# and SRAS_B# to WE_A#, SCAS_A#, SRAS_A# on J17
3. Changed WE_A#, SCAS_A# and SRAS_A# to WE_B#, SCAS_B# and SRAS_B# on J16.
4. Pin K25 of the CPU connector has been changed from reserved to VCC_CMOS.
5. A20M#, INIT, SLP, IGNNE NMI,INTR, STPCLK# and SMI are now pulled up to VCC_CMOS.
6. A20M#, INIT, SLP, IGNNE NMI,INTR, STPCLK# and SMI have series resistors and 680 ohm pullups from 2.7K pullups.
7. Removed Pullup on FERR#. Processor assembly or interposer cards must pull this signal up.
8. Modified Boot Block flash to support 28F004B5.
9. Removed Series resistor from MAB12#. Processor Assembly must configure BX FSB frequency.
10. Removed flash daughter card from schematics.
11. Changed MAB12#_R net to FQS.
12. Removed FQS pullups(formerly MAB12#_R).
13. Added R308 as series termination on BXDCLKO.
14. Update RTC Crystal section.
15. Removed speaker connector.
16. Pin names A01-A09 changed to A1-A9 on ISA and DIMM connectors
17. Changed FB1-FB4, FB9 part # to BLM41P750S, 75 Ohm/100 MHz/3 A

Changes made to Revision D.

1. Added Signals PWROK(A24) +12V(A33) MB12#_R(B33) to J19A.
2. Moved J20
3. Added C229 to -PCIRST

Changes made to Revision C.

1. Tied VBAT (pin 65) to 3.3V on Super I/O.

Changes made to Revision B.

1. Swapped AD23 and AD19 on 400 pin connector.
2. Separated CSEL on IDE0 and IDE1
3. Swapped pins 1 and 3 (V5 with TP) on CPU-Fan connector.
4. Tied VBAT (pin 65) to 5.0V on Super I/O.
5. Changed RP48 to 4.7K. (Pullups for mouse and keyboard.)
6. Inverted POWERON# signal (SUSC#) from PIIX4 to control soft-on feature.
7. Changed Bulk decoupling on +12 and -12 to 2x220uF from 2x400uF.
8. Changed Bulk decoupling cap C154 from 10uF to 47uF to reduce BOM line items.

Revision E

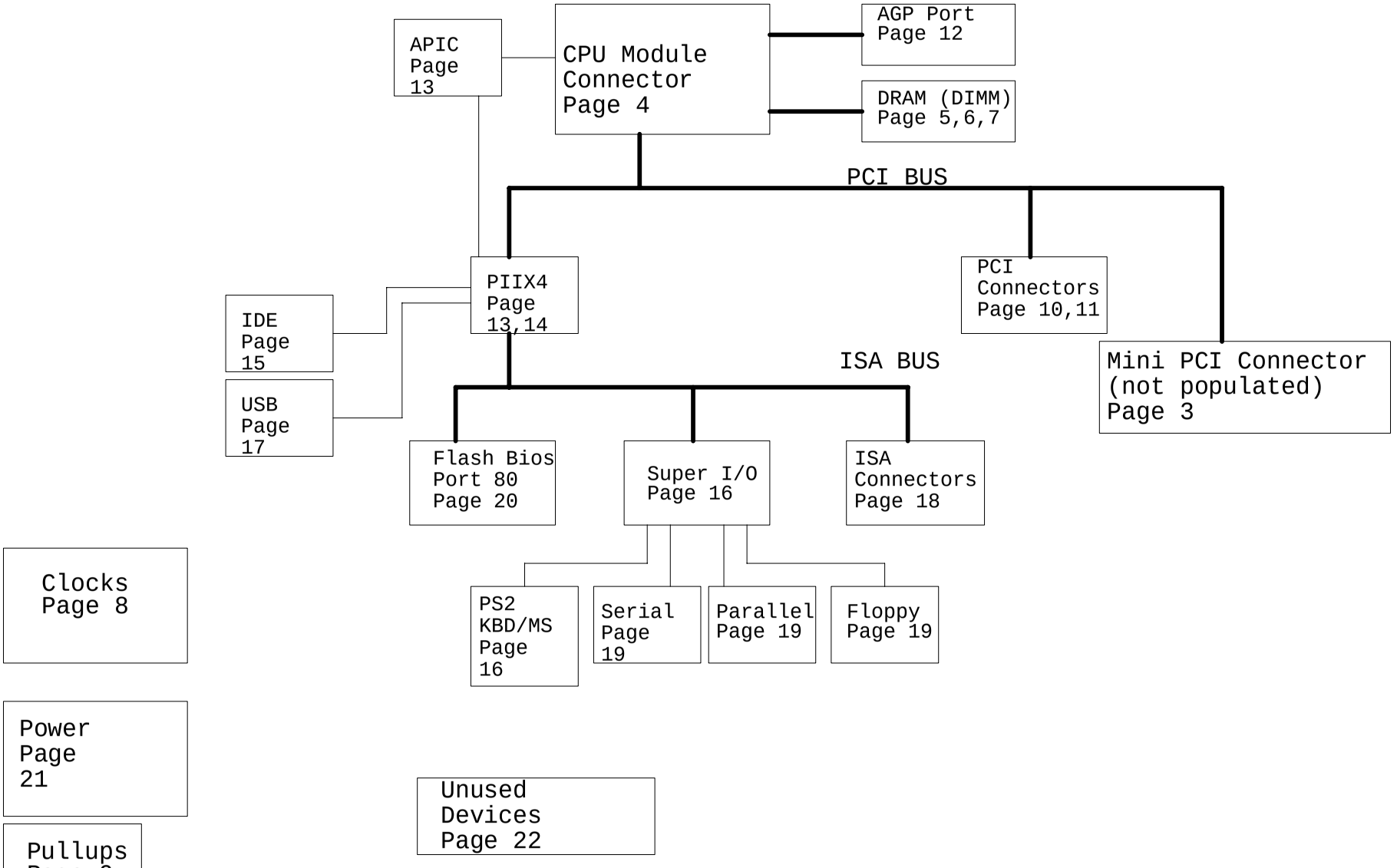
THIS SCHEMATIC IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF PROPOSAL, SPECIFICATION OR SAMPLE.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. Intel does not warrant or represent that such use will not infringe such rights.

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

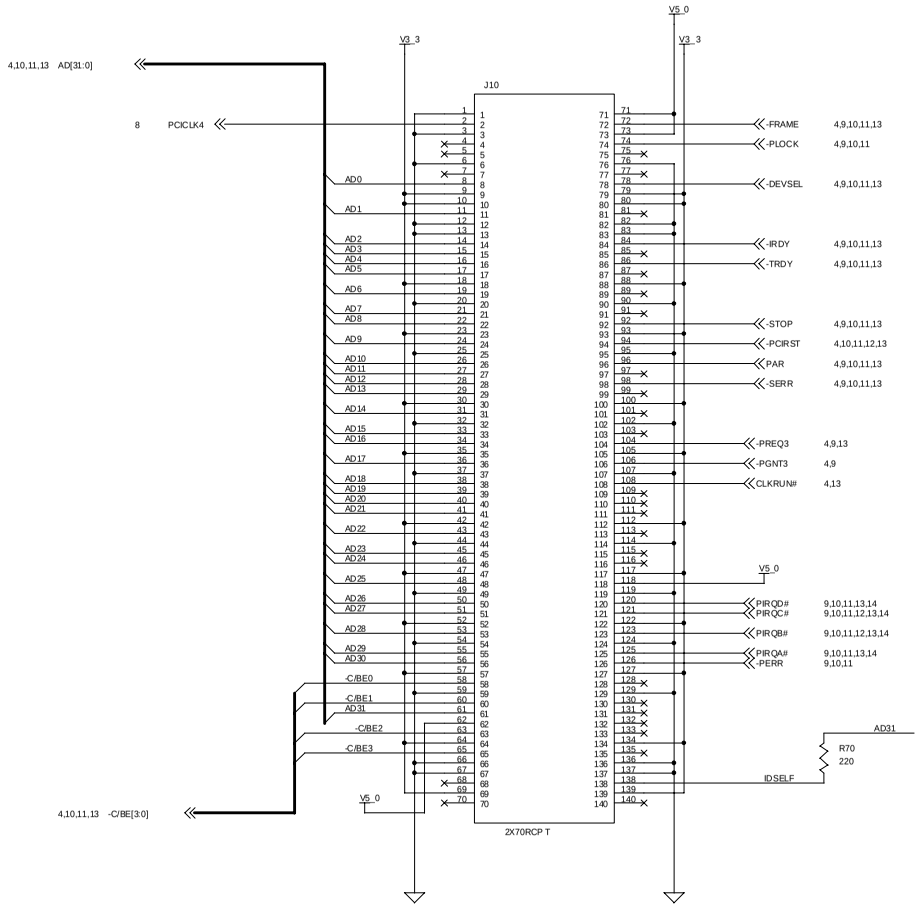
Title: Changes		
Size: C	Document Number	Rev: E
Date: Friday, February 16, 2001	Sheet 1 of 22	



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

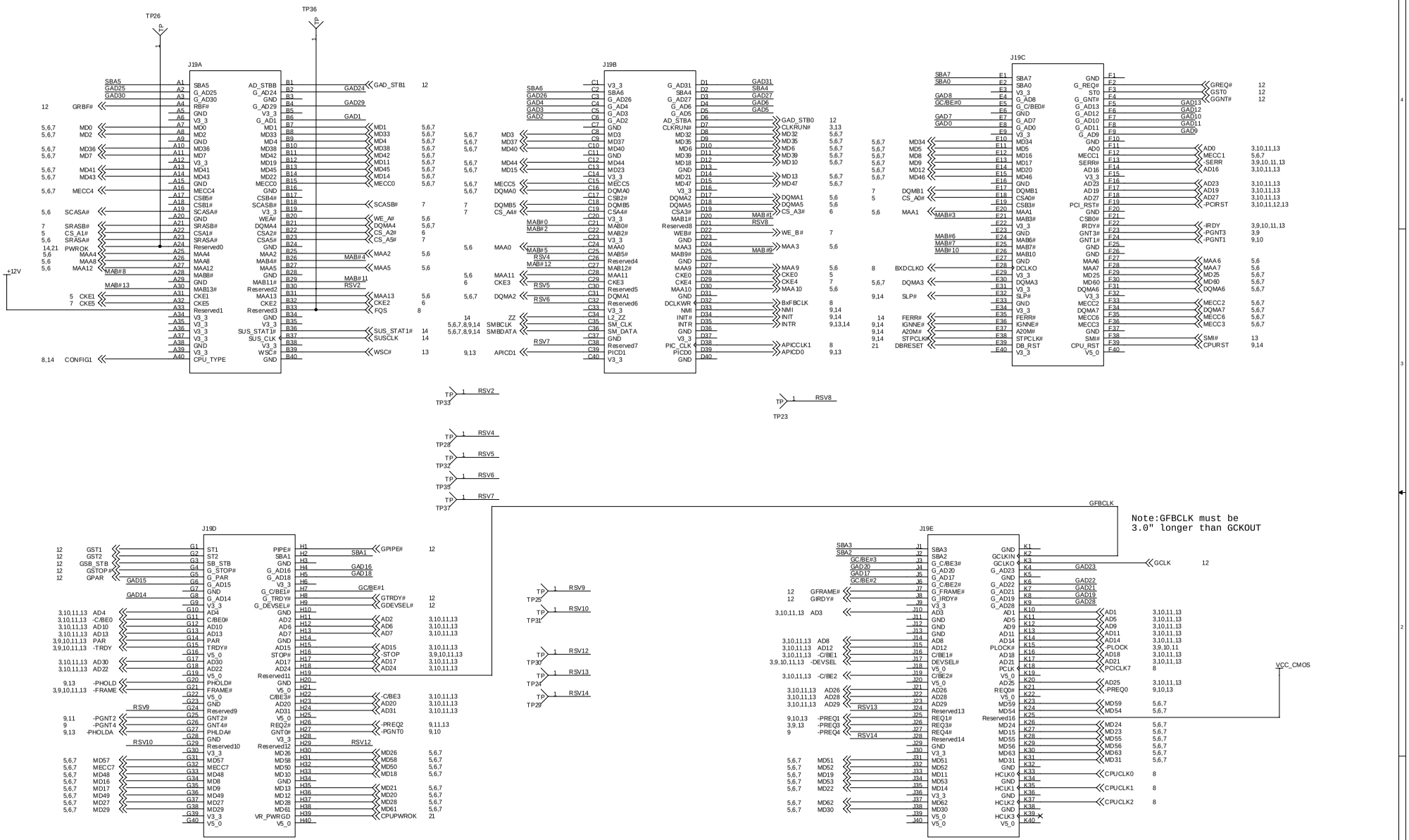
Title: Block Diagram		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 2 of 22	

Do not populate J10



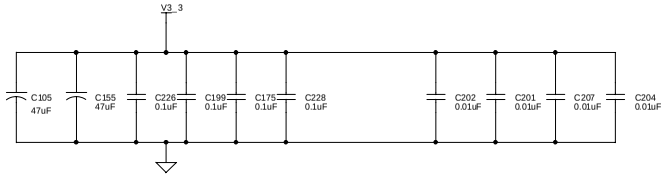
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	Mini PCI Connector	
Size C	Document Number <Doc>	Rev E
Date: Friday, February 16, 2001	Sheet 3 of 22	

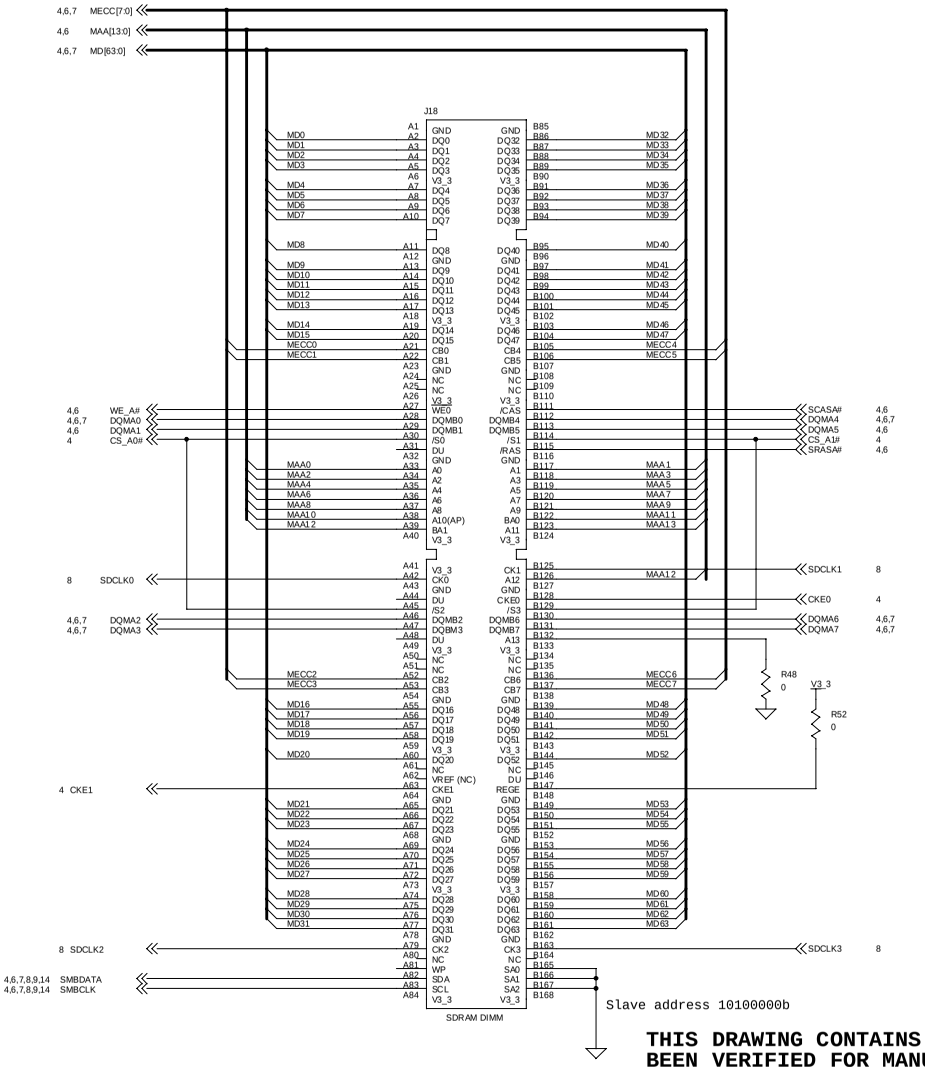


THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: CPU Connector			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 4 of 22		

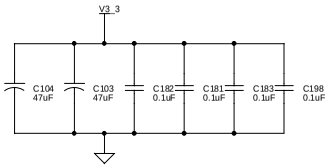


Socket 0

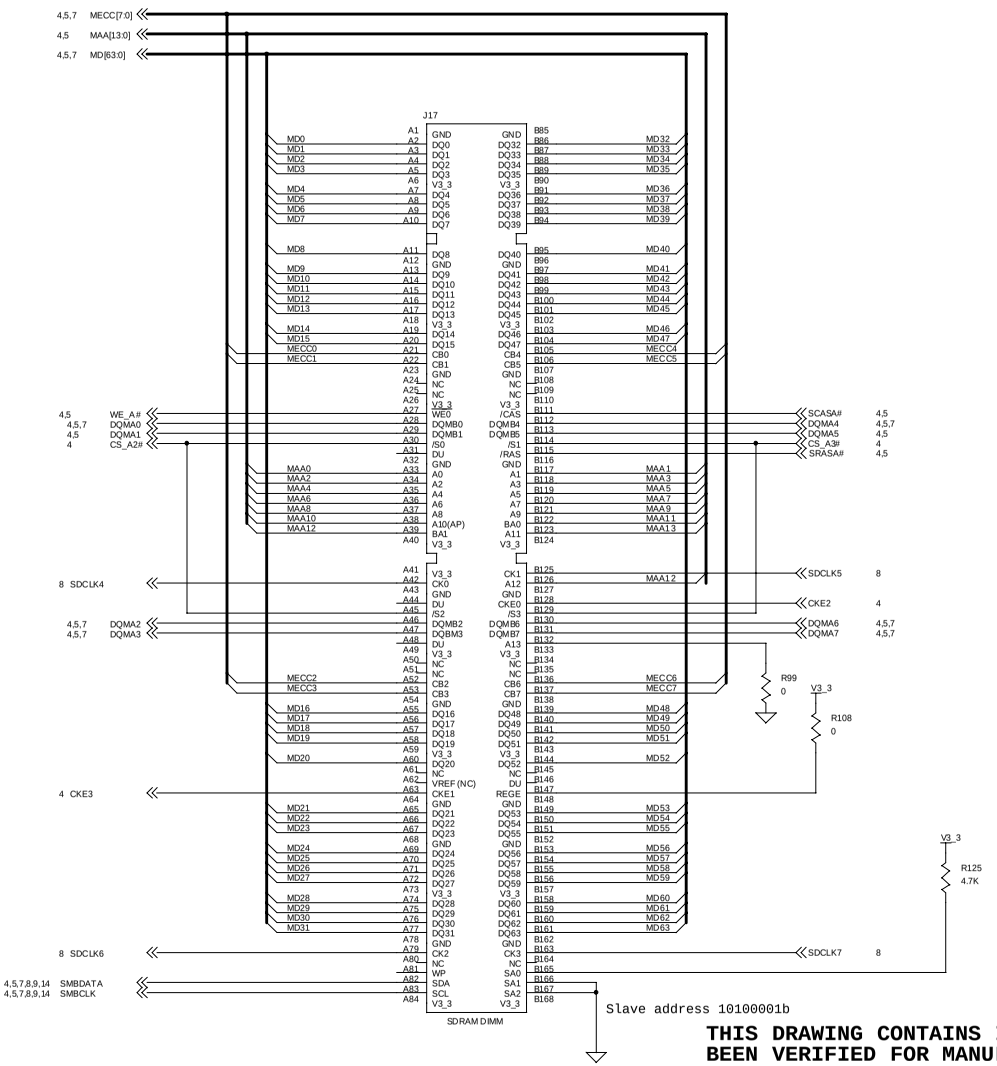


THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: DIMM0		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 5 of 22	

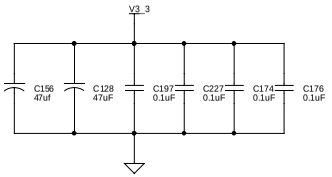


Socket 1



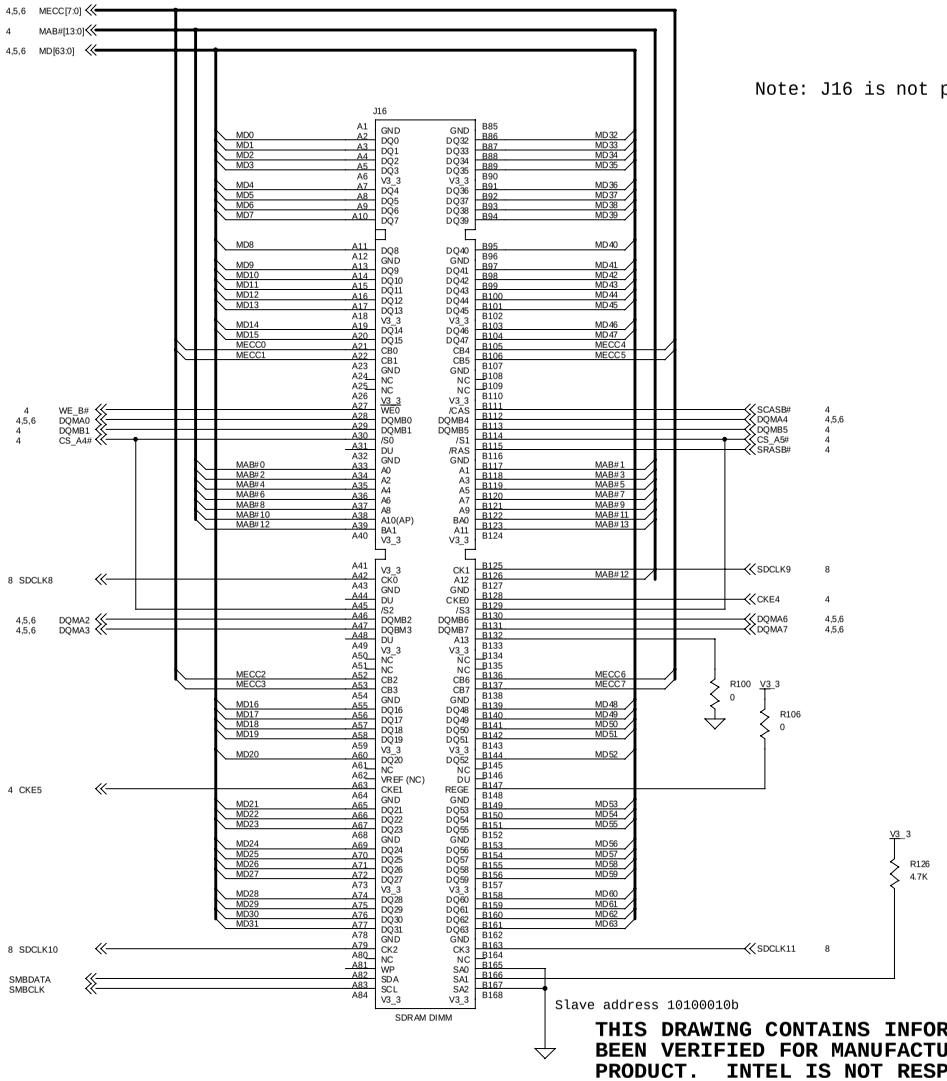
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: DIMM1			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 6 of 22		



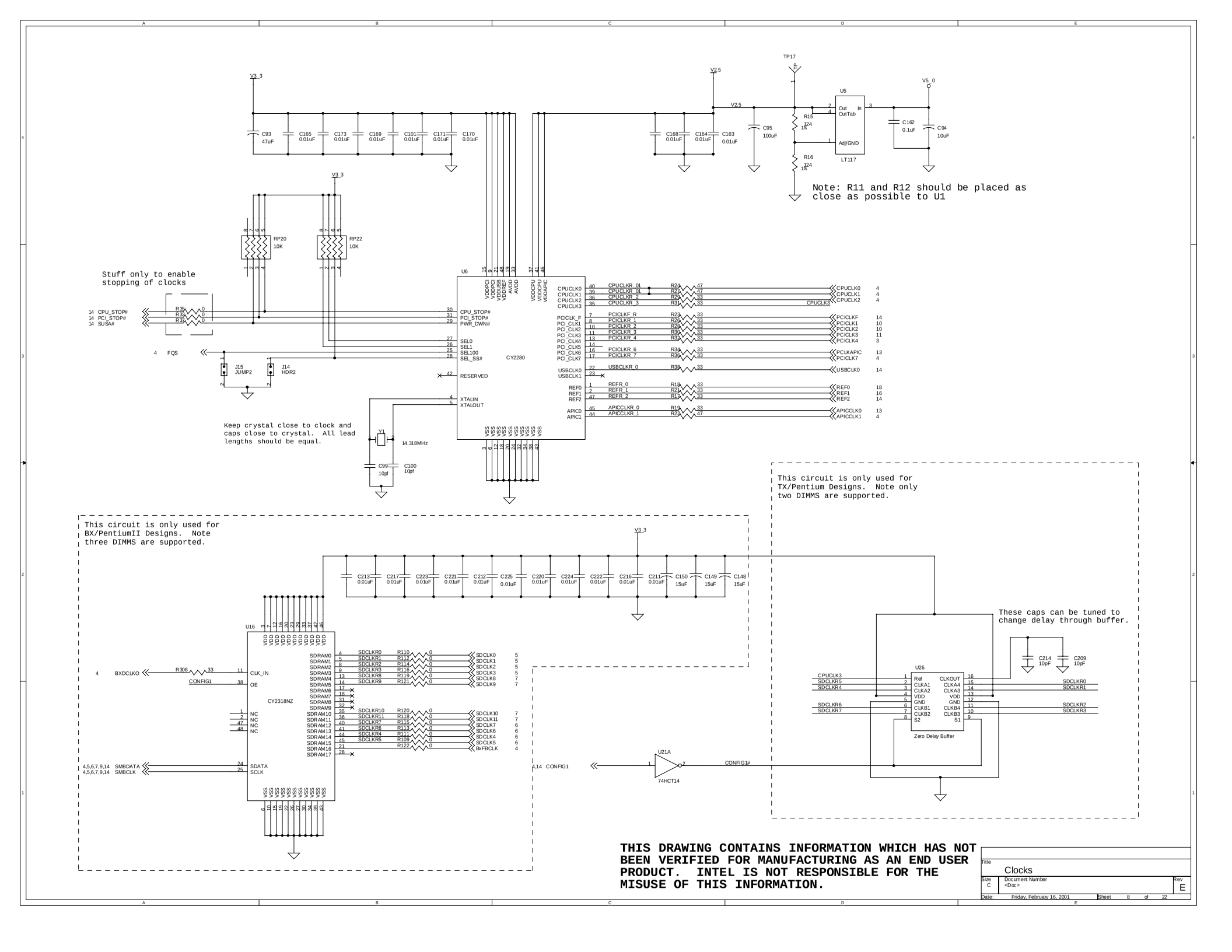
Socket 2

Note: J16 is not populated

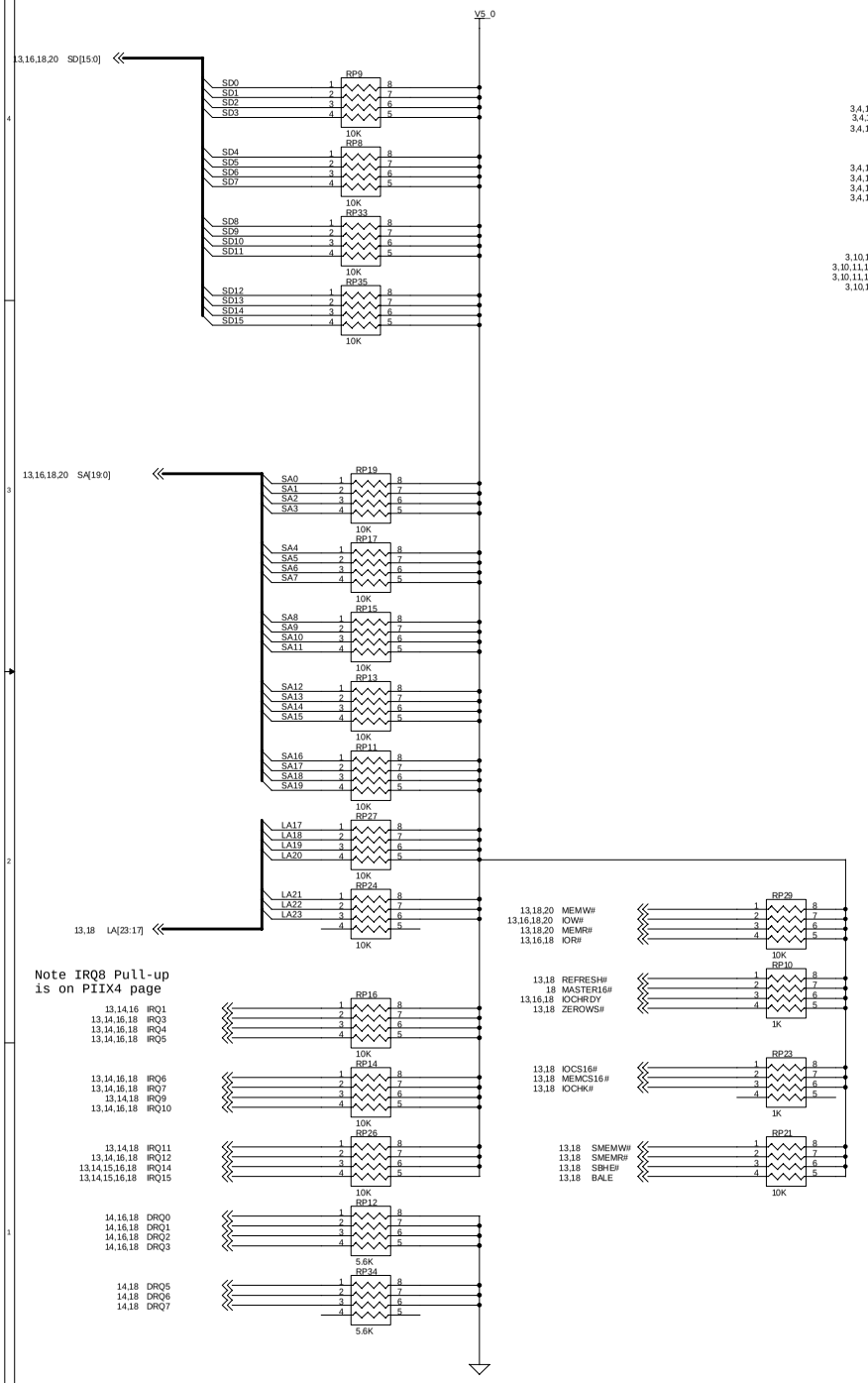


THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

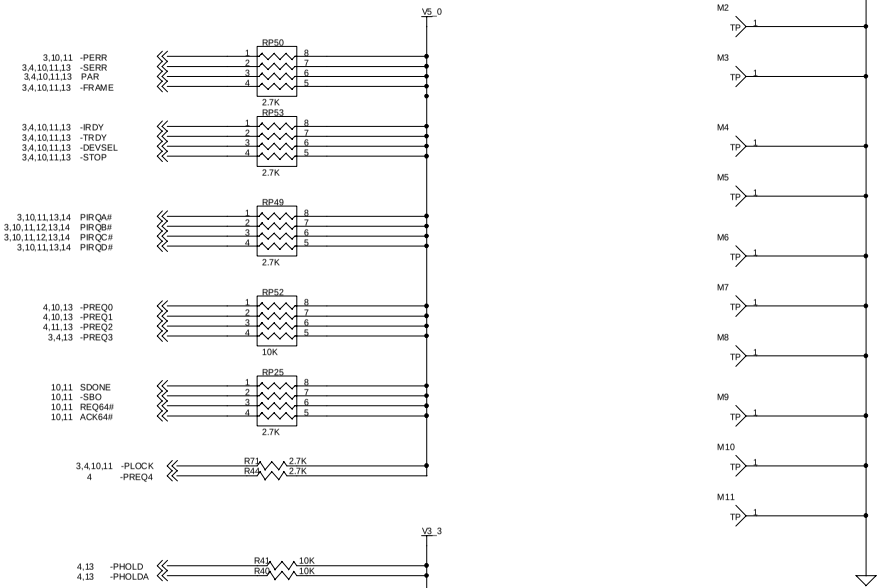
Title	DIMM2	
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 7 of 22	


Note: R11 and R12 should be placed as close as possible to U1
Stuff only to enable stopping of clocks
Keep crystal close to clock and caps close to crystal. All lead lengths should be equal.
This circuit is only used for BX/PentiumII Designs. Note three DIMMS are supported.
This circuit is only used for TX/Pentium Designs. Note only two DIMMS are supported.
These caps can be tuned to change delay through buffer.
CY2280
CY2318NZ
Zero Delay Buffer
LT117
74HCT14
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
Title
Clocks
Size C
Document Number <Doc>
Rev E
Date: Friday, February 16, 2001
Sheet 8 of 22

ISA Pullups



PCI Pullups



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	ISA/PCI Pullups	
Size C	Document Number <Doc>	Rev E
Date: Friday, February 16, 2001	Sheet 9 of 22	

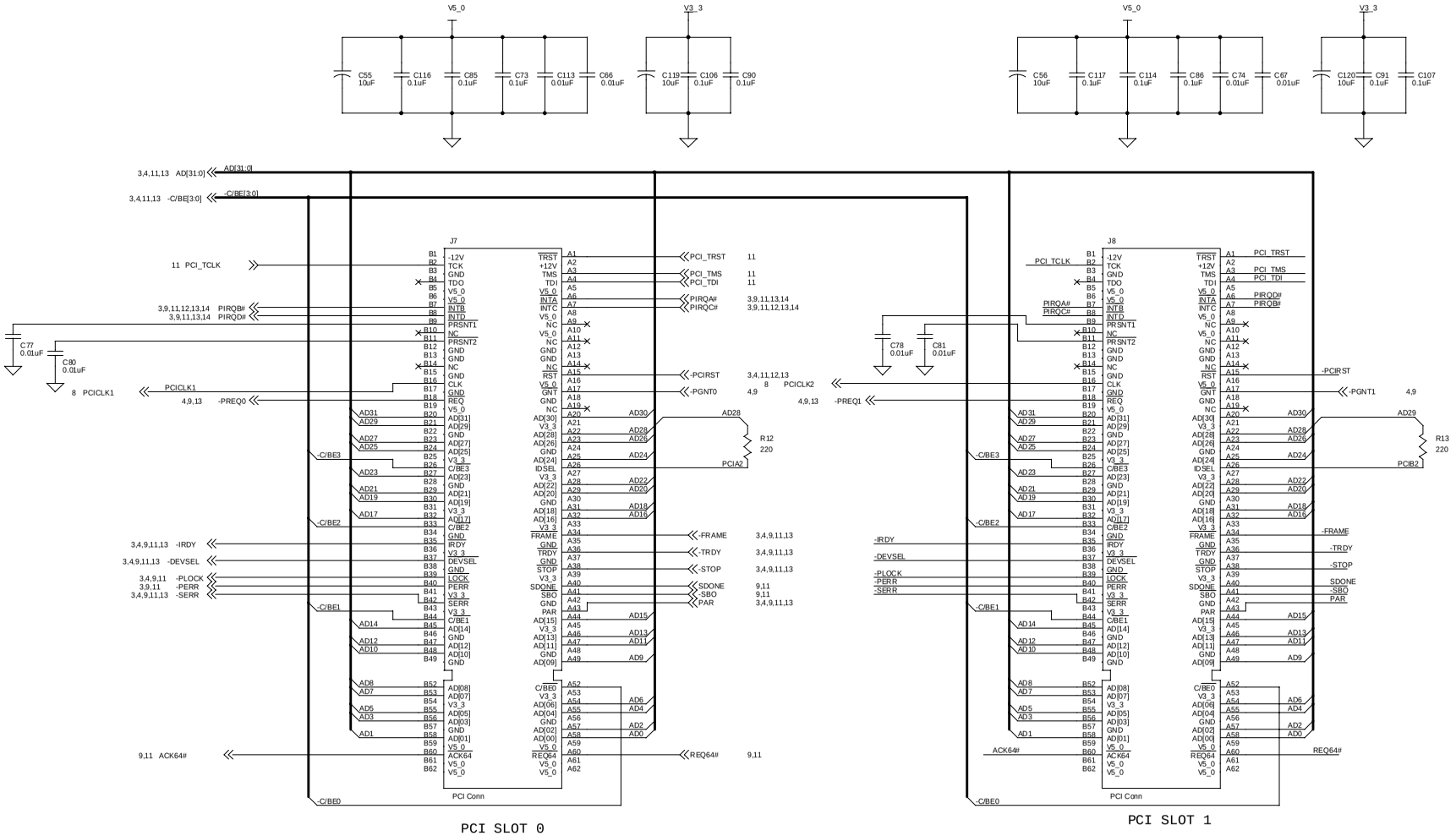
J7/J8 V5_0:
    A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
    B5, B6, B19, B22, B59, B61, B62

J7/J8 V3_3:
    A21, A27, A33, A39 A45, A53
    B25, B31, B36, B41, B43, B54

J7/J8 NC:
    A9, A11, A14, A19
    B10, B14

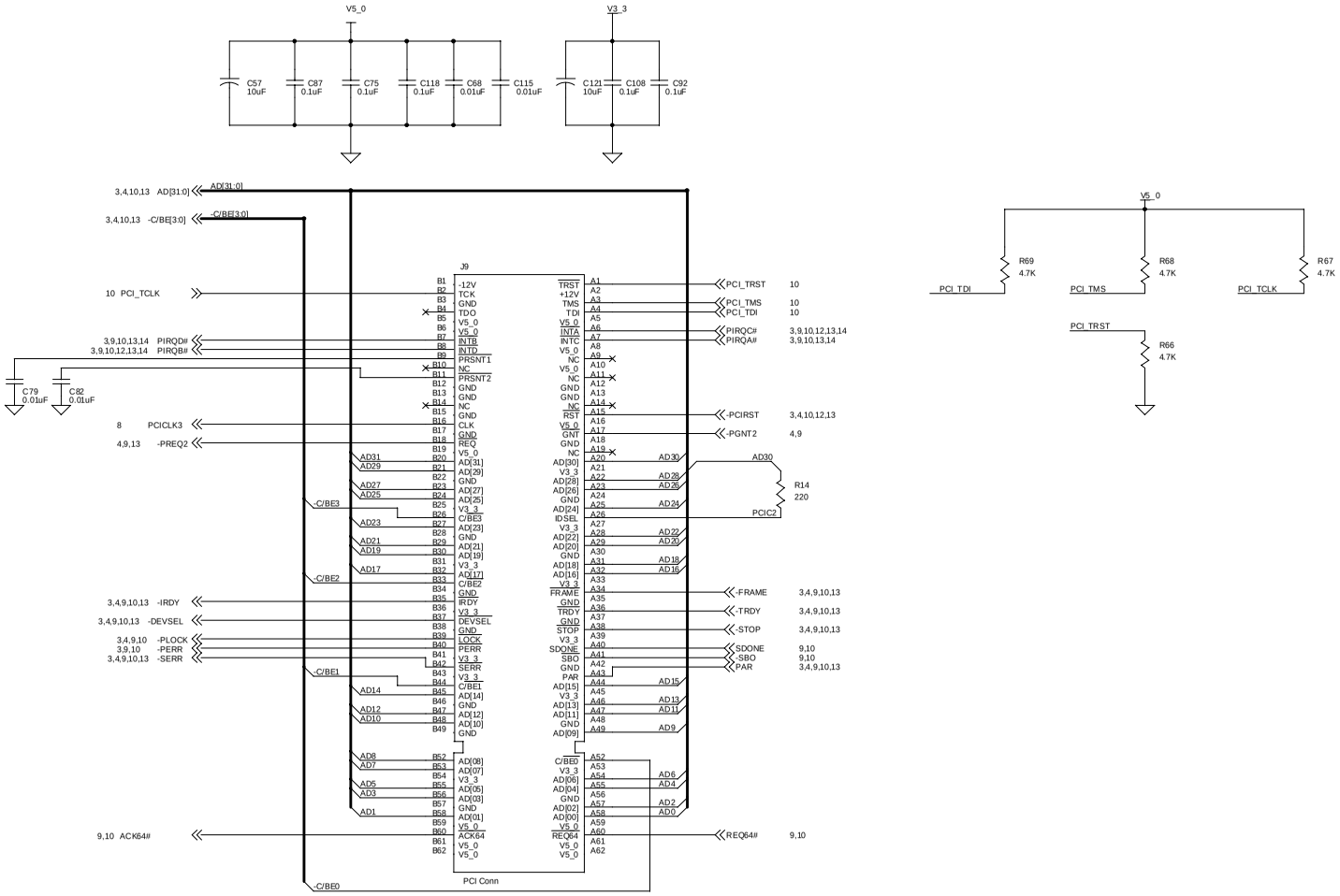
J7/J8 GND:
   A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
   B3, B12, B13, B15, B17, B28, B34, B38, B46, B49,
B57

J7/J8 +12V: A2
      -12V: B1



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

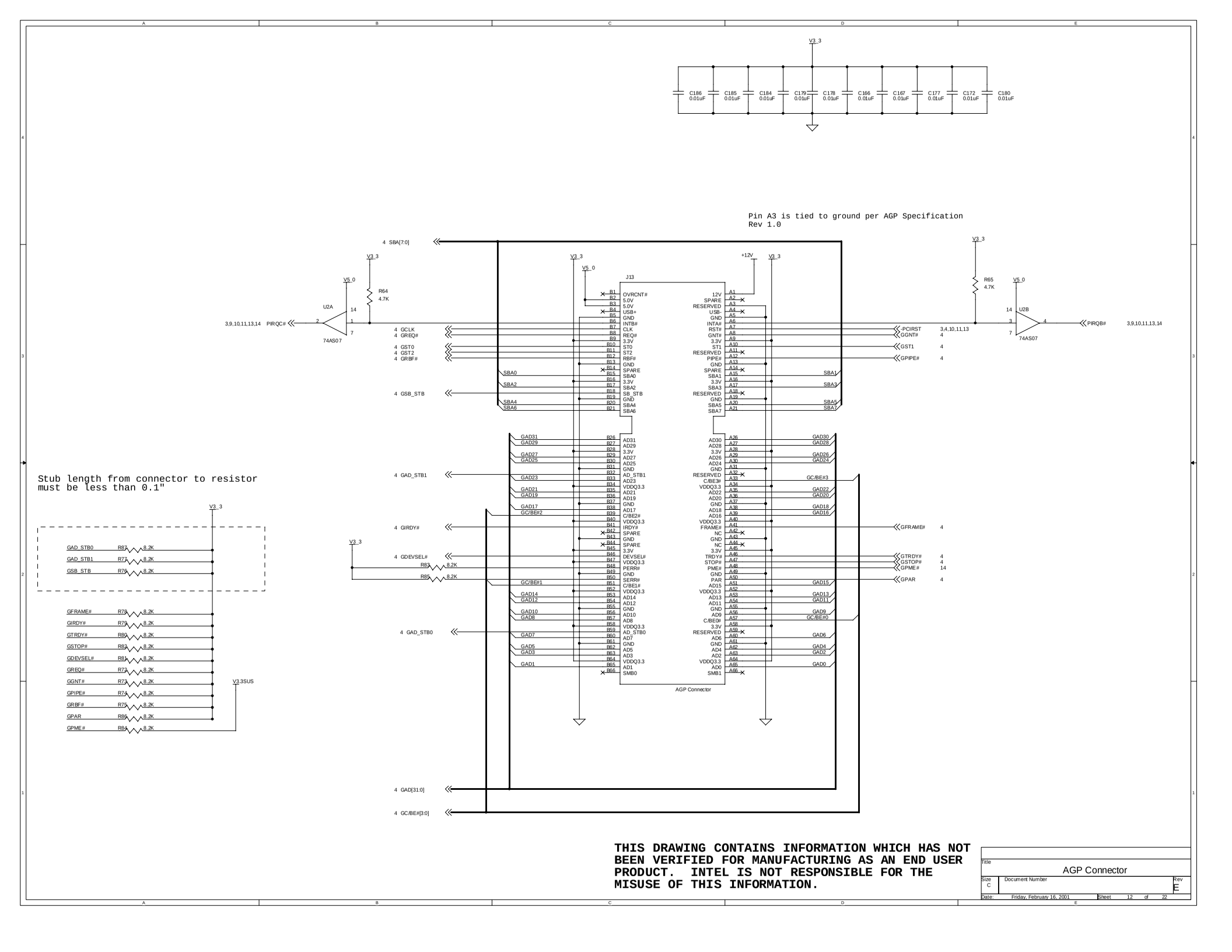
Title: PCI Slots 0 & 1		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 10 of 22	



PCI SLOT 2

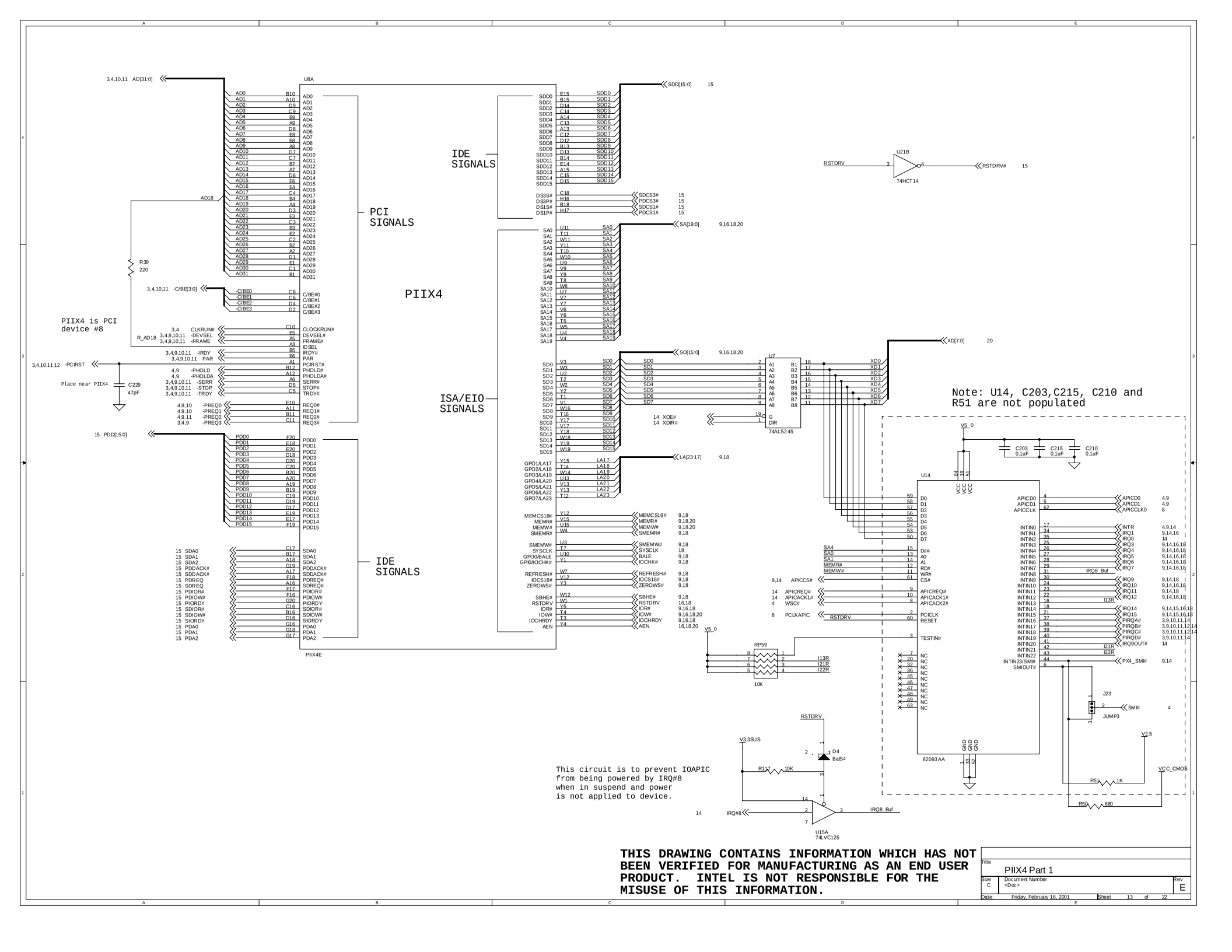
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

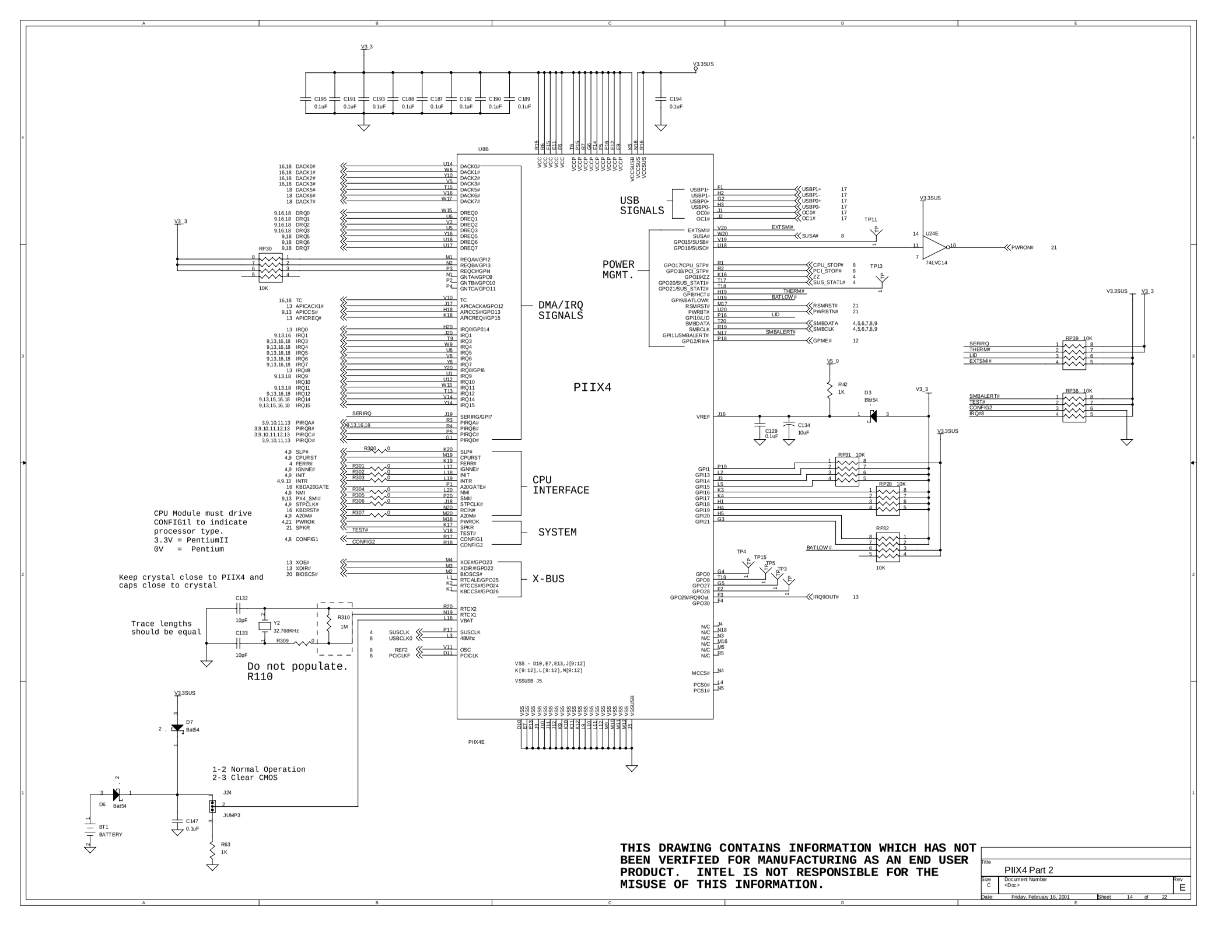
Title: PCI Slot 2			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 11 of 22		



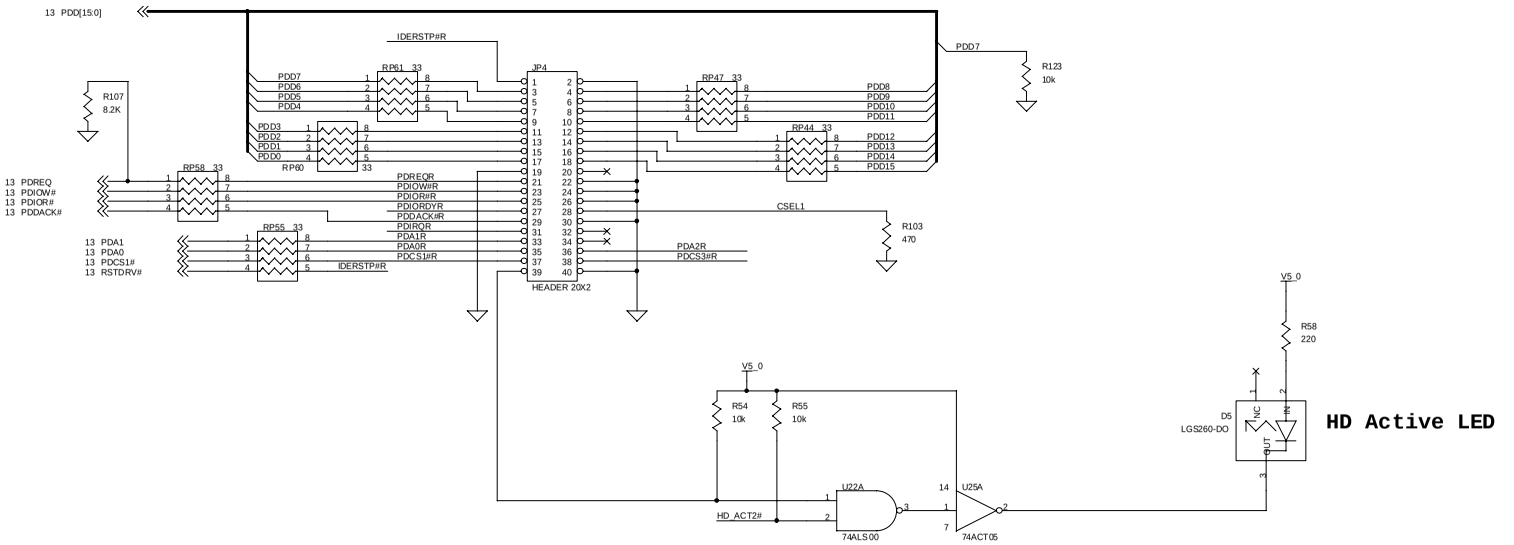
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	AGP Connector		
Size C	Document Number		Rev E
Date: Friday, February 16, 2001	Sheet 12 of 22		

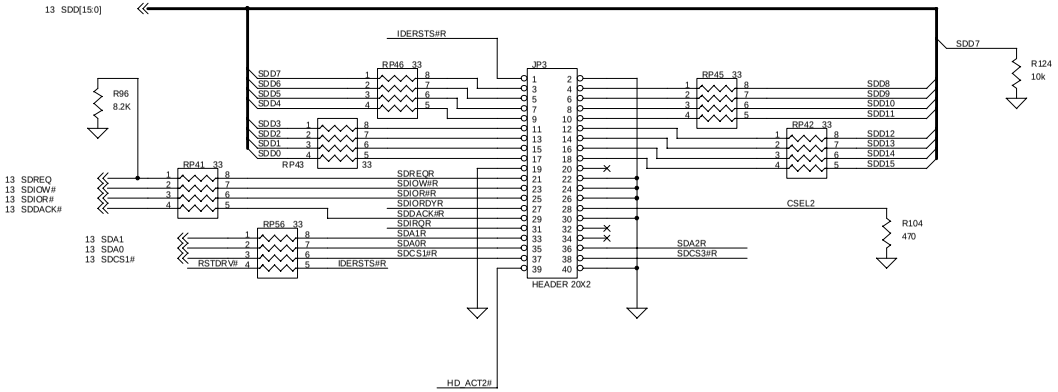

PIIX4 is PCI device #8
PCI SIGNALS
IDE SIGNALS
PIIX4
ISA/EIO SIGNALS
IDE SIGNALS
PIIX4E
U8A
Note: U14, C203,C215, C210 and R51 are not populated
This circuit is to prevent IOAPIC from being powered by IRQ#8 when in suspend and power is not applied to device.
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
Title
PIIX4 Part 1
Size C
Document Number <Doc>
Rev E
Date: Friday, February 16, 2001
Sheet 13 of 22

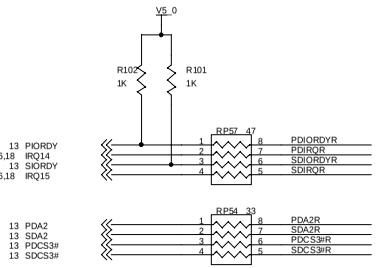

PIIX4
DMA/IRQ SIGNALS
CPU INTERFACE
SYSTEM
X-BUS
USB SIGNALS
POWER MGMT.
U8B
PIIX4E
CPU Module must drive CONFIG1l to indicate processor type.
3.3V = PentiumII
0V = Pentium
Keep crystal close to PIIX4 and caps close to crystal
Trace lengths should be equal
Do not populate. R110
1-2 Normal Operation
2-3 Clear CMOS
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
Title
PIIX4 Part 2
Size C
Document Number <Doc>
Rev E
Date: Friday, February 16, 2001
Sheet 14 of 22

Primary IDE Connector



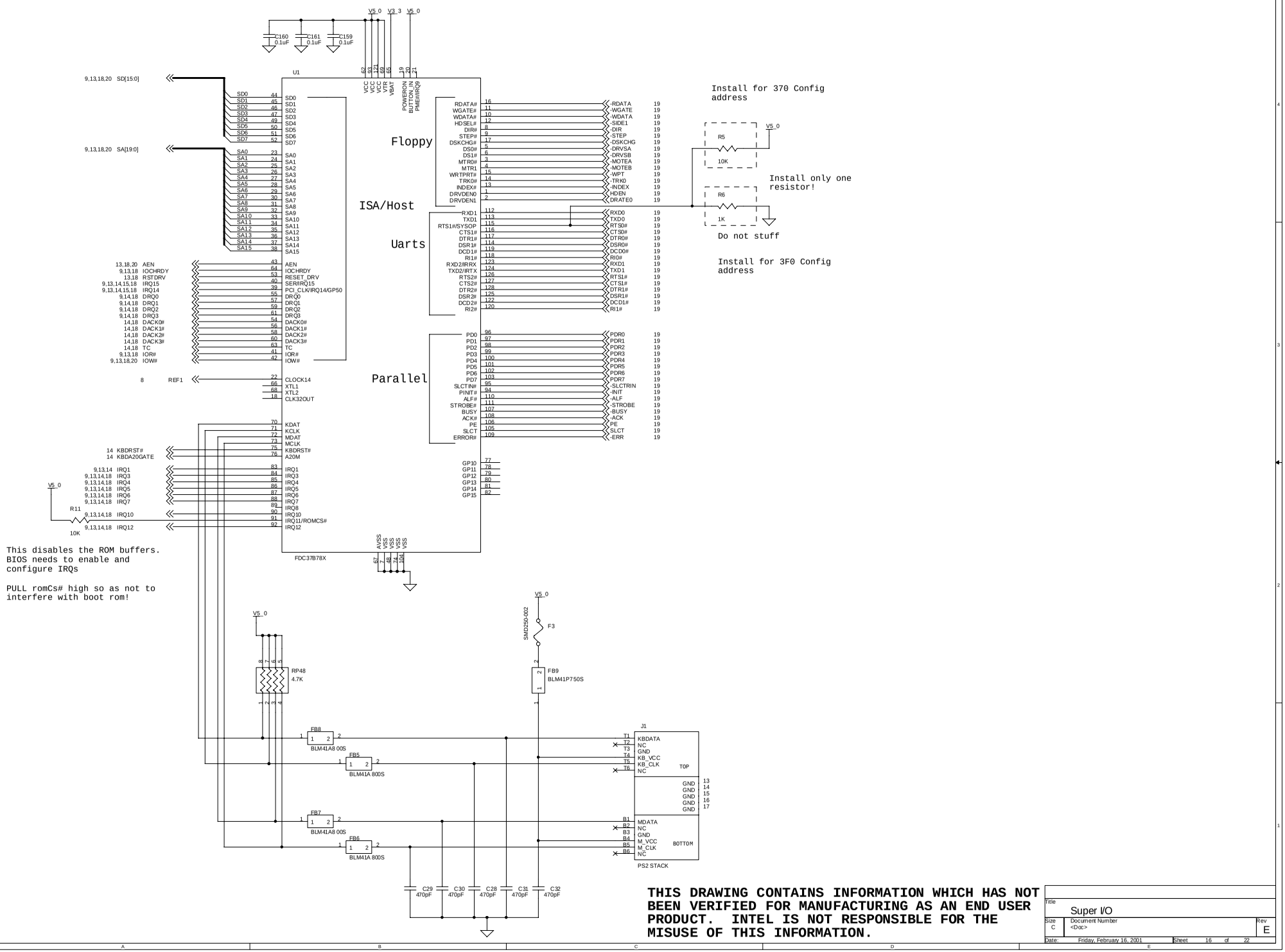
Secondary IDE Connector





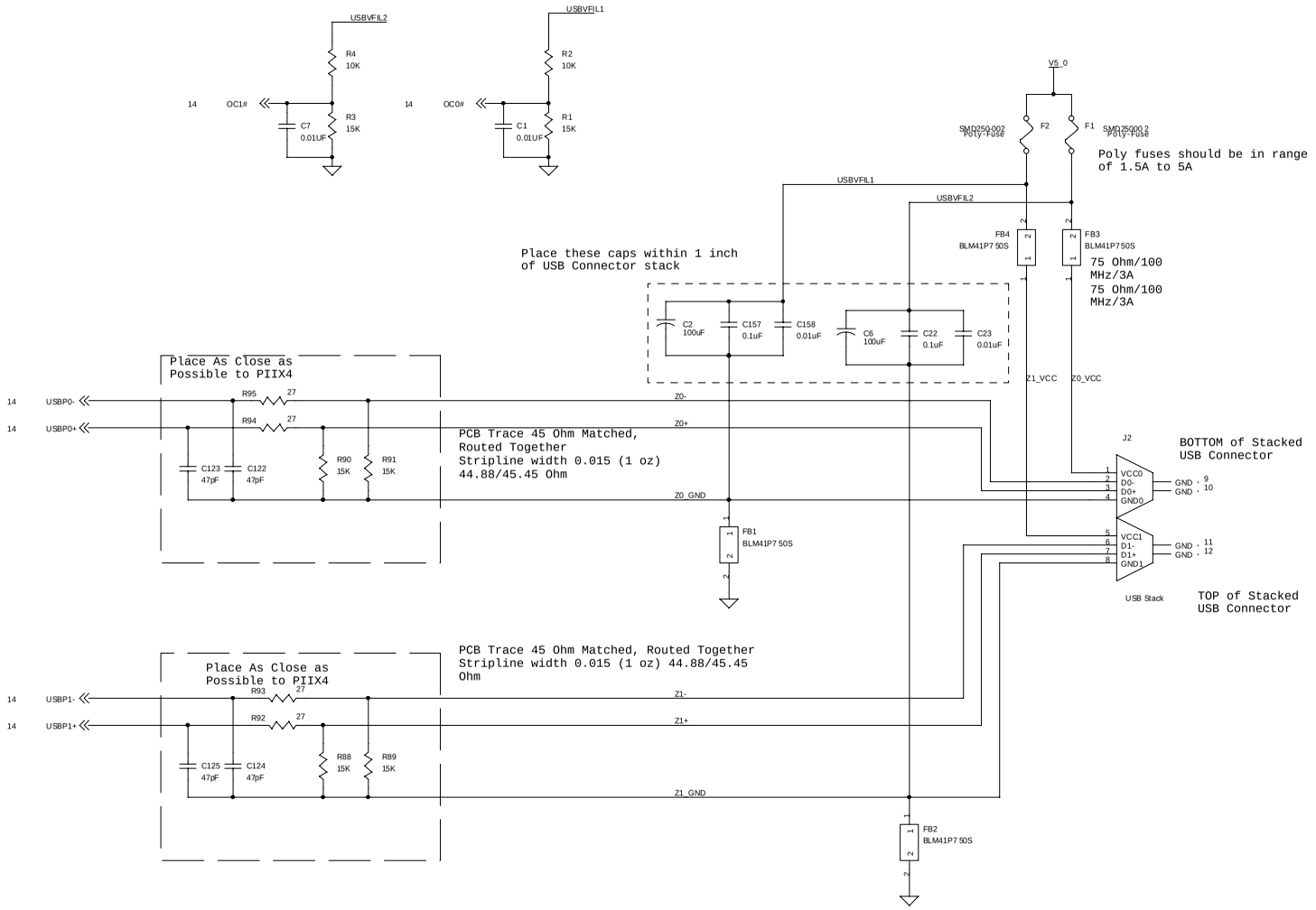
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: IDE Connectors		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 15 of 22	



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: Super I/O			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 16 of 22		



NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or
double space to any other signal.

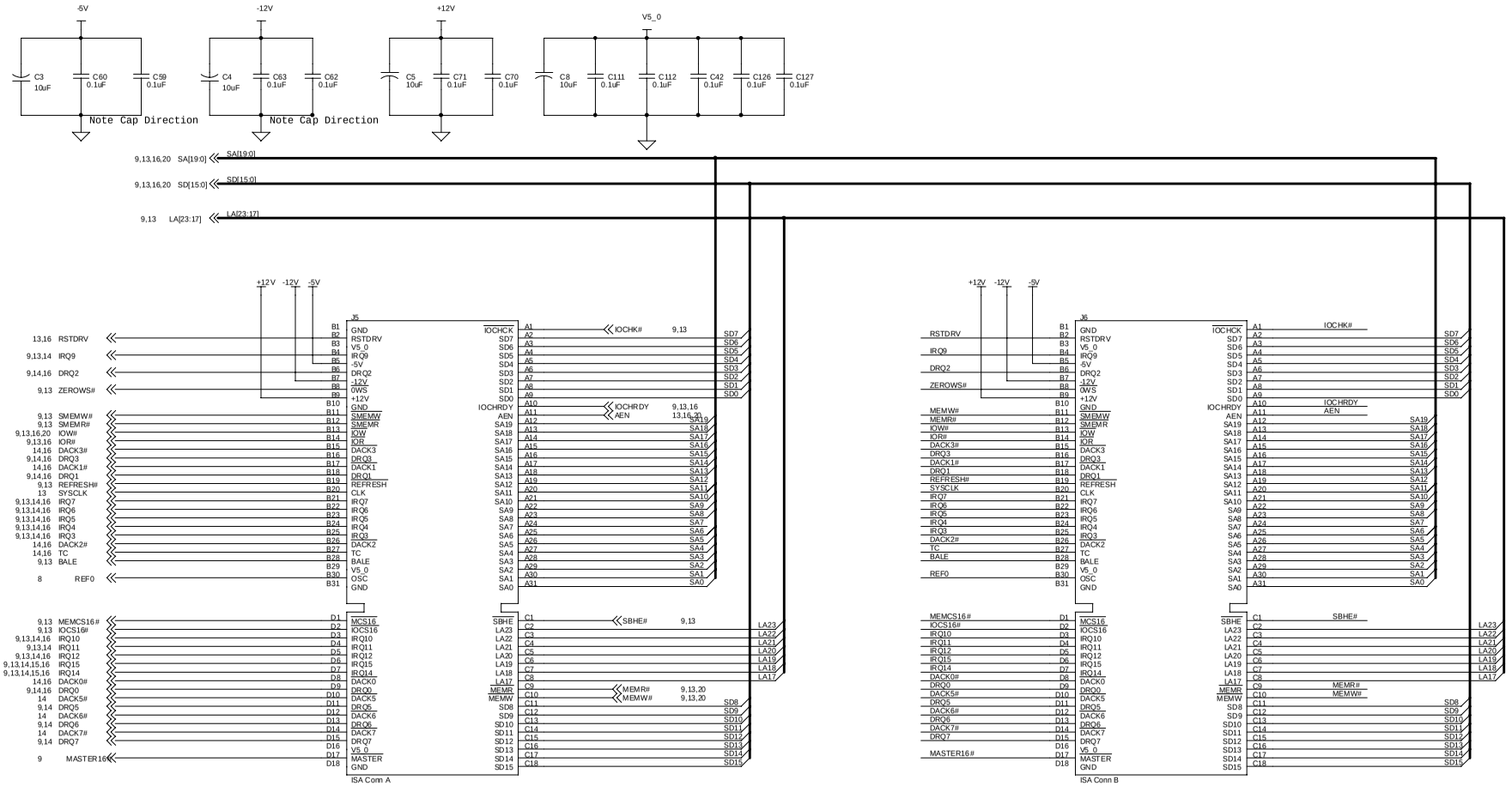
NOTE 3: Place ferrites at connector.

NOTE 4: Poly-fuse min 1.5A
max 5A.

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: USB Connectors			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 17 of 22		

ISA Slots



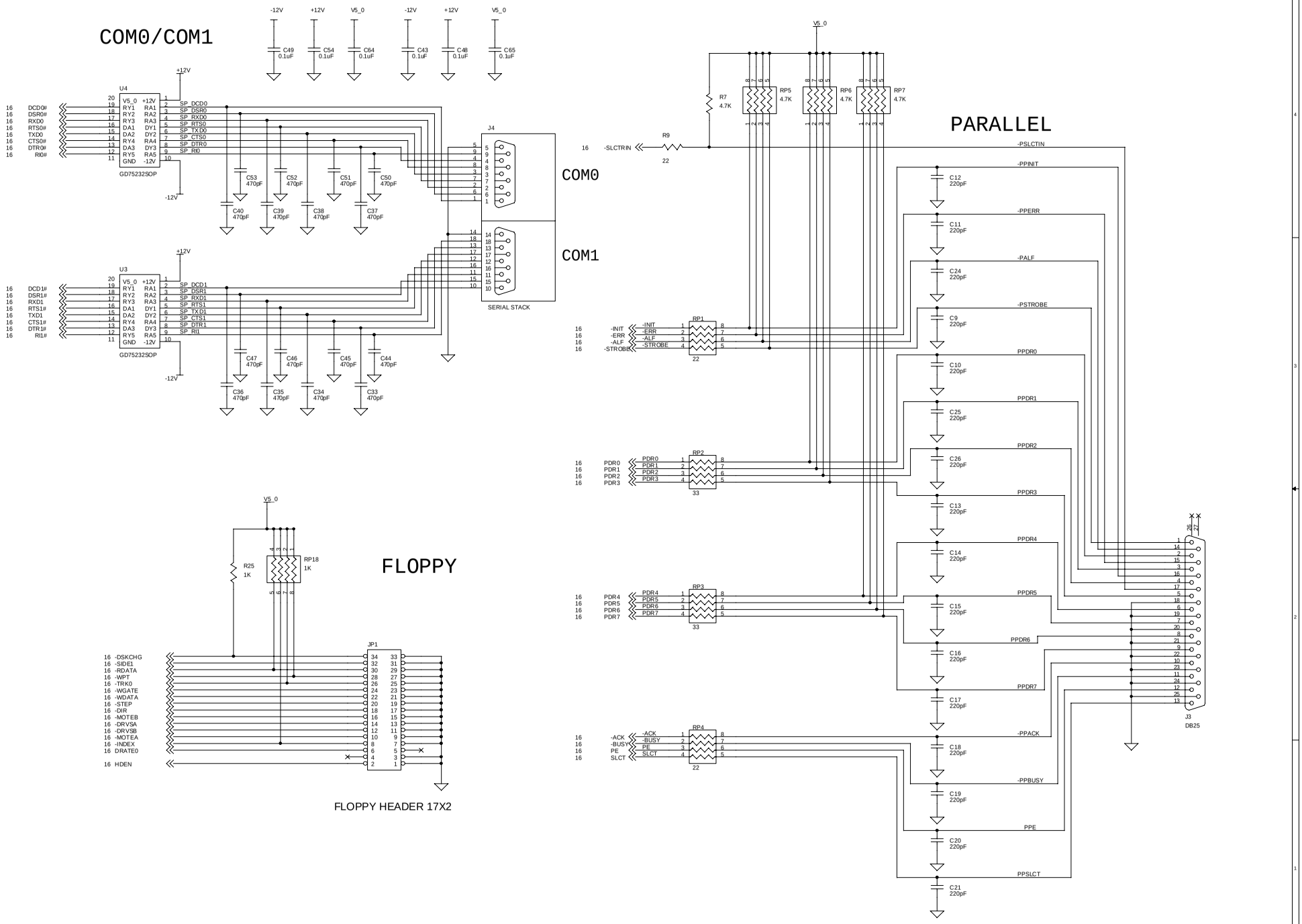
J5/J6 V5_0:
B03, B29, B31, D16

J5/J6 GND:
B01, B10, D18

J5/J6: +12V B09
-12V B07
-5V B05

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

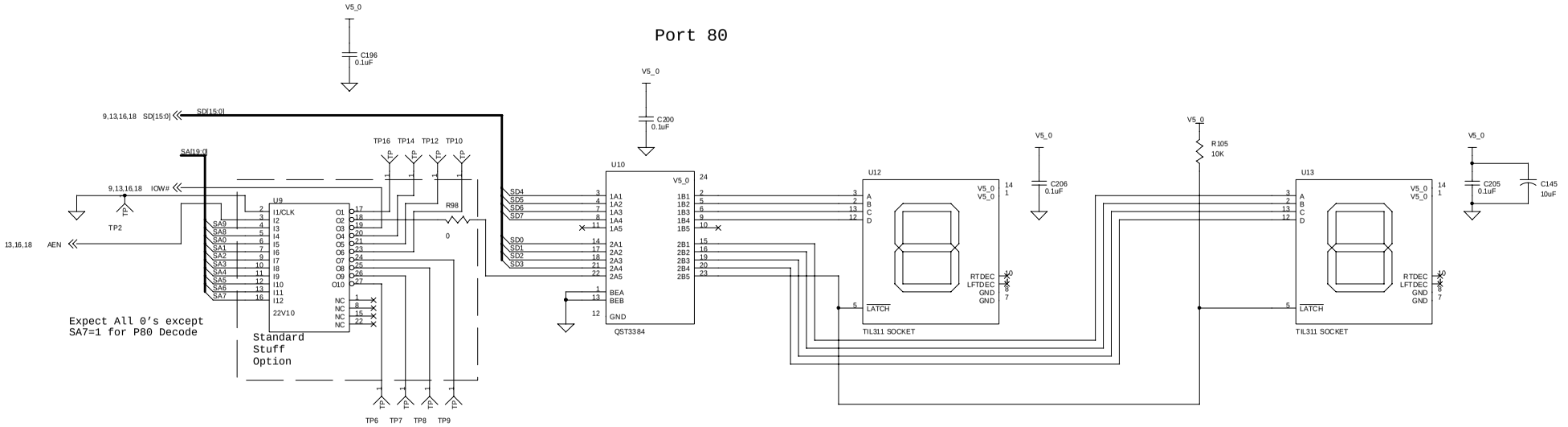
Title: ISA Connectors			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 18 of 22		

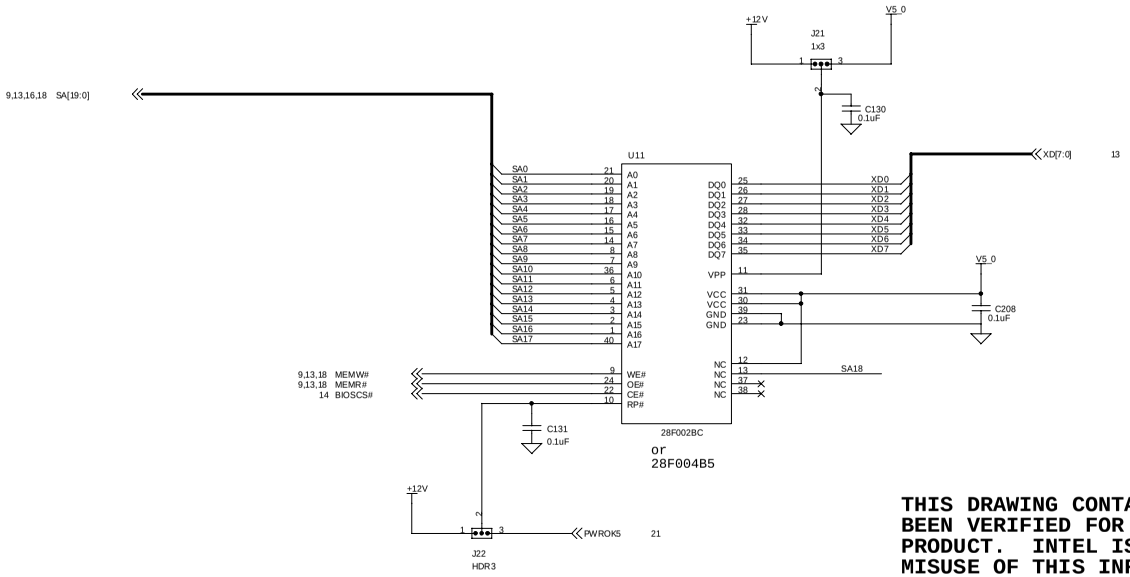


THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	COMx, DB25, Floppy	
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 19 of 22	

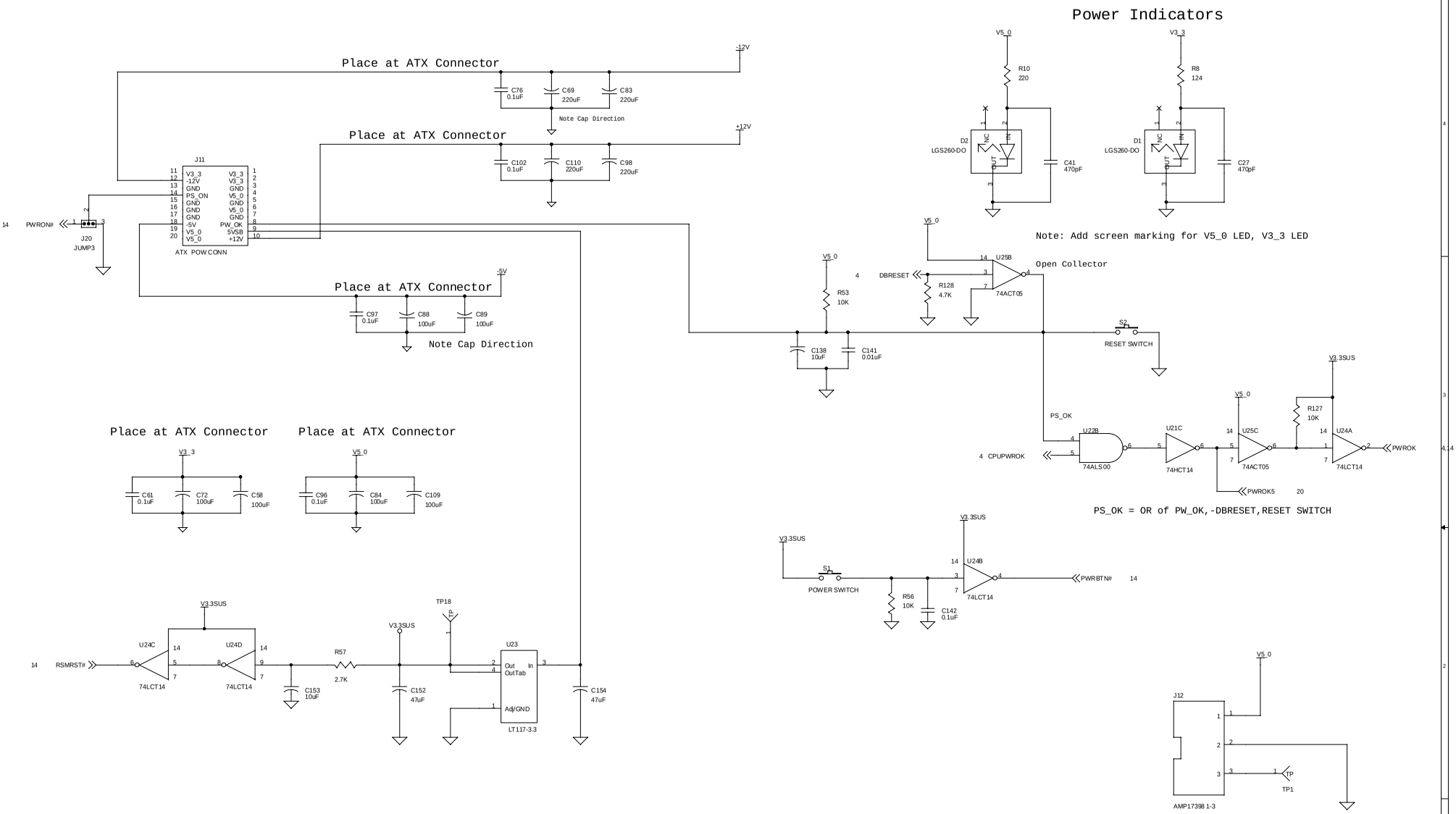
Port 80





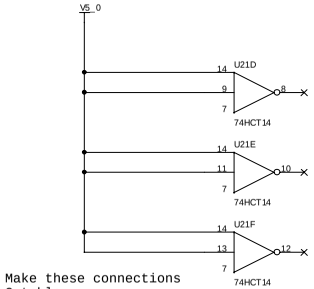
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: BIOS/ Port 80		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 20 of 22	

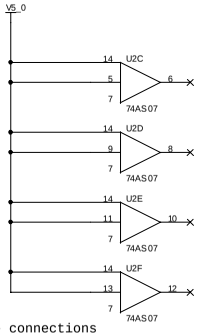


THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

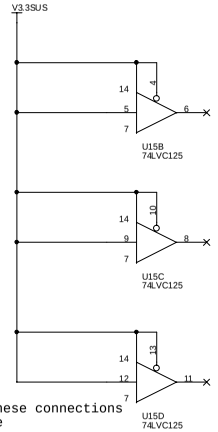
Title	ATX Power Connector	
Size C	Document Number <Doc>	Rev E
Date: Friday, February 16, 2001	Sheet 21 of 22	



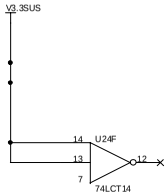
Make these connections
Cutable



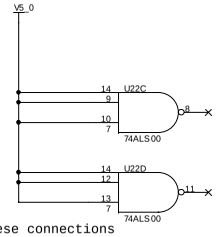
Make these connections
Cutable



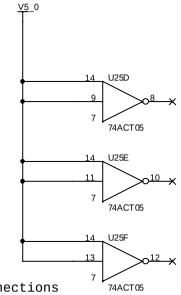
Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: Unused Gates		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 22 of 22	

Intel(R) 440BX Scalable Performance Board

Revision A3

History

Rev A3 changes
1. Changed Q6,Q4,Q5,Q7 to Q1,Q2,Q3,Q4 respectively and changed the MOSFET to a Fairchild FDV301N and changed the pinout for the SOT-23 package to correct it.
2. Added a 270 ohm pull-up to PREQ# page 10
3. Corrected the ITP female socket routing. Pinout was correct in A2, but the signals were routed incorrectly.
4. Changed silkscreen to read "Flexible Intel(R) 440BX AGPset/PGA370 Processor adapter"
5. Page 3: Silkscreen pin numbers for Socket-370 on TOP and BOTTOM layers.
6. Changed R6,R7 to 270 ohms
7. Made C1 a Don't Pop.
8. Changed all Don't Pops to have EMPTY as their value. this way they sort together when generating BOM.
9. Page 6, BX. Removed R16,R17,R18. Added silkscreen pin numbering for BX. Added four testpoints to ground under BX. Placed tuning caps C86,87,88 within 1/2 inch of BX.
10. Page 10. Changed 3.3V power to QS3257 to 5.0V. Changed R40 from 3.3K to 270 ohm.
11. BSEL0 pulled to 3.3V. (it was pulled to 2.5V).
12. R105 changed from 680 ohms to 280 ohms.
13. HCLK0,HCLK1 routing changed. These two signals must be on same layer, bottom layer, and not traverse multiple layers.
14. Also, on connector, pin K33, HCLK0 and pin K35, HCLK1 have been swapped. Now, in rev A3, HCLK0 is K35, and HCLK1 is K33. This is to accomodate routing these two signals on the same (bottom) layer. Otherwise, they would have criss-crossed. This has no effect on the circuit since the clocks are tied together on baseboard.
15. The three AGTL+ test signals BNR#,HD4#,HA27# had a min. of 1.6", this has been changed to a min. of 1.8".
16. Page 9. The AGTL+ signals min. has been changed to 1.8" (used to be 1.6").

Rev A2 Changes

HOST INTERFACE
1. Changed socket370 to socket370-256
2. Removed two 74LV07As from Host Interface page since these signals are being pulled up to VCC_CMOS on baseboard.
3. Removed RP1,RP2, R3,R2 pullups for CMOS signals.
4. Removed BSEL# pullup 270 ohm
5. Replaced Q1 with a MOSFET per design guide.
6. Added HRESET# termination on host interface page.
7. Added AH4 RESET pin and connected it to X4 RESET2#
8. Added 650 ohm pullup to FLUSH#

VID/Test Debug/Unused
1. Changed LC PLL component values per Aug 99 flexible design guide
2. Added 10K RP to VID
3. Removed 330 ohm RP from VID
4. Added CMOS conversion logic for THERMTRIP#
5. Added new BSEL0#,BSEL1# circuitry

S370-256 Power
1. Removed 20 1uF bypass caps. They are on the package for CuMine. C10-C24,C30-C34

BX Host Interface
1. Added CPURST# termination and layout guidelines
BX Memory Interface
2. Changed cap on DCLKWR to 20pf from 0.1uF. Removed resisitor.
3. Added 10K series resistor to MAB#12 (removed from baseboard)

Connector
1. VCC_CMOS to RESERVED16
2. Change BSEL# to BSEL0#

GTL+ Termination
1. Added new layout guidelines per flexible design guide Aug 99
2. Added four more VTT decoupling caps to bring the total to 20.
3. Changed 51 ohm pullup on PRDY0# to 150 ohm

Bus Ratio/Thermal/ITP
1. removed pullup on HRESET# (followed flexible design guide)
2. move 270 ohm as a pullup for STBY# on MAX1617 per datasheet typical operating circuit. This place cap directly on VCC of MAX1617 per datasheet.
3. removed 10K "do not papulate" resistor from STBY#.
4. removed "do not populate" for QS3257
5. added "do not populate" for RP62 0 ohm for QS3257
6. removed R48 51 ohm pullup on PRDY#
7. Added 150 ohm pullups to PRDY1#, PRDY2#, PRDY3#
8. Replaced NAND gate inverter with FET for DBRESET.

Rev A1 Changes

1. Removed translator logic for PREQ0#
2. Removed termination resistors on BX side for GTL+
3. Added 20pF load on HCLK for BX clock compensating

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

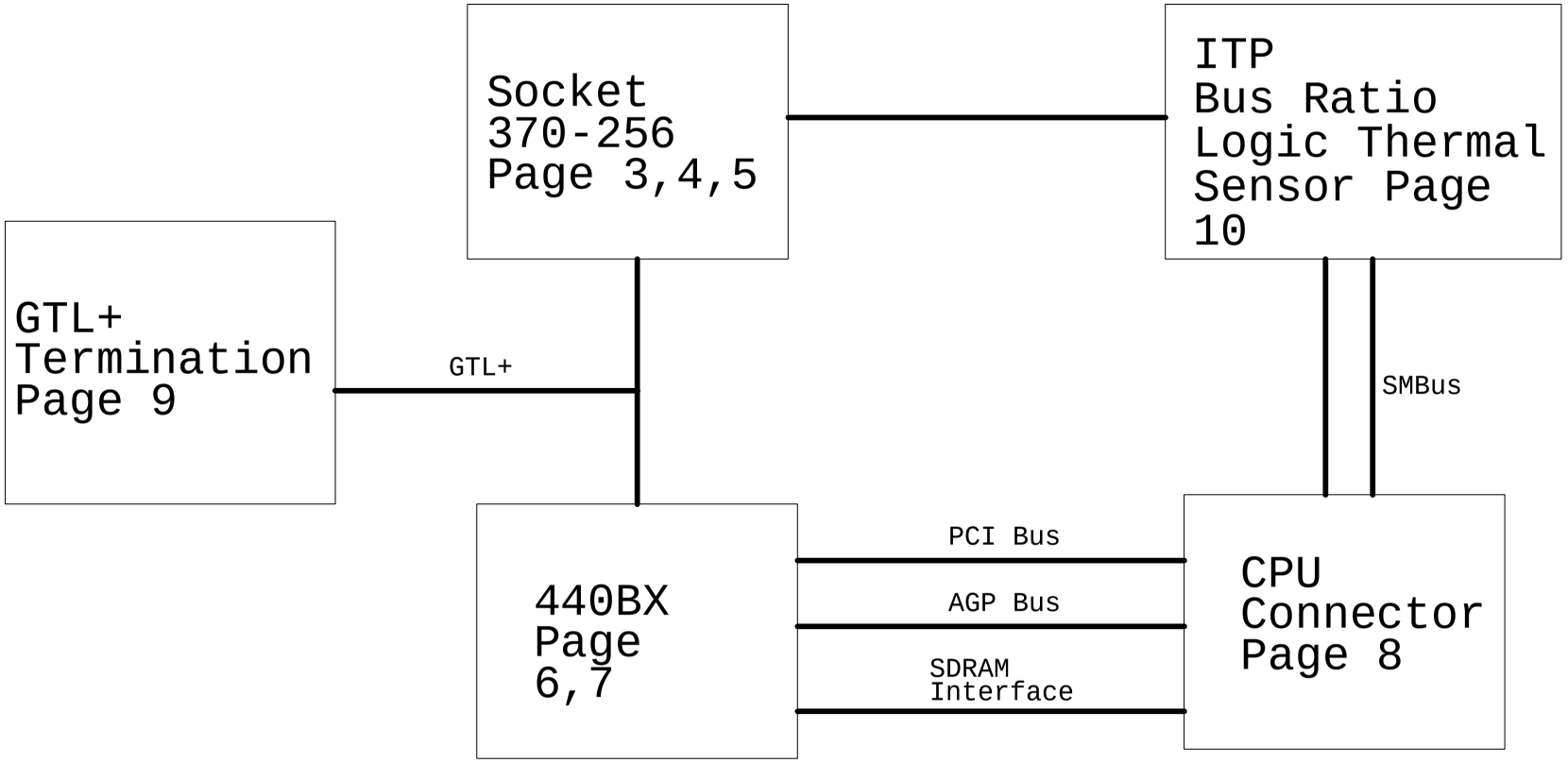
Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. Intel does not warrant or represent that such use will not infringe such rights.

THIS SCHEMATIC IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF PROPOSAL, SPECIFICATION OR SAMPLE.

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title	Intel(R) 440BX Scalable Performance Board	
Size C	Document Number	Rev A3
Date: Wednesday, April 26, 2000	Sheet 1 of 12	



Voltage
Regulator
Page 11

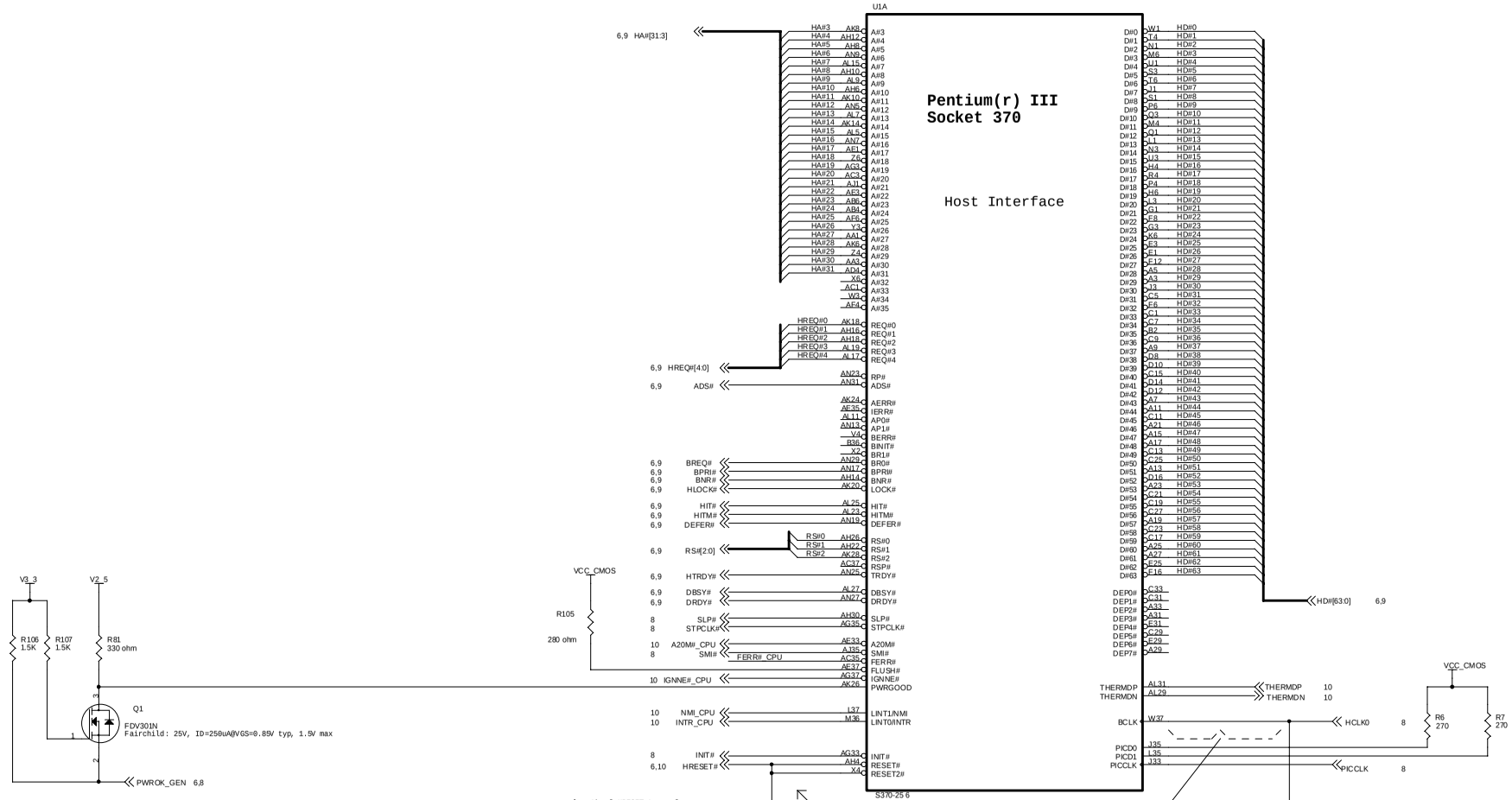
Layout
Guidelines
Page 12

THIS SCHEMATIC IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF PROPOSAL, SPECIFICATION OR SAMPLE.

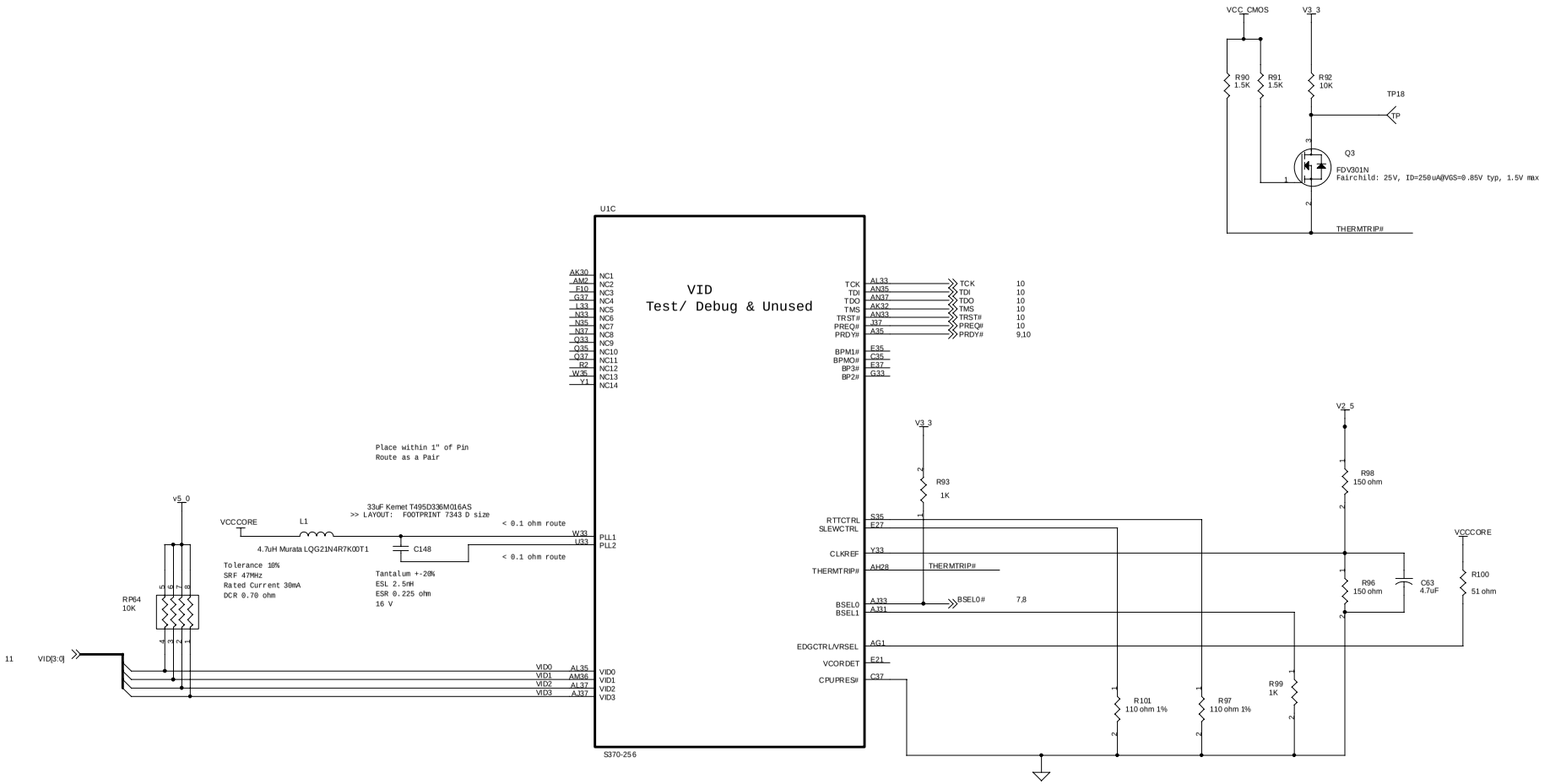
Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title	Diagram	
Size C	Document Number: Intel(R) 440BX Scalable Performance Board	Rev A3
Date: Wednesday, April 26, 2000	Sheet 2 of 12	

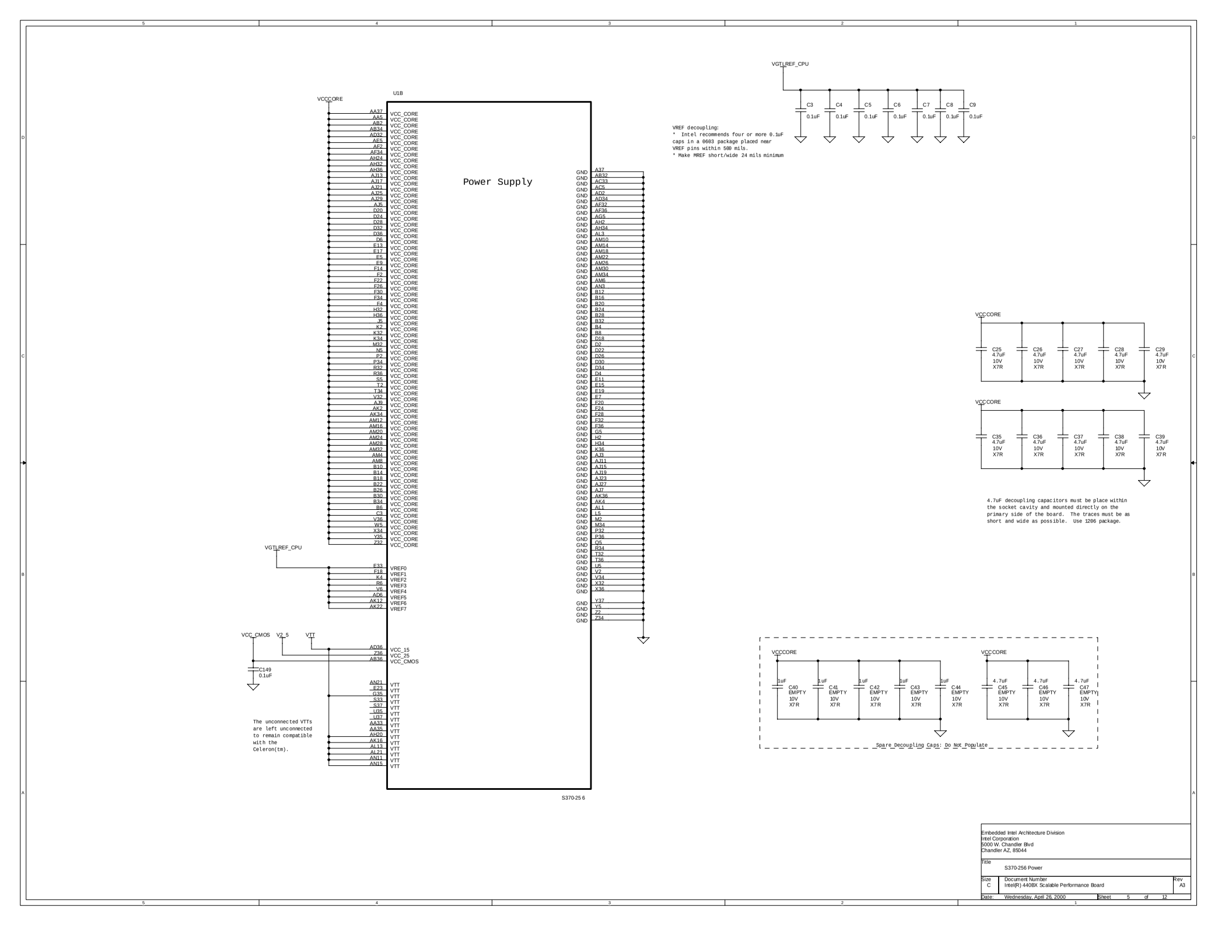
>>LAYOUT: Silkscreen. Number socket-370 on top and bottow layer.



Embedded Intel Architecture Division Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044	
Title	S370-256 Host Interface
Size: C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev: A3
Date: Wednesday, April 26, 2000	Sheet 3 of 12



Embedded Intel Architecture Division Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044	
Title	S370-256 Other
Size C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev A3
Date: Wednesday, April 26, 2000	Sheet 4 of 12



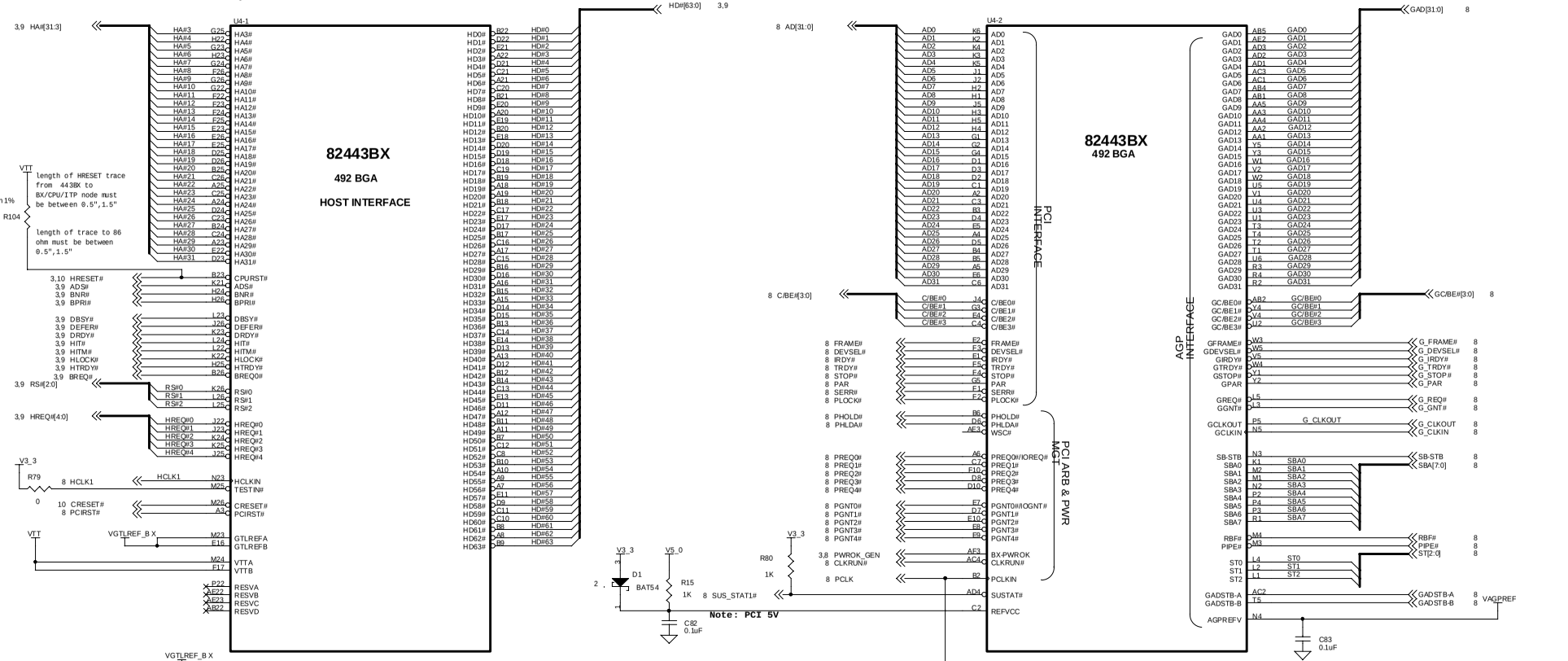
Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

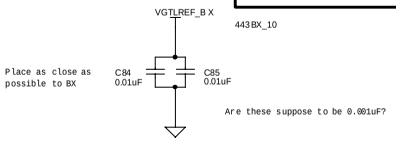
Title: S370-256 Power

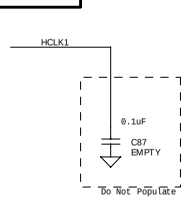
Size: C | Document Number: Intel(R) 440BX Scalable Performance Board | Rev: A3

Date: Wednesday, April 26, 2000 | Sheet 5 of 12

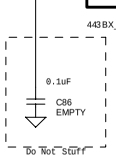
>>LAYOUT: Silkscreen. Put 82443BX pin numbers on both top and bottom layers.



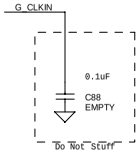




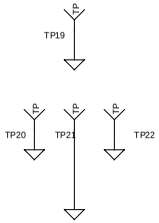
>>LAYOUT: place cap within 1/2 inch of BX.



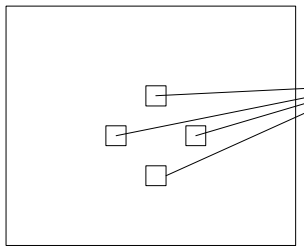
>>LAYOUT: place cap within 1/2 inch of BX.



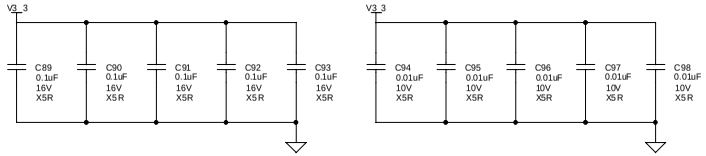
>>LAYOUT: place cap within 1/2 inch of BX.



82443BX bottom view



>>LAYOUT: GROUND PADS within inner ring of balls of BX on bottom layer



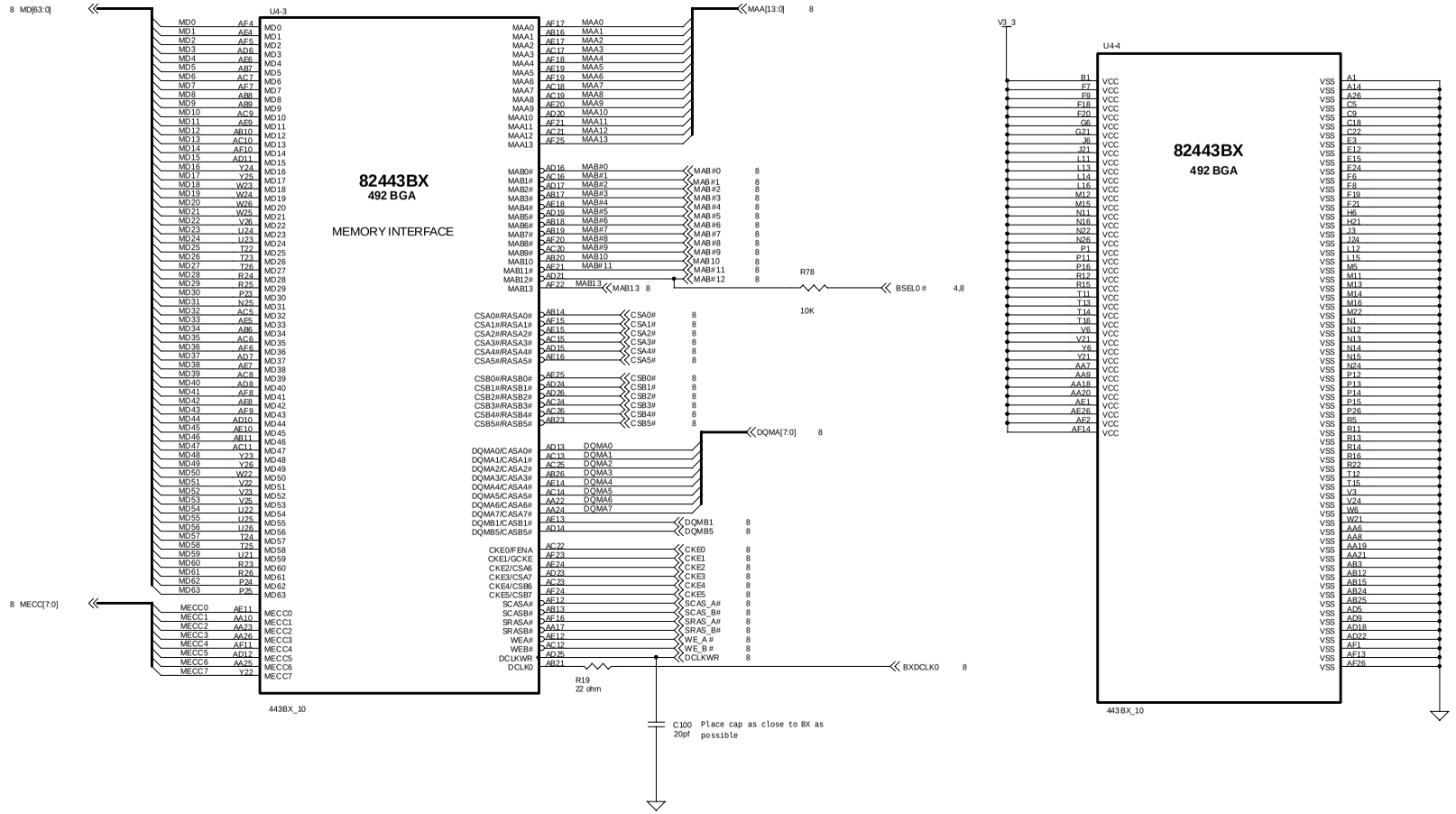
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title: 440BX Host Inteface

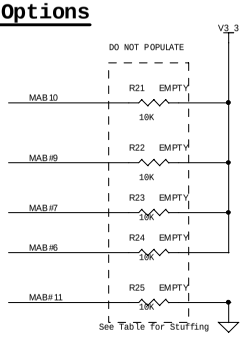
Size: C | Document Number: Intel(R) 440BX Scalable Performance Board | Rev: A3

Date: Wednesday, April 26, 2000 | Sheet 6 of 12



BX Strapping Options

Resistor	Function	Board Default Setting	Signal
R21	Quick Start Select	Do Not Stuff	MAB10#
R22	AGP Disable	Do Not Stuff	MAB9#
R23	Memory Module Configuration	Do Not Stuff	MAB7#
R24	Host Bus Buffer Mode Select	Do Not Stuff	MAB6#
R25	In-Order Queue Depth Enable.	Do Not Stuff	MAB11#



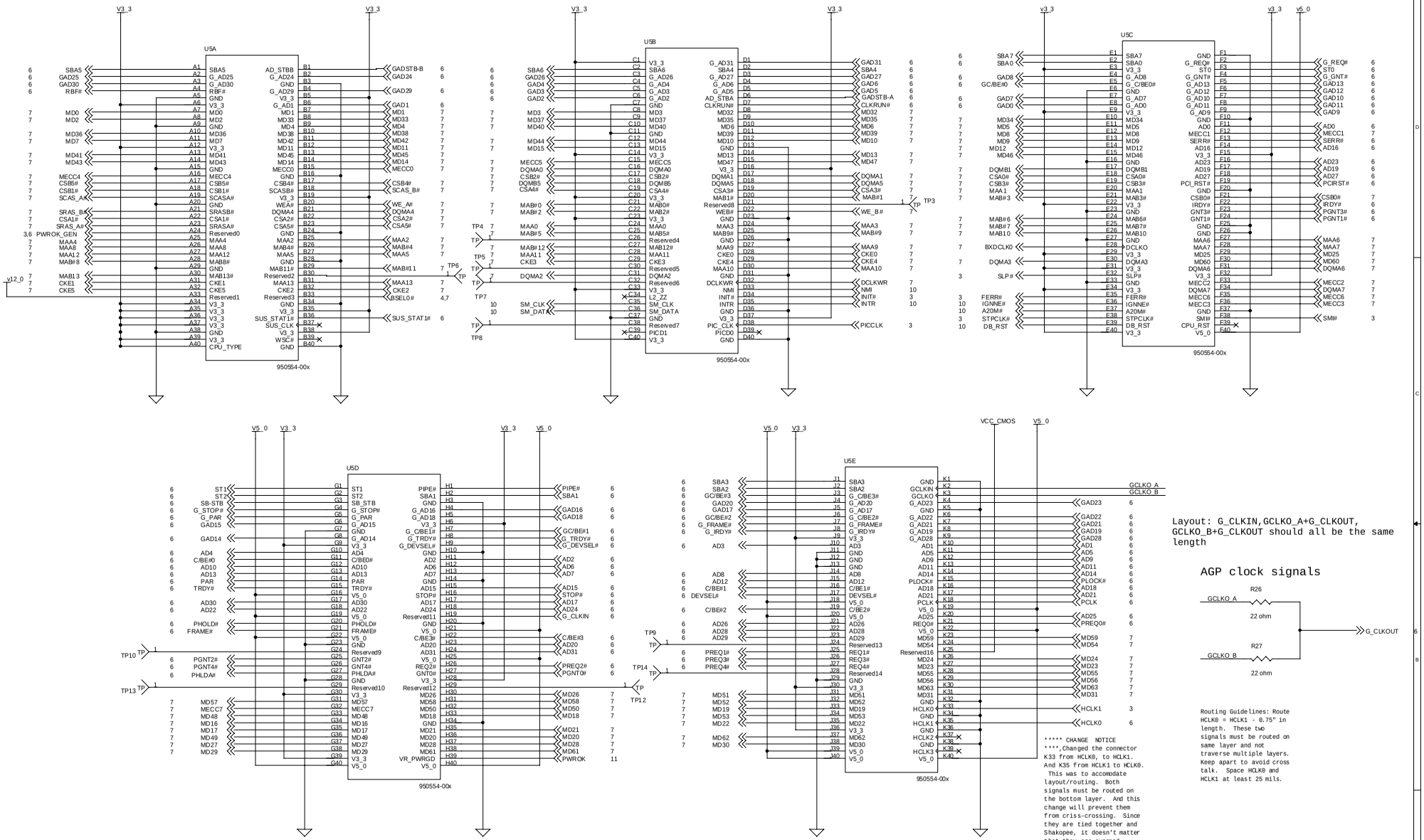
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title: 440BX Memory Interface

Size	Document Number	Rev
C	Intel(R) 440BX Scalable Performance Board	A3

Date: Wednesday, April 26, 2000 Sheet 7 of 12



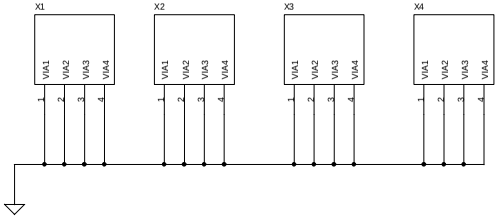
Layout: G_CLKIN,GCLKO_A+G_CLKOUT, GCLKO_B+G_CLKOUT should all be the same length

AGP clock signals

Routing Guidelines: Route HCLK0 = HCLK1 - 0.75" in length. These two signals must be routed on same layer and not traverse multiple layers. Keep apart to avoid cross talk. Space HCLK0 and HCLK1 at least 25 mils.

***** CHANGE NOTICE
****,Changed the connector K33 from HCLK0, to HCLK1. And K35 from HCLK1 to HCLK0. This was to accomodate layout/routing. Both signals must be routed on the bottom layer. And this change will prevent them from criss-crossing. Since they are tied together and Shakopee, it doesn't matter that they are swapped.

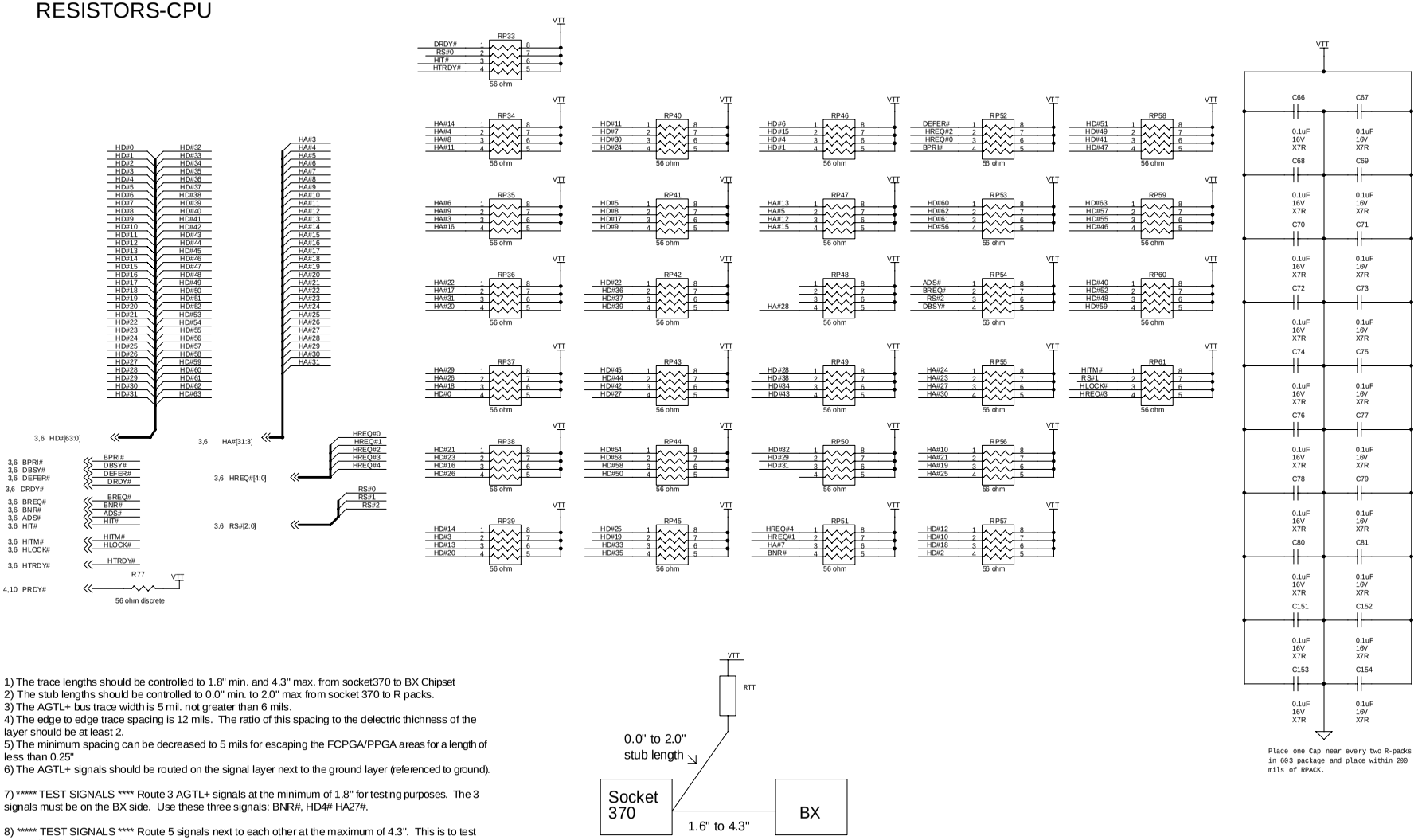
Mounting Holes



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Embedded Intel Architecture Division	
Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044	
Title: Connectors	
Size: C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev: A3
Date: Wednesday, April 26, 2000	Sheet 8 of 12

GTL+ TERMINATION RESISTORS-CPU



Place one Cap near every two R-packs in 603 package and place within 200 mils of RPACK.

1) The trace lengths should be controlled to 1.8" min. and 4.3" max. from socket370 to BX Chipset
2) The stub lengths should be controlled to 0.0" min. to 2.0" max from socket 370 to R packs.
3) The AGTL+ bus trace width is 5 mil. not greater than 6 mils.
4) The edge to edge trace spacing is 12 mils. The ratio of this spacing to the delectric thichness of the layer should be at least 2.
5) The minimum spacing can be decreased to 5 mils for escaping the FCPGA/PPGA areas for a length of less than 0.25"
6) The AGTL+ signals should be routed on the signal layer next to the ground layer (referenced to ground).

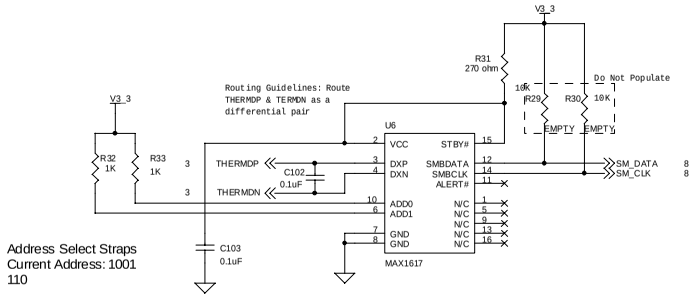
7) ***** TEST SIGNALS **** Route 3 AGTL+ signals at the minimum of 1.8" for testing purposes. The 3 signals must be on the BX side. Use these three signals: BNR#, HD4# HA27#.

8) ***** TEST SIGNALS **** Route 5 signals next to each other at the maximum of 4.3". This is to test crosstalk. The five signals are: HD29#, HD28#, HD43#, HD37#, HD44#.

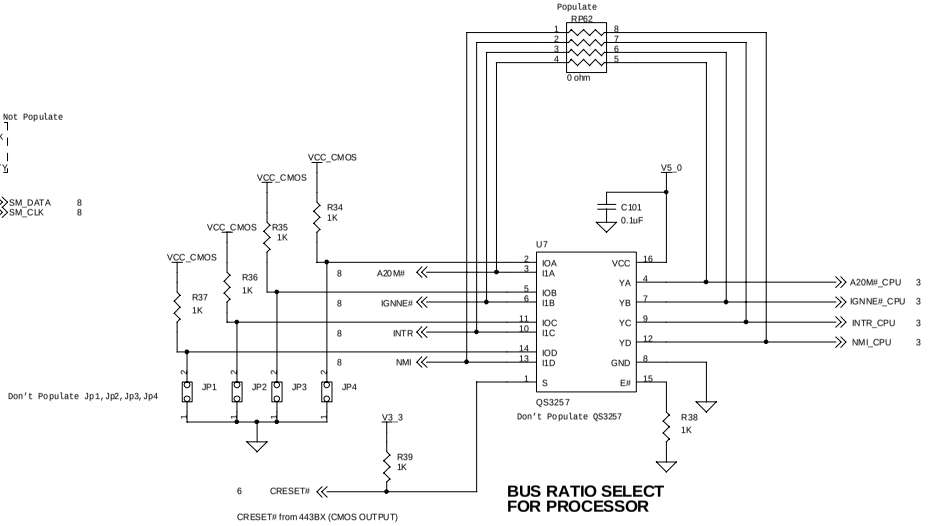
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

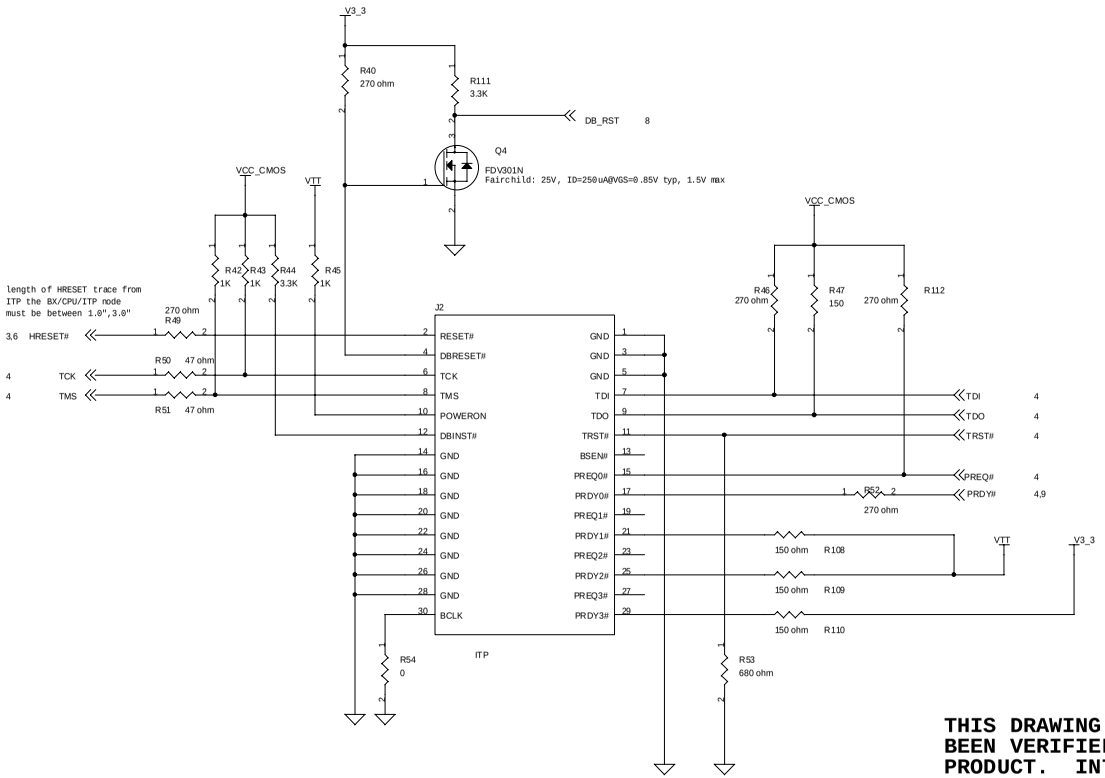
Title	GTL Termination	
Size C	Document Number: Intel(R) 440BX Scalable Performance Board	Rev A3
Date: Wednesday, April 26, 2000	Sheet 9 of 12	

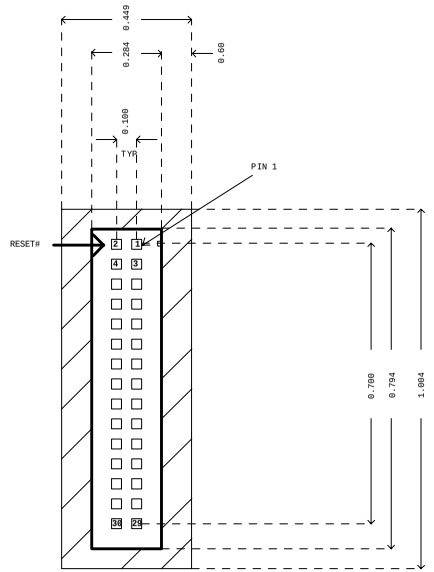


THERMAL SENSOR



BUS RATIO SELECT FOR PROCESSOR

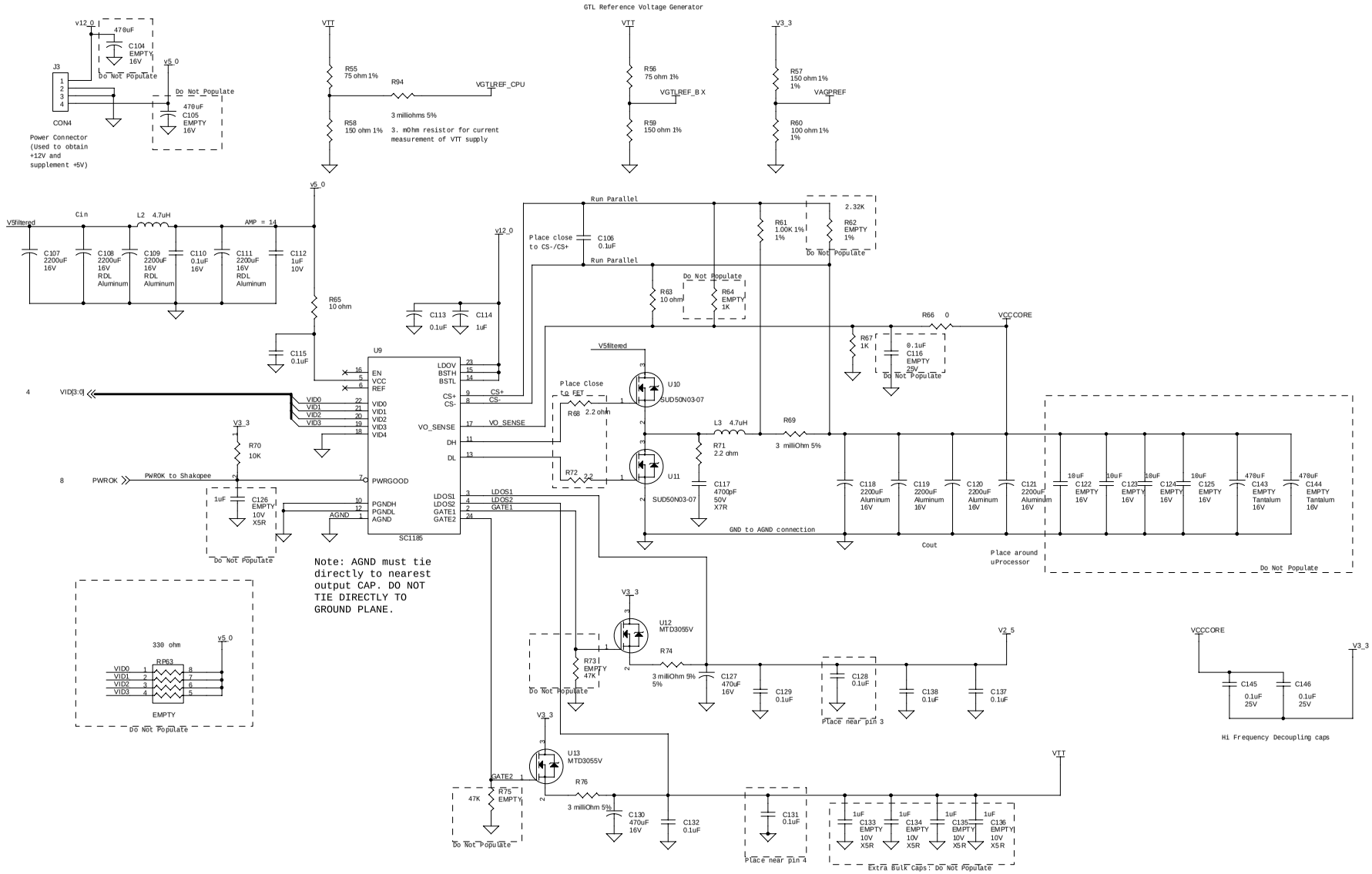




>>> LAYOUT
1.5V connector, AMP 104078-4 Vertical Recepticle, Top View
of ITP connector with component keep-out area.

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Embedded Intel Architecture Division Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044	
Title: Bus Ratio, Thermal, ITP	
Size: C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev: A3
Date: Wednesday, April 26, 2000	Sheet 10 of 12



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title	Voltage Regulator	
Size C	Document Number Intel(R) 440BX Scalable Performance Board	Rev A3
Date: Wednesday, April 26, 2000	Sheet 11 of 12	

Layout guideline checklist

Board

[ ] An 8 layer board, see right for stack up
[ ] The impedance of all signal layers are to be between 55 and 75 ohms.
[ ] The board impedance should be between 55 and 75 ohms (65 +/- 15%).
[ ] FR-4 material should be used for the board fab.
[ ] The ground plane should not be split.
[ ] If a signal must be routed for a short distance on a power plane, then use the VCC plane.
[ ] Keep vias for decoupling caps as close to the cap pads as possible.

S370_256 Host Interface

[ ] length of HRESET trace from CPU to BX/CPU/ITP node must be between 0.5",1.5"

[ ] HRESET# length of trace to 86 ohm must be between 0.5",1.5"

[ ] Pins AH4,X4 must be daisy chained

[ ] capacitor site on BCLK must be within 0.5" from socket370

[ ] Number pins on top and bottom of board. Silkscreen.

[ ] Place C86,C87,C88 within 1/2 inch of chip

[ ] Add 4 ground pads below BX in inner ring of balls as shown.

S370_256 Other

[ ] PLL1, PLL2 traces < 0.1 ohm route

S370_256 Power

[ ] VCC_CORE decoupling -- 4.7uF decoupling capacitors must be place within the socket cavity and mounted directly on the primary side of the motherboard. The traces must be as short and wide as possible. Use 1206 package.

[ ] VREF decoupling -- Intel recommends four or more 0.1uF caps in a 0603 package placed near VREF pins within 500 mils.
[ ] VREF decoupling --Make MREF short/wide 24 mils minimum

[ ] For VTT decoupling -- place one Cap near every two R-packs in 603 package and place within 200 mils of RPACK.

440BX Host Interface

[ ] length of HRESET trace from 443BX to BX/CPU/ITP node must be between 0.5",1.5"

[ ] length of trace to 86 ohm must be between 0.5",1.5"

440BX Memory Interface

[ ] Place DCLKWR cap as close to BX as possible

Bus Ratio, Thermal, ITP

[ ] length of HRESET trace from ITP the BX/CPU/ITP node must be between 1.0",3.0"

[ ] Route THERMDP & TERMDN as a differential pair

[ ] Make sure you route the ITP connector right. See page10 for the footprint.

8 Layer Board with the following stackup:

Signal (GTL +VTT)
GND
Signal - GTL
Signal
3.3 (most of the board) / GND (Under the S370 + BX)
Signal - GTL
GND
Signal - GTL - VccCore

Use the same stackup thicknesses as baseboard.

Trace Impedance:55 - 75Ohms. (shoot for 65, lower is better than higher!)
Top/bottom layer should be ½ oz cu, inner layers 1 oz cu

Connector

[ ] HCLK0 = HCLK1 - 0.75" in length. IMPORTANT route HCLK0 and HCLK1 on same layer, don't traverse multiple layers. Place on bottom layer. But keep two signals apart by a spacing of 25 mils. to avoid cross talk.

[ ] G_CLKIN,GCLKO_A+G_CLKOUT, GCLKO_B+G_CLKOUT should all be the same length

GTL Termination

[ ] The trace lengths should be controlled to 1.8" min. and 4.3" max. from socket370 to BX Chipset

[ ] The stub lengths should be controlled to 0.0" min. to 2.0" max from socket 370 to R packs.

[ ] The AGTL+ bus trace width is 5 mil. not greater than 6 mils.

[ ] The edge to edge trace spacing is 12 mils. The ratio of this spacing to the delectric thichness of the layer should be at least 2.

[ ] The minimum spacing can be decreased to 5 mils for escaping the FCPGA/PPGA areas for a length of less than 0.25"

[ ] The AGTL+ signals should be routed on the signal layer next to the ground layer (referenced to ground).

[ ] ***** TEST SIGNALS **** Route 3 AGTL+ signals at the minimum of 1.8" for testing purposes. The 3 signals must be on the BX side. Use these three signals: BNR#, HD4# HA27#.

[ ] ***** TEST SIGNALS **** Route 5 signals next to each other at the maximum of 4.3". This is to test crosstalk. The five signals are: HD29#, HD28#, HD43#, HD37#, HD44#.

Silkscreen

[ ] Flexible Intel(R) 440BX AGPset/PGA370 Processor adapter

Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title	Layout Guidelines	
Size C	Document Number Intel(R) 440BX Scalable Performance Board	Rev A3
Date: Wednesday, April 26, 2000	Sheet 12 of 12	