



Point of Sale Terminal Design Guide

Application Note

May 1998





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1.0 Introduction

The point of sale (POS) terminal is an embedded PC platform with custom features designed for a retail and service environment. The major difference between a POS terminal and a normal PC is that a POS terminal is a cost-effective custom design, with unneeded PC features removed.

More and more industries are switching to POS terminals to replace cash registers, causing the market for POS terminal systems to grow enormously. Because POS terminal systems are usually connected to a network and often require a graphical user interface, high performance POS terminal systems are in demand.

The design described in this document was created to reduce the development cycle for point of sale terminal designers. This design provides a head-start in product development which can result in faster time to market.

Caution: The design has *not* been implemented in hardware. This document is for reference only. Customers are responsible for validating designs created using the information in this document.

1.1 Design Overview

This design is based on the Intel Embedded Processor Module. The processor used in the Embedded Processor Module is either a 133 MHz Intel® Pentium® processor with VRT technology (for the EMBMOD133) or a 166 MHz Intel® Pentium® processor with MMX™ technology (for the EMBMOD166). The EMBMOD133 module is used in this design.

The design closely emulates a PC environment and uses common, standard components. Four serial ports support peripherals, such as barcode scanners, digital scales, card readers and customer price displays. A printer and cash drawer can be connected using the parallel port and a keyboard can be connected using the PS/2 connector provided in the design.

Designers should check for device availability before designing-in any of the components included in the document. This document describes the operation of the POS terminal design from a hardware perspective. BIOS and operating system operation is not discussed. The design has not been implemented in hardware.

This design guide is meant to be used together with the *Intel 430HX PCIset Design Guide* (order number 297467) and *AP-757, Intel Embedded Processor Module Design Guide* (order number 273120). Design issues covered in those documents are not repeated here. See “Related Documents” on page 13 for more information on how to obtain documents referenced in this document. The schematics for this design are provided in Appendix B, “Schematics.” They are also available in OrCAD format from the Intel Developer’s web site at www.intel.com.

1.2 POS Terminal Design Features

Key features of the POS terminal described in this design include:

- Intel Embedded Processor Module (EMBMOD133)
- 4-Mbyte application flash memory
- 64-bit video graphics controller with 2 Mbytes of DRAM
- Four serial ports

- One parallel port
- PCMCIA socket

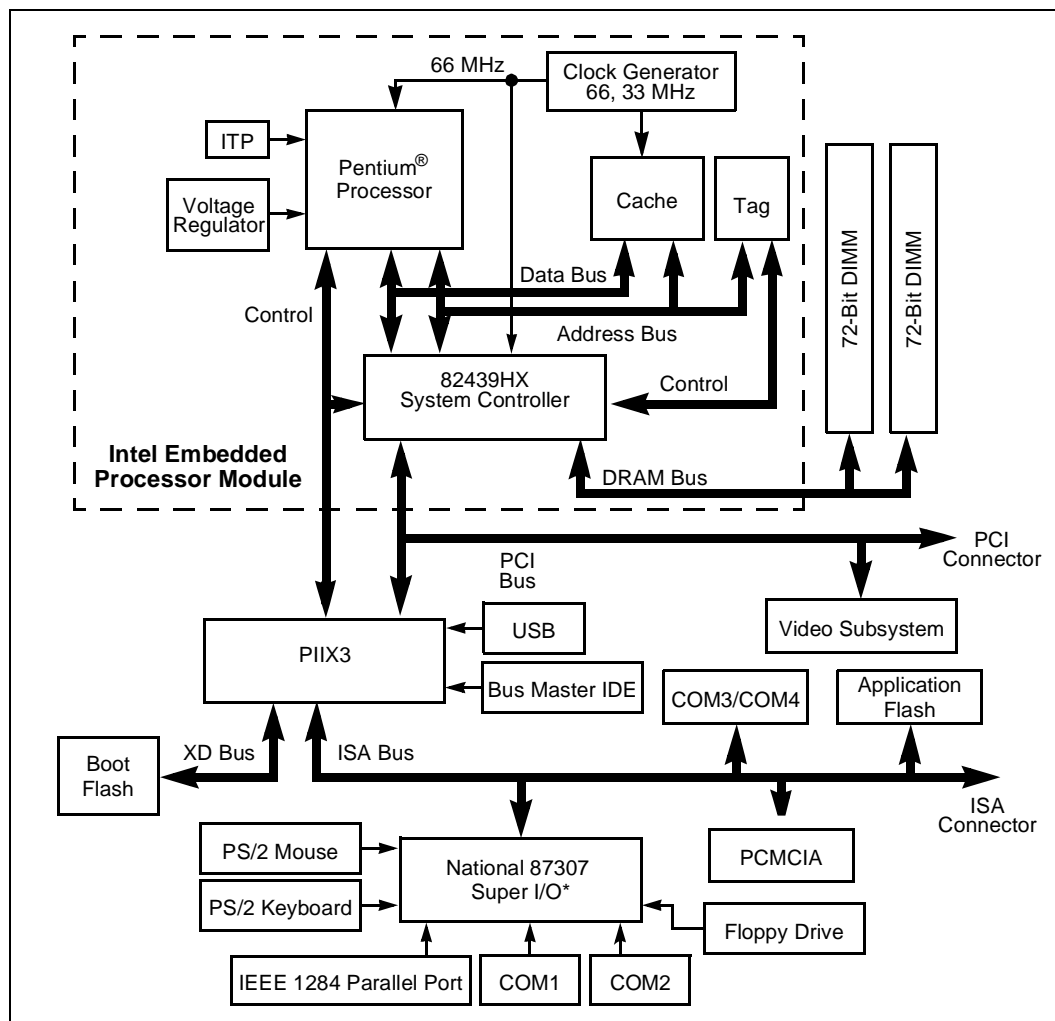
The Intel Embedded Processor Module contains:

- 133 MHz Intel Pentium processor with VRT technology
- 82439HX System Controller
- 256 Kbytes of L2 cache
- Clock generator
- Voltage regulator

2.0 POS Terminal Design Overview

Figure 1 is the block diagram for the POS terminal design.

Figure 1. POS Terminal Design Block Diagram



2.1 Core Components

The core components of this POS terminal design are:

- Intel Embedded Processor Module, EMBMOD133
- Intel 82371SB PCI ISA IDE Xcelerator
- DRAM
- BIOS ROM

2.1.1 Intel Embedded Processor Module EMBMOD133

The Intel Embedded Processor Module EMBMOD133 is a high performance subsystem for use in embedded, industrial and communication applications where flexibility and the ability to upgrade is important.

The Intel Embedded Processor Module contains a Pentium processor, an 82439HX system controller (TXC), a 256 Kbyte L2 cache, a clock generator and a voltage regulator for the Pentium processor, all incorporated in a single board.

2.1.2 Intel 82371SB PCI ISA IDE Xcelerator

The Intel 82371SB is the PCI south bridge. It connects to the Embedded Processor Module via the PCI bus. It integrates many common I/O functions found in ISA-based PC systems:

- Seven-channel DMA controller
- Two 82C59 interrupt controllers
- 8254 timer/counter
- Power management support

2.1.3 Dynamic Random Access Memory (DRAM)

The POS terminal in this design provides two connectors for two 168-pin JEDEC, DRAM DIMM modules. The DRAM DIMMs will either be 3.3 V FPM or 3.3 V EDO type memory. The DIMM will provide a 64-bit or 72-bit interface directly to the Embedded Processor Module.

2.1.4 Flash BIOS

Flash BIOS is used to boot the POS terminal during power-up. The system flash BIOS is a 128 Kbyte, 12 V programmable flash device. The system is set up for in-circuit reprogramming of the BIOS, and the flash device is socketed and writable. This device is addressable on the XD bus extension of the ISA bus. The ROM is controlled by the Intel 82371SB PCI to ISA bridge chip.

2.2 Peripheral components

The peripheral components in this POS terminal design include:

- Video controller
- PS/2 keyboard
- RTC/NVRAM
- Application flash memory
- Four serial ports
- One parallel port
- PCI connector
- ISA connector
- IDE port
- PCMCIA socket
- PS/2 mouse port

This design is modular. Peripherals can be easily removed if they are not required in the final design.

2.2.1 Video Controller

The Cirrus Logic CL-GD7555* Video and Graphics Controller is capable of controlling a CRT, TFT, DSTN or TV display. It connects directly to the 32-bit PCI (v2.1) host bus with a 33 MHz clock rate.

2.2.2 PS/2 Keyboard

Keyboard support is provided by the National Semiconductor 87307 Super I/O* device. The keyboard connectors are PS/2 type.

2.2.3 RTC/NVRAM

The RTC and NVRAM is contained within the National Semiconductor 87307 Super I/O device. CMOS backup is provided by a 3 V battery.

2.2.4 Application Flash Memory

There are 4 Mbytes of application flash memory on the POS terminal motherboard. This flash memory serves as non-volatile memory. The operating system and POS software can be stored in this flash device. To use the application flash as a disk, appropriate software must be installed. To boot from a flash device, changes may be needed in the BIOS or the flash driver software.

The design's application flash memory consists of one Intel 28F320S5 from the Word-Wide FlashFile™ Memory Family. This 16-bit, word-wide FlashFile memory provides high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. Key enhancements include:

- Common Flash Interface (CFI) support
- Scalable Command Set (SCS) support
- S5 technology
- Enhanced suspend capabilities

2.2.5 Serial and Parallel Ports

There are four serial ports in the POS terminal design. COM1 and COM2 are generated and supported by the National Semiconductor 87307 Super I/O device. COM3 and COM4 are generated and controlled by the Exar ST16C452* Dual Asynchronous Receiver/Transmitter.

GD 75232* drivers/receivers from Texas Instruments provide the interface between the UART and the communication ports. This device provides a low-cost solution for this function and allows easy interconnection of the UART and communication ports. It also complies with the requirements of the EIA/TIA-232-E and ITU standards.

The parallel port on the POS terminal design is generated and controlled by the National Semiconductor 87307 Super I/O device. The parallel port uses a DB25 connector.

2.2.6 IDE Port

Two standard IDE interfaces are provided by the 82371SB. One 40-pin IDE connector is included in the design. This allows up to two IDE devices (one master and one slave) to be supported in a single connector.

2.2.7 PCMCIA Interface

The Cirrus Logic CL-PD6720* is used as the host adapter chip to control two PCMCIA sockets. Only one socket is implemented in this design. The chip is fully PCMCIA (v2.1) and JEIDA (v4.1) compliant. The CL-PD6720 provides fully buffered PCMCIA interfaces. No external logic is required for buffering signals to or from the interface. Power consumption can be controlled by limiting signal transitions on the PCMCIA bus.

2.2.8 PS/2 Mouse Port

A PS/2-type mouse port is provided by the National Semiconductor 87307 Super I/O device.

3.0 POS Terminal Design Details

For more information about the POS terminal design, please refer to the schematics located in Appendix B, “Schematics.”

3.1 Intel Embedded Processor Module (EMBMOD133)

The Embedded Processor Module has two connectors and a heat sink for the Pentium processor. The two connectors carry power, clocks, the DRAM memory interface and the 33 MHz PCI interface. 3 V and 5 V power is provided to the Embedded Processor Module. The module generates the core voltage. This core voltage is provided to the POS terminal baseboard for the power-on sequencing circuitry.

For more information, please refer to the *Intel Embedded Processor Module* datasheet (order number 273105) and *AP-757, Embedded Processor Module Design Guide* (order number 273120).

3.2 Intel 82371SB PCI ISA IDE Xcelerator

The Intel 82371SB requests control of the PCI bus by asserting the PHOLD# signal, and becomes the PCI master upon receipt of the PHOLDA# signal from the Embedded Processor Module. The Intel 82371SB contains the PCI and ISA interrupt controller, along with various ISA legacy functions such as a DMA controller, a bus master IDE Interface, an ISA bus interface, an ISA bus clock control, an XD bus control, a USB interface and a BIOS ROM interface.

For more information on the Intel 82371SB PCI ISA IDE Xcelerator, please refer to the *Intel 82371FB (PIIX) and 82371SB (PIIX3) PCI-TO-ISA/IDE Xcelerator* datasheet (order number 290550) and the *Intel 82371SB PCI-TO-ISA/IDE Xcelerator (PIIX3) Timing Specification* (order number 272963).

3.3 PCMCIA Connector

The PCMCIA connector has three main components:

- PCMCIA host adapter (CL-PD6710)
- PCMCIA connector
- Analog power controller circuit

3.3.1 PCMCIA Host Adapter

The Cirrus Logic PCMCIA host adapter (CL-PD6720) is a single chip capable of controlling two PCMCIA sockets. One PCMCIA socket is implemented in the design. The CL-PD6720 is fully compliant with the PCMCIA (v2.1) and JEIDA (v4.1) specifications and is optimized for use in palmtops and laptops, in which the main design objectives are reduced form-factor and low-power consumption. This chip also provides fully buffered PCMCIA interfaces. No external logic is required for buffering signals to or from the interface, and power consumption can be controlled by limiting signal transitions on the PCMCIA bus.

The chip also supports fully mixed voltage operation, a key feature for low power system design and low-power card operation. The core, ISA interface, and the PCMCIA socket interface can all operate independent of each other at either 3.3 V or 5 V.

The design can support either 3.3 V or 5 V operation and can be switched back and forth between 3.3 V and 5 V operation. Automatic voltage sensing has not been implemented in this design; the correct voltage must be set by the driver.

3.3.2 PCMCIA Voltage Control

The Linear Technology (LTC 1472*) switching matrix routes power to both the +5V (VCC) and +12V (VPP) power supply pins on the individual PC Card sockets. The VCC output of the LTC 1472 is switched between three operating states: OFF, 3.3 V and 5 V. The VPP output is switched between four operating states: 0 V, VCC, 12 V and Hi-Z. The VCC output of the LTC 1472 can supply up to 1 A of current and the VPP output up to 120 mA. Both switches have built-in current limiting and thermal shutdown to protect the card, socket, and power supply against accidental short-circuit conditions.

3.4 Serial and Parallel Communications

COM1 and COM2 are generated and supported by the National Semiconductor 87307 Super I/O device. COM3 and COM4 are generated and controlled by the Exar ST16C452 Dual Asynchronous Receiver/Transmitter with Parallel Printer Port device.

COM3 occupies 03E8 - 03EF and COM4 occupies 02E8 - 02EF in the address range. An additional logic decoding circuit decodes COM3 and COM4 on ST15C452. This is performed by the CSA# and CSB# signals on the UART.

The Exar ST16C452 chip is a dual universal asynchronous receiver and transmitter (UART) with a bidirectional Centronics* compatible parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50 Hz to 1.5 MHz.

The ST16C452 on-board status registers indicate the error conditions, type and status of the transfer operation being performed. Additional features include:

- Complete MODEM control capability
- A processor interrupt system that may be software tailored to the user's requirements
- Internal loop-back capability for on-board diagnostic testing

Connection to the LPT1 parallel port is made using a 25-pin female D-sub connector. This is a multi-mode IBM PC/XT*, PC/AT* and PS/2-compatible bidirectional parallel port. Since the ST16C452 does not supply another parallel port in this design, INTP and INTSEL can be "no connect."

The GD75232 driver/receiver from Texas Instruments is used as an interface between the UART and the communication ports. The GD75232 combines three drivers and five receivers in a single chip, which decreases the device count and reduces the board space required. One GD75232 supports one communication port, which makes the design modular.

Clamped diodes are added for port protection. This is an optional item but it ensures that excessive voltage does not cause damage to the GD75232.

3.5 Application Flash

The Intel 28F320S5 flash device from the Word-Wide FlashFile™ memory family operates with 5 V on both V_{CC} and V_{PP} .

The BYTE# pin allows either x8 or x16 read/program to the 28F320S5 flash device. When low, BYTE# selects 8-bit mode, and address A0 selects between the low byte and the high byte. When high, BYTE# enables 16-bit operation, address A1 becomes the lowest order address, and address A0 is not used (don't care).

The 28F320S5 also incorporates a dual chip-enable function with two input pins, CE0# and CE1#. These pins have exactly the same function as the regular chip enable pin, CE#. Both CE0# and CE1# must be active low to enable the device. If either signal becomes inactive, the chip is disabled. Device selection occurs with the falling edge of CE0# or CE1#. The first rising edge of CE0# or CE1# disables the device. For minimum chip designs, CE1# may be tied to ground and system logic may use CE0# as the chip enable input.

Memory holes must be used to address the flash. It can either be at 512 Kbyte – 640 Kbyte (080000H-0A0000H) or between 15 Mbyte and 16 Mbyte (F00000H-FFFFFFH). In this design, a 512-Kbyte window below 16 Mbyte (F80000H-FFFFFFH) is used. General purpose I/O from the National Semiconductor 87307 Super I/O are used to select one of eight pages in the 28F320S5 memory device.

If the application flash is required to act as a disk, suitable drivers should be used.

3.6 Video Controller

The CL-GD7555 Video and Graphics Controller can control a CRT, TFT, DSTN, or TV display. The controller supports mixed voltage operation. Active power management provides power-down control of selected unused internal functional blocks during display. The CL-GD7555 also connects directly to the 32-bit PCI (v2.1) host bus with a 33 MHz clock rate.

The CL-GD7555's V-port allows cost-effective implementation of many multimedia features such as MPEG video playback, TV tuning, video capture and teleconferencing. The chip also supports TFT flat panel displays (up to 1024 x 768 resolution) and color dual-scan STN flat panel displays (up to 800 x 600 resolution).

In this design, the CL-GD7555 is implemented with a 2-Mbyte frame buffer using four 256K x 16 DRAMs. The TFT/DSTN display is not implemented in this design. The CRT controller generates horizontal and vertical signals (HSYNC and VSYNC) for a CRT monitor. It supports up to 1280 x 1024 resolution with 256 colors.

The IDSEL signal is routed to AD13. The INTR signal is connected to PIRQ1.

3.7 Power

Power is supplied to the board through an ATX power connector. ATX power supplies provide 5 V, 3.3 V, +12 V, -5 V and -12 V outputs. All these values are used in the design. When using this power supply there is no need for additional voltage regulators.

4.0 Design Considerations

There should be decoupling capacitors for every schematic page and one bulk capacitor for the entire design. This provides a short between power and ground for high frequency signals and to reduce inductance.

If a part is to be removed from the design, the outputs can be left unconnected but the inputs should be pulled either high or low. Since the TFT/DSTN display is not implemented for this design, connect the video controller power pins to V_{CC} .

5.0 Summary

This design was created to shorten the development cycle for POS terminal designs. It is intended to be implemented on a single board for reduced cost. Peripherals are designed in a modular fashion and can be easily removed for specific applications.

Caution: The design has *not* been implemented in hardware. This document is for reference only. Customers are responsible for validating designs created using the information included in this document.

6.0 Related Documents

Copies of Intel documents that have an order number referenced in this document (see Table 1) may be downloaded from the Intel web site at <http://www.intel.com>. To order printed copies, call 1-800-548-4725.

Table 2 lists documents available from other vendors.

Table 1. Intel Documents

Document Name	Order Number
<i>Intel Embedded Processor Module</i> datasheet	273105
<i>Intel Embedded Processor Module Design Guide</i>	273120
<i>Intel Embedded Processor Module (EMBMOD133) Thermal Design Guide</i>	273143
<i>Pentium® Processor</i> datasheet	241997
<i>Pentium® Processor Family Developer's Manual</i>	241428
<i>Intel Architecture Software Developer's Manual</i> (Vols. 1, 2 and 3)	243190, 243191 and 243192
<i>Intel 430HX PCIset 82439HX System Controller (TXC)</i> datasheet	290551
<i>Intel 430HX PCIset 82439HX System Controller (TXC) Timing Specification</i>	272945
<i>Intel 430HX PCIset Design Guide</i>	297467
<i>82371FB (PIIX) and 82371SB (PIIX3) PCI-TO-ISA/IDE Xcelerator</i> datasheet	290550
<i>82371SB PCI-TO-ISA/IDE Xcelerator (PIIX3) Timing Specification</i>	272963
<i>The Advantages of Using the 82371SB PCI-TO-ISA/IDE Xcelerator (PIIX3) with the Intel 430HX PCIset in Embedded Designs</i>	273009
<i>Intel Word-Wide FlashFile™ Memory 28F320S5</i> datasheet	290609

Table 2. Third Party Vendor Documents

Document Name
<i>National Semiconductor PC87307VUL Super I/O datasheet</i>
<i>Cirrus Logic CL-GD7555 Advance Hardware Reference Manual</i>
<i>Cirrus Logic CL-PD 6720 datasheet</i>
<i>Exar ST16C452 Dual UART with Parallel Printer Port datasheet</i>
<i>Specifications Lattice ispGAL22V10 In-System Programmable E²CMOS PLD Generic Array Logic datasheet</i>
<i>Linear Technology LTC 1472 Protected PCMCIA Vcc and Vpp Switching Matrix datasheet</i>
<i>Texas Instruments GD75232 Multiple RS-232 Drivers and Receivers datasheet</i>

7.0 Contact Information

Intel Corporation
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Santa Clara, CA 95052-9959
Web site: <http://www.national.com>

Cirrus Logic
31000 West Warren Avenue
Fremont, CA 94538
Web site: <http://www.cirrus.com>

EXAR Corporation
48720 Kato Road
Fremont, CA 94538
Web site: <http://www.exar.com>

Siemens Microelectronics, Inc.
10950 North Tantau Avenue
Cupertino, CA 95014
Web site: <http://www.siemens.com>

Texas Instruments Incorporated
P.O. Box 809066
Dallas, TX 75244-9066
Web site: <http://www.ti.com>

Appendix A Bill of Materials

Note: Intel does not guarantee device availability. Designers should check for device availability before designing-in any of the components included in the document.

Table 3. POS Design Guide Bill of Materials (Sheet 1 of 4)

POS Design Guide: Embedded Processor Module Connectors Revised: Wednesday, March 11, 1998			
Revision: 1.00			
The estimated bill of material cost for this design is US\$400, as of 3/20/98.			
Bill Of Materials March 20, 1998 8:19:09			Page1
Item	Quantity	Reference	Part
1	1	BT1	HU 2032-1 SOCKET
2	10	C1, C2, C3, C36, C38, C39, C44, C45, C46, C47	0.001uF
3	37	C4, C24, C32, C33, C34, C35, C37, C48, C65, C73, C74, C85, C86, C112, C113, C124, C125, C149, C150, C151, C213, C214, C215, C216, C230, C231, C232, C233, C237, C242, C267, C268, C288, C289, C290, C291, C292	0.01uF
4	124	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C21, C22, C23, C25, C26, C27, C28, C29, C30, C31, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C64, C66, C67, C68, C70, C71, C72, C76, C77, C79, C80, C82, C83, C84, C88, C89, C91, C92, C93, C94, C95, C96, C100, C101, C103, C104, C106, C107, C109, C110, C111, C115, C116, C118, C119, C121, C122, C123, C128, C143, C144, C145, C146, C147, C148, C161, C162, C163, C164, C165, C166, C167, C168, C169, C207, C208, C209, C210, C211, C212, C225, C226, C227, C228, C229, C235, C236, C240, C241, C244, C247, C253, C260, C261, C262, C266, C269, C270, C272, C274, C277, C280, C282, C283, C285, C293, C294	0.1uF
5	12	C19, C20, C245, C246, C248, C249, C254, C255, C275, C276, C278, C279	100uF
6	27	C40, C41, C42, C43, C69, C75, C78, C81, C87, C90, C99, C102, C105, C108, C114, C117, C120, C141, C142, C202, C203, C221, C222, C256, C263, C264, C271	10uF
7	17	RP1, R1, RP2, R2, RP3, RP4, R6, R8, R16, R23, R30, R31, C62, C63, C97, C126, C127	0
8	1	C98	100pF
9	14	C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C158, C159	10pF
10	25	C152, C153, C154, C155, C156, C157, C172, C173, C174, C175, C177, C178, C179, C180, C184, C185, C186, C187, C188, C189, C190, C191, C250, C251, C252	470pF
11	2	C160, C259	22uF
12	16	C170, C171, C176, C181, C182, C183, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201	220pF
13	12	C204, C205, C206, C217, C223, C224, C234, C239, C258, C265, C284, C287	1uF
14	6	C218, C219, C220, C238, C281, C296	CAP
15	1	C243	.1uF

Table 3. POS Design Guide Bill of Materials (Sheet 2 of 4)

16	1	C257	4.7nF
17	1	C273	1000pF
18	1	C286	220uF
19	1	C295	0.0022uF
20	4	D1, D53, D54, D55	LGS260-DO
21	1	D2	FMMD914
22	40	D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52	D1N916A
23	10	D23, D24, D25, D26, D27, D28, D29, D30, D31, D32	D1N916
24	1	D56	BZX84C2V7
25	1	D57	BZX84C2V4
26	1	D58	1N5817
27	6	FB1, FB2, FB3, FB4, FB5, FB6	BLM41A800S
28	2	FB8, FB7	CB70
29	2	F1, F2	SMD125-002
30	1	JP1	FLOPPY HEADER 17X2
31	1	JP2	1x4
32	1	J1	EPM DRAM Conn 140-Pin
33	1	J2	EPM PCI Conn 120-Pin
34	1	J3	Embedded Processor Module DRAM Conn 140-Pin
35	1	J4	Embedded Processor Module PCI Conn 120-Pin
36	2	J6, J5	Molex 71736-00011
37	1	J7	IDE Conn
38	2	J9, J8	PCI Conn
39	1	J10	ISA Conn A
40	1	J11	ISA Conn B
41	1	J12	PS2 STACK
42	4	J13, J14, J17, J23	1x2
43	3	J15, J24, J25	1x3
44	1	J16	1x1
45	1	J18	SERIAL STACK
46	1	J19	DB25
47	1	J20	CONNECTOR DB15HD
48	1	J21	JUMP3
49	1	J22	ATX POW CONN
50	1	J26	PCMCIA Connector
51	2	L1, L2	INDUCTOR
52	2	P2, P1	DB9
53	2	Q1, Q2	NDS9953A
54	8	R4, RP5, RP6, R7, RP45, RP49, R53, R59	22

Table 3. POS Design Guide Bill of Materials (Sheet 3 of 4)

55	25	R5, RP7, R14, RP17, RP18, RP20, RP21, RP25, RP30, RP32, RP34, RP36, RP38, RP39, RP40, RP41, R46, R47, R48, R49, R50, R51, R55, R77, R78	10K
56	14	RP8, RP9, RP10, RP11, RP12, RP13, R13, RP14, RP15, RP16, RP46, RP47, R68, R69	33
57	20	R10, R11, RP19, RP28, R33, R34, R36, R38, R39, R41, RP42, R42, RP43, R43, RP44, R44, R45, R58, R70, R76	4.7K
58	4	RP22, RP26, R37, R40	330
59	11	RP23, RP24, R25, R26, RP27, R27, R28, RP29, RP31, RP33, R35	2.7K
60	2	RP35, RP37	5.6K
61	8	R3, R18, R19, R29, R32, RP48, R60, R79	1K
62	5	R9, R21, R22, R67, R72	220
63	3	R12, R15, R17	47
64	2	R20, R73	215
65	1	R24	10
66	1	R52	22M
67	1	R54	120K
68	1	R56	8.2K
69	1	R57	20K
70	3	R61, R62, R63	150
71	1	R64	180
72	2	R66, R65	R
73	1	R71	51K
74	1	R74	130
75	1	R75	110
76	1	S1	RESET SWITCH
77	2	TP2, TP1	12MHZ
78	1	TP3	MWE#
79	1	TP4	MRAS2#
80	1	TP5	MRAS0#
81	1	TP6	MCAS0#
82	1	TP7	MCAS1#
83	1	TP8	MCAS2#
84	1	TP9	MCAS3#
85	1	TP10	MCAS4#
86	1	TP11	MCAS5#
87	1	TP12	MCAS6#
88	1	TP13	MCAS7#
89	1	TP14	14MHZ
90	1	TP15	PCLK_PIIIX3
91	1	TP16	24MHZ
92	1	TP17	BIOSCS#
93	1	TP18	PDIAG#
94	1	TP19	SYSCLK

Table 3. POS Design Guide Bill of Materials (Sheet 4 of 4)

95	1	TP20	14MHZ_ISA
96	1	TP21	P12
97	1	TP22	P16
98	1	TP23	P17
99	1	TP24	P20
100	1	TP25	P21
101	1	TP26	X1
102	1	TP27	G10
103	1	TP28	G11
104	1	TP29	G12
105	1	TP30	G13
106	1	TP31	G14
107	1	TP32	G15
108	1	TP33	G16
109	1	TP34	G17
110	1	TP35	G20
111	1	TP36	G21
112	1	TP37	G22
113	1	U1	82371SB (PIIX3)
114	1	U2	74ACT04
115	3	U3, U5, U6	74ALS245
116	1	U4	74HCT14
117	1	U7	74ALS08
118	1	U8	74ALS00
119	1	U9	74ACT05
120	1	U10	PC87307IBU-VUL
121	1	U11	28F001BX-T150
122	4	U12, U13, U27, U29	GD75232SOP
123	1	U14	CL-GD7555
124	4	U15, U16, U17, U18	HYB514171BJ-60
125	1	U19	27C512
126	1	U20	74LS30
127	1	U21	74LS04
128	1	U22	ispGAL22V10
129	1	U23	28F320S5
130	1	U24	74LS08
131	1	U25	74LS260
132	1	U28	ST16C452
133	1	U30	TLC393C
134	1	U31	7404
135	1	U32	CL-PD6720
136	1	U33	LTC1472
137	1	Y1	32.768KHZ

Appendix B BIOS Checklist

This section is a checklist to specify the hardware configuration for a BIOS vendor to customize the BIOS.

Table 4. Hardware Design Specification

Intel 430HX chipset	
Manufacturer	Intel Corporation
Bus	Host
Embedded Processor Module	
Manufacturer	Intel Corporation
Speed	133 MHz
Memory - System	
Configuration	EDO, FPM
Speeds Supported	60, 70
Memory - Cache (External)	
Configuration	256 Kbyte
ROM	
Manufacturer	Intel Corporation
Part #	28F001BX-T150
Size	128 Kbyte
Super I/O	
Manufacture / Part #	National Semiconductor 87307

Table 5. Items connected to Super I/O

IDE	
Floppy	
Serial	
Parallel	
Keyboard Controller	
Real Time Clock	

Table 6. Onboard Peripherals

Onboard Peripherals	Manufacturer and Part Number	Resident Bus	If PCI, specify Vendor/ Device ID	If PCI, specify Dev.# or IDSEL	Option ROM Embedded in BIOS?	Supported IRQs	Address Range
Video	Cirrus Logic CL-GD7555	PCI		AD13	-		
PC Card Controller	Cirrus Logic CL-PD6720	ISA	-	-	-	3, 4, 5, 7, 9, 12, 14 (Programmable)	I/O address: 0000-FFFFH (Programmable) Memory address: 010000-FFFFFFH (Programmable)
UART (Com3, Com4)	Exar ST16C462	ISA				COM3: IRQ4 COM4: IRQ3	I/O address: COM3: 03E8-03EFH COM4: 02E8-02EFH
OTHER							

Table 7. PCI Routing Information

Physical Slot # or Onboard Device	IDSEL # or DEV. #	PCI BUS #	INT or PIRQ pins from the chip set are connected to these INT pins coming from each slot			
			PIRQ 0 or INT A	PIRQ 1 or INT B	PIRQ 2 or INT C	PIRQ 3 or INT D
Slot 0	AD28	0	x		x	
Slot 1	AD29	0		x		x

Table 8. Connectors

Serial
Parallel
PS/2 Mouse
PS/2 Keyboard
Video
Other

Table 9. Software Design Specification – Feature List

USB
Enhanced IDE
PCI v2.1 Spec
PNP Spec
Other

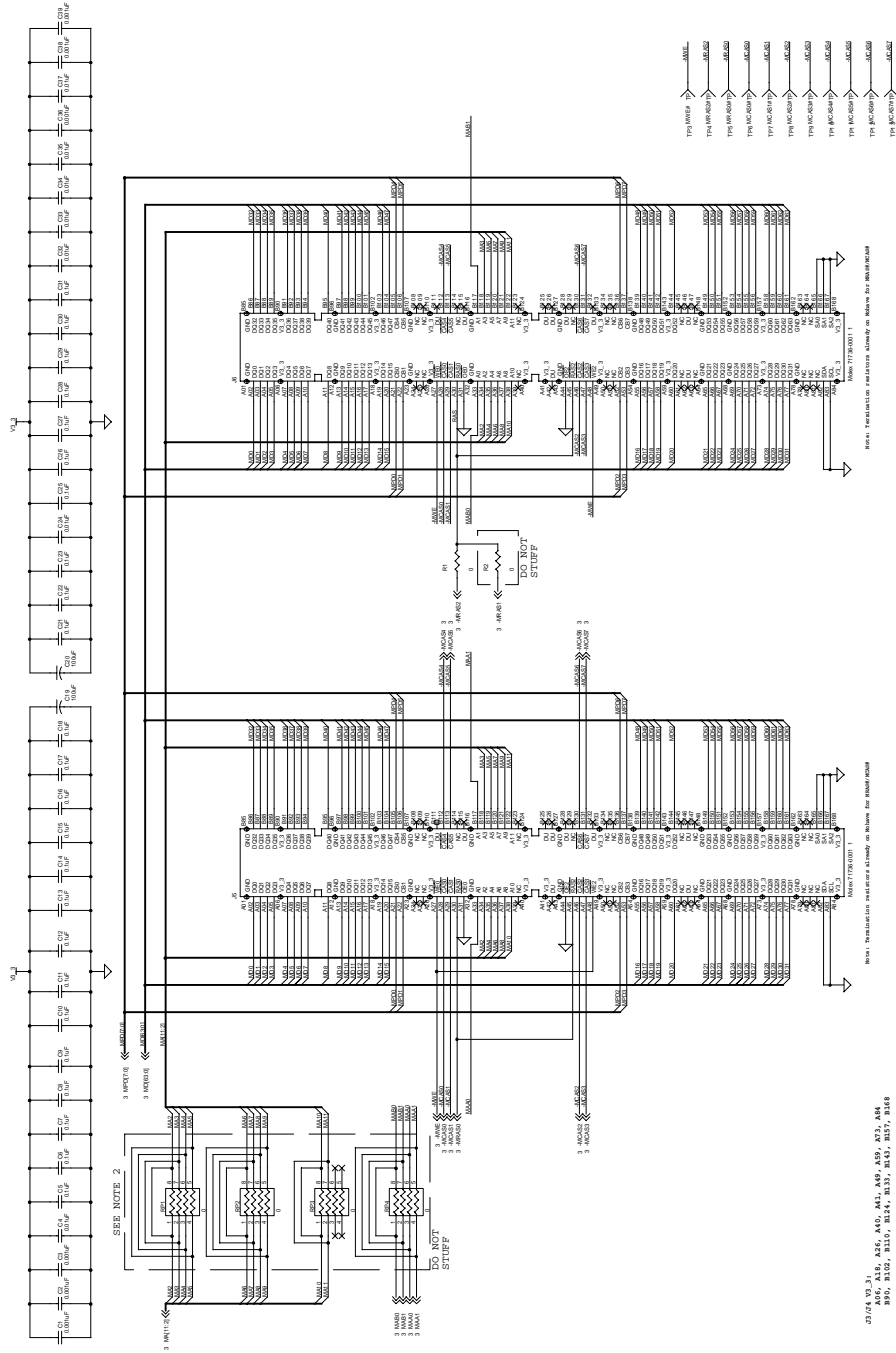
Appendix C Schematics

C.1 POS Terminal Reference Design Schematics

Schematics are provided for the following items:

- Embedded Processor Module Connectors
- DRAM DIMM socket
- 82371SB PCI to ISA Bridge
- ISA interface
- PCI slots 0 and 1
- ISA sockets
- ISA pullup/pulldown
- Super I/O
- Flash BIOS
- I/O connectors
- Video controller
- Video DRAM and VGA BIOS ROM
- PCMCIA connector
- Application flash
- Serial and parallel communications
- Power

DRAM (DIMM) SOCKETS

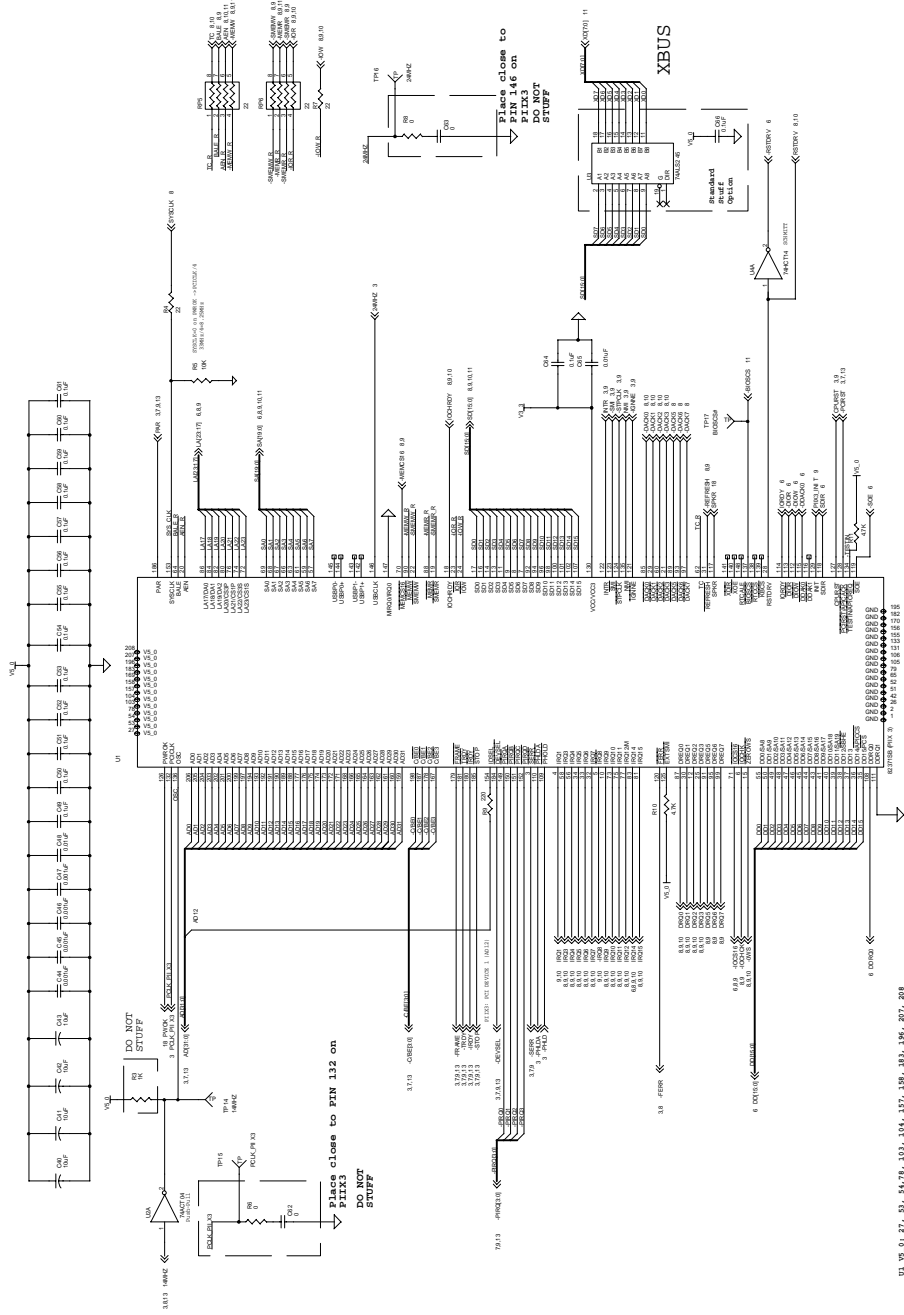


NOTE 1: Place Test Points close to J3/J4 DIMM Connectors
 NOTE 2: Use R-PACK pad geometry. Shunt pads with trace. Route on surface (cuttable)

- 27/24 30 31
- 27/24 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000

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INTEL 82371SB PCI ISA XCELERATOR

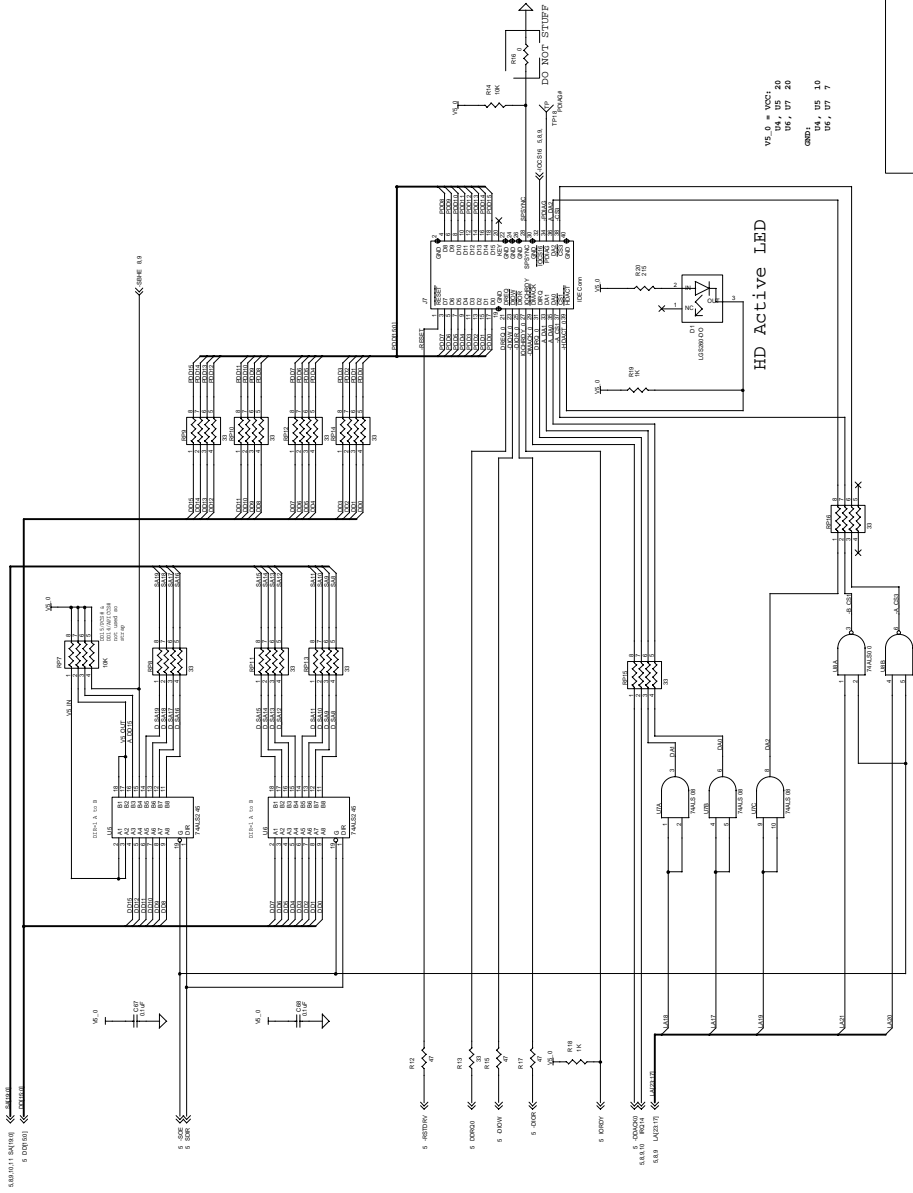


NOTE: 5 mil trace/space gives -70 Ohm Zo for PCI bus as d-stripline

U1 W8.01 21 53 54 78 103 104 137 158 183 196 207 208
 U1 W3.31 130 134
 U1 W8.1 1.2 26 42 51 52 65 79 105 106 131 133 135 136 170 182 185 111 147

Title		POS Design Guide : 82371 SB PCI to ISA Bridge
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IDE Interface



VS 0 = VDD1
 US 4, US 20
 US 7, US 20
 OS 4, US 10
 US 4, US 7

NOTE 1: Cuttable trace RP7 to VS_0

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PCI SLOTS

JPGT V0.0:
 A5, A6, A10, A12, A30, A61, A62 | A1, A3, A4
 A5, A6, A10, A12, A30, A61, A62

JPGT V0.1:
 A13, A15, A16, A19, A20, A21, A22
 A25, A32, A34, A41, A44, A46

JPGT V0.2:
 A7, A11, A14, A19
 A10, A16

JPGT V0.3:
 A17, A18, A23, A24, A25, A27, A28, A29, A31
 A33, A35, A37, A38, A39, A40, A43, A45, A47
 A51, A52, A53, A54, A55, A56, A57, A58

JPGT V1.20: B1
 V1.21: B1
 V1.22: B1
 V1.23: B1
 V1.24: B1
 V1.25: B1

JPGT V1.26: B1
 V1.27: B1

JPGT V1.28: B1
 V1.29: B1

JPGT V1.30: B1
 V1.31: B1

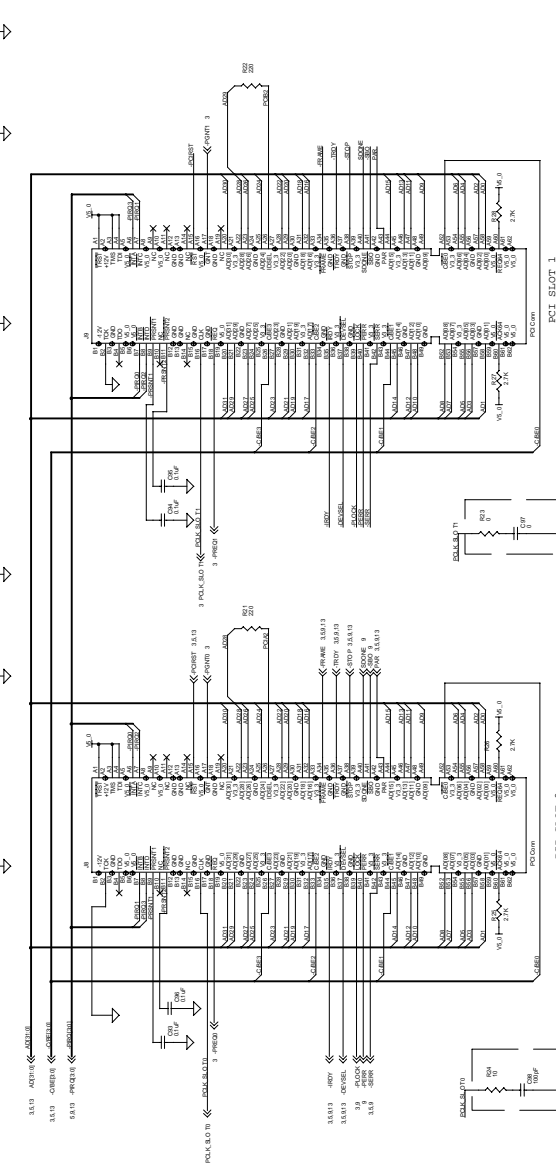
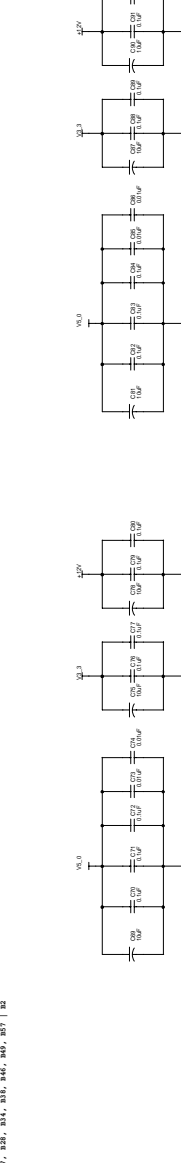
JPGT V1.32: B1
 V1.33: B1

JPGT V1.34: B1
 V1.35: B1

JPGT V1.36: B1
 V1.37: B1

JPGT V1.38: B1
 V1.39: B1

JPGT V1.40: B1
 V1.41: B1

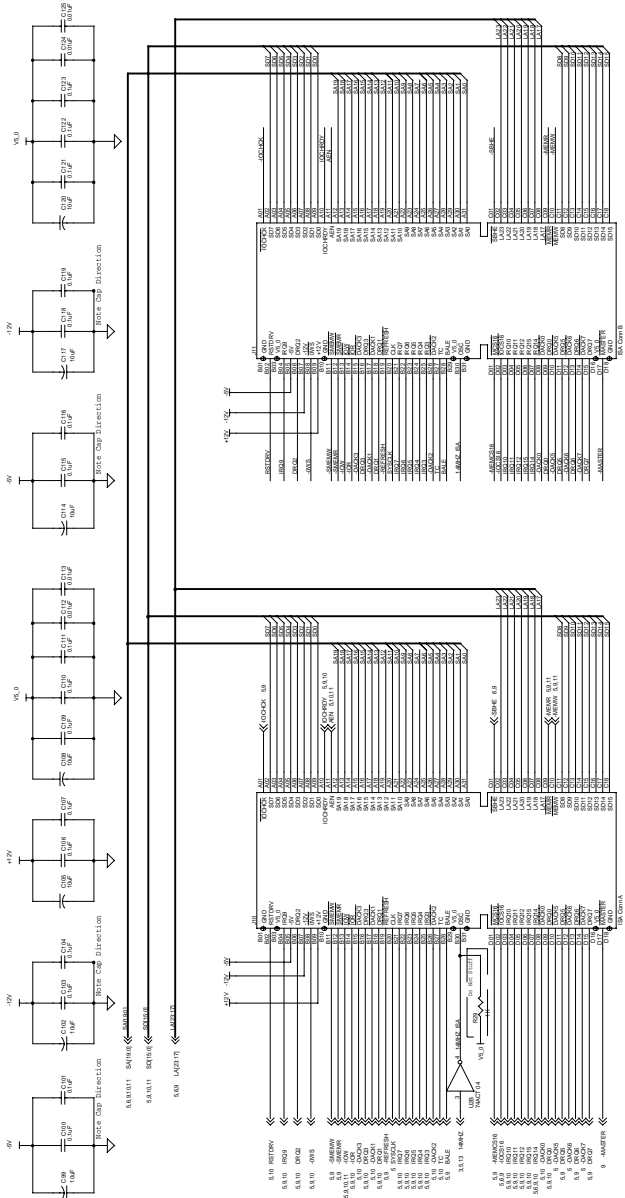


Place close to PCI slot 0
DO NOT STUFF

Place close to PCI slot 1
DO NOT STUFF

Title	POS Design Guide : PCI Slots 0 & 1		
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ISA Slots

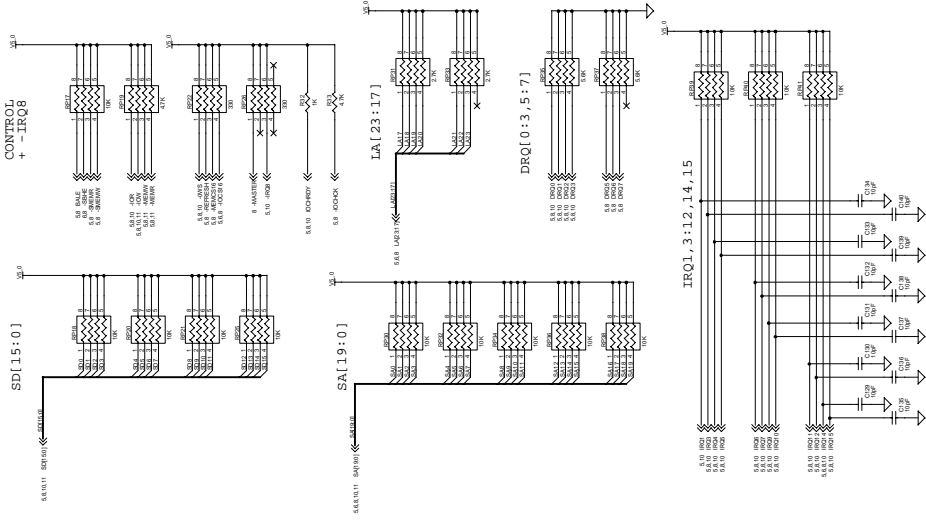


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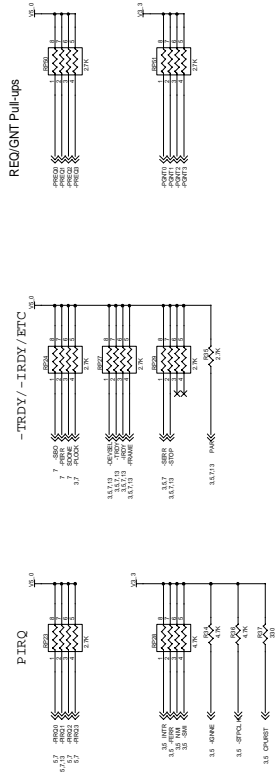
NOTE 1: ISA Conn B is a shared slot with PCI slot 3
 (see ATX spec)

Title		POS Design Guide : ISA Sockets	
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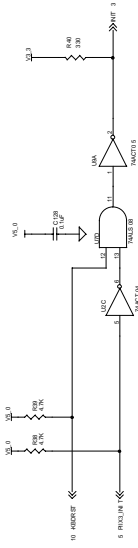
ISA Pullup/Pulldown



PCI Pullup/Pulldown



Note: 64-BIT PCI Strap Off At PCI Connectors
 Note: Pullups on Mohave -PREQ/PENGT[3:0]



Title: POS Design Guide - ISA Pullup/Pulldown

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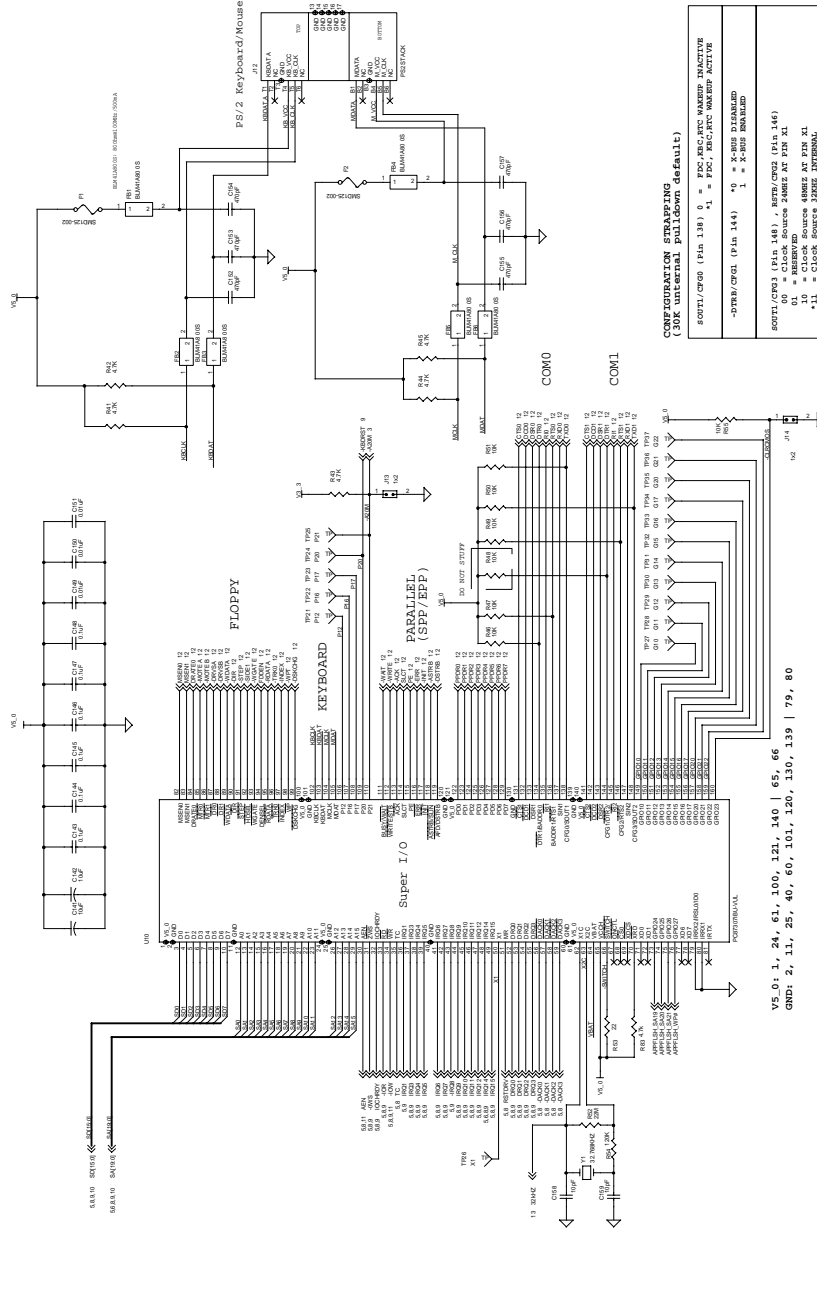
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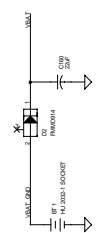
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SUPER I/O



V5.0: 1, 24, 61, 100, 121, 140 | 65, 66
 GND: 2, 11, 25, 40, 60, 101, 120, 130, 139 | 79, 80

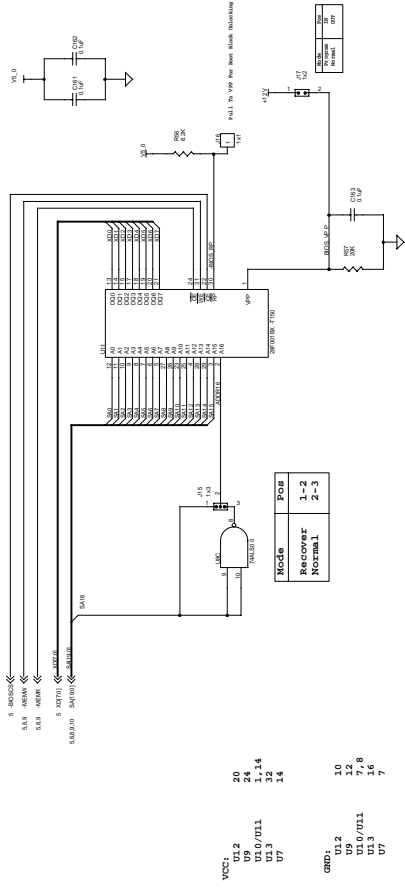


NOTE 1: Place oscillator circuit close to X1C/X2C. Parastic $\leq 8pF$
 NOTE 2: Crystal is parallel, resonant, (N cut) or XY bar, Q=35, C1=9-13pF
 NOTE 3: Test points are a hole/via such that a 25-mil square pin can be inserted.

**COMPONENTS ON SUPER I/O
 (30K internal pullup/default)**

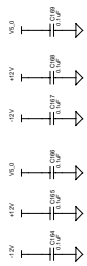
SOPT1/CP00 (Pin 138)	0 = PNP MICROWIRE, 1 = PNP MICROWIRE
-STRM/CV01 (Pin 144)	0 = PNP MICROWIRE, 1 = PNP MICROWIRE ACTIVE
SOPT1/CP03 (Pin 148)	00 = Clock source 2MHz AT PIN X1
SOPT1/CP04 (Pin 149)	10 = Clock source 4MHz AT PIN X1
SOPT1/CP05 (Pin 150)	00 = Clock source 1MHz INTERNAL
SOPT1/CP06 (Pin 151)	00 = Pull up PNP MICROWIRE
SOPT1/CP07 (Pin 152)	00 = Pull up PNP MICROWIRE
SOPT1/CP08 (Pin 153)	00 = Pull up PNP MICROWIRE
SOPT1/CP09 (Pin 154)	00 = Pull up PNP MICROWIRE
SOPT1/CP10 (Pin 155)	00 = Pull up PNP MICROWIRE
SOPT1/CP11 (Pin 156)	00 = Pull up PNP MICROWIRE
SOPT1/CP12 (Pin 157)	00 = Pull up PNP MICROWIRE
SOPT1/CP13 (Pin 158)	00 = Pull up PNP MICROWIRE
SOPT1/CP14 (Pin 159)	00 = Pull up PNP MICROWIRE
SOPT1/CP15 (Pin 160)	00 = Pull up PNP MICROWIRE
SOPT1/CP16 (Pin 161)	00 = Pull up PNP MICROWIRE
SOPT1/CP17 (Pin 162)	00 = Pull up PNP MICROWIRE
SOPT1/CP18 (Pin 163)	00 = Pull up PNP MICROWIRE
SOPT1/CP19 (Pin 164)	00 = Pull up PNP MICROWIRE
SOPT1/CP20 (Pin 165)	00 = Pull up PNP MICROWIRE
SOPT1/CP21 (Pin 166)	00 = Pull up PNP MICROWIRE
SOPT1/CP22 (Pin 167)	00 = Pull up PNP MICROWIRE
SOPT1/CP23 (Pin 168)	00 = Pull up PNP MICROWIRE
SOPT1/CP24 (Pin 169)	00 = Pull up PNP MICROWIRE
SOPT1/CP25 (Pin 170)	00 = Pull up PNP MICROWIRE
SOPT1/CP26 (Pin 171)	00 = Pull up PNP MICROWIRE
SOPT1/CP27 (Pin 172)	00 = Pull up PNP MICROWIRE
SOPT1/CP28 (Pin 173)	00 = Pull up PNP MICROWIRE
SOPT1/CP29 (Pin 174)	00 = Pull up PNP MICROWIRE
SOPT1/CP30 (Pin 175)	00 = Pull up PNP MICROWIRE
SOPT1/CP31 (Pin 176)	00 = Pull up PNP MICROWIRE
SOPT1/CP32 (Pin 177)	00 = Pull up PNP MICROWIRE
SOPT1/CP33 (Pin 178)	00 = Pull up PNP MICROWIRE
SOPT1/CP34 (Pin 179)	00 = Pull up PNP MICROWIRE
SOPT1/CP35 (Pin 180)	00 = Pull up PNP MICROWIRE
SOPT1/CP36 (Pin 181)	00 = Pull up PNP MICROWIRE
SOPT1/CP37 (Pin 182)	00 = Pull up PNP MICROWIRE
SOPT1/CP38 (Pin 183)	00 = Pull up PNP MICROWIRE
SOPT1/CP39 (Pin 184)	00 = Pull up PNP MICROWIRE
SOPT1/CP40 (Pin 185)	00 = Pull up PNP MICROWIRE
SOPT1/CP41 (Pin 186)	00 = Pull up PNP MICROWIRE
SOPT1/CP42 (Pin 187)	00 = Pull up PNP MICROWIRE
SOPT1/CP43 (Pin 188)	00 = Pull up PNP MICROWIRE
SOPT1/CP44 (Pin 189)	00 = Pull up PNP MICROWIRE
SOPT1/CP45 (Pin 190)	00 = Pull up PNP MICROWIRE
SOPT1/CP46 (Pin 191)	00 = Pull up PNP MICROWIRE
SOPT1/CP47 (Pin 192)	00 = Pull up PNP MICROWIRE
SOPT1/CP48 (Pin 193)	00 = Pull up PNP MICROWIRE
SOPT1/CP49 (Pin 194)	00 = Pull up PNP MICROWIRE
SOPT1/CP50 (Pin 195)	00 = Pull up PNP MICROWIRE
SOPT1/CP51 (Pin 196)	00 = Pull up PNP MICROWIRE
SOPT1/CP52 (Pin 197)	00 = Pull up PNP MICROWIRE
SOPT1/CP53 (Pin 198)	00 = Pull up PNP MICROWIRE
SOPT1/CP54 (Pin 199)	00 = Pull up PNP MICROWIRE
SOPT1/CP55 (Pin 200)	00 = Pull up PNP MICROWIRE

BOOT BLOCK FLASH

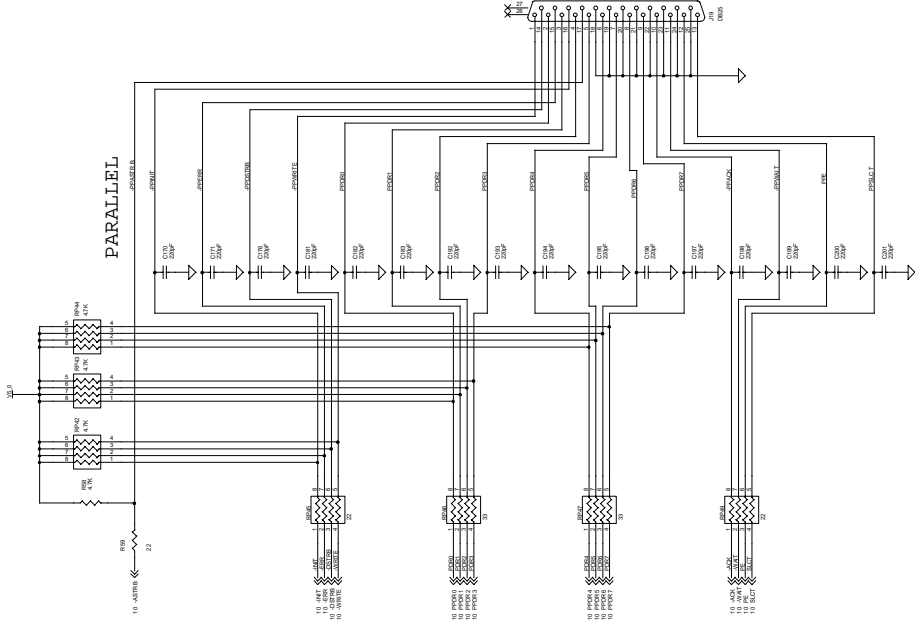
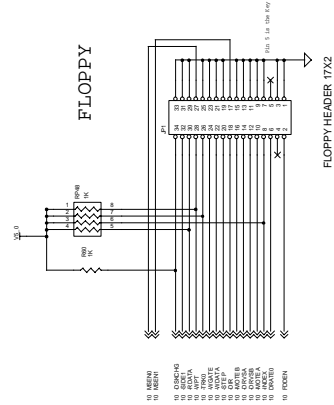
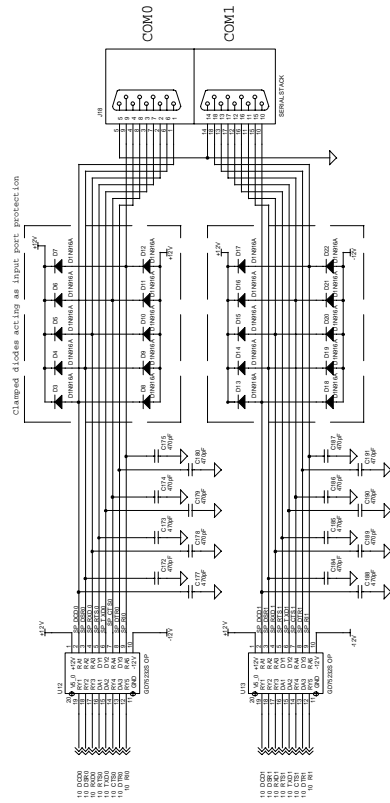


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of	18	

I/O CONNECTORS



COM0 / COM1



Title

POS Design Guide : I/O Connectors

Size

Document Number

A4

(Doc)

Rev

1,00

Date:

Wednesday, May 13, 1998

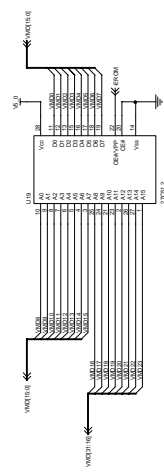
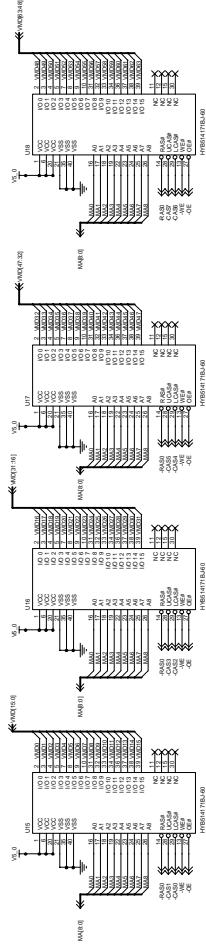
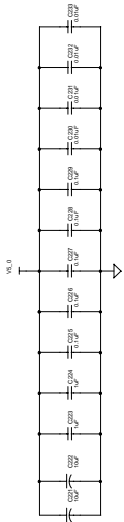
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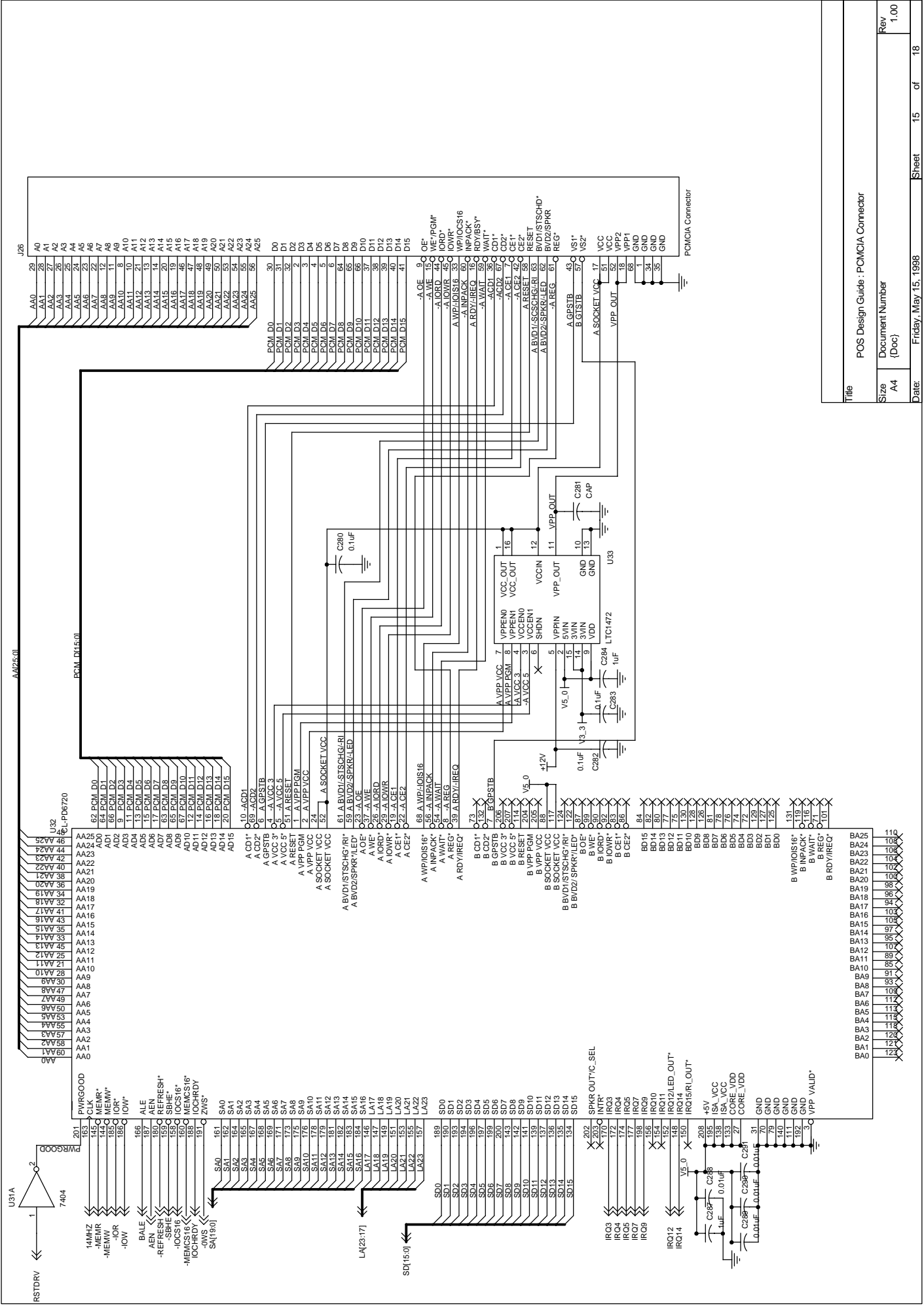
18

VIDEO DRAM



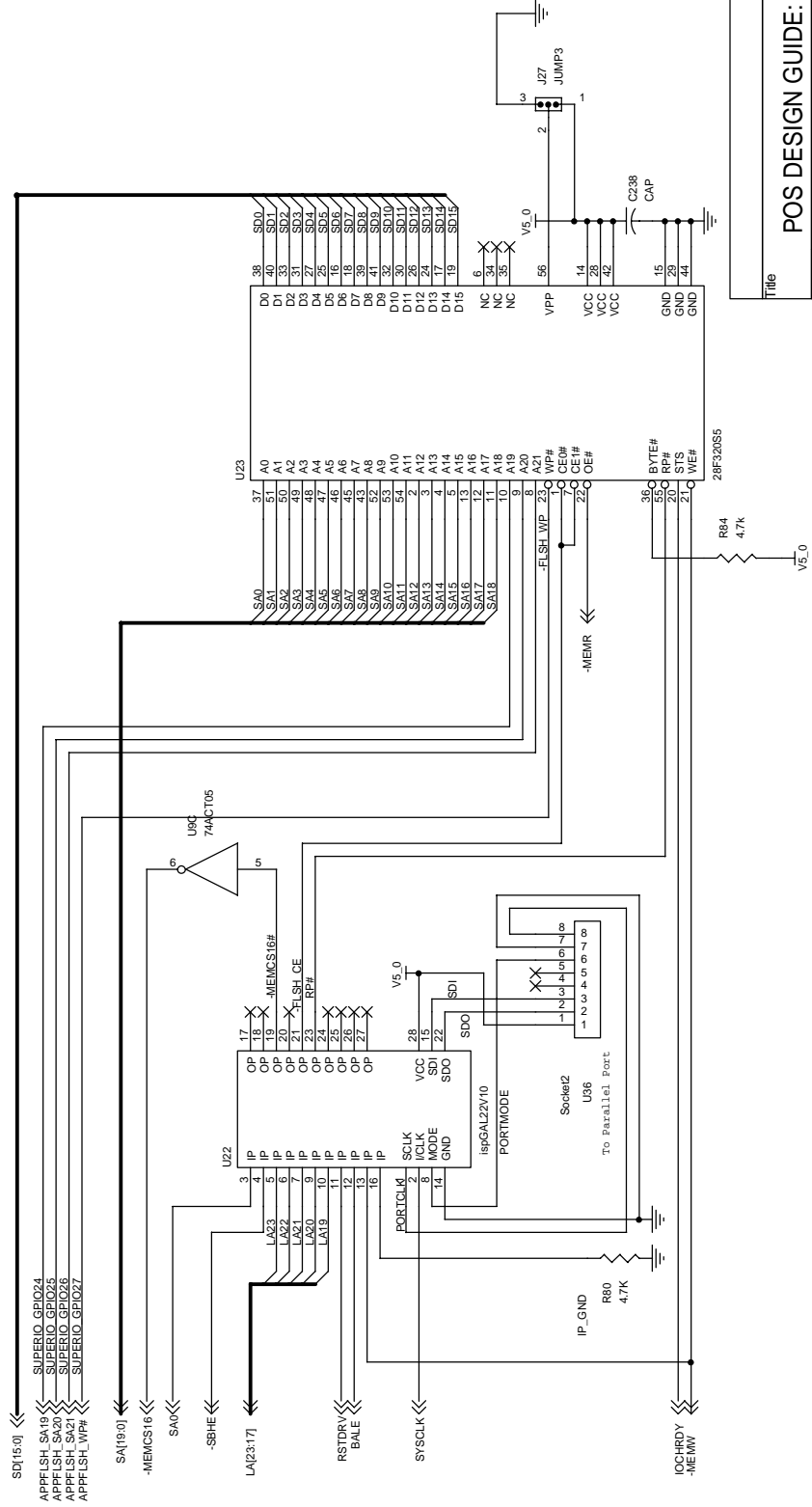
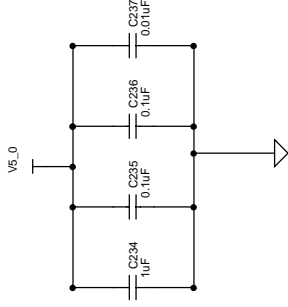
VGA BIOS ROM

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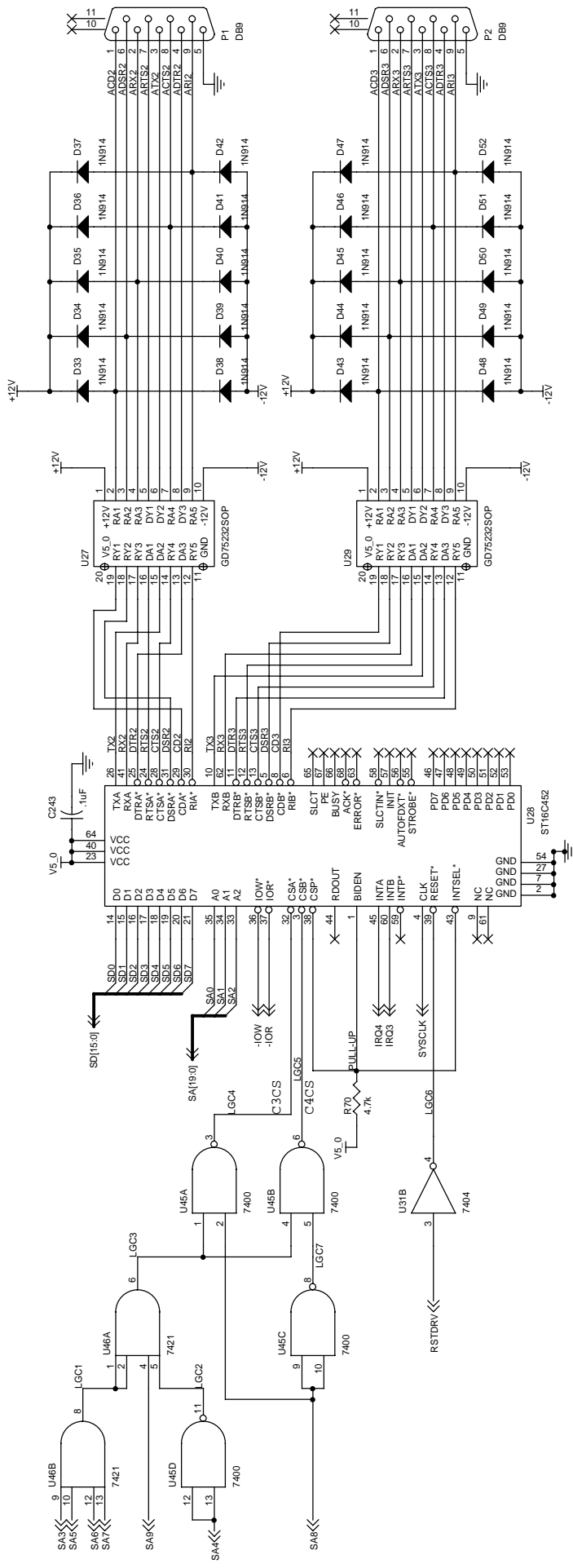
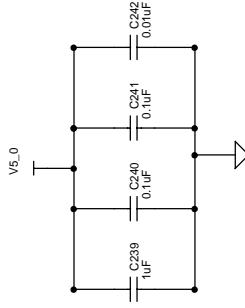
Title		POS Design Guide : PCMCIA Connector
Size	Document Number	
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APPLICATION FLASH



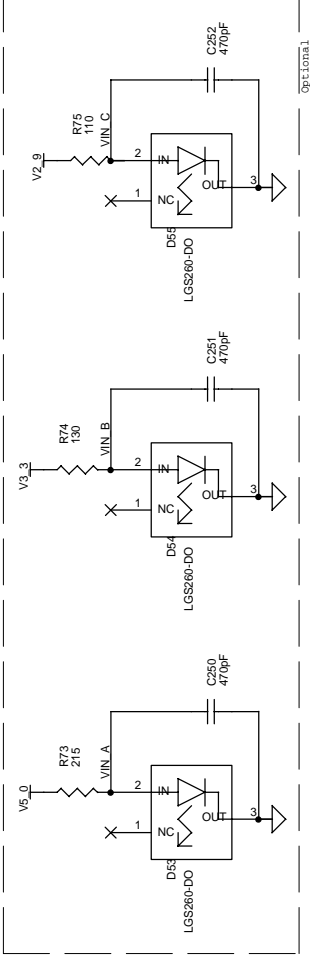
Title		POS DESIGN GUIDE: Application Flash	
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ADDITIONAL COMMUNICATION PORTS

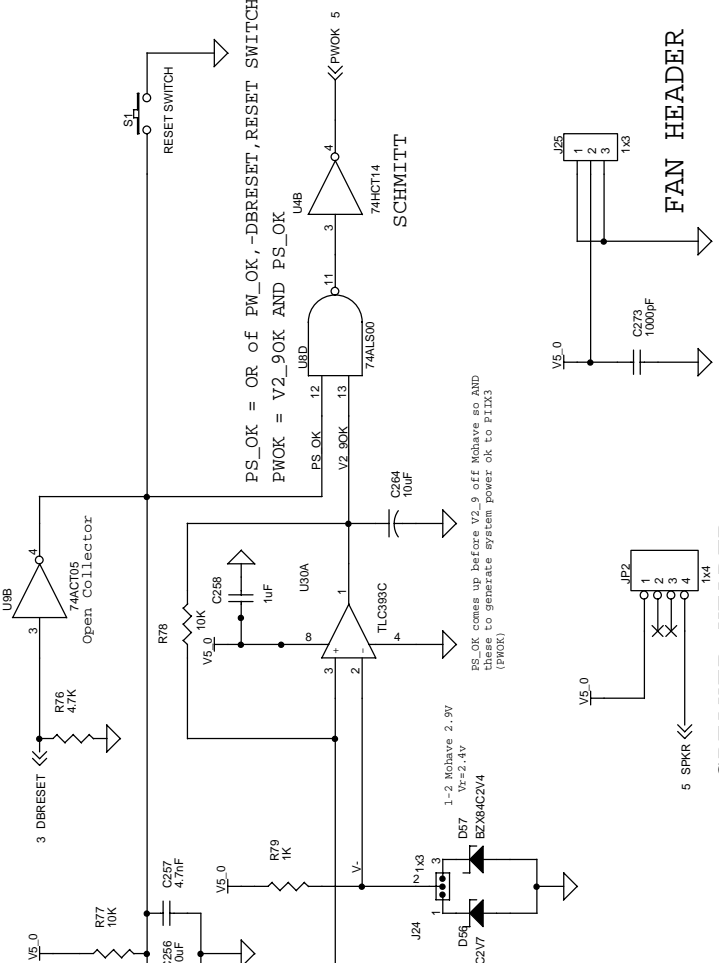


Title		POS Design Guide : Serial communications	
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Power Indicators



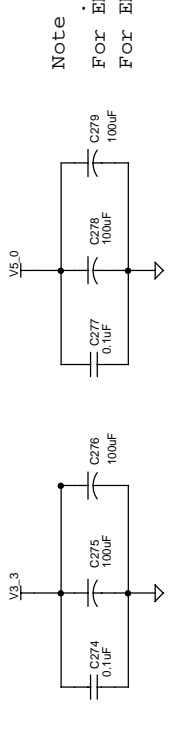
Note: Add screen marking for V5_0 LED, V3_3 LED, V2_9 LED



PS_OK comes up before V2_9 off Mohave so AND gate to generate system power OK to PLL3 (PWOK)

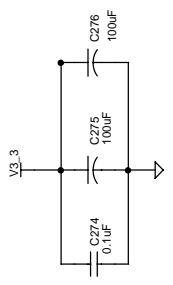
SPEAKER HEADER

Place at ATX Connector

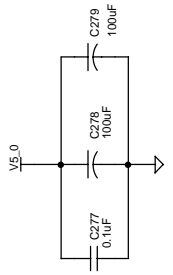


Note :
For EMDMOD133, use D10 which is 2.7V.
For EMBMOD166, use D11 which is 2.3V.

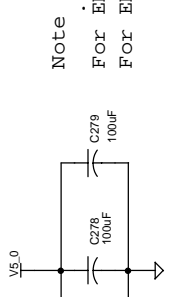
Place at ATX Connector



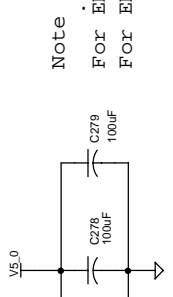
Place at ATX Connector



Place at ATX Connector



Place at ATX Connector



Place at ATX Connector

