Point of Sale Terminal Design Guide

Application Note

May 1998

Order Number: 273170-001

Application Note

Contents

Figures

Tables

1.0 Introduction

The point of sale (POS) terminal is an embedded PC platform with custom features designed for a retail and service environment. The major difference between a POS terminal and a normal PC is that a POS terminal is a cost-effective custom design, with unneeded PC features removed.

More and more industries are switching to POS terminals to replace cash registers, causing the market for POS terminal systems to grow enormously. Because POS terminal systems are usually connected to a network and often require a graphical user interface, high performance POS terminal systems are in demand.

The design described in this document was created to reduce the development cycle for point of sale terminal designers. This design provides a head-start in product development which can result in faster time to market.

Caution: The design has ***not*** been implemented in hardware. This document is for reference only. Customers are responsible for validating designs created using the information in this document.

1.1 Design Overview

This design is based on the Intel Embedded Processor Module. The processor used in the Embedded Processor Module is either a 133 MHz Intel® Pentium® processor with VRT technology (for the EMBMOD133) or a 166 MHz Intel® Pentium® processor with MMX™ technology (for the EMBMOD166). The EMBMOD133 module is used in this design.

The design closely emulates a PC environment and uses common, standard components. Four serial ports support peripherals, such as barcode scanners, digital scales, card readers and customer price displays. A printer and cash drawer can be connected using the parallel port and a keyboard can be connected using the PS/2 connector provided in the design.

Designers should check for device availability before designing-in any of the components included in the document. This document describes the operation of the POS terminal design from a hardware perspective. BIOS and operating system operation is not discussed. The design has not been implemented in hardware.

This design guide is meant to be used together with the *Intel 430HX PCIset Design Guide (*order number 297467*)* and *AP-757, Intel Embedded Processor Module Design Guide* (order number 273120). Design issues covered in those documents are not repeated here. See “Related Documents” on page 13 for more information on how to obtain documents referenced in this document. The schematics for this design are provided in Appendix B, “Schematics.” They are also available in OrCAD format from the Intel Developer’s web site at www.intel.com.

1.2 POS Terminal Design Features

Key features of the POS terminal described in this design include:

- Intel Embedded Processor Module (EMBMOD133)
- 4-Mbyte application flash memory
- 64-bit video graphics controller with 2 Mbytes of DRAM
- Four serial ports

- One parallel port
- PCMCIA socket

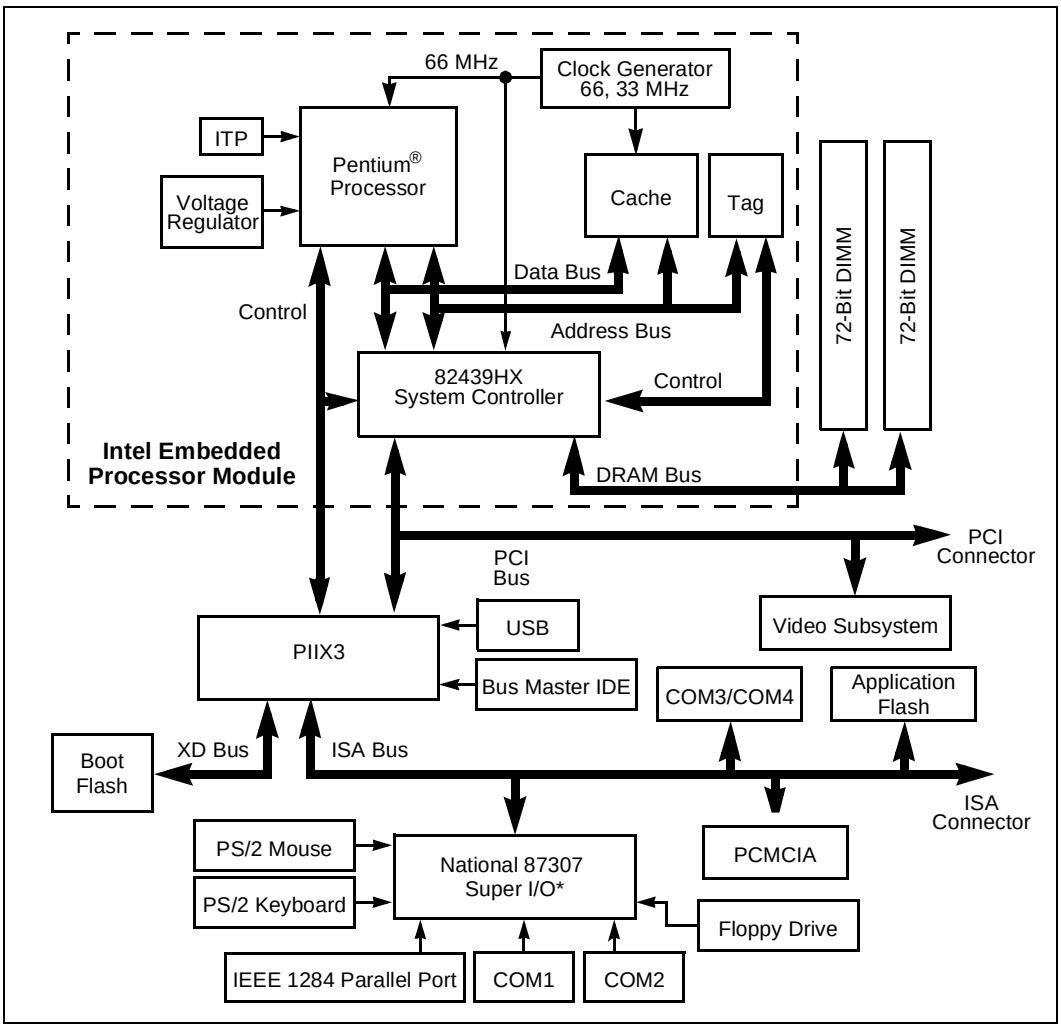
The Intel Embedded Processor Module contains:

- 133 MHz Intel Pentium processor with VRT technology
- 82439HX System Controller
- 256 Kbytes of L2 cache
- Clock generator
- Voltage regulator

2.0 POS Terminal Design Overview

Figure 1 is the block diagram for the POS terminal design.

Figure 1. POS Terminal Design Block Diagram



2.1 Core Components

The core components of this POS terminal design are:

- Intel Embedded Processor Module, EMBMOD133
- Intel 82371SB PCI ISA IDE Xcelerator
- DRAM
- BIOS ROM

2.1.1 Intel Embedded Processor Module EMBMOD133

The Intel Embedded Processor Module EMBMOD133 is a high performance subsystem for use in embedded, industrial and communication applications where flexibility and the ability to upgrade is important.

The Intel Embedded Processor Module contains a Pentium processor, an 82439HX system controller (TXC), a 256 Kbyte L2 cache, a clock generator and a voltage regulator for the Pentium processor, all incorporated in a single board.

2.1.2 Intel 82371SB PCI ISA IDE Xcelerator

The Intel 82371SB is the PCI south bridge. It connects to the Embedded Processor Module via the PCI bus. It integrates many common I/O functions found in ISA-based PC systems:

- Seven-channel DMA controller
- Two 82C59 interrupt controllers
- 8254 timer/counter
- Power management support

2.1.3 Dynamic Random Access Memory (DRAM)

The POS terminal in this design provides two connectors for two 168-pin JEDEC, DRAM DIMM modules. The DRAM DIMMs will either be 3.3 V FPM or 3.3 V EDO type memory. The DIMM will provide a 64-bit or 72-bit interface directly to the Embedded Processor Module.

2.1.4 Flash BIOS

Flash BIOS is used to boot the POS terminal during power-up. The system flash BIOS is a 128 Kbyte, 12 V programmable flash device. The system is set up for in-circuit reprogramming of the BIOS, and the flash device is socketed and writable. This device is addressable on the XD bus extension of the ISA bus. The ROM is controlled by the Intel 82371SB PCI to ISA bridge chip.

2.2 Peripheral components

The peripheral components in this POS terminal design include:

- Video controller
- PS/2 keyboard
- RTC/NVRAM
- Application flash memory
- Four serial ports
- One parallel port
- PCI connector
- ISA connector
- IDE port
- PCMCIA socket
- PS/2 mouse port

This design is modular. Peripherals can be easily removed if they are not required in the final design.

2.2.1 Video Controller

The Cirrus Logic CL-GD7555* Video and Graphics Controller is capable of controlling a CRT, TFT, DSTN or TV display. It connects directly to the 32-bit PCI (v2.1) host bus with a 33 MHz clock rate.

2.2.2 PS/2 Keyboard

Keyboard support is provided by the National Semiconductor 87307 Super I/O* device. The keyboard connectors are PS/2 type.

2.2.3 RTC/NVRAM

The RTC and NVRAM is contained within the National Semiconductor 87307 Super I/O device. CMOS backup is provided by a 3 V battery.

2.2.4 Application Flash Memory

There are 4 Mbytes of application flash memory on the POS terminal motherboard. This flash memory serves as non-volatile memory. The operating system and POS software can be stored in this flash device. To use the application flash as a disk, appropriate software must be installed. To boot from a flash device, changes may be needed in the BIOS or the flash driver software.

The design's application flash memory consists of one Intel 28F320S5 from the Word-Wide FlashFile™ Memory Family. This 16-bit, word-wide FlashFile memory provides high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. Key enhancements include:

- Common Flash Interface (CFI) support
- Scalable Command Set (SCS) support
- S5 technology
- Enhanced suspend capabilities

2.2.5 Serial and Parallel Ports

There are four serial ports in the POS terminal design. COM1 and COM2 are generated and supported by the National Semiconductor 87307 Super I/O device. COM3 and COM4 are generated and controlled by the Exar ST16C452* Dual Asynchronous Receiver/Transmitter.

GD 75232* drivers/receivers from Texas Instruments provide the interface between the UART and the communication ports. This device provides a low-cost solution for this function and allows easy interconnection of the UART and communication ports. It also complies with the requirements of the EIA/TIA-232-E and ITU standards.

The parallel port on the POS terminal design is generated and controlled by the National Semiconductor 87307 Super I/O device. The parallel port uses a DB25 connector.

2.2.6 IDE Port

Two standard IDE interfaces are provided by the 82371SB. One 40-pin IDE connector is included in the design. This allows up to two IDE devices (one master and one slave) to be supported in a single connector.

2.2.7 PCMCIA Interface

The Cirrus Logic CL-PD6720* is used as the host adapter chip to control two PCMCIA sockets. Only one socket is implemented in this design. The chip is fully PCMCIA (v2.1) and JEIDA (v4.1) compliant. The CL-PD6720 provides fully buffered PCMCIA interfaces. No external logic is required for buffering signals to or from the interface. Power consumption can be controlled by limiting signal transitions on the PCMCIA bus.

2.2.8 PS/2 Mouse Port

A PS/2-type mouse port is provided by the National Semiconductor 87307 Super I/O device.

3.0 POS Terminal Design Details

For more information about the POS terminal design, please refer to the schematics located in Appendix B, “Schematics.”

3.1 Intel Embedded Processor Module (EMBMOD133)

The Embedded Processor Module has two connectors and a heat sink for the Pentium processor. The two connectors carry power, clocks, the DRAM memory interface and the 33 MHz PCI interface. 3 V and 5 V power is provided to the Embedded Processor Module. The module generates the core voltage. This core voltage is provided to the POS terminal baseboard for the power-on sequencing circuitry.

For more information, please refer to the *Intel Embedded Processor Module* datasheet (order number 273105) and *AP-757, Embedded Processor Module Design Guide* (order number 273120).

3.2 Intel 82371SB PCI ISA IDE Xcelerator

The Intel 82371SB requests control of the PCI bus by asserting the PHOLD# signal, and becomes the PCI master upon receipt of the PHOLDA# signal from the Embedded Processor Module. The Intel 82371SB contains the PCI and ISA interrupt controller, along with various ISA legacy functions such as a DMA controller, a bus master IDE Interface, an ISA bus interface, an ISA bus clock control, an XD bus control, a USB interface and a BIOS ROM interface.

For more information on the Intel 82371SB PCI ISA IDE Xcelerator, please refer to the *Intel 82371FB (PIIX) and 82371SB (PIIX3) PCI-TO-ISA/IDE Xcelerator* datasheet (order number 290550) and the *Intel 82371SB PCI-TO-ISA/IDE Xcelerator (PIIX3) Timing Specification* (order number 272963).

3.3 PCMCIA Connector

The PCMCIA connector has three main components:

- PCMCIA host adapter (CL-PD6710)
- PCMCIA connector
- Analog power controller circuit

3.3.1 PCMCIA Host Adapter

The Cirrus Logic PCMCIA host adapter (CL-PD6720) is a single chip capable of controlling two PCMCIA sockets. One PCMCIA socket is implemented in the design. The CL-PD6720 is fully compliant with the PCMCIA (v2.1) and JEIDA (v4.1) specifications and is optimized for use in palmtops and laptops, in which the main design objectives are reduced form-factor and low-power consumption. This chip also provides fully buffered PCMCIA interfaces. No external logic is required for buffering signals to or from the interface, and power consumption can be controlled by limiting signal transitions on the PCMCIA bus.

The chip also supports fully mixed voltage operation, a key feature for low power system design and low-power card operation. The core, ISA interface, and the PCMCIA socket interface can all operate independent of each other at either 3.3 V or 5 V.

The design can support either 3.3 V or 5 V operation and can be switched back and forth between 3.3 V and 5 V operation. Automatic voltage sensing has not been implemented in this design; the correct voltage must be set by the driver.

3.3.2 PCMCIA Voltage Control

The Linear Technology (LTC 1472*) switching matrix routes power to both the +5V (VCC) and +12V (VPP) power supply pins on the individual PC Card sockets. The VCC output of the LTC 1472 is switched between three operating states: OFF, 3.3 V and 5 V. The VPP output is switched between four operating states: 0 V, VCC, 12 V and Hi-Z. The VCC output of the LTC 1472 can supply up to 1 A of current and the VPP output up to 120 mA. Both switches have built-in current limiting and thermal shutdown to protect the card, socket, and power supply against accidental short-circuit conditions.

3.4 Serial and Parallel Communications

COM1 and COM2 are generated and supported by the National Semiconductor 87307 Super I/O device. COM3 and COM4 are generated and controlled by the Exar ST16C452 Dual Asynchronous Receiver/Transmitter with Parallel Printer Port device.

COM3 occupies 03E8 - 03EF and COM4 occupies 02E8 - 02EF in the address range. An additional logic decoding circuit decodes COM3 and COM4 on ST15C452. This is performed by the CSA# and CSB# signals on the UART.

The Exar ST16C452 chip is a dual universal asynchronous receiver and transmitter (UART) with a bidirectional Centronics* compatible parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50 Hz to 1.5 MHz.

The ST16C452 on-board status registers indicate the error conditions, type and status of the transfer operation being performed. Additional features include:

- Complete MODEM control capability
- A processor interrupt system that may be software tailored to the user’s requirements
- Internal loop-back capability for on-board diagnostic testing

Connection to the LPT1 parallel port is made using a 25-pin female D-sub connector. This is a multi-mode IBM PC/XT*, PC/AT* and PS/2-compatible bidirectional parallel port. Since the ST16C452 does not supply another parallel port in this design, INTP and INTSEL can be “no connect.”

The GD75232 driver/receiver from Texas Instruments is used as an interface between the UART and the communication ports. The GD75232 combines three drivers and five receivers in a single chip, which decreases the device count and reduces the board space required. One GD75232 supports one communication port, which makes the design modular.

Clamped diodes are added for port protection. This is an optional item but it ensures that excessive voltage does not cause damage to the GD75232.

3.5 Application Flash

The Intel 28F320S5 flash device from the Word-Wide FlashFile™ memory family operates with 5 V on both V_{CC} and V_{PP}.

The BYTE# pin allows either x8 or x16 read/program to the 28F320S5 flash device. When low, BYTE# selects 8-bit mode, and address A0 selects between the low byte and the high byte. When high, BYTE# enables 16-bit operation, address A1 becomes the lowest order address, and address A0 is not used (don't care).

The 28F320S5 also incorporates a dual chip-enable function with two input pins, CE0# and CE1#. These pins have exactly the same function as the regular chip enable pin, CE#. Both CE0# and CE1# must be active low to enable the device. If either signal becomes inactive, the chip is disabled. Device selection occurs with the falling edge of CE0# or CE1#. The first rising edge of CE0# of CE1# disables the device. For minimum chip designs, CE1# may be tied to ground and system logic may use CE0# as the chip enable input.

Memory holes must be used to address the flash. It can either be at 512 Kbyte – 640 Kbyte (080000H-0A0000H) or between 15 Mbyte and 16 Mbyte (F00000H-FFFFFFH). In this design, a 512-Kbyte window below 16 Mbyte (F80000H-FFFFFFH) is used. General purpose I/O from the National Semiconductor 87307 Super I/O are used to select one of eight pages in the 28F320S5 memory device.

If the application flash is required to act as a disk, suitable drivers should be used.

3.6 Video Controller

The CL-GD7555 Video and Graphics Controller can control a CRT, TFT, DSTN, or TV display. The controller supports mixed voltage operation. Active power management provides power-down control of selected unused internal functional blocks during display. The CL-GD7555 also connects directly to the 32-bit PCI (v2.1) host bus with a 33 MHz clock rate.

The CL-GD7555's V-port allows cost-effective implementation of many multimedia features such as MPEG video playback, TV tuning, video capture and teleconferencing. The chip also supports TFT flat panel displays (up to 1024 x 768 resolution) and color dual-scan STN flat panel displays (up to 800 x 600 resolution).

In this design, the CL-GD7555 is implemented with a 2-Mbyte frame buffer using four 256K x 16 DRAMs. The TFT/DSTN display is not implemented in this design. The CRT controller generates horizontal and vertical signals (HSYNC and VSYNC) for a CRT monitor. It supports up to 1280 x 1024 resolution with 256 colors.

The IDSEL signal is routed to AD13. The INTR signal is connected to PIRQ1.

3.7 Power

Power is supplied to the board through an ATX power connector. ATX power supplies provide 5 V, 3.3 V, +12 V, -5 V and -12 V outputs. All these values are used in the design. When using this power supply there is no need for additional voltage regulators.

4.0 Design Considerations

There should be decoupling capacitors for every schematic page and one bulk capacitor for the entire design. This provides a short between power and ground for high frequency signals and to reduce inductance.

If a part is to be removed from the design, the outputs can be left unconnected but the inputs should be pulled either high or low. Since the TFT/DSTN display is not implemented for this design, connect the video controller power pins to V_{CC}.

5.0 Summary

This design was created to shorten the development cycle for POS terminal designs. It is intended to be implemented on a single board for reduced cost. Peripherals are designed in a modular fashion and can be easily removed for specific applications.

Caution: The design has ***not*** been implemented in hardware. This document is for reference only. Customers are responsible for validating designs created using the information included in this document.

6.0 Related Documents

Copies of Intel documents that have an order number referenced in this document (see Table 1) may be downloaded from the Intel web site at http://www.intel.com. To order printed copies, call 1-800-548-4725.

Table 2 lists documents available from other vendors.

Table 1. Intel Documents

Document Name	Order Number
Intel Embedded Processor Module datasheet	273105
Intel Embedded Processor Module Design Guide	273120
Intel Embedded Processor Module (EMBMOD133) Thermal Design Guide	273143
Pentium® Processor datasheet	241997
Pentium® Processor Family Developer's Manual	241428
Intel Architecture Software Developer's Manual (Vols. 1, 2 and 3)	243190, 243191 and 243192
Intel 430HX PCIset 82439HX System Controller (TXC) datasheet	290551
Intel 430HX PCIset 82439HX System Controller (TXC) Timing Specification	272945
Intel 430HX PCIset Design Guide	297467
82371FB (PIIX) and 82371SB (PIIX3) PCI-TO-ISA/IDE Xcelerator datasheet	290550
82371SB PCI-TO-ISA/IDE Xcelerator (PIIX3) Timing Specification	272963
The Advantages of Using the 82371SB PCI-TO-ISA/IDE Xcelerator (PIIX3) with the Intel 430HX PCIset in Embedded Designs	273009
Intel Word-Wide FlashFile™ Memory 28F320S5 datasheet	290609

Table 2. Third Party Vendor Documents

Document Name
National Semiconductor PC87307VUL Super I/O datasheet
Cirrus Logic CL-GD7555 Advance Hardware Reference Manual
Cirrus Logic CL-PD 6720 datasheet
Exar ST16C452 Dual UART with Parallel Printer Port datasheet
Specifications Lattice ispGAL22V10 In-System Programmable E^2CMOS PLD Generic Array Logic datasheet
Linear Technology LTC 1472 Protected PCMCIA Vcc and Vpp Switching Matrix datasheet
Texas Instruments GD75232 Multiple RS-232 Drivers and Receivers datasheet

7.0 Contact Information

Intel Corporation
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
Web site: http://www.intel.com

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-9959
Web site: http://www.national.com

Cirrus Logic
31000 West Warren Avenue
Fremont, CA 94538
Web site: http://www.cirrus.com

EXAR Corporation
48720 Kato Road
Fremont, CA 94538
Web site: http://www.exar.com

Siemens Microelectronics, Inc.
10950 North Tantau Avenue
Cupertino, CA 95014
Web site: http://www.siemens.com

Texas Instruments Incorporated
P.O. Box 809066
Dallas, TX 75244-9066
Web site: http://www.ti.com

Appendix A Bill of Materials

Note: Intel does not guarantee device availability. Designers should check for device availability before designing-in any of the components included in the document.

Table 3. POS Design Guide Bill of Materials (Sheet 1 of 4)

POS Design Guide: Embedded Processor Module Connectors Revised: Wednesday, March 11, 1998			
Revision: 1.00			
The estimated bill of material cost for this design is US$400, as of 3/20/98.			
Bill Of Materials March 20,1998 8:19:09			Page1
Item	**Quantity**	**Reference**	**Part**
1	1	BT1	HU 2032-1 SOCKET
2	10	C1, C2, C3, C36, C38, C39, C44, C45, C46, C47	0.001uF
3	37	C4, C24, C32, C33, C34, C35, C37, C48, C65, C73, C74, C85, C86, C112, C113, C124, C125, C149, C150, C151, C213, C214, C215, C216, C230, C231, C232, C233, C237, C242, C267, C268, C288, C289, C290, C291, C292	0.01uF
4	124	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C21, C22, C23, C25, C26, C27, C28, C29, C30, C31, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C64, C66, C67, C68, C70, C71, C72, C76, C77, C79, C80, C82, C83, C84, C88, C89, C91, C92, C93, C94, C95, C96, C100, C101, C103, C104, C106, C107, C109, C110, C111, C115, C116, C118, C119, C121, C122, C123, C128, C143, C144, C145, C146, C147, C148, C161, C162, C163, C164, C165, C166, C167, C168, C169, C207, C208, C209, C210, C211, C212, C225, C226, C227, C228, C229, C235, C236, C240, C241, C244, C247, C253, C260, C261, C262, C266, C269, C270, C272, C274, C277, C280, C282, C283, C285, C293, C294	0.1uF
5	12	C19, C20, C245, C246, C248, C249, C254, C255, C275, C276, C278, C279	100uF
6	27	C40, C41, C42, C43, C69, C75, C78, C81, C87, C90, C99, C102, C105, C108, C114, C117, C120, C141, C142, C202, C203, C221, C222, C256, C263, C264, C271	10uF
7	17	RP1, R1, RP2, R2, RP3, RP4, R6, R8, R16, R23, R30, R31, C62, C63, C97, C126, C127	0
8	1	C98	100pF
9	14	C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C158, C159	10pF
10	25	C152, C153, C154, C155, C156, C157, C172, C173, C174, C175, C177, C178, C179, C180, C184, C185, C186, C187, C188, C189, C190, C191, C250, C251, C252	470pF
11	2	C160, C259	22uF
12	16	C170, C171, C176, C181, C182, C183, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201	220pF
13	12	C204, C205, C206, C217, C223, C224, C234, C239, C258, C265, C284, C287	1uF
14	6	C218, C219, C220, C238, C281, C296	CAP
15	1	C243	.1uF

Table 3. POS Design Guide Bill of Materials (Sheet 2 of 4)

16	1	C257	4.7nF
17	1	C273	1000pF
18	1	C286	220uF
19	1	C295	0.0022uF
20	4	D1, D53, D54, D55	LGS260-DO
21	1	D2	FMMD914
22	40	D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52	D1N916A
23	10	D23, D24, D25, D26, D27, D28, D29, D30, D31, D32	D1N916
24	1	D56	BZX84C2V7
25	1	D57	BZX84C2V4
26	1	D58	1N5817
27	6	FB1, FB2, FB3, FB4, FB5, FB6	BLM41A800S
28	2	FB8, FB7	CB70
29	2	F1, F2	SMD125-002
30	1	JP1	FLOPPY HEADER 17X2
31	1	JP2	1x4
32	1	J1	EPM DRAM Conn 140-Pin
33	1	J2	EPM PCI Conn 120-Pin
34	1	J3	Embedded Processor Module DRAM Conn 140-Pin
35	1	J4	Embedded Processor Module PCI Conn 120-Pin
36	2	J6, J5	Molex 71736-00011
37	1	J7	IDE Conn
38	2	J9, J8	PCI Conn
39	1	J10	ISA Conn A
40	1	J11	ISA Conn B
41	1	J12	PS2 STACK
42	4	J13, J14, J17, J23	1x2
43	3	J15, J24, J25	1x3
44	1	J16	1x1
45	1	J18	SERIAL STACK
46	1	J19	DB25
47	1	J20	CONNECTOR DB15HD
48	1	J21	JUMP3
49	1	J22	ATX POW CONN
50	1	J26	PCMCIA Connector
51	2	L1, L2	INDUCTOR
52	2	P2, P1	DB9
53	2	Q1, Q2	NDS9953A
54	8	R4, RP5, RP6, R7, RP45, RP49, R53, R59	22

Table 3. POS Design Guide Bill of Materials (Sheet 3 of 4)

55	25	R5, RP7, R14, RP17, RP18, RP20, RP21, RP25, RP30, RP32, RP34, RP36, RP38, RP39, RP40, RP41, R46, R47, R48, R49, R50, R51, R55, R77, R78	10K
56	14	RP8, RP9, RP10, RP11, RP12, RP13, R13, RP14, RP15, RP16, RP46, RP47, R68, R69	33
57	20	R10, R11, RP19, RP28, R33, R34, R36, R38, R39, R41, RP42, R42, RP43, R43, RP44, R44, R45, R58, R70, R76	4.7K
58	4	RP22, RP26, R37, R40	330
59	11	RP23, RP24, R25, R26, RP27, R27, R28, RP29, RP31, RP33, R35	2.7K
60	2	RP35, RP37	5.6K
61	8	R3, R18, R19, R29, R32, RP48, R60, R79	1K
62	5	R9, R21, R22, R67, R72	220
63	3	R12, R15, R17	47
64	2	R20, R73	215
65	1	R24	10
66	1	R52	22M
67	1	R54	120K
68	1	R56	8.2K
69	1	R57	20K
70	3	R61, R62, R63	150
71	1	R64	180
72	2	R66, R65	R
73	1	R71	51K
74	1	R74	130
75	1	R75	110
76	1	S1	RESET SWITCH
77	2	TP2, TP1	12MHZ
78	1	TP3	MWE#
79	1	TP4	MRAS2#
80	1	TP5	MRAS0#
81	1	TP6	MCAS0#
82	1	TP7	MCAS1#
83	1	TP8	MCAS2#
84	1	TP9	MCAS3#
85	1	TP10	MCAS4#
86	1	TP11	MCAS5#
87	1	TP12	MCAS6#
88	1	TP13	MCAS7#
89	1	TP14	14MHZ
90	1	TP15	PCLK_PIIX3
91	1	TP16	24MHZ
92	1	TP17	BIOSCS#
93	1	TP18	PDIAG#
94	1	TP19	SYSCLK

Table 3. POS Design Guide Bill of Materials (Sheet 4 of 4)

95	1	TP20	14MHZ_ISA
96	1	TP21	P12
97	1	TP22	P16
98	1	TP23	P17
99	1	TP24	P20
100	1	TP25	P21
101	1	TP26	X1
102	1	TP27	G10
103	1	TP28	G11
104	1	TP29	G12
105	1	TP30	G13
106	1	TP31	G14
107	1	TP32	G15
108	1	TP33	G16
109	1	TP34	G17
110	1	TP35	G20
111	1	TP36	G21
112	1	TP37	G22
113	1	U1	82371SB (PIIX3)
114	1	U2	74ACT04
115	3	U3, U5, U6	74ALS245
116	1	U4	74HCT14
117	1	U7	74ALS08
118	1	U8	74ALS00
119	1	U9	74ACT05
120	1	U10	PC87307IBU-VUL
121	1	U11	28F001BX-T150
122	4	U12, U13, U27, U29	GD75232SOP
123	1	U14	CL-GD7555
124	4	U15, U16, U17, U18	HYB514171BJ-60
125	1	U19	27C512
126	1	U20	74LS30
127	1	U21	74LS04
128	1	U22	ispGAL22V10
129	1	U23	28F320S5
130	1	U24	74LS08
131	1	U25	74LS260
132	1	U28	ST16C452
133	1	U30	TLC393C
134	1	U31	7404
135	1	U32	CL-PD6720
136	1	U33	LTC1472
137	1	Y1	32.768KHZ

Appendix B BIOS Checklist

This section is a checklist to specify the hardware configuration for a BIOS vendor to customize the BIOS.

Table 4. Hardware Design Specification

Intel 430HX chipset	
Manufacturer	Intel Corporation
Bus	Host
Embedded Processor Module	
Manufacturer	Intel Corporation
Speed	133 MHz
Memory - System	
Configuration	EDO, FPM
Speeds Supported	60, 70
Memory - Cache (External)	
Configuration	256 Kbyte
ROM	
Manufacturer	Intel Corporation
Part #	28F001BX-T150
Size	128 Kbyte
Super I/O	
Manufacture / Part #	National Semiconductor 87307

Table 5. Items connected to Super I/O

IDE	
Floppy	
Serial	
Parallel	
Keyboard Controller	
Real Time Clock	

Table 6. Onboard Peripherals

Onboard Peripherals	Manufacturer and Part Number	Resident Bus	If PCI, specify Vendor/ Device ID	If PCI, specify Dev.# or IDSEL	Option ROM Embed-ded in BIOS?	Supported IRQs	Address Range
Video	Cirrus Logic CL-GD7555	PCI		AD13	-		
PC Card Controller	Cirrus Logic CL-PD6720	ISA	-	-	-	3, 4, 5, 7, 9, 12, 14 (Program-mable)	**I/O address:** 0000-FFFFH (Programmable) **Memory address**: 010000-FFFFFFH (Programmable)
UART (Com3, Com4)	Exar ST16C462	ISA				**COM3**: IRQ4 **COM4**: IRQ3	**I/O address:** COM3: 03E8-03EFH COM4: 02E8-02EFH
OTHER							

Table 7. PCI Routing Information

Physical Slot # or Onboard Device	IDSEL # or DEV. #	PCI BUS #	INT or PIRQ pins from the chip set are connected to these INT pins coming from each slot			
			PIRQ 0 or INT A	PIRQ 1 or INT B	PIRQ 2 or INT C	PIRQ 3 or INT D
Slot 0	AD28	0	x		x	
Slot 1	AD29	0		x		x

Table 8. Connectors

Serial
Parallel
PS/2 Mouse
PS/2 Keyboard
Video
Other

Table 9. Software Design Specification – Feature List

USB
Enhanced IDE
PCI v2.1 Spec
PNP Spec
Other

Appendix C Schematics

C.1 POS Terminal Reference Design Schematics

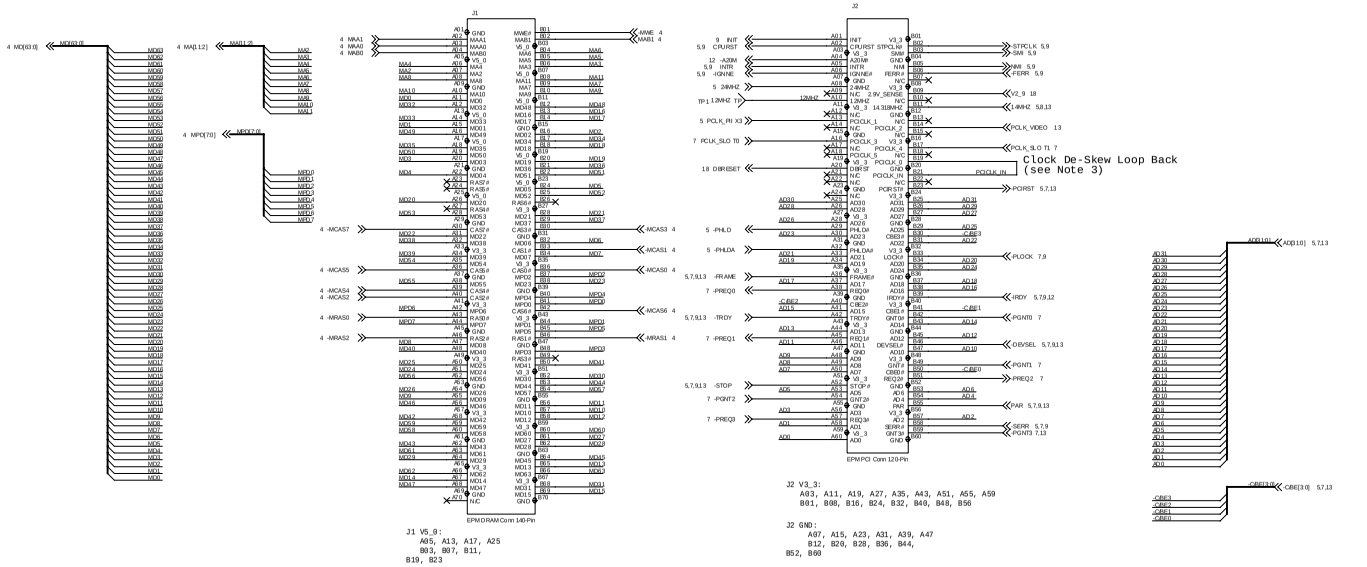
Schematics are provided for the following items:

- Embedded Processor Module Connectors
- DRAM DIMM socket
- 82371SB PCI to ISA Bridge
- ISA interface
- PCI slots 0 and 1
- ISA sockets
- ISA pullup/pulldown
- Super I/O
- Flash BIOS
- I/O connectors
- Video controller
- Video DRAM and VGA BIOS ROM
- PCMCIA connector
- Application flash
- Serial and parallel communications
- Power

Embedded Processor Module Connectors

DRAM

ADDRESS/DATA/CLOCKS



J1 V5_0:
A05, A13, A17, A25
B03, B07, B11,
B19, B23

J1 V3_3:
A33, A41, A49, A57, A65
B27, B35, B43, B51,
B59, B67

J1 GND:
A01, A09, A21, A29, A37, A45, A53, A61, A69
B15, B31, B39, B47, B55, B63, B70

J2 V3_3:
A03, A11, A19, A27, A35, A43, A51, A55, A59
B01, B08, B16, B24, B32, B40, B48, B56

J2 GND:
A07, A15, A23, A31, A39, A47
B12, B20, B28, B36, B44,
B52, B60

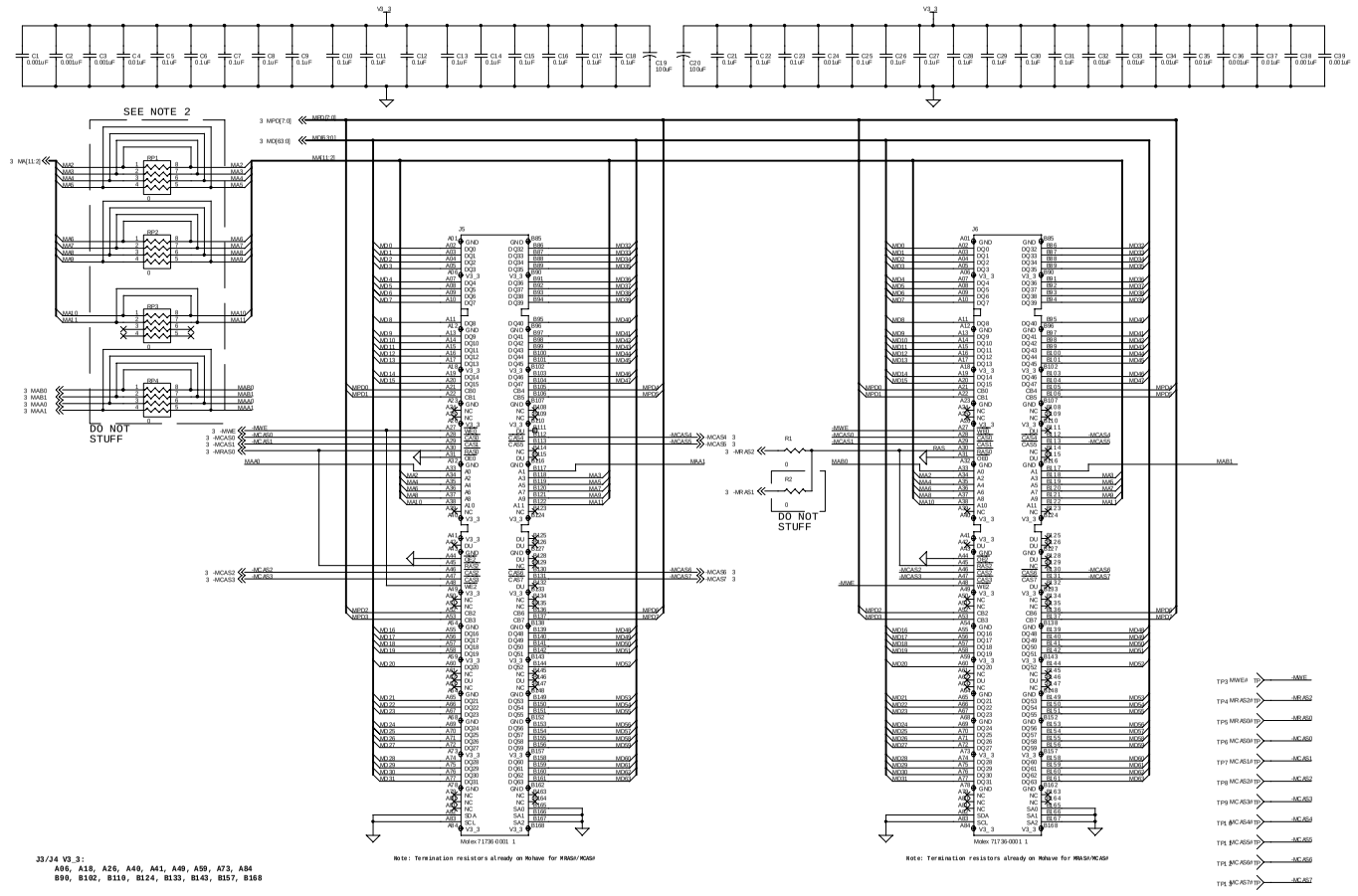
NOTE 0: Connectors are female
NOTE 1: PCLK_PIIX3, PCLK_VIDEO, PCLK_SLOT0, PCLK_SLOT2, PCLK_SLOT23 must be equal length.
NOTE 3: PCLK_0 to PCICLK_IN roundtrip must be same length as signals in NOTE 1.
NOTE 4: Split PCLK_SLOT23 to supply both PCI SLOT 2 and PCI SLOT 3 as close to the PCI slots as possible. Stubs must be of equal length.
NOTE 5: Separate all clocks from any other trace by 10 mil. (SYSCLK, 25MHZ, 14MHZ, PCLK_PIIX3, PCLK_VIDEO, PCLK_SLOT0, PCLK_SLOT1, PCLK_SLOT23

24MHZ/14MHZ/SYSCLK
24MHZ (3v): PIIX3(USBCLK), X1(Super I/O) 14MHZ (3v): PIIX3(OSC), ISA Slots (OSC) SYSCLK 8.25MHZ (PIIX3) -> ISA Slots

PCI Clock Distribution (33MHZ)	
PCICLK_0	(B19) De-Skew Loopback
PCICLK_1/PCLK_PIIX3	(A13) PIIX3
PCICLK_2/PCLK_VIDEO	(B14) Video (Virge GX)
PCICLK_3/PCLK_SLOT0	(A16) PCI Expansion Slot 0
PCICLK_4/PCLK_SLOT1	(B17) PCI Expansion Slot 1
PCICLK_5/PCLK_SLOT23	(A18) PCI Expansion Slots 2/3

Title	POS Design Guide : Embedded Processor Module Connectors				
Size A4	Document Number {Doc}				Rev 1.00
Date:	Wednesday, May 13, 1998	Sheet	3	of	18

DRAM (DIMM) SOCKETS



J3/J4 V3_3:
A06, A18, A26, A40, A41, A49, A59, A73, A84
B90, B102, B110, B124, B133, B143, B157, B168

J3/J4 GND:
A01, A12, A23, A32, A43, A54, A64, A68, A78 | A31, A44, A82, A83
B85, B96, B107, B116, B127, B138, B148, B152, B162 | B165, B166, B167

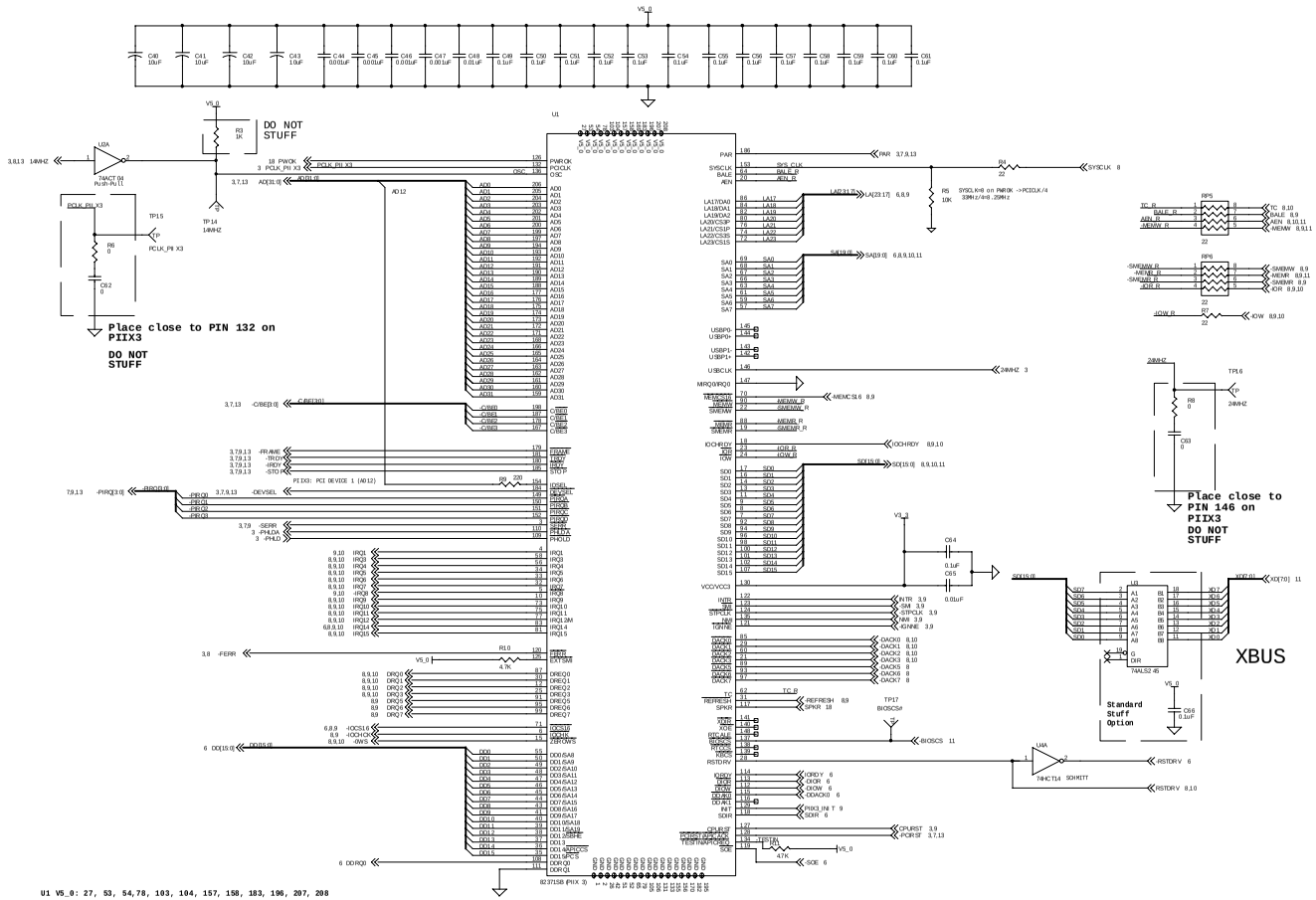
J3/J4 NC:
A24, A25, A39, A50, A51, A61, A63, A79, A80, A81
B108, B109, B114, B123, B129, B135, B145, B147, B163, B164

J3/J4 DU: A42, A62
B111, B115, B125, B126, B128, B132, B134, B135, B146

NOTE 1: Place Test Points close to J3/J4 DIMM Connectors
NOTE 2: Use R-PACK pad geometry. Shunt pads with trace. Route on surface (cuttable)

Title: POS Design Guide : DRAM DIMM Sockets			
Size: A4	Document Number: {Doc}		Rev: 1.00
Date: Wednesday, May 13, 1998	Sheet 4 of 18		

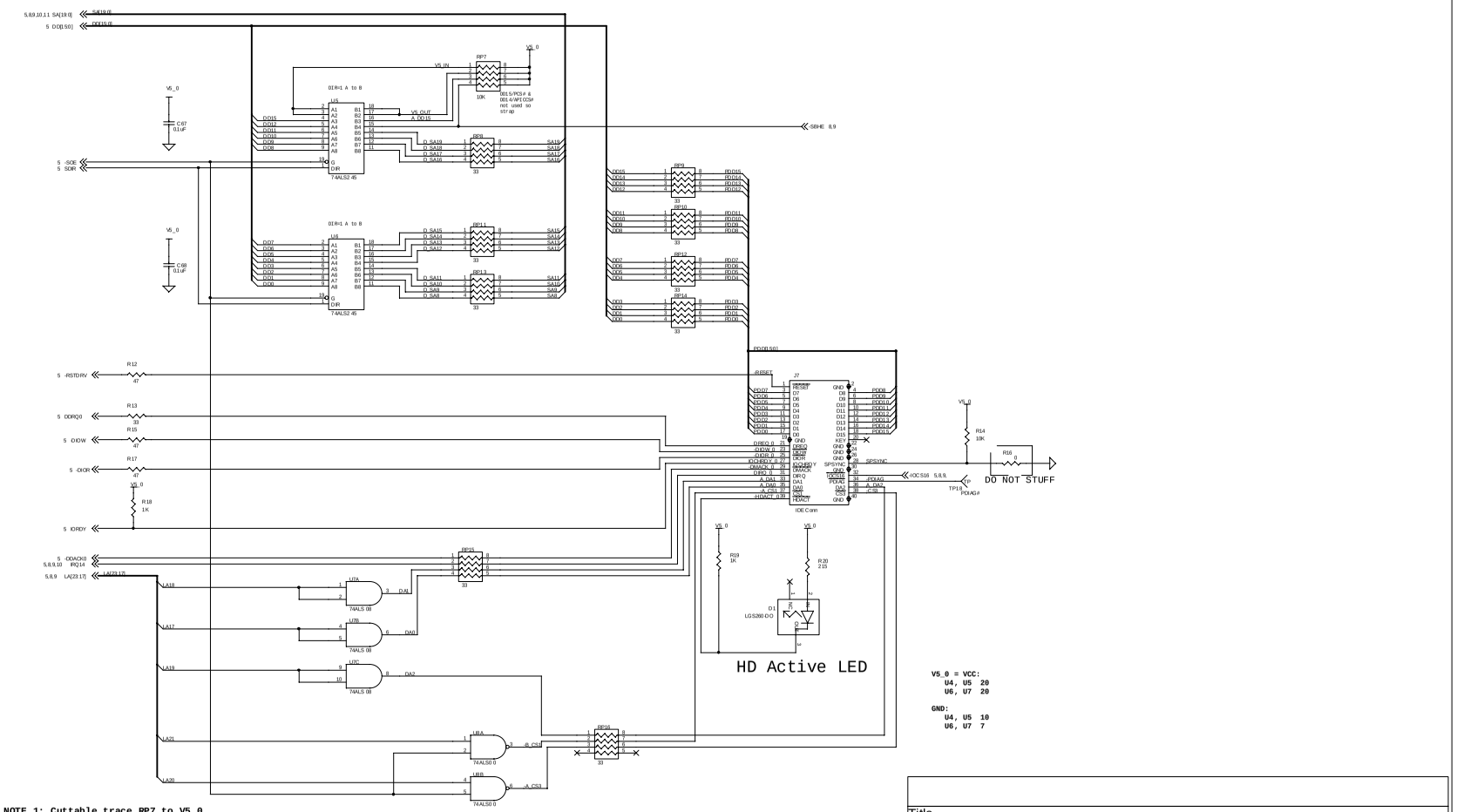
INTEL 82371SB PCI ISA IDE XCELERATOR



NOTE1: 5 mil trace/space gives ~70 Ohm Zo for PCI bus as d-stripline

Title	POS Design Guide : 82371SB PCI to ISA Bridge	
Size A4	Document Number {Doc}	Rev 1.00
Date: Wednesday, May 13, 1998	Sheet 5 of 18	

IDE Interface



NOTE 1: Cuttable trace RP7 to V5_0

Title	POS Design Guide : ISA Interface	
Size A4	Document Number {Doc}	Rev 1.00
Date: Wednesday, May 13, 1998	Sheet 6 of 18	

J6/J7 V5_0:
A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
B5, B6, B19, B22, B59, B61, B62

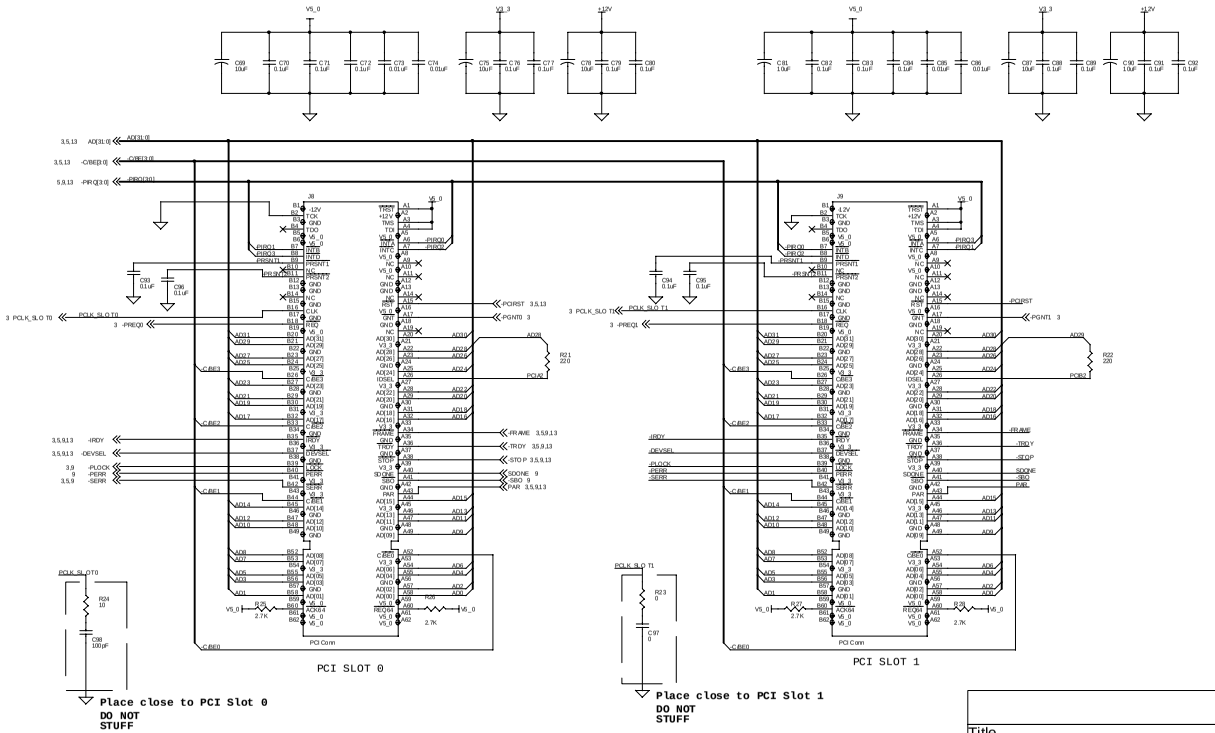
J6/J7 V3_3:
A21, A27, A33, A39 A45, A53
B25, B31, B36, B41, B43, B54

J6/J7 NC:
A9, A11, A14, A19
B10, B14

J6/J7 GND:
A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
B3, B12, B13, B15, B17, B28, B34, B38, B46, B49, B57 | B2

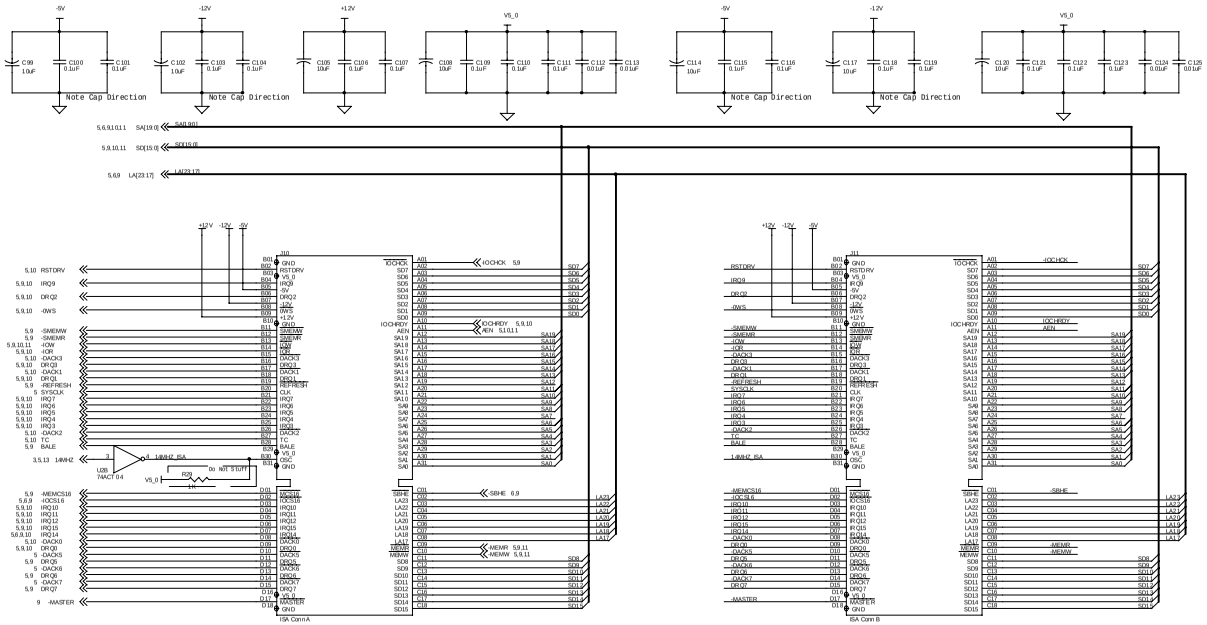
J6/J7 +12V: A2
-12V: B1

PCI SLOTS



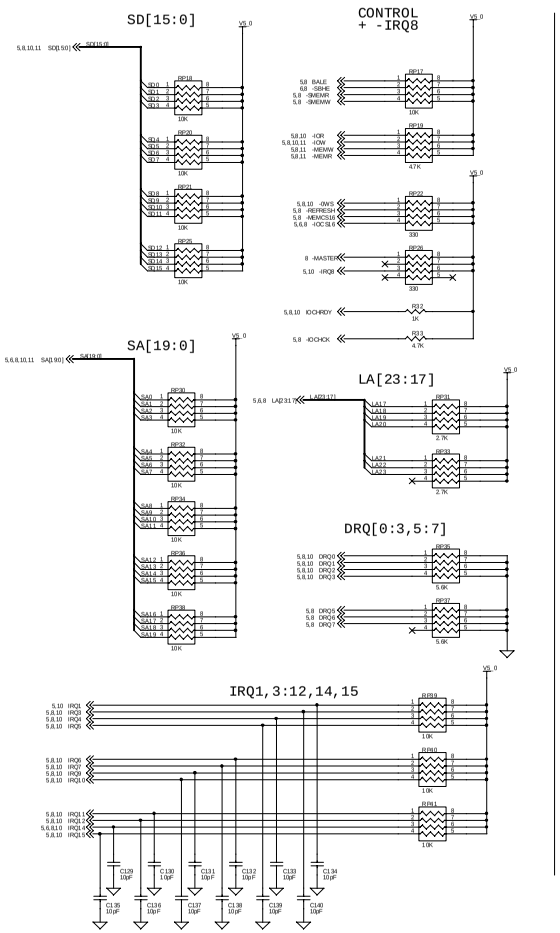
Title	POS Design Guide : PCI Slots 0 & 1		
Size A4	Document Number {Doc}		Rev 1.00
Date: Wednesday, May 13, 1998		Sheet of 18	

ISA Slots

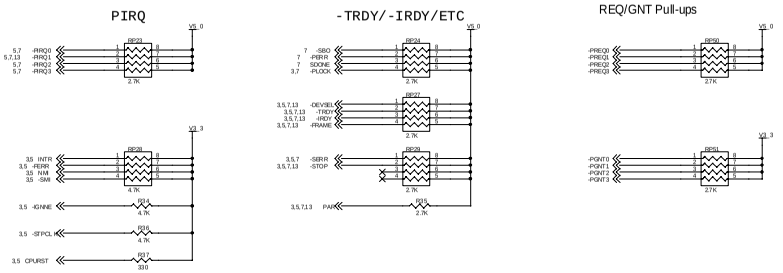


Title	POS Design Guide : ISA Sockets	
Size A4	Document Number {Doc}	Rev 1.00
Date: Wednesday, May 13, 1998	Sheet 8 of 18	

ISA Pullup/Pulldown

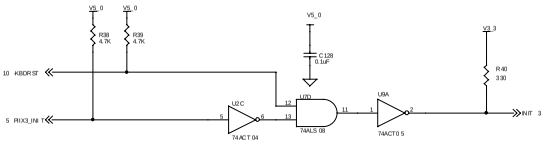


PCI Pullup/Pulldown



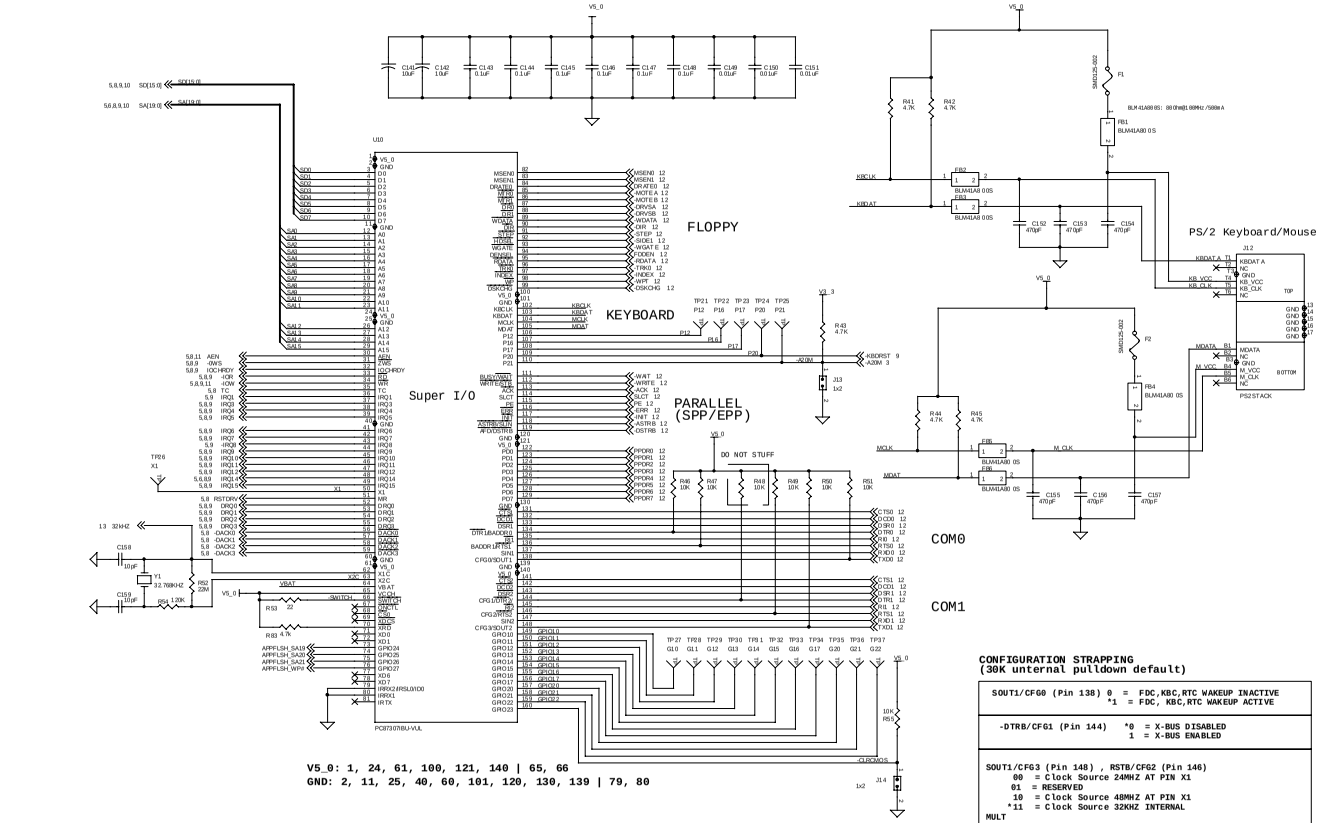
Note: 64-BIT PCI Strap Off At PCI Connectors

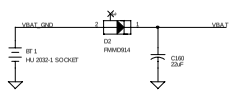
Note: Pullups on Mohave -PREQ/PGNT[3:0]



Title: POS Design Guide : ISA Pullup/Pulldown		
Size: A4	Document Number: {Doc}	Rev: 1.00
Date: Wednesday, May 13, 1998	Sheet 9 of 18	

SUPER I/O





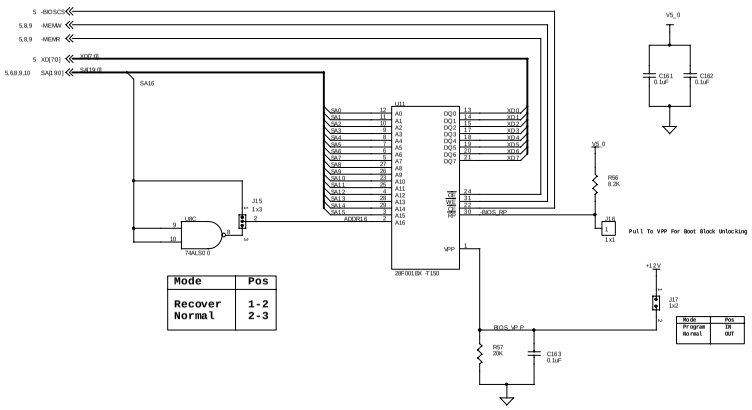
CONFIGURATION STRAPPING
(30K unternal pulldown default)

SOUT1/CF60 (Pin 138) 0 = FDC,KBC,RTC WAKEUP INACTIVE *1 = FDC, KBC,RTC WAKEUP ACTIVE
-DTRB/CF61 (Pin 144) *0 = X-BUS DISABLED 1 = X-BUS ENABLED
SOUT1/CFG3 (Pin 148) , RSTB/CFG2 (Pin 146) 00 = Clock Source 24MHZ AT PIN X1 01 = RESERVED 10 = Clock Source 48MHZ AT PIN X1 *11 = Clock Source 32KHZ INTERNAL MULT
RTS1/BADDR1 (Pin 136), DTR1/BADDR0 (Pin 134) 00 = Full PNP ISA 01 = Wake in Wait for Key (index pnp isa) 10 = PNP Motherbd (wake in config state index 0x15C) *11 = PNP Motherbd (wake in config state index 0x2E)

NOTE 1: Place oscillator circuit close to X1C/X2C. Paracitic <=8pF
NOTE 2: Crystal is parallel, resonant, (N cut) or XY bar, Q>=35, Cl=9-13pF
NOTE 3: Test points are a hole/via such that a 25-mil square pin can be inserted.

Title	POS DESIGN GUIDE: Super I/O	
Size A4	Document Number {Doc}	Rev 1.00
Date: Wednesday, May 13, 1998	Sheet 10 of 18	

BOOT BLOCK FLASH



Mode	Pos
Recover	1-2
Normal	2-3

Mode	Pos
Program	IN
Normal	OUT

VCC:

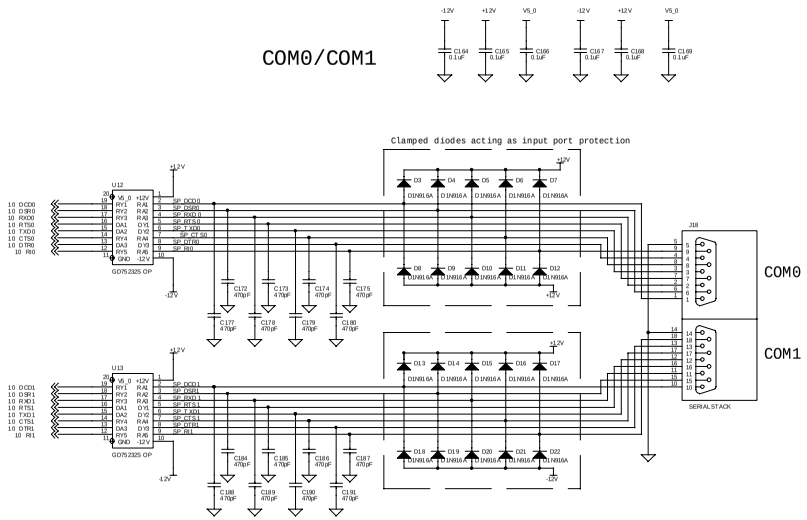
U12	20
U9	24
U10/U11	1, 14
U13	32
U7	14

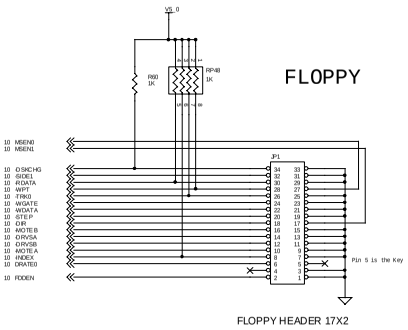
GND:

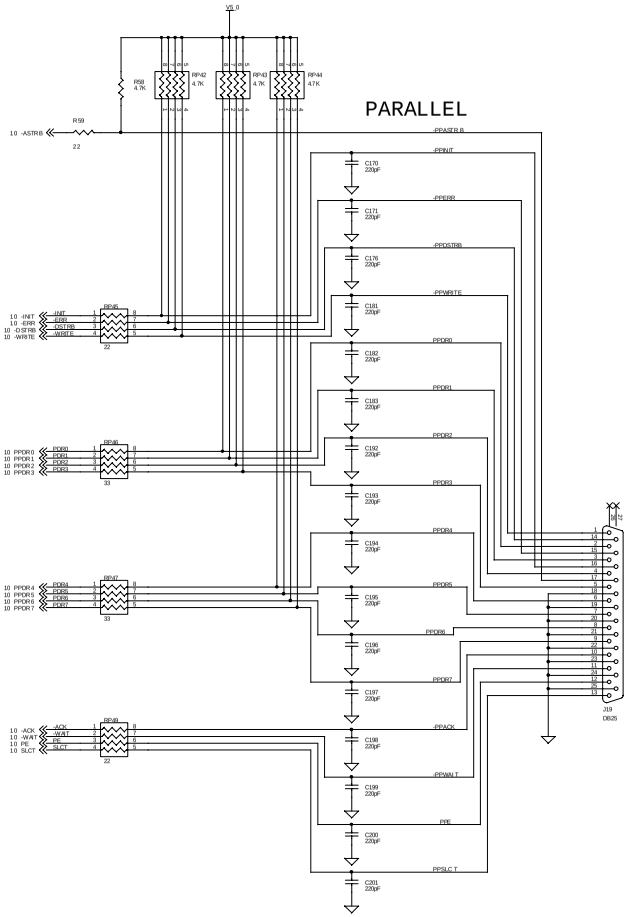
U12	10
U9	12
U10/U11	7, 8
U13	16
U7	7

Title: POS Design Guide : Flash Bios		
Size: A4	Document Number: {Doc}	Rev: 1.00
Date: Wednesday, May 13, 1998	Sheet 11 of 18	

I/O CONNECTORS

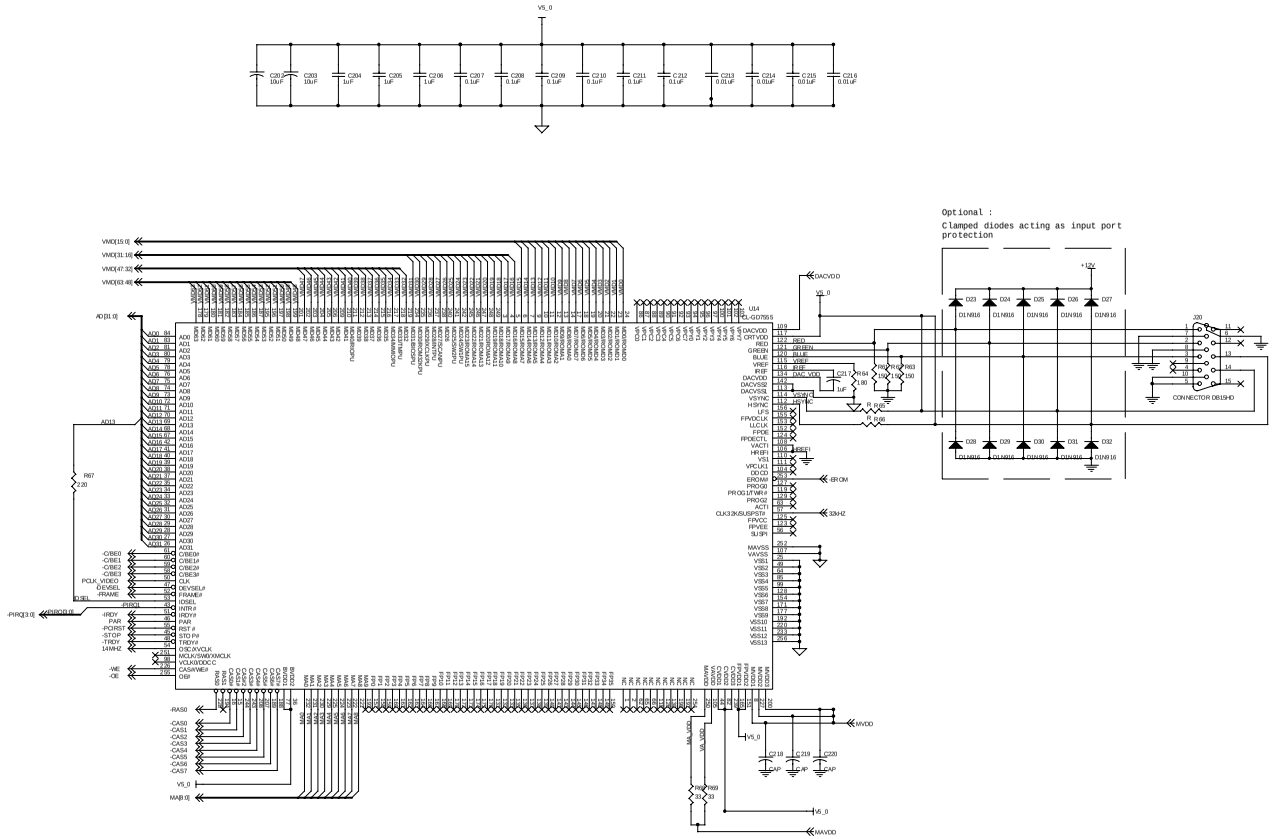






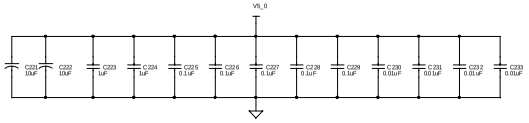
Title: POS Design Guide : I/O Connectors		
Size: A4	Document Number: {Doc}	Rev: 1.00
Date: Wednesday, May 13, 1998	Sheet 12 of 18	

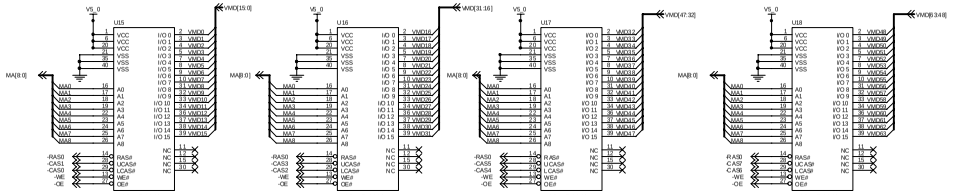
VIDEO CONTROLLER

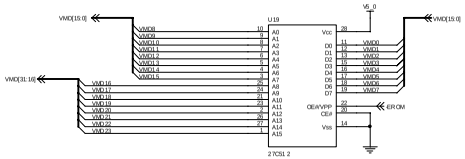


Title	POS Design Guide : Video Controller		
Size A4	Document Number {Doc}		Rev 1.00
Date: Friday, May 15, 1998	Sheet 13 of 18		

VIDEO DRAM

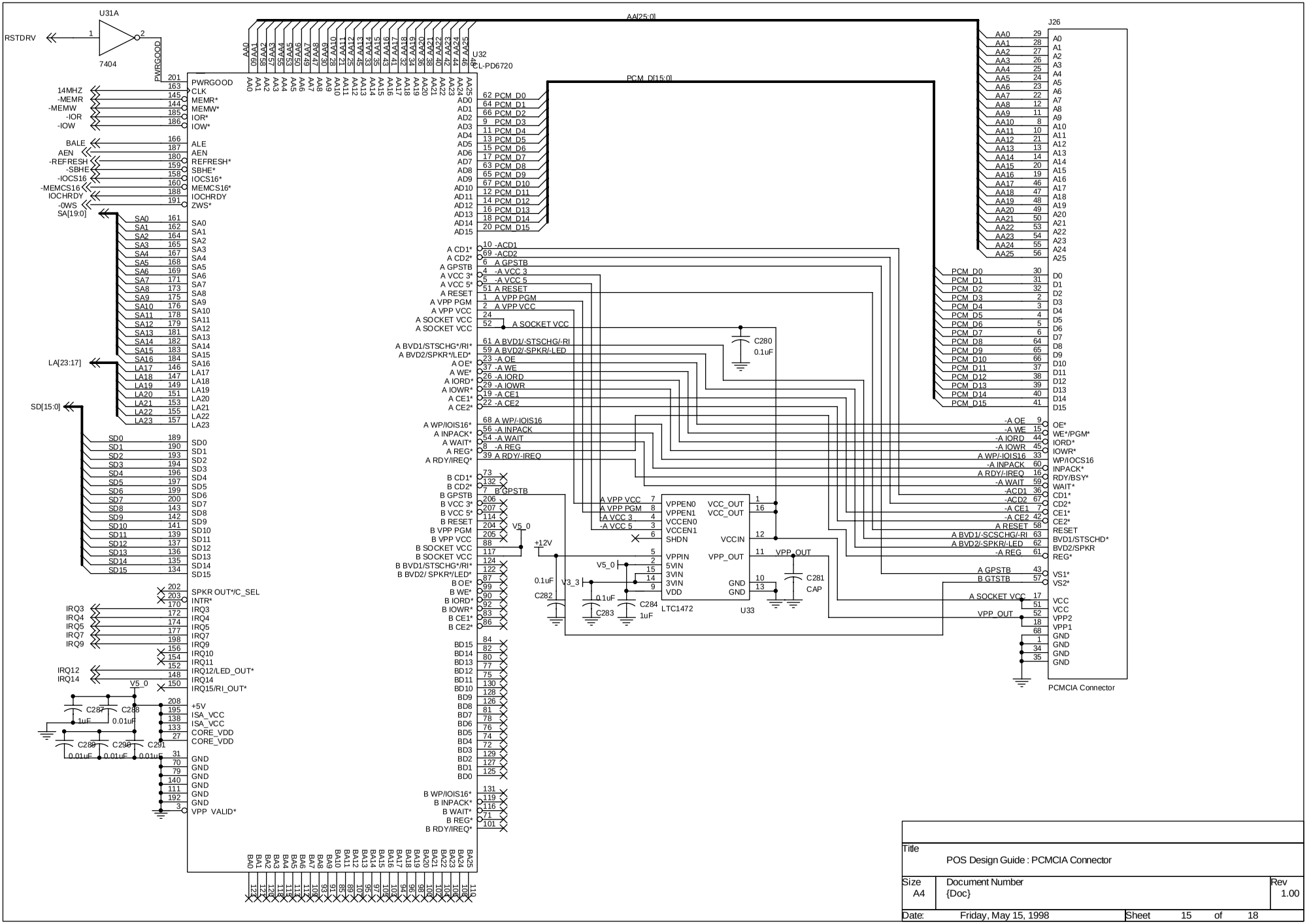






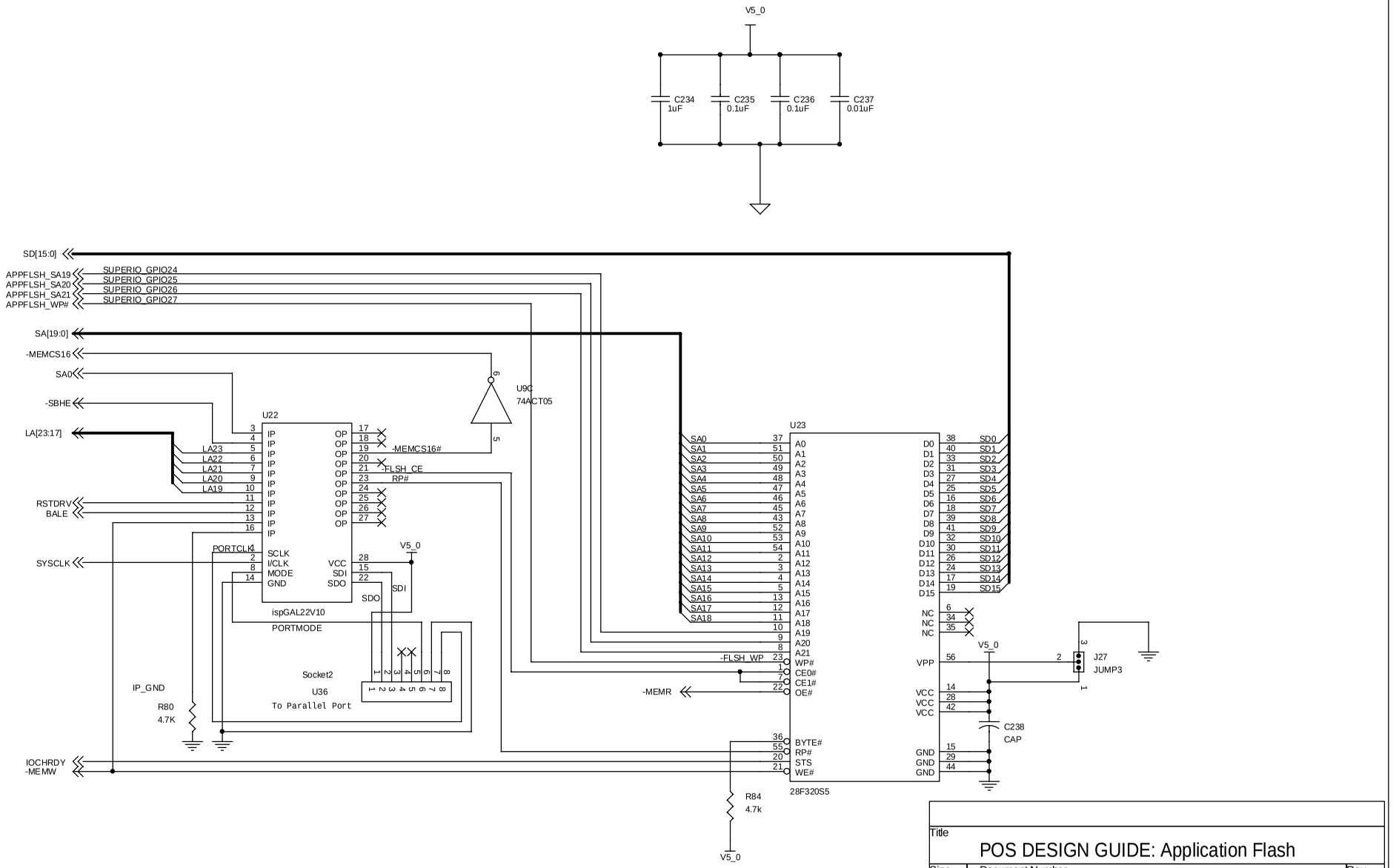
VGA BIOS ROM

Title	POS Design Guide : Video DRAM and VGA BIOS ROM		
Size A4	Document Number {Doc}		Rev 1.00
Date: Friday, May 15, 1998		Sheet 14 of 18	

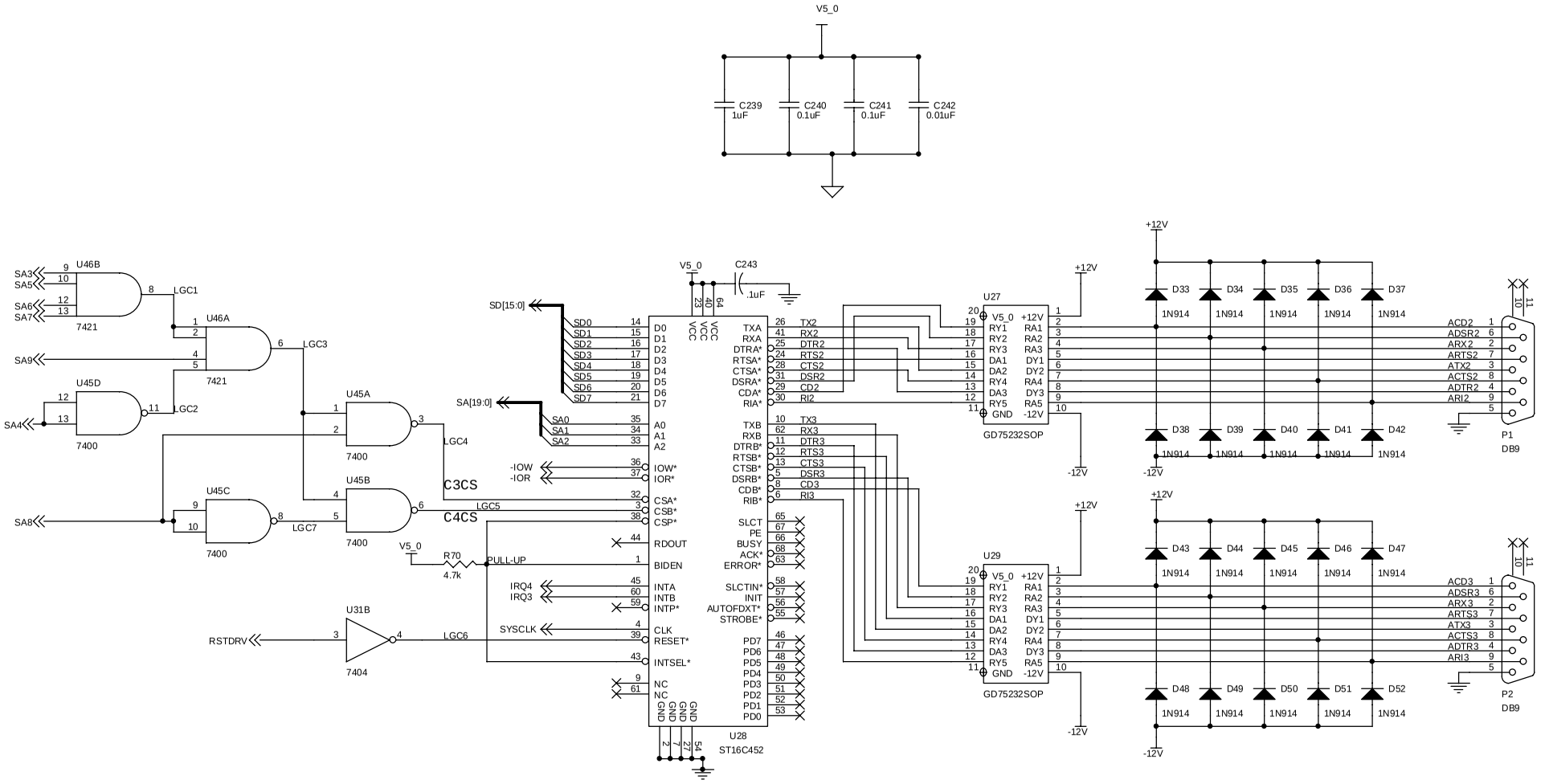


Title	POS Design Guide : PCMCIA Connector	
Size A4	Document Number {Doc}	Rev 1.00
Date: Friday, May 15, 1998	Sheet 15 of 18	

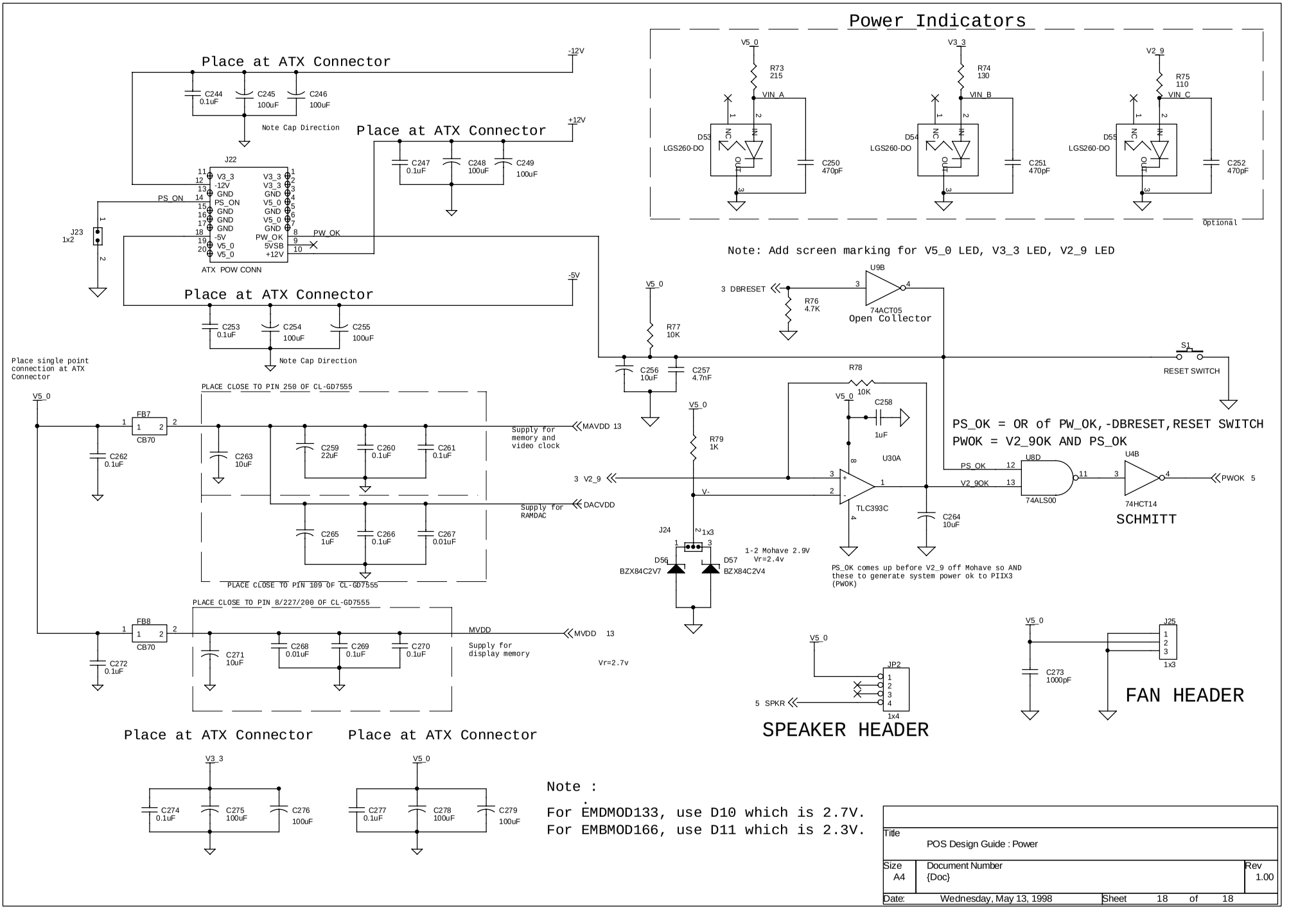
APPLICATION FLASH



ADDITIONAL COMMUNICATION PORTS



Title	POS Design Guide : Serial communications		
Size A4	Document Number {Doc}		Rev 1.00
Date: Friday, May 15, 1998	Sheet 17 of 18		


Power Indicators
Place at ATX Connector
-12V
C244 0.1uF
C245 100uF
C246 100uF
Note Cap Direction
Place at ATX Connector
+12V
C247 0.1uF
C248 100uF
C249 100uF
J22
V3_3
-12V
GND
PS_ON
GND
GND
GND
-5V
V5_0
V5_0
V3_3
V3_3
GND
V5_0
V5_0
GND
PW_OK
5VSB
+12V
PW_OK
J23 1x2
ATX POW CONN
Place at ATX Connector
-5V
C253 0.1uF
C254 100uF
C255 100uF
Note Cap Direction
Place single point connection at ATX Connector
V5_0
R73 215
VIN_A
D53 LGS260-DO
C250 470pF
V3_3
R74 130
VIN_B
D54 LGS260-DO
C251 470pF
V2_9
R75 110
VIN_C
D55 LGS260-DO
C252 470pF
Optional
Note: Add screen marking for V5_0 LED, V3_3 LED, V2_9 LED
U9B
3 DBRESET
R76 4.7K
74ACT05
Open Collector
V5_0
R77 10K
C256 10uF
C257 4.7nF
S1
RESET SWITCH
PS_OK = OR of PW_OK,-DBRESET,RESET SWITCH
PWOK = V2_9OK AND PS_OK
PLACE CLOSE TO PIN 250 OF CL-GD7555
V5_0
FB7
CB70
C262 0.1uF
C263 10uF
C259 22uF
C260 0.1uF
C261 0.1uF
Supply for memory and video clock
MAVDD 13
Supply for RAMDAC
DACVDD
C265 1uF
C266 0.1uF
C267 0.01uF
PLACE CLOSE TO PIN 109 OF CL-GD7555
V5_0
R79 1K
3 V2_9
V-
R78 10K
V5_0
C258 1uF
U30A
TLC393C
C264 10uF
PS_OK
V2_9OK
U8D
74ALS00
U4B
74HCT14
SCHMITT
PWOK 5
J24 1x3
D56 BZX84C2V7
D57 BZX84C2V4
1-2 Mohave 2.9V Vr=2.4v
PS_OK comes up before V2_9 off Mohave so AND these to generate system power ok to PIIX3 (PWOK)
PLACE CLOSE TO PIN 8/227/200 OF CL-GD7555
FB8
CB70
C272 0.1uF
C271 10uF
C268 0.01uF
C269 0.1uF
C270 0.1uF
MVDD
Supply for display memory
MVDD 13
Vr=2.7v
V5_0
JP2
5 SPKR
1x4
SPEAKER HEADER
V5_0
C273 1000pF
J25
1x3
FAN HEADER
Place at ATX Connector
V3_3
C274 0.1uF
C275 100uF
C276 100uF
Place at ATX Connector
V5_0
C277 0.1uF
C278 100uF
C279 100uF
Note :
For EMDMOD133, use D10 which is 2.7V.
For EMBMOD166, use D11 which is 2.3V.
Title
POS Design Guide : Power
Size A4
Document Number {Doc}
Rev 1.00
Date: Wednesday, May 13, 1998
Sheet 18 of 18