Interfacing the Low-Power Embedded Pentium® Processor with MMX™ Technology to the 82439HX System Controller

Application Note

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Application Note

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1.0 Introduction

This application note describes a method for interfacing the low-power embedded Pentium processor with MMX technology to the 82439HX System Controller. Several features of the 82439HX System Controller make it an attractive device for embedded system designers, including the ability to cache large amounts of memory (up to 512 Mbytes of DRAM), error checking and correction, and parity. The I/O voltage supply (V_{CC2}) for the low-power embedded Pentium processor with MMX technology micron is 2.5 V. The 82439HX System Controller I/O interface is 3.3 V and does not meet the 2.5 V I/O interface requirement of the low-power embedded Pentium processor with MMX technology. To enable this configuration, level shifters (sometimes called bus switches) may be used to limit the 3.3 V outputs of the 82439HX System Controller to meet the 2.5 V specification requirements of the low-power embedded Pentium processor with MMX technology.

This paper describes one method for using level shifters to connect the 2.5 V I/Os on the Pentium processor to 3.3 V I/O devices. In addition, this paper describes a method for terminating a 3.3 V clock generator to obtain a 2.5 V clock signal for the low-power embedded Pentium processor with MMX technology.

2.0 DC Analysis

Table 1 shows the DC specifications for the low-power embedded Pentium processor with MMX technology and the 82439HX System Controller. Note that although there is only 100 mV of noise margin when the 82439HX System Controller is driving a 0, the specification is stated with a 4 mA load. For all of the interface signals between the low-power embedded Pentium processor with MMX technology and the 82439HX System Controller, the DC load should be limited to device leakage currents and should be in the µA range. Therefore, the actual drive levels will be much closer to the supply rails and the noise margin will be increased.

Table 1. DC Specifications

82439HX System Controller		Low-Power Embedded Pentium® Processor with MMX™ Technology		Noise Margin
V_{IL}	0.800 V	V_{OL}	0.400 V	400 mV
V_{IH}	2.0 V	V_{OH}	2.175 @ 1 mA	175 mV
V_{OL}	0.4 V @ 4 mA	V_{IL}	0.5 V	100 mV
V_{OH}	2.4 V	V_{IH}	1.925 V	475 mV

Table 1 shows that it is possible to interface the low-power embedded Pentium processor with MMX technology to the 82439HX System Controller if the maximum voltage passed to the processor is limited to 2.5 V, and all other voltage levels below 2.5 V are passed without attenuation. An N-channel MOSFET with the gate tied to 3.5 V can be used to achieve these voltages. These MOSFETs are available in level shifters.

3.0 Overview of the Interface Method

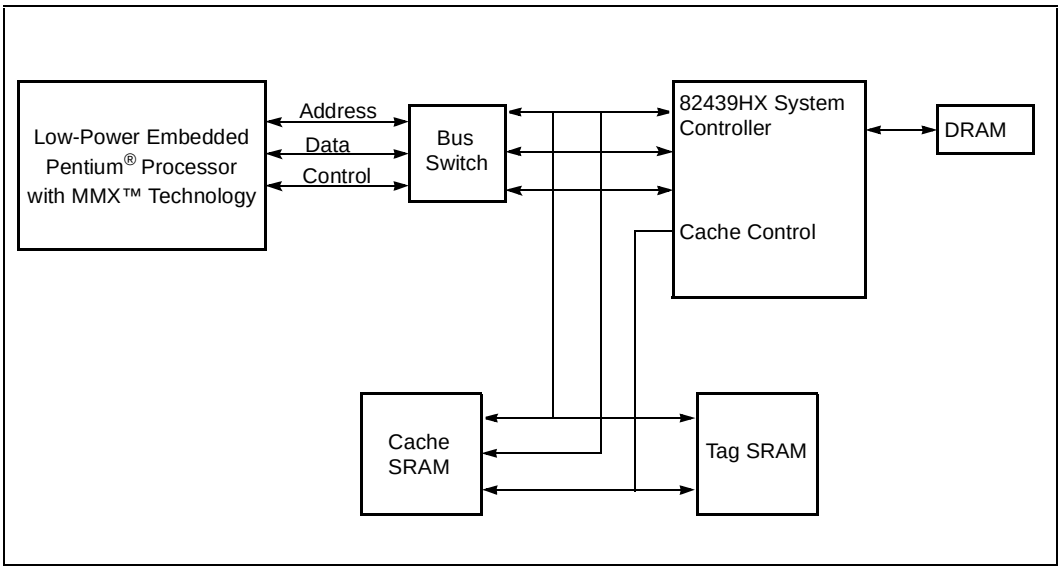
The method described here is to run any signal that might be driven by a device with 3.3 V I/Os through an N-channel MOSFET. Table 2 lists all pins on the low-power embedded Pentium processor with MMX technology that may need to be protected by a bus switch (level shifter). If a pin is not used, it can be tied to the appropriate voltage through a resistor. The CLK input is a special case discussed in "Clocking" on page 8.

Table 2. Input and Bidirectional Pins

A20M#	BUSCHK#	IGNNE#	PICCLK	TMS
A[31:3]	CLK	INIT	PICD[1:0]	TRST#
AHOLD	D[63:0]	INTR	R/S#	WB/WT#
AP	DP[7:0]	INV	RESET	
BE[4:0]#	EADS#	KEN#	SMI#	
BF[2:0]	EWBE#	NA#	STPCLK#	
BOFF#	FLUSH#	NMI	TCK	
BRDY#	HOLD	PEN#	TDI	

The block diagram in Figure 1 illustrates one method for configuring a system.

Figure 1. Block Diagram of System with Level Shifters



Another possible system configuration would use 2.5 V cache SRAMs. In this configuration, it may be necessary to run some of the cache control lines through the level shifters depending on the specification of the cache devices.

4.0 Level Shifters

The level shifters are N-channel MOSFETs with the gate tied to a reference voltage of 3.5 V (see Figure 2). When either the source or drain of the MOSFET reaches a voltage of about one volt less than the gate voltage, the MOSFET stops conducting. As shown in Figure 3, this limits the voltage that can be passed by the MOSFET to V_{gate} - 1 V. This assumes that the current through the switch is in the µA range. For larger currents, the maximum pass voltage decreases.

Figure 2. N-Channel MOSFETs with Gate Tied to 3.5 V

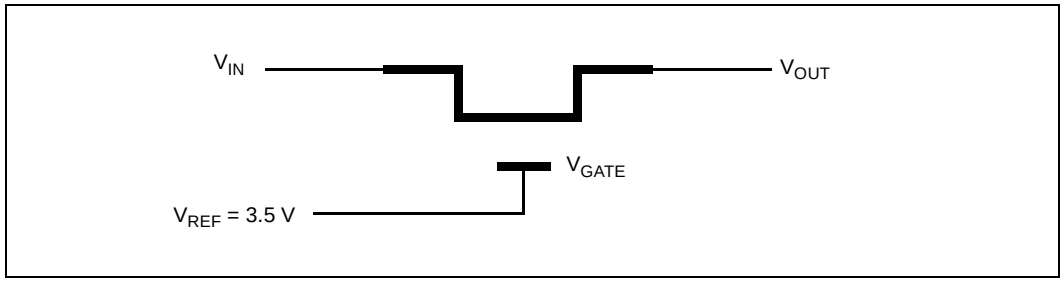
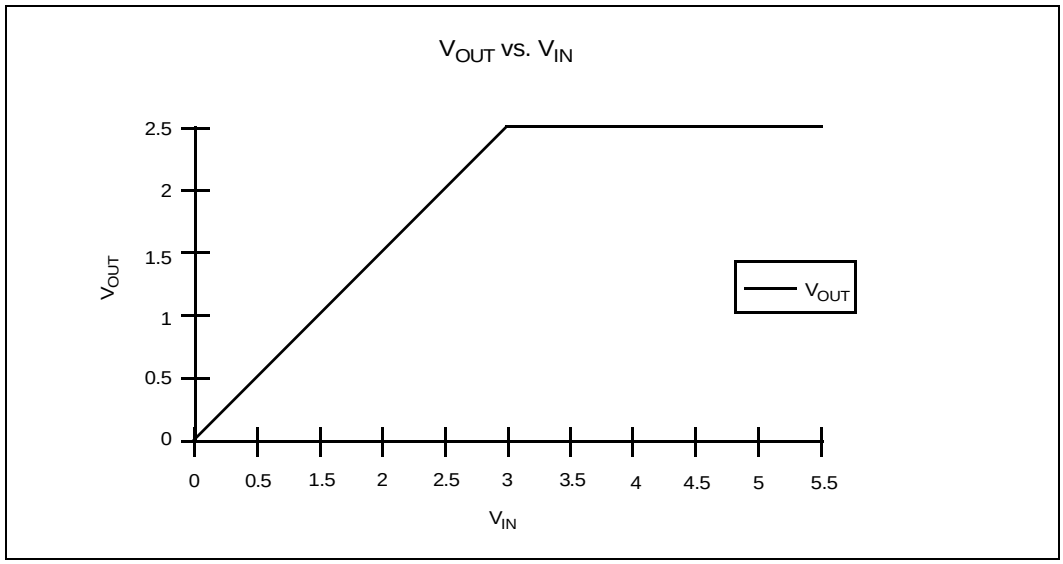


Figure 3. V_{OUT} vs. V_{IN}



Be careful to choose a bus switch that does not contain both P- and N-channel MOSFETs in parallel. These devices will not limit the passed voltage because the P-channel MOSFET passes voltages above V_{gate} -1 V. Examples of devices that could be used are the QS32X861 from Quality Semiconductor or CrossBar* (SN74CBTXXXX) switches from Texas Instruments.

The bias voltage to the level shifters must be a well-regulated 3.5 V. Do not use a 3.3 V PC supply because this voltage can be as low as 3.0 V. This would mean the pass voltage would be limited to about 2.0 V, which does not leave any margin to meet the V_{IH} specification of the 82439HX System Controller. Note that the level shifters consume little power, so there is no need for a separate power plane operating at 3.5 V.

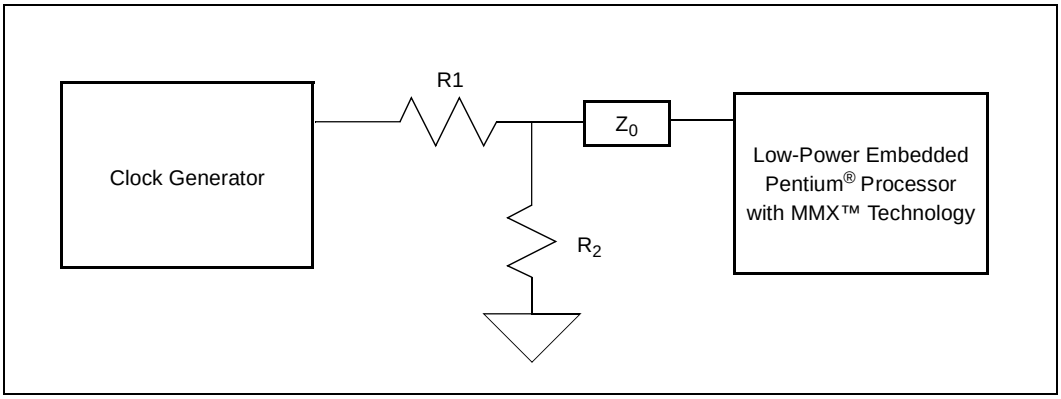
The propagation delay through the switch is due to RC delay and tends to be in the 200 ps range for switches with on-resistances in the 5 -7 Ω range driving a 50 pF load.

5.0 Clocking

Another issue to address in using the low-power embedded Pentium processor with MMX technology with the 82439HX System Controller is generating the proper clocks. The processor needs a 2.5 V clock signal. The 82439HX System Controller requires a 3.3 V clock. To generate these clocks, use a clock driver with 2.5 V and 3.3 V outputs.

You can also use a 3.3 V clock generator and derive the 2.5 V clock signal using the circuit shown in Figure 4.

Figure 4. Circuit for 3.3 V Clock Generator



R1 and R2 must be chosen so that the parallel combination, in series with the output impedance, matches the characteristic impedance of the transmission line (Z_0). Furthermore, R1 and R2 must be chosen such that the resulting voltage divider converts the 3.3 V peak-to-peak clock signal to a 2.5 V signal.

If we assume Z_0 = 65 Ω, $R1_T$ = R1+ R_O, and the output impedance of the clock generator (R_O) is 15 Ω, then we have:

$$R1_T * R2 / (R1_T + R2) = 65$$

and

$$R1_T/R2 = 0.8/2.5$$

If we let $R1_T$ = 0.8 and R2 = 2.5, then scale $R1_T$ and R2 so that the parallel combination is 65 Ω, then we have:

$R_P = 0.8 * 2.5 /(2.5 +0.8) = .6061$ (the parallel combination of 0.8 and 2.5 ohms)

$R1_T' = 65 / R_P * 0.8 = 85.8 \rightarrow R1' = 70.8$

$R2' = 65 / R_P * 2.5 = 268$

69.8 Ω and 267 Ω precision resistors are readily available and could be used. The small change in R1 from the calculated value will not have a material affect on the operation of the circuit.

Be certain to place R1 as close to the clock generator as possible and place R2 as close to R1 as possible. Refer to the *82439HX Design Guide* (order number 297467) for further recommendations on clocking.

6.0 Layout Issues

Care must be taken when performing board layout for this configuration. There will be at least three different supply voltages (1.8 V, 2.5 V and 3.3 V), so carefully plan how to cut the power planes. Keep in mind that the supply planes must be able to supply the required DC current and be properly bypassed at high frequencies to keep the supplies within the specified levels for each device.

Another layout issue is controlling crosstalk. When passing a voltage above $V_{gate} - 1$ V, the level shifters will act like very high impedance drivers. This makes the signal being driven more susceptible to cross-talk. Take care to allow extra spacing between the control signals listed in Table 3. The minimum spacing required depends on the design. Perform signal integrity simulations to verify the design.

Table 3. Control Signals Requiring Extra Spacing

all clocks	RESET	INIT	TDI
ADS#	NA#	IGNNE#	R/S#
BRDY#	KEN#	STPCLK#	NMI, SMI and INTR
EADS#	A20M#	TRST#	

7.0 Summary

It is possible to interface the low-power embedded Pentium processor with MMX technology to the 82439HX System Controller using level shifters. Any input or bidirectional signal on the processor that is not directly tied to a reference plane must be protected. The required clock for the processor can be generated from a 3.3 V clock source using the termination method shown.

Also, more attention must be paid to signal quality. There may be more reference planes in the design that must avoid crossing with high speed signals. Simulations of crosstalk should be performed to verify spacing between critical control signals.