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REVISIONS

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

INTEL^(R) PENTIUM^(R) M PROCESSOR /
 INTEL^(R) E7501 CHIPSET
 PLATFORM REFERENCE SCHEMATICS

REV A2.1

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NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

DRAWING

BOM RELEASE DATE		PB NUMBER	
SIGNATURE	DATE	intel CORPORATION	5000 W CHANDLER BLVD CHANDLER, AZ 85226
DRN BY			
CHK BY		TITLE	
ENGR			
APVD			
APVD			
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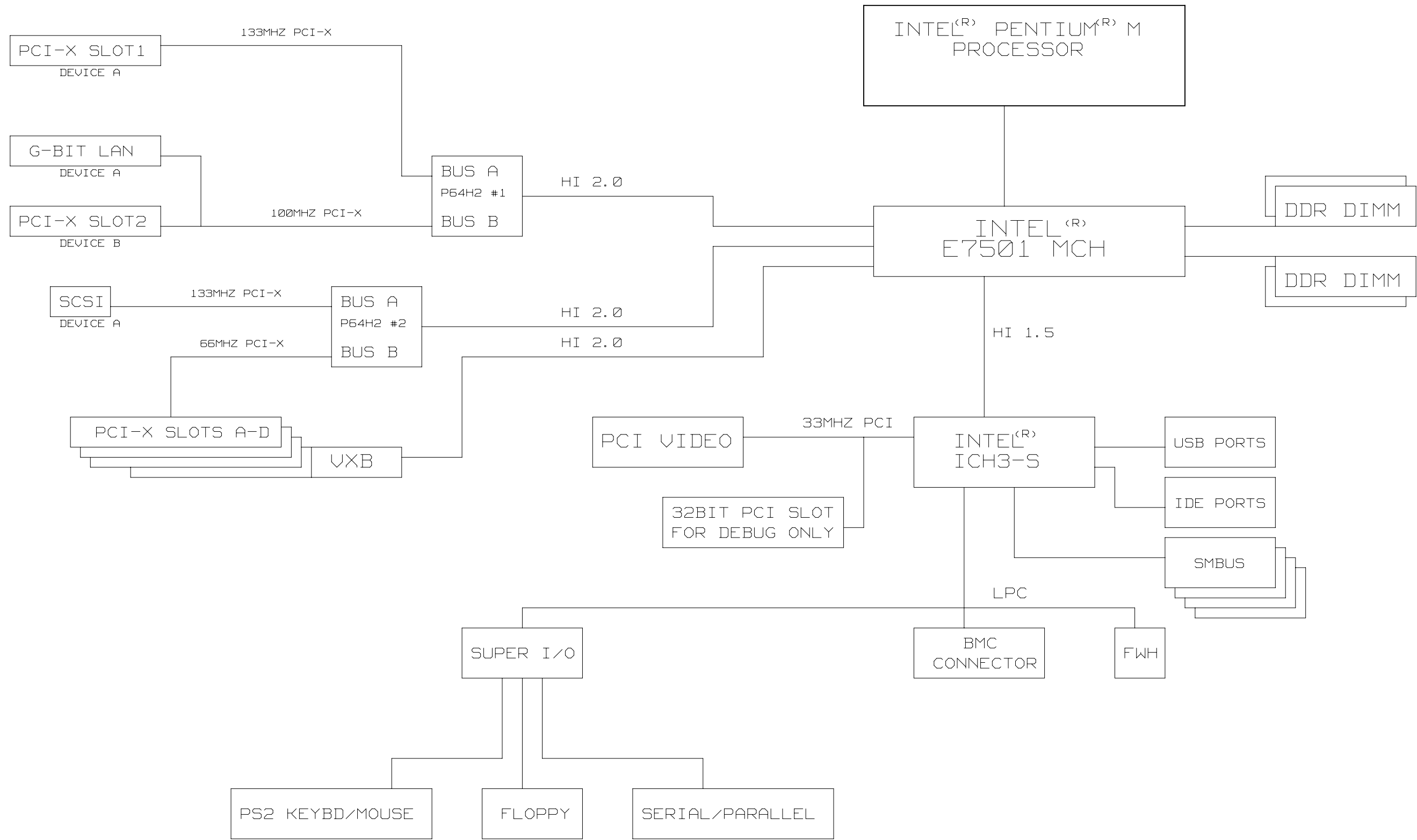
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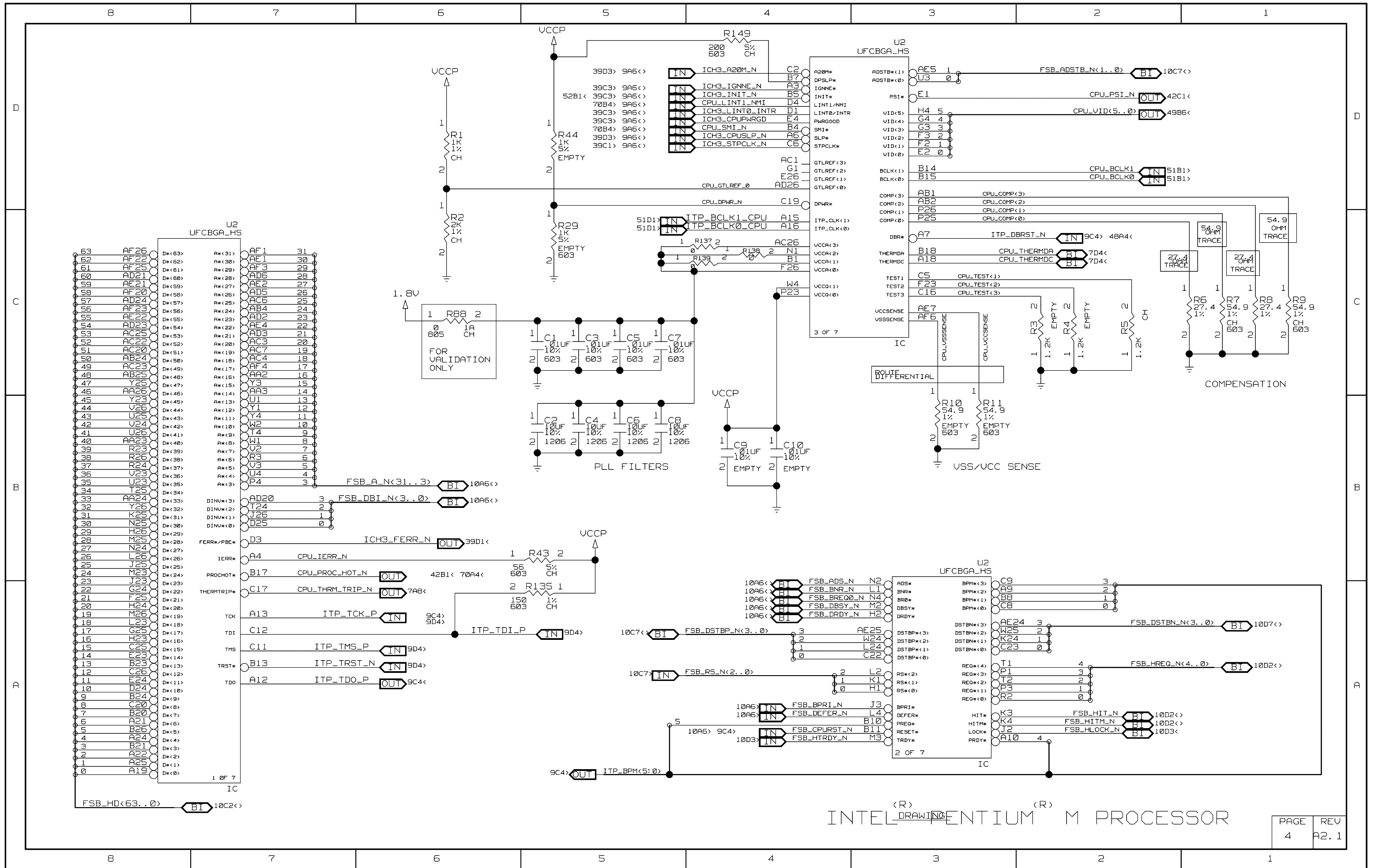
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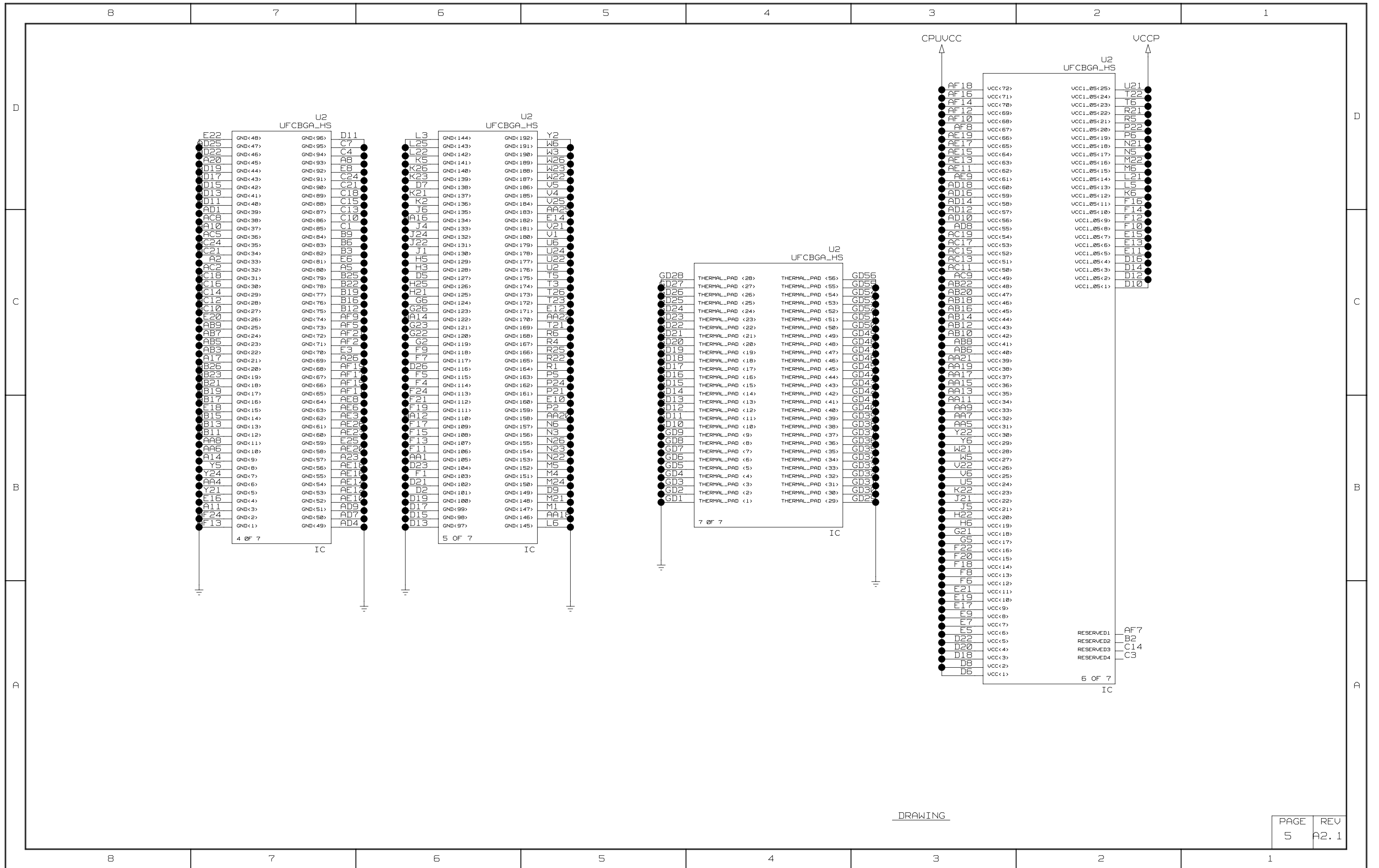
SYSTEM BLOCK DIAGRAM



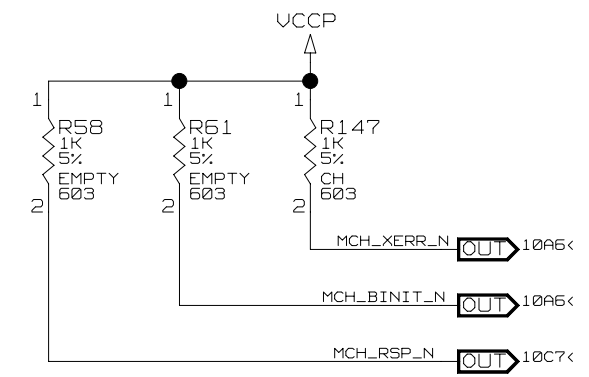
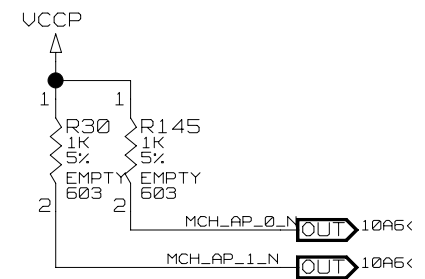
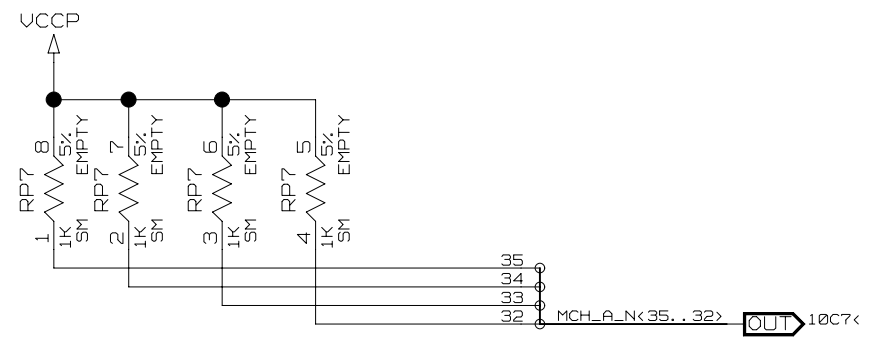
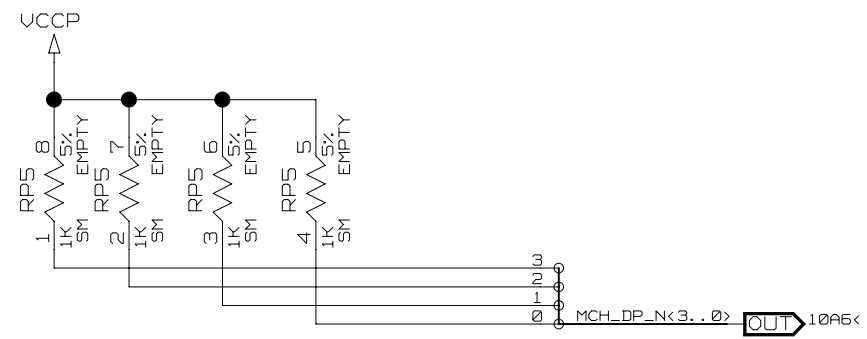
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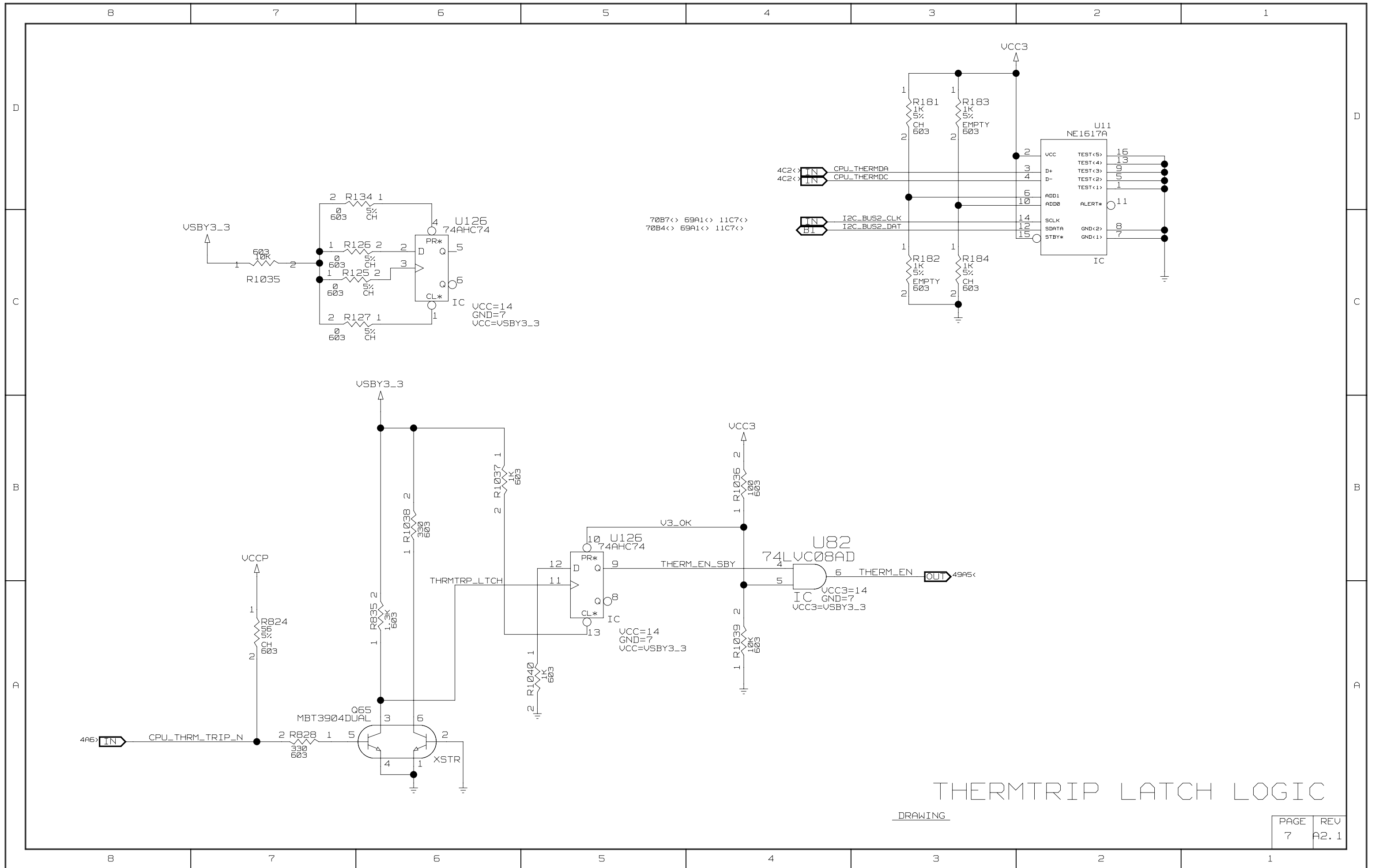
INTEL (R) DRAWING (R) PENTIUM M PROCESSOR



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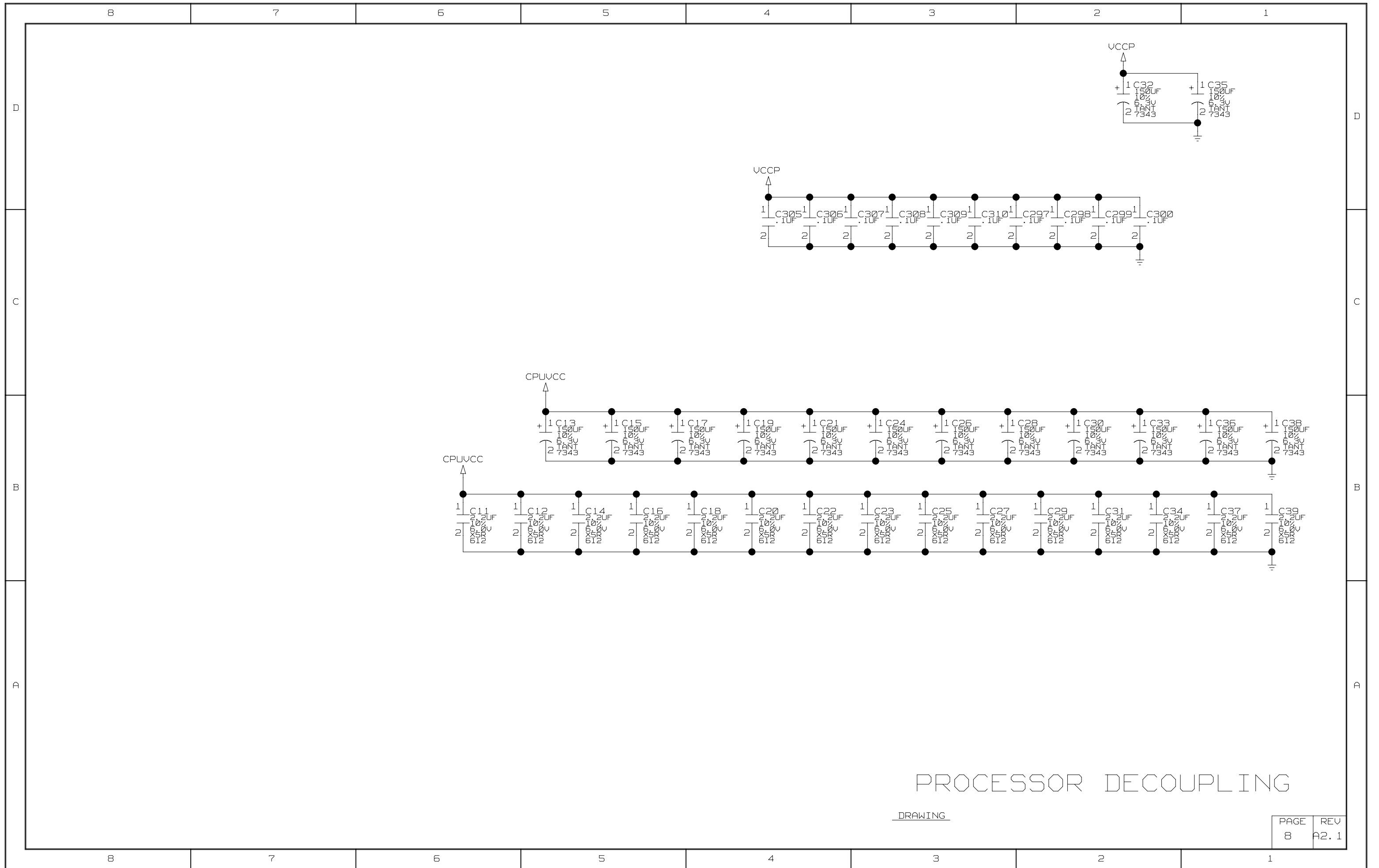


MCH PULL-UP RESISTORS
DRAWING



THERMTRIP LATCH LOGIC

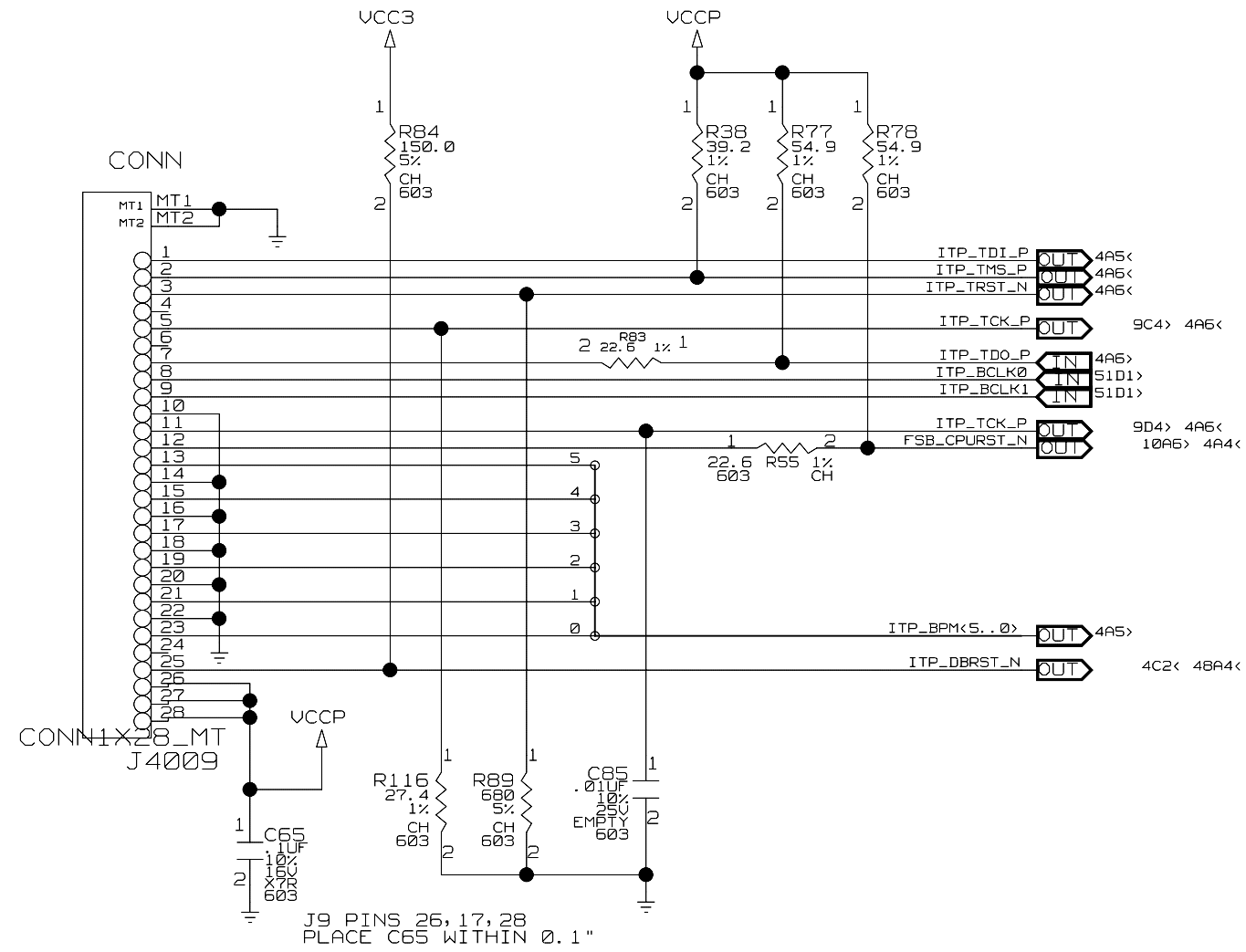
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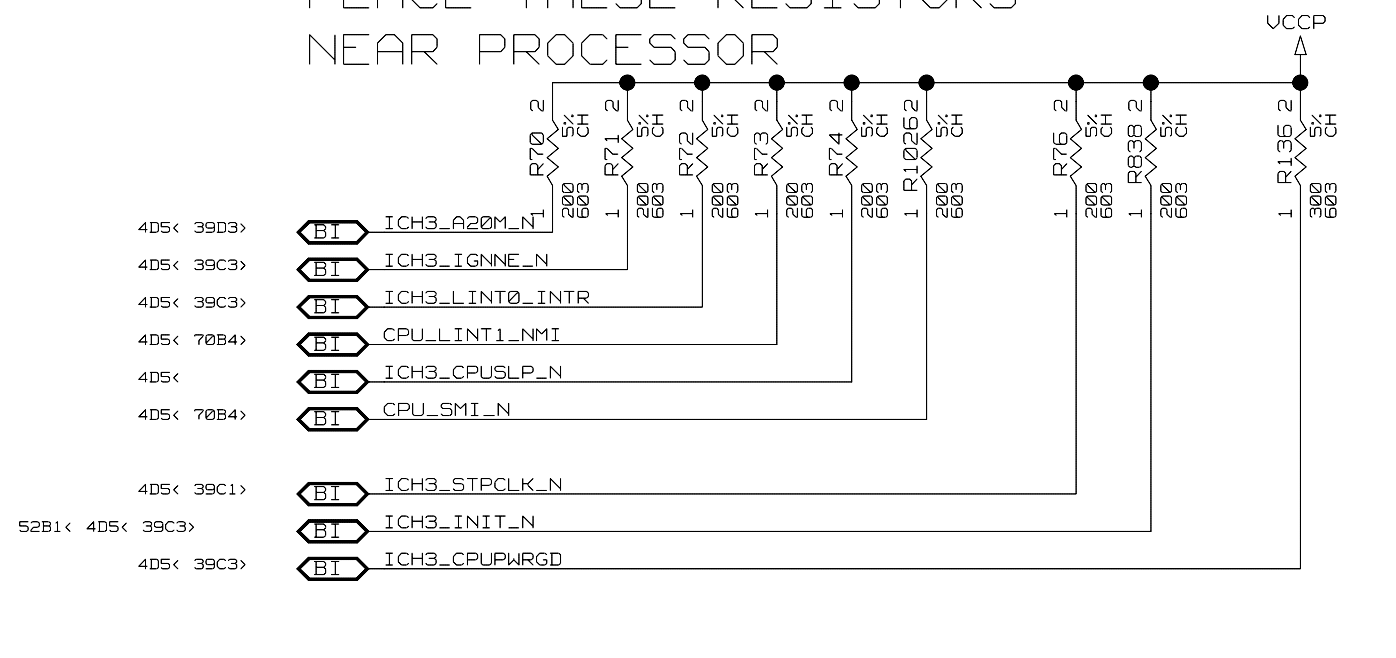
PROCESSOR DECOUPLING

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PLACE THESE RESISTORS
NEAR PROCESSOR



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INTEL^(R) E7501 MCH

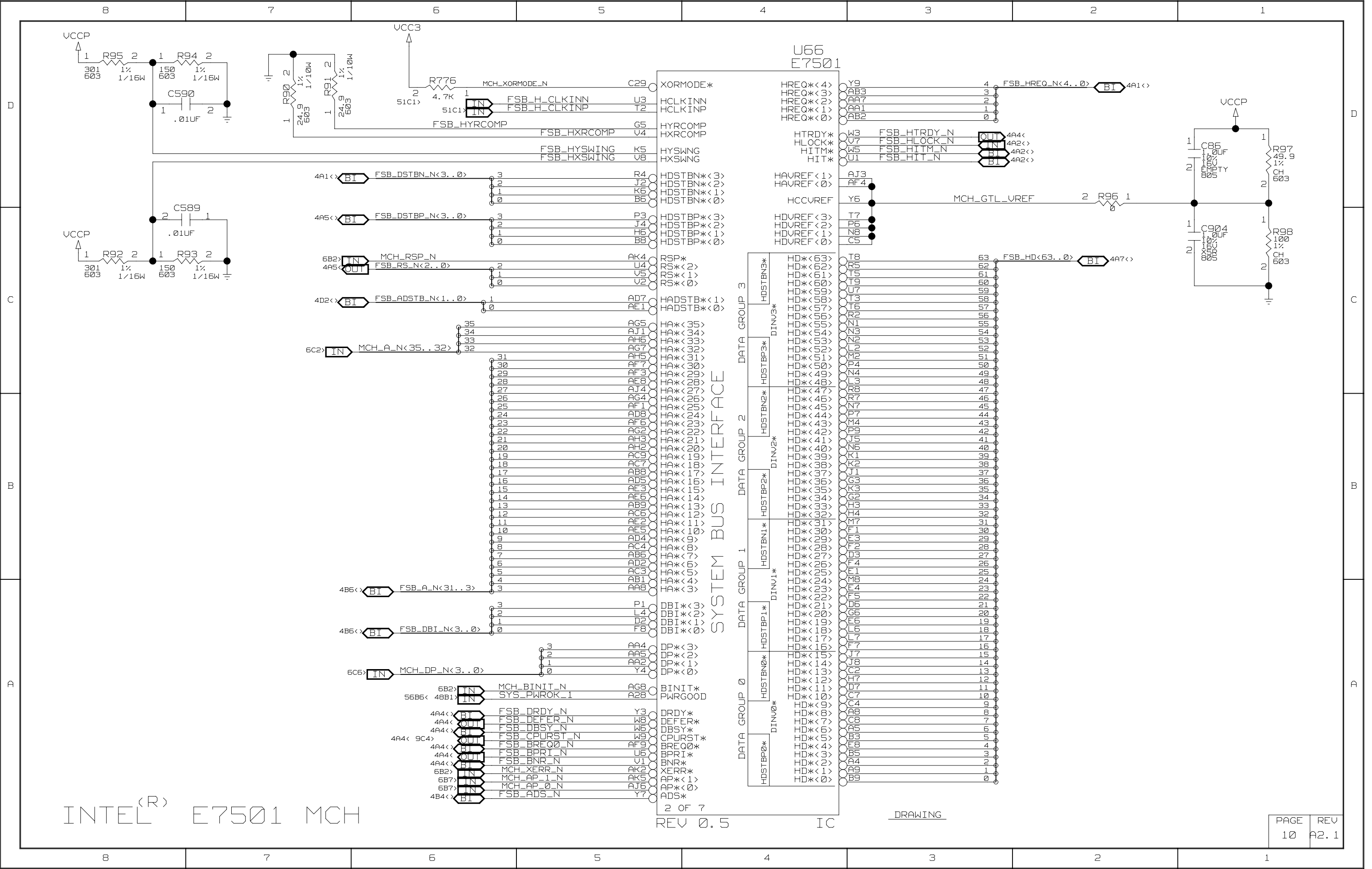
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SYSTEM BUS INTERFACE

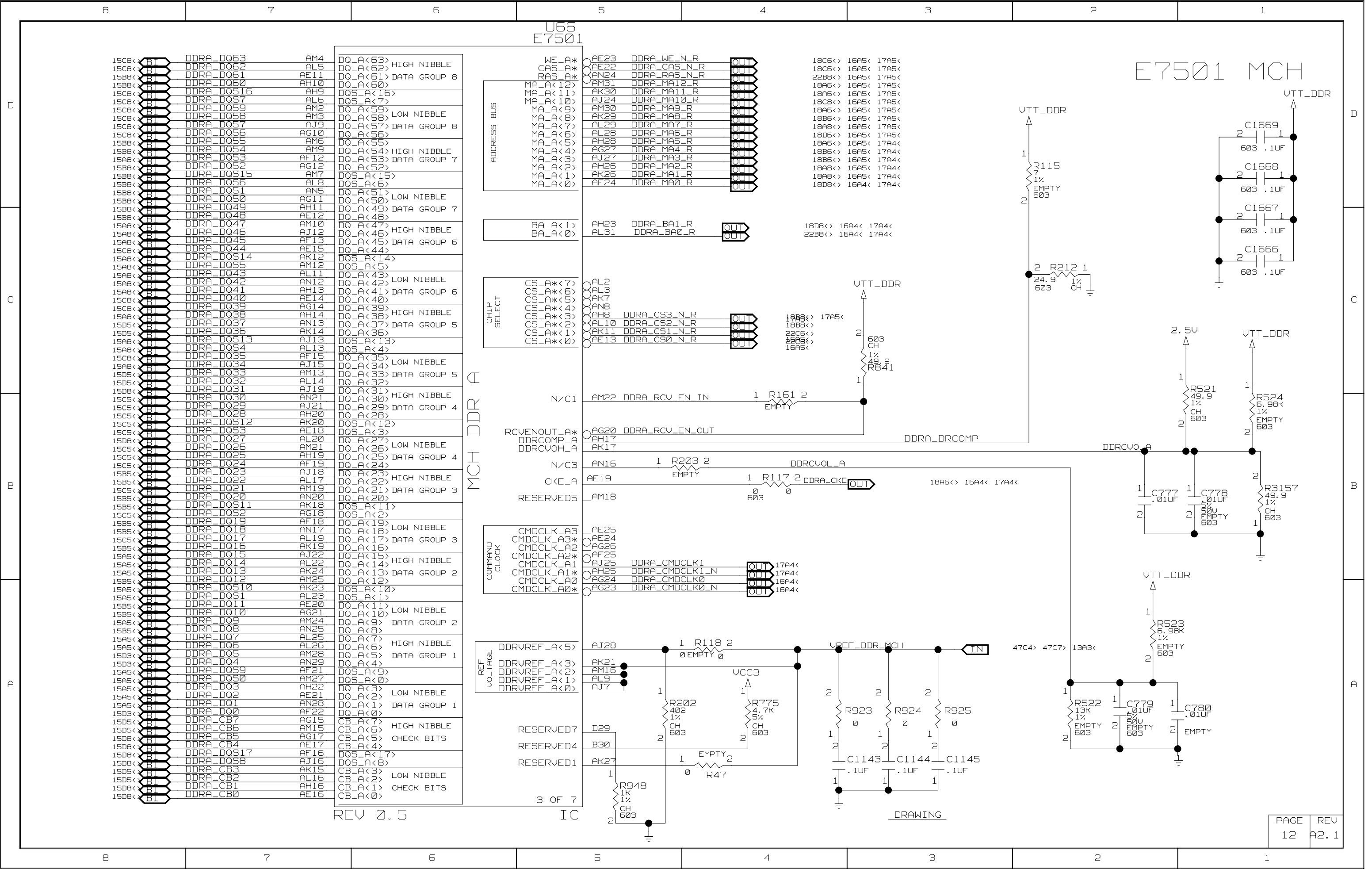




E7501 MCH

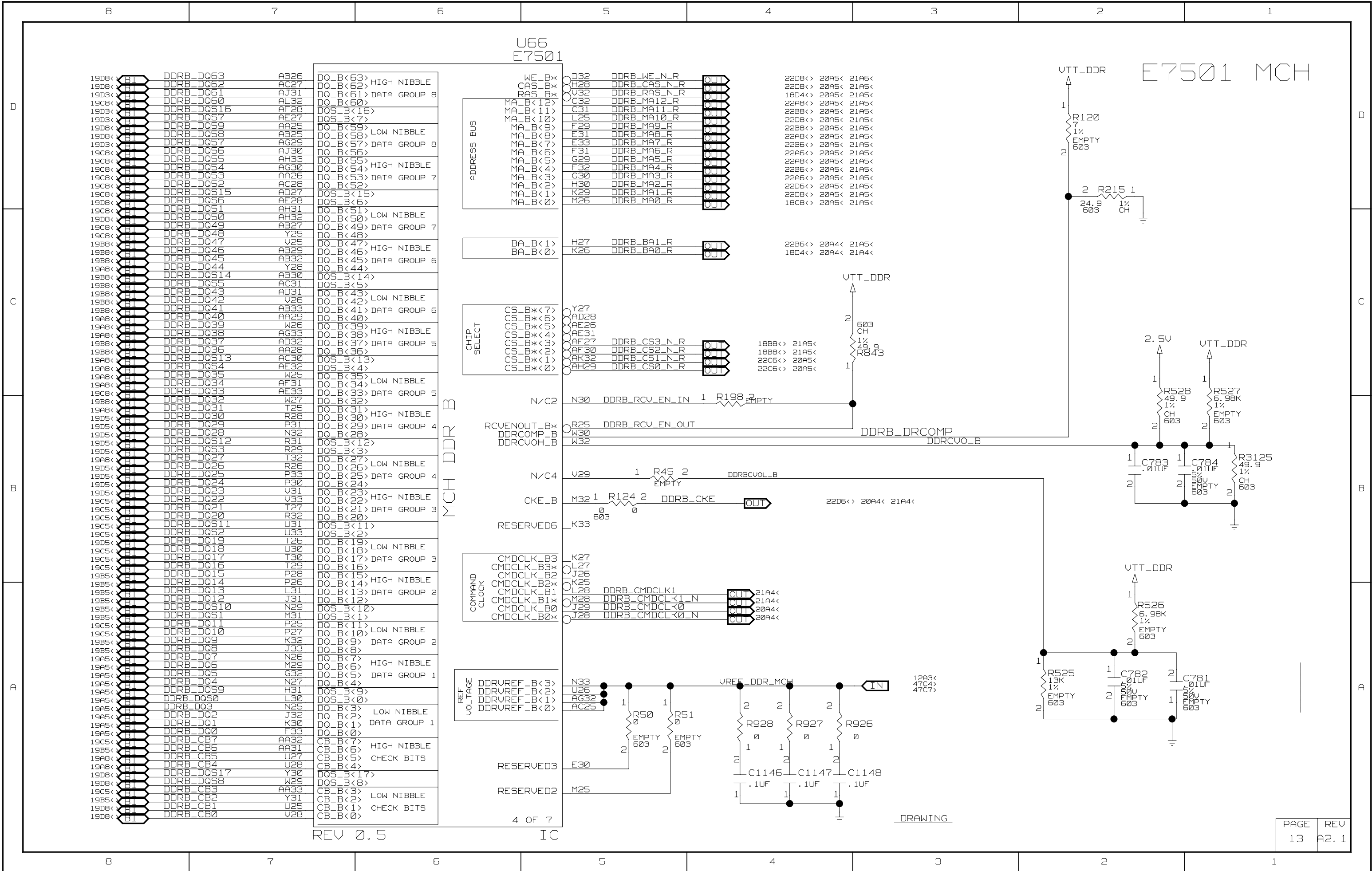
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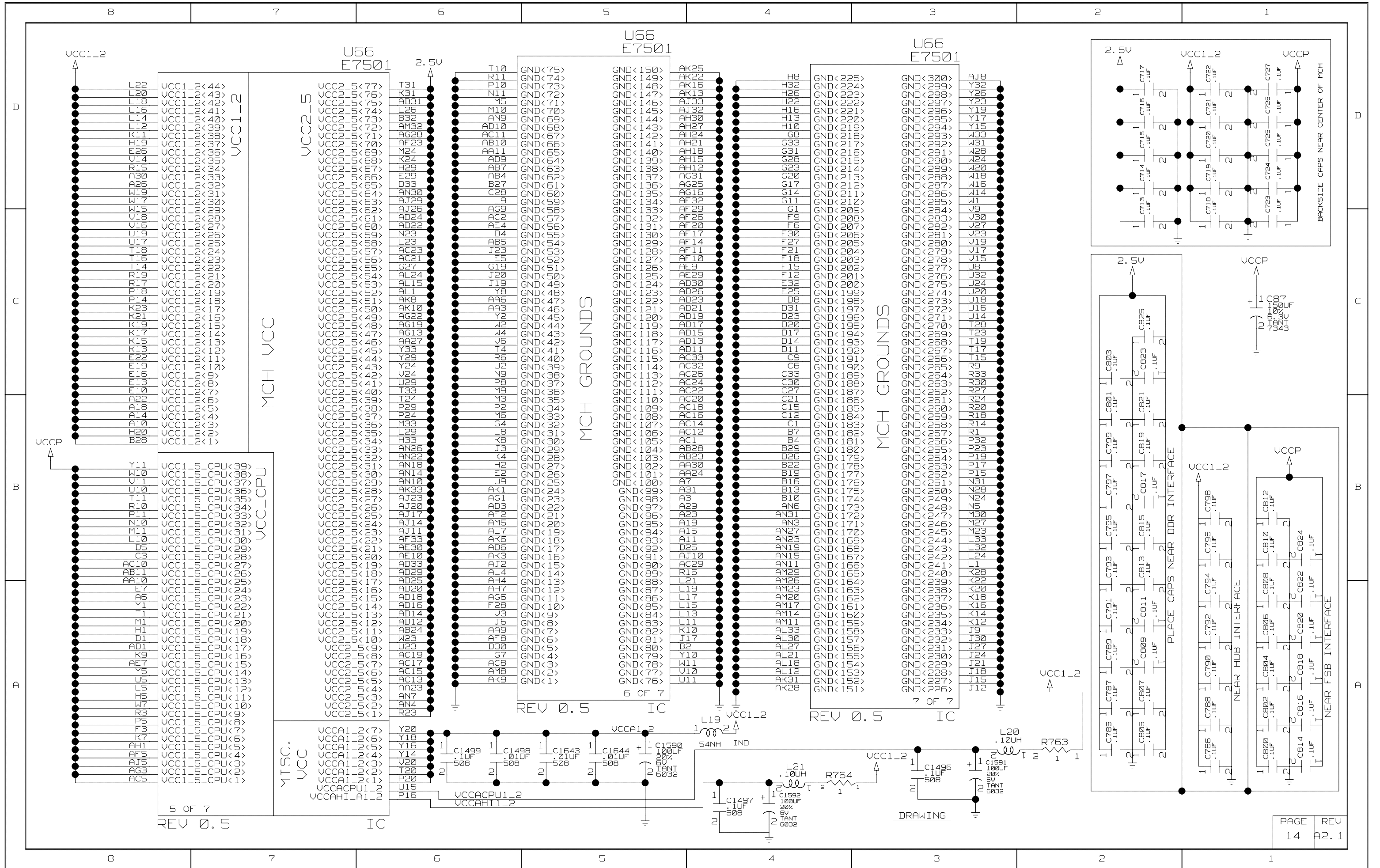


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IC

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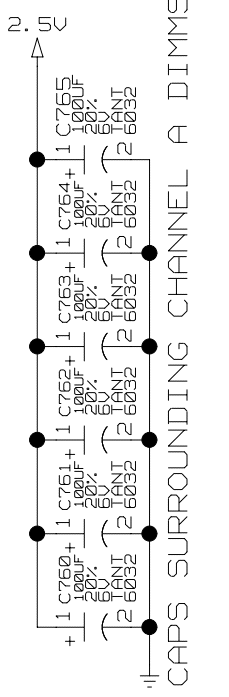
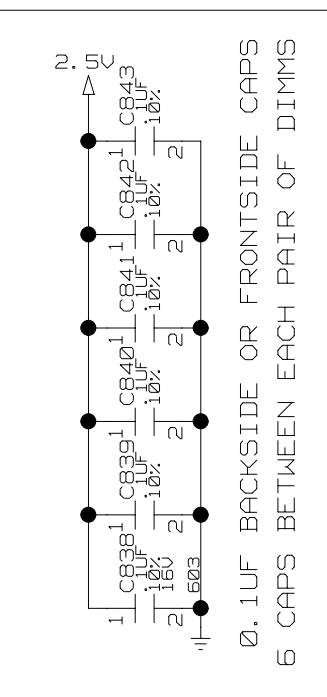
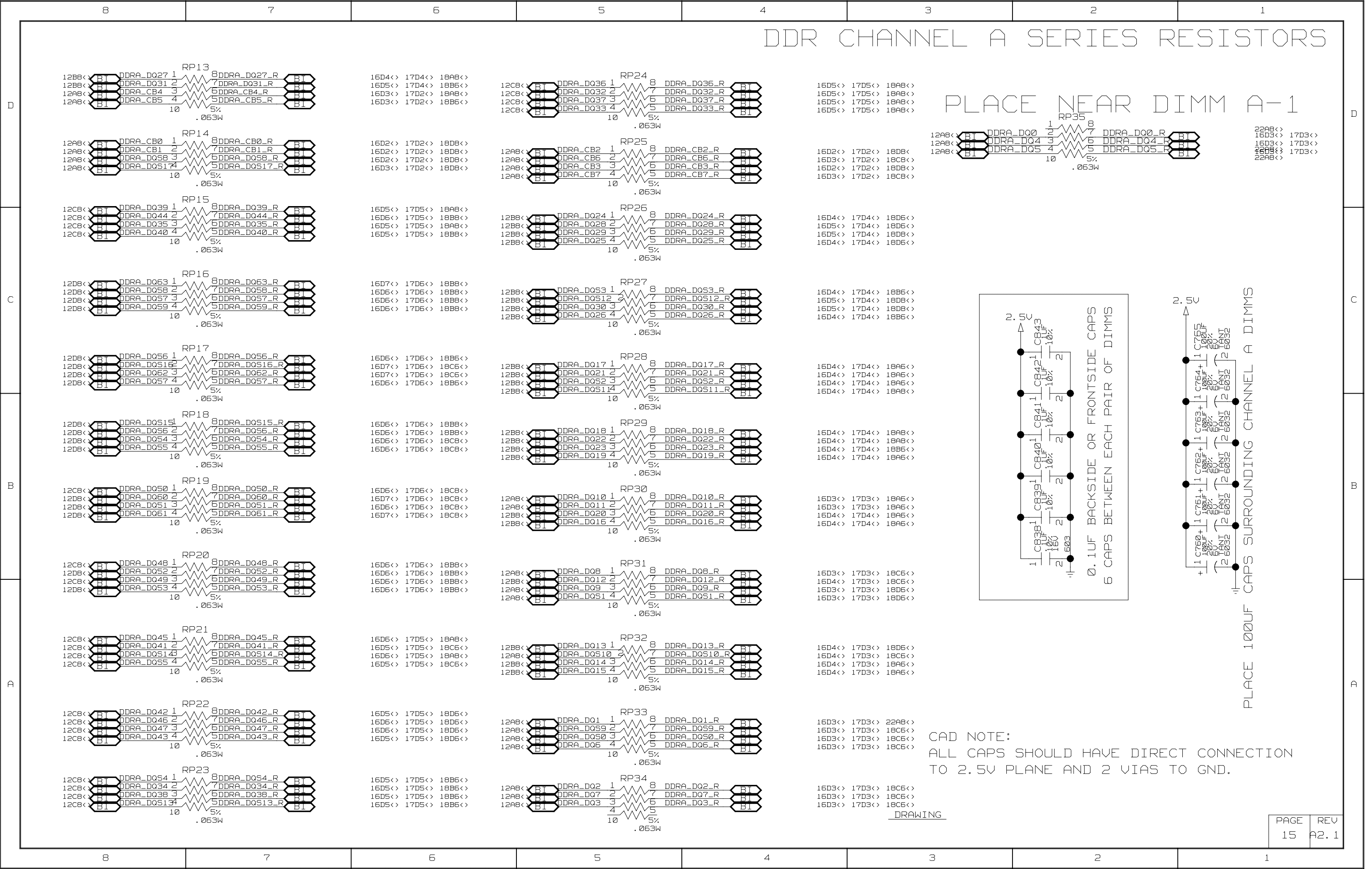
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REV 0.5 IC

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DDR CHANNEL A SERIES RESISTORS

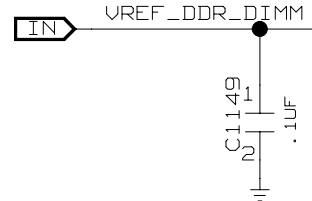
PLACE NEAR DIMM A-1



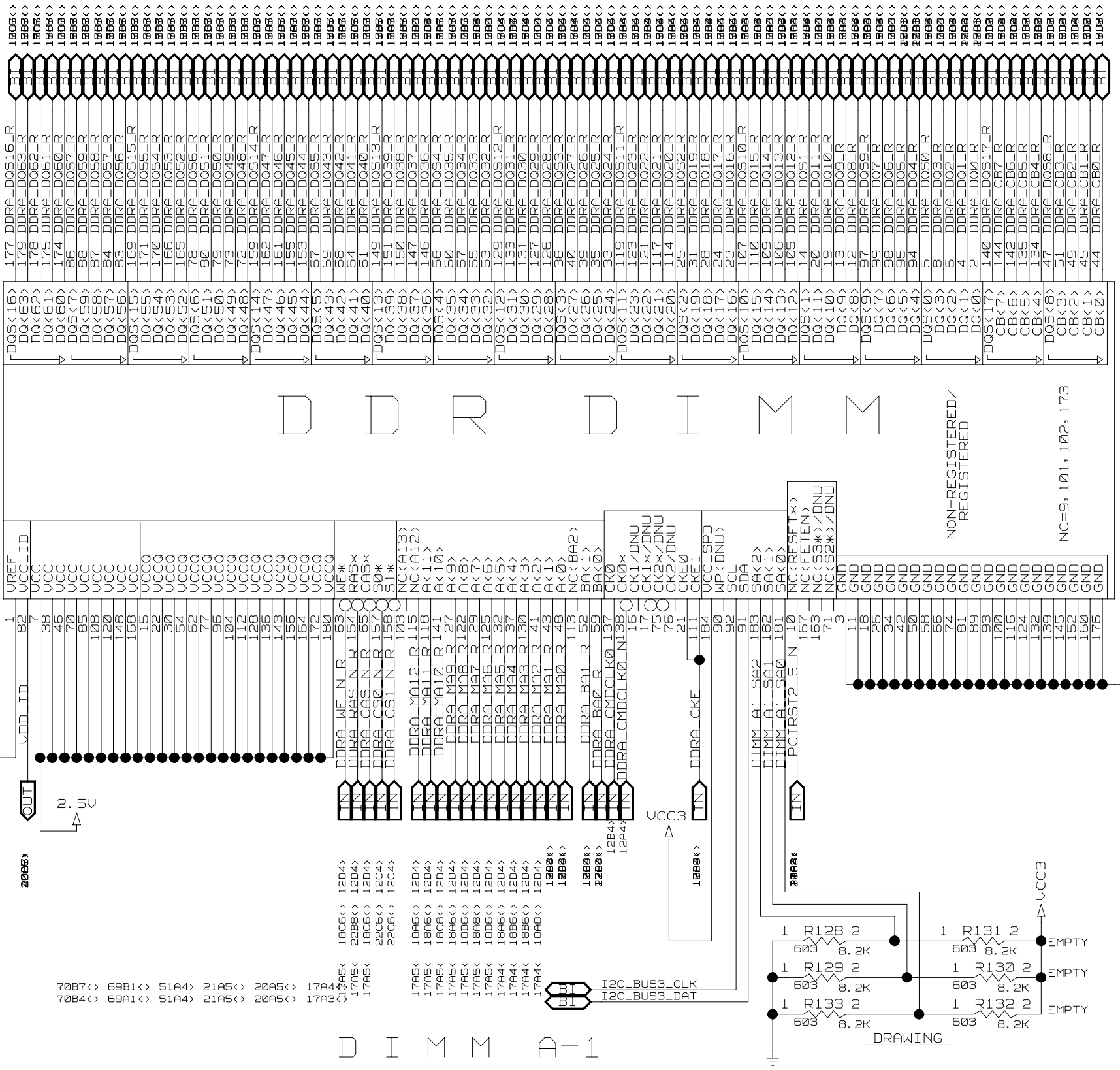
CAD NOTE:
ALL CAPS SHOULD HAVE DIRECT CONNECTION TO 2.5V PLANE AND 2 VIAS TO GND.

DRAWING

17B8<> 47C7> 47B4>
21B8<> 20B8<>

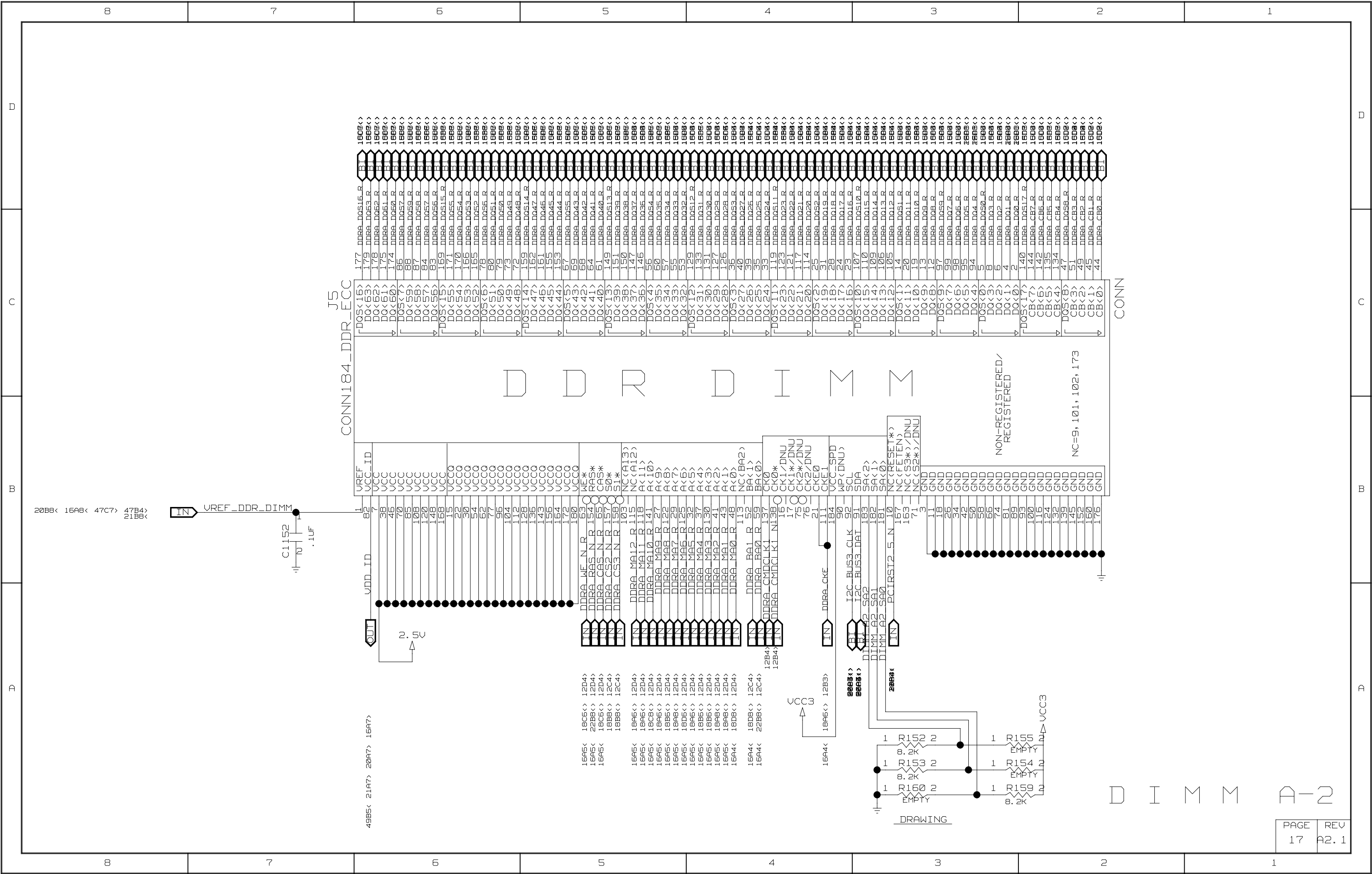


J2 CONN184_DDR_ECC

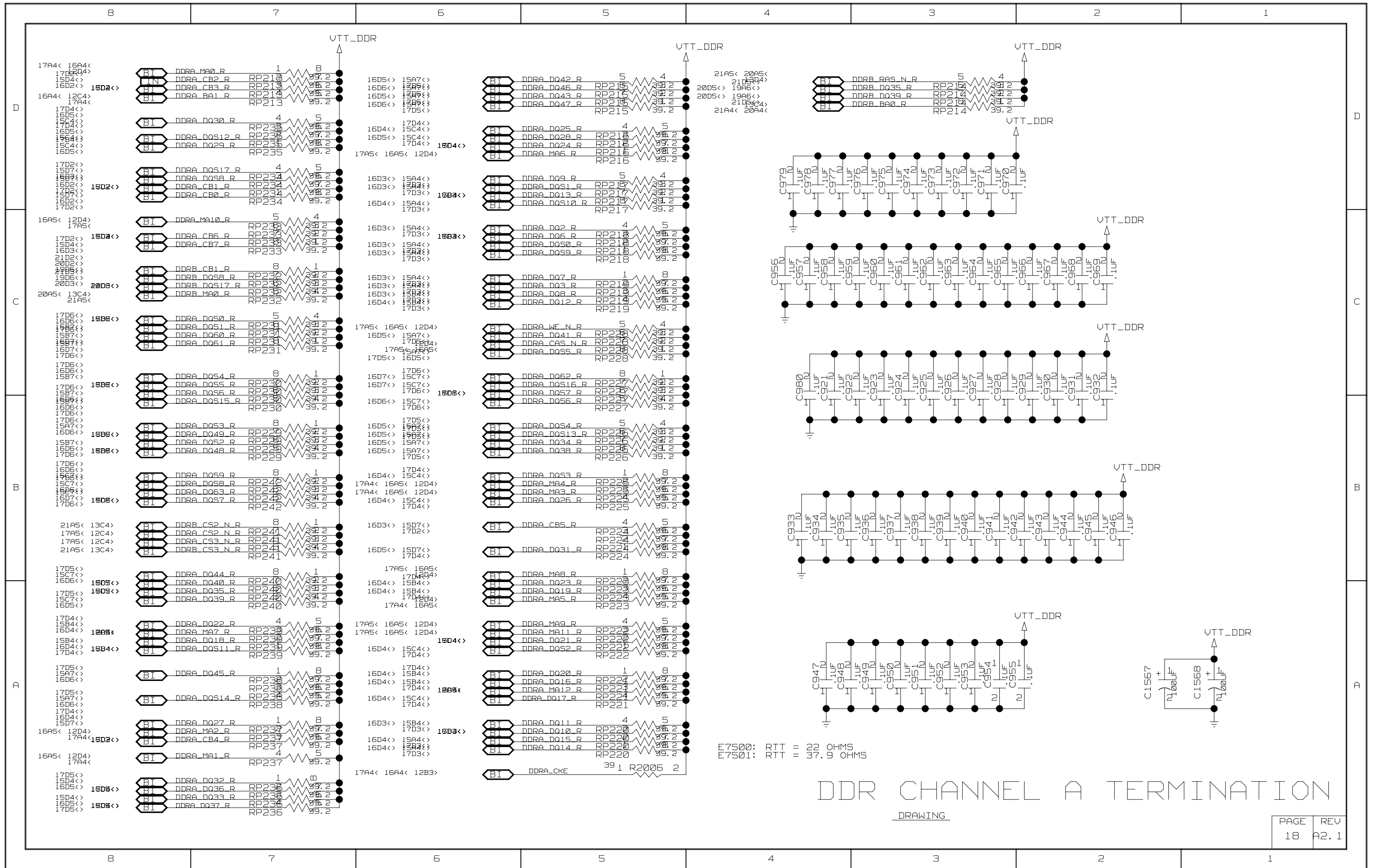


D I M M A - 1

PLACE DIMM A-1 CLOSEST TO MCH



DRAWING



DDR CHANNEL A TERMINATION

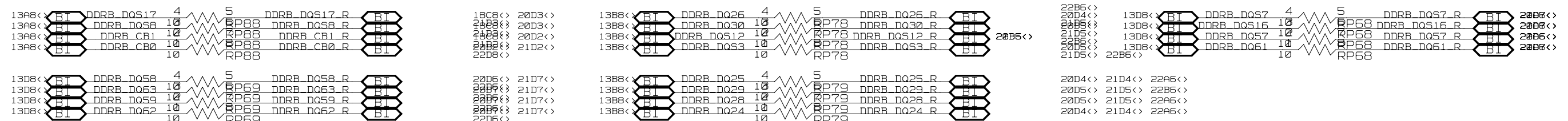
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DDR CHANNEL B SERIES RESISTORS

8 7 6 5 4 3 2 1

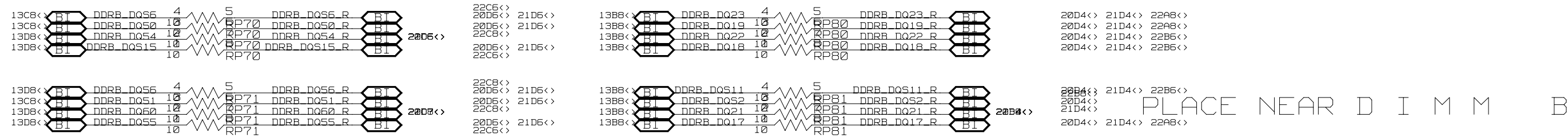
D

D

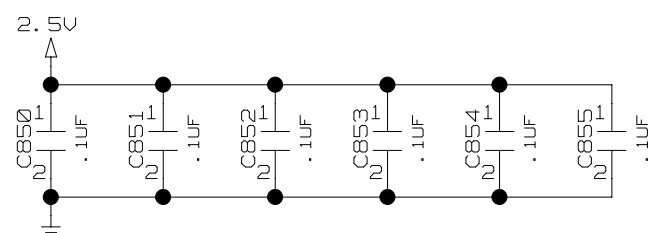


C

C



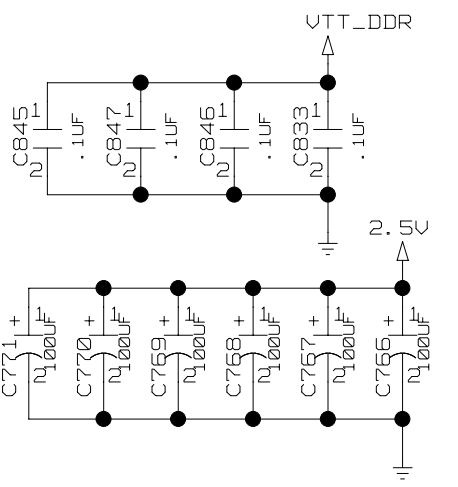
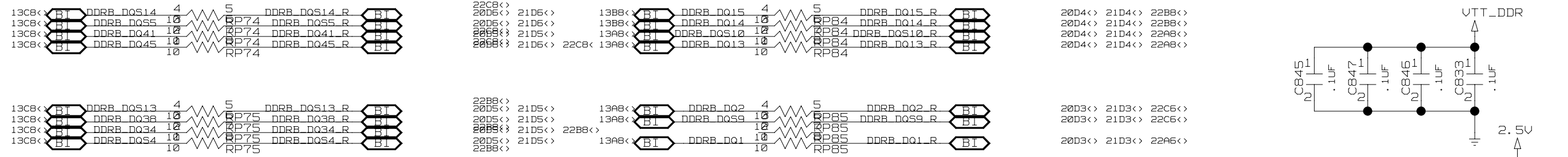
PLACE NEAR DIMM B-1



0.1 uF BACKSIDE OR FRONTSIDE CAPS
6 CAPS BETWEEN EACH PAIR OF DIMMS

B

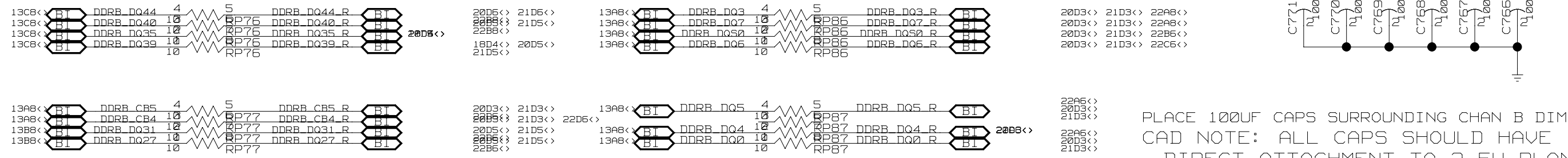
B



PLACE 100UF CAPS SURROUNDING CHAN B DIMMS
CAD NOTE: ALL CAPS SHOULD HAVE
DIRECT ATTACHMENT TO 2.5V PLANE,
AND 2 VIAS TO GND

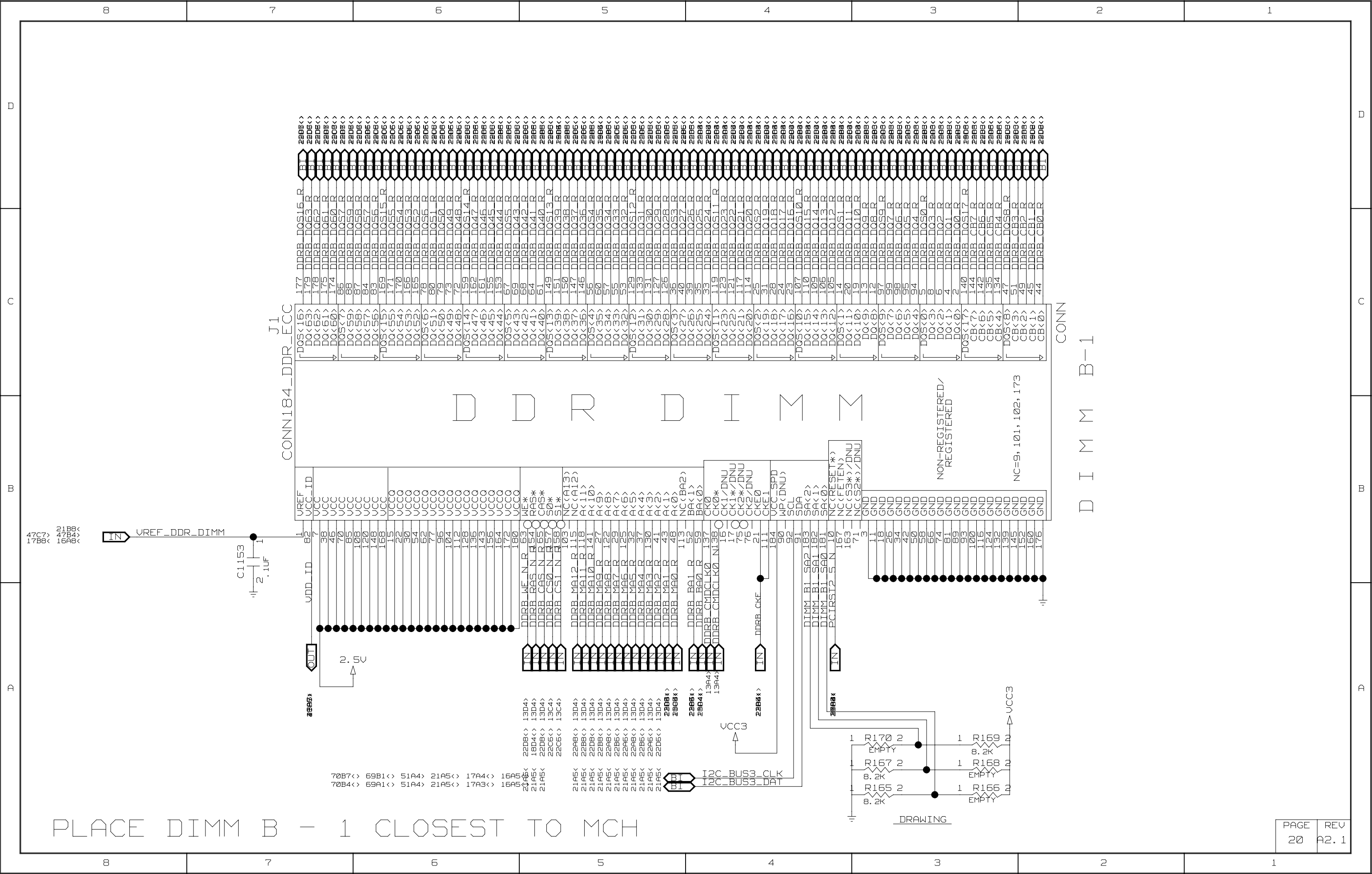
A

A



DRAWING

8 7 6 5 4 3 2 1

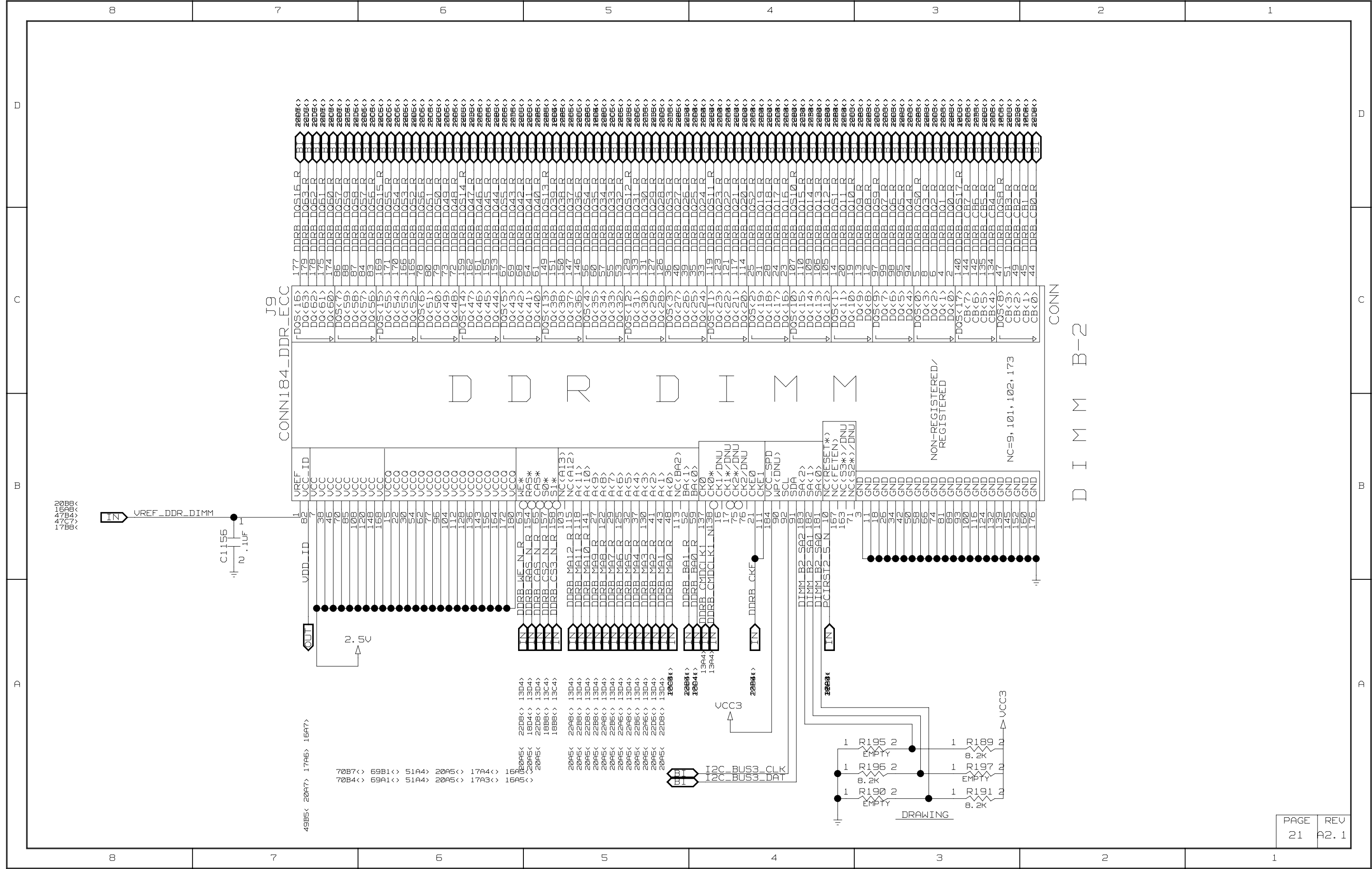


J1
CONN184_DDR_ECC

DDR DIMM

CONN
DIMM B-1

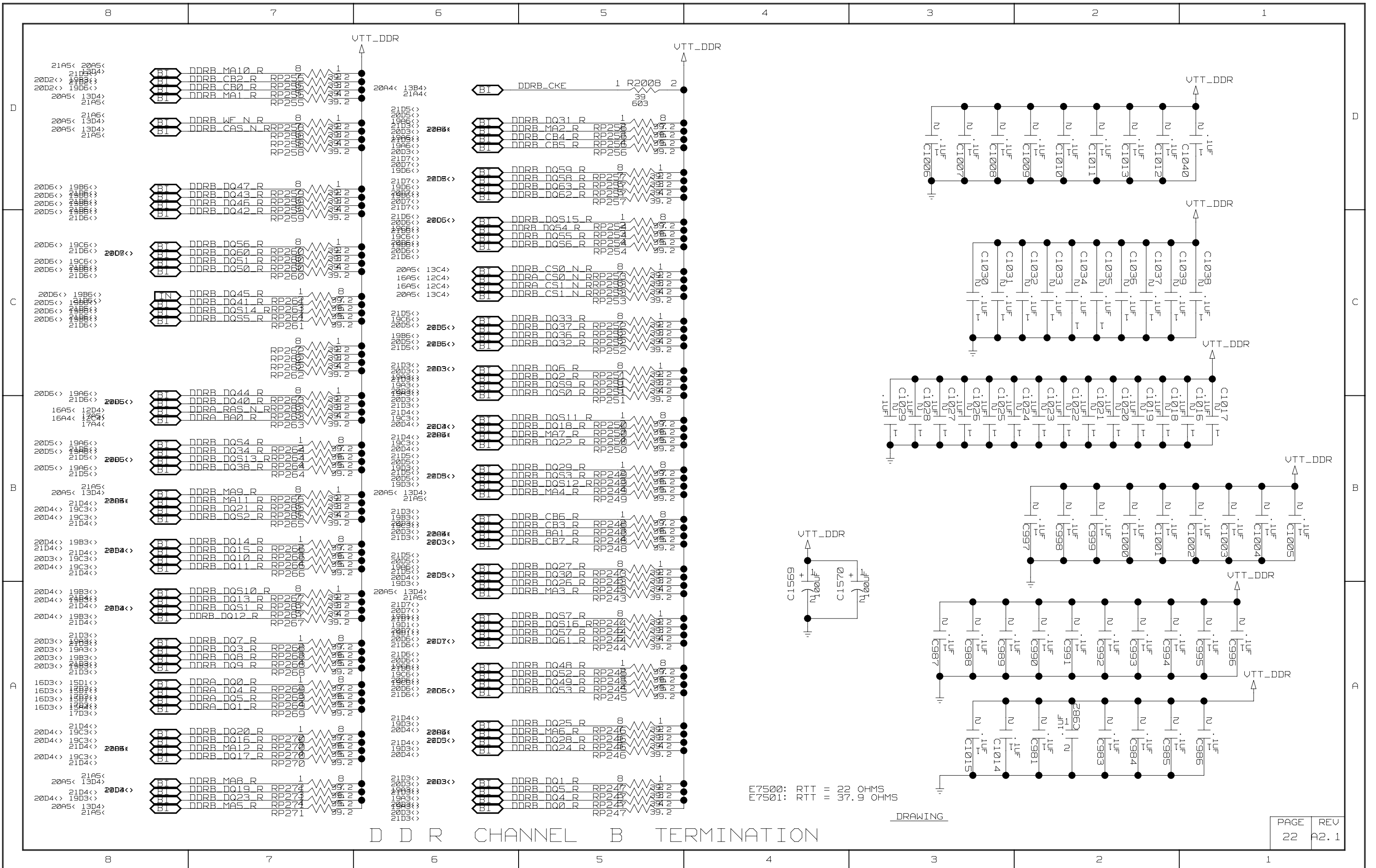
PLACE DIMM B - 1 CLOSEST TO MCH



20B8<
16A6<
47B4>
47C7>
17B8<

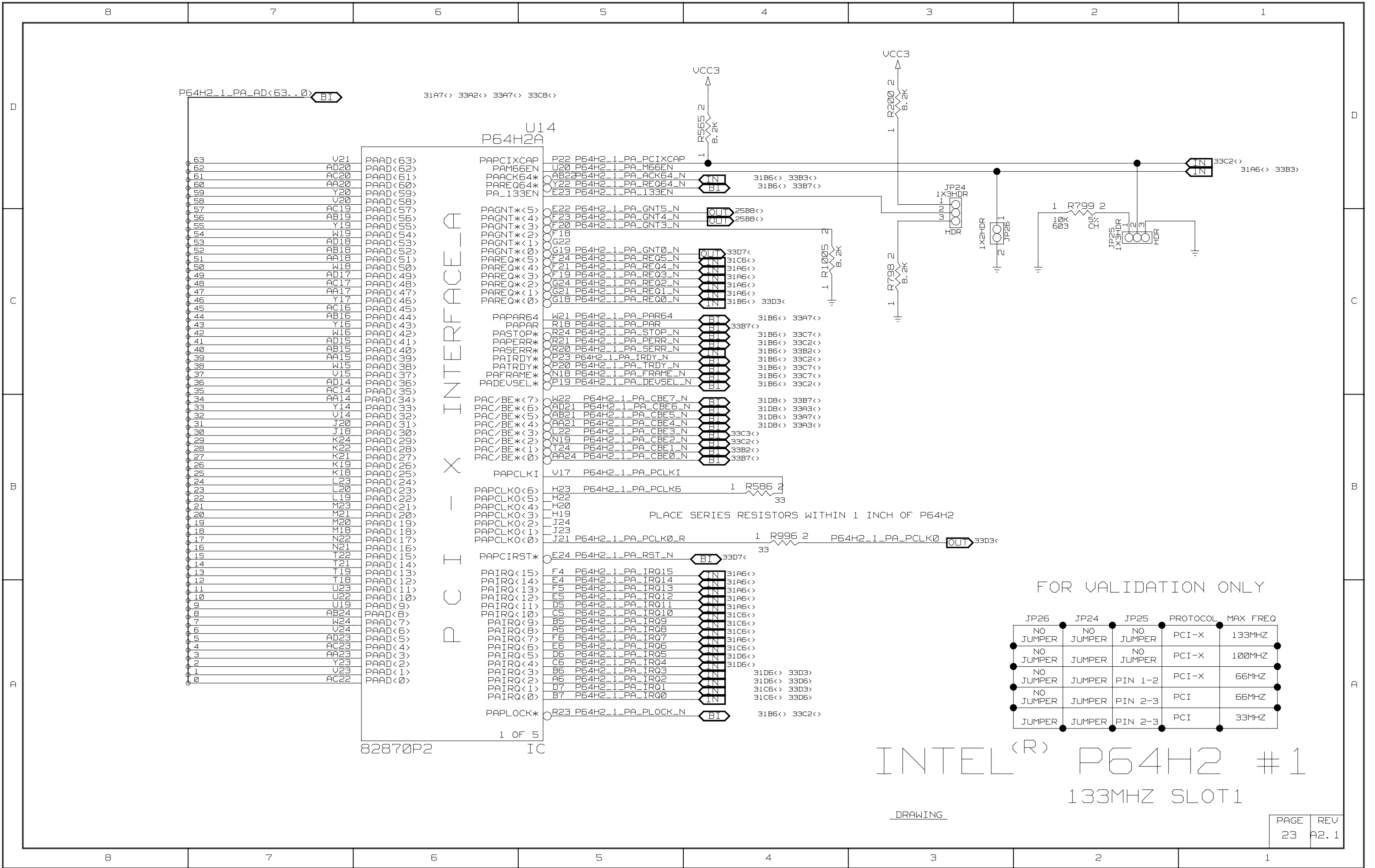
J9
CONN184_DDR_ECC

UDD_ID	VREF_ID	Signal	Pin	Notes
82	82	VREF	1	
36	36	VCC	2	
40	40	VCC	3	
70	70	VCC	4	
85	85	VCC	5	
108	108	VCC	6	
120	120	VCC	7	
148	148	VCC	8	
168	168	VCC	9	
15	15	VCC	10	
22	22	VCC	11	
34	34	VCC	12	
54	54	VCC	13	
62	62	VCC	14	
77	77	VCC	15	
96	96	VCC	16	
112	112	VCC	17	
128	128	VCC	18	
139	139	VCC	19	
149	149	VCC	20	
150	150	VCC	21	
164	164	VCC	22	
172	172	VCC	23	
180	180	VCC	24	
63	63	ME*	25	
154	154	PA5*	26	
165	165	CA5*	27	
157	157	SA0*	28	
159	159	SA1*	29	
103	103	NC(A13)	30	
115	115	NC(A12)	31	
141	141	A<11>	32	
141	141	A<10>	33	
27	27	A<9>	34	
29	29	A<8>	35	
29	29	A<7>	36	
132	132	A<6>	37	
32	32	A<5>	38	
37	37	A<4>	39	
130	130	A<3>	40	
41	41	A<2>	41	
43	43	A<1>	42	
48	48	A<0>	43	
113	113	NC(BA2)	44	
59	59	BA<1>	45	
59	59	BA<0>	46	
137	137	CK0*	47	
137	137	CK1*/DNU	48	
16	16	CK2*/DNU	49	
75	75	CK3*/DNU	50	
76	76	CK4*/DNU	51	
21	21	CHE0	52	
111	111	CHE1	53	
184	184	VCC_SPD	54	
90	90	MP<DNU>	55	
92	92	SCL	56	
91	91	SDA	57	
183	183	DIMM_B2_SA2	58	
182	182	DIMM_B2_SA1	59	
181	181	DIMM_B2_SA0	60	
10	10	PCIRST2_S<N>	61	
157	157	NC(PRESET*)	62	
153	153	NC(FETEN)	63	
171	171	NC(S3*)/DNU	64	
171	171	NC(S2*)/DNU	65	
11	11	GND	66	
18	18	GND	67	
26	26	GND	68	
34	34	GND	69	
42	42	GND	70	
50	50	GND	71	
58	58	GND	72	
60	60	GND	73	
74	74	GND	74	
81	81	GND	75	
89	89	GND	76	
93	93	GND	77	
100	100	GND	78	
116	116	GND	79	
124	124	GND	80	
132	132	GND	81	
139	139	GND	82	
145	145	GND	83	
152	152	GND	84	
160	160	GND	85	
176	176	GND	86	



E7500: RTT = 22 OHMS
E7501: RTT = 37.9 OHMS

DRAWING



P C I - X I N T E R F A C E - A

63	V21	PAAD<63>
62	AD20	PAAD<62>
61	AC20	PAAD<61>
60	AA20	PAAD<60>
59	Y20	PAAD<59>
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49	AD17	PAAD<49>
48	AC17	PAAD<48>
47	AA17	PAAD<47>
46	Y17	PAAD<46>
45	AC16	PAAD<45>
44	AB16	PAAD<44>
43	Y16	PAAD<43>
42	W16	PAAD<42>
41	AD15	PAAD<41>
40	AB15	PAAD<40>
39	AA15	PAAD<39>
38	W15	PAAD<38>
37	V15	PAAD<37>
36	AD14	PAAD<36>
35	AC14	PAAD<35>
34	AA14	PAAD<34>
33	Y14	PAAD<33>
32	V14	PAAD<32>
31	J20	PAAD<31>
30	J18	PAAD<30>
29	K24	PAAD<29>
28	K22	PAAD<28>
27	K21	PAAD<27>
26	K19	PAAD<26>
25	K18	PAAD<25>
24	L23	PAAD<24>
23	L20	PAAD<23>
22	L19	PAAD<22>
21	M23	PAAD<21>
20	M21	PAAD<20>
19	M20	PAAD<19>
18	M18	PAAD<18>
17	N22	PAAD<17>
16	N21	PAAD<16>
15	T22	PAAD<15>
14	T21	PAAD<14>
13	T19	PAAD<13>
12	T18	PAAD<12>
11	U23	PAAD<11>
10	U22	PAAD<10>
9	U19	PAAD<9>
8	AB24	PAAD<8>
7	W24	PAAD<7>
6	V24	PAAD<6>
5	AD23	PAAD<5>
4	AC23	PAAD<4>
3	AA23	PAAD<3>
2	Y23	PAAD<2>
1	V23	PAAD<1>
0	AC22	PAAD<0>

PAPCIXCAP	P22 P64H2_1_PA_PCIXCAP	
PAM66EN	U20 P64H2_1_PA_M66EN	
PAACK64*	AB22 P64H2_1_PA_ACK64_N	31B6<> 33B3<>
PAREQ64*	Y22 P64H2_1_PA_REQ64_N	31B6<> 33B7<>
PA_133EN	E23 P64H2_1_PA_133EN	
PAGNT*<5>	F22 P64H2_1_PA_GNT5_N	2588<>
PAGNT*<4>	F23 P64H2_1_PA_GNT4_N	2588<>
PAGNT*<3>	F20 P64H2_1_PA_GNT3_N	
PAGNT*<2>	F18	
PAGNT*<1>	G22	
PAGNT*<0>	G19 P64H2_1_PA_GNT0_N	33D7<
PAREQ*<5>	F24 P64H2_1_PA_REQ5_N	31C6<>
PAREQ*<4>	F21 P64H2_1_PA_REQ4_N	31A6<>
PAREQ*<3>	F19 P64H2_1_PA_REQ3_N	31A6<>
PAREQ*<2>	G24 P64H2_1_PA_REQ2_N	31A6<>
PAREQ*<1>	G21 P64H2_1_PA_REQ1_N	31A6<>
PAREQ*<0>	G18 P64H2_1_PA_REQ0_N	31B6<> 33D3<
PAPAR64	W21 P64H2_1_PA_PAR64	31B6<> 33A7<>
PAPAR	R18 P64H2_1_PA_PAR	33B7<>
PASTOP*	R24 P64H2_1_PA_STOP_N	31B6<> 33C7<>
PAPER*	R21 P64H2_1_PA_PERR_N	31B6<> 33C2<>
PASERR*	R20 P64H2_1_PA_SERR_N	31B6<> 33B2<>
PAIRDY*	P23 P64H2_1_PA_IRDY_N	31B6<> 33C2<>
PATRDY*	P20 P64H2_1_PA_TRDY_N	31B6<> 33C7<>
PAFRAME*	N18 P64H2_1_PA_FRAME_N	31B6<> 33C7<>
PADEVSEL*	P19 P64H2_1_PA_DEVSEL_N	31B6<> 33C2<>
PAC/BE*<7>	W22 P64H2_1_PA_CBE7_N	31D8<> 33B7<>
PAC/BE*<6>	AD21 P64H2_1_PA_CBE6_N	31D8<> 33A3<>
PAC/BE*<5>	AB21 P64H2_1_PA_CBE5_N	31D8<> 33A7<>
PAC/BE*<4>	AA21 P64H2_1_PA_CBE4_N	31D8<> 33A3<>
PAC/BE*<3>	L22 P64H2_1_PA_CBE3_N	33C3<>
PAC/BE*<2>	N19 P64H2_1_PA_CBE2_N	33C2<>
PAC/BE*<1>	T24 P64H2_1_PA_CBE1_N	33B2<>
PAC/BE*<0>	AA24 P64H2_1_PA_CBE0_N	33B7<>
PAPCLKI	V17 P64H2_1_PA_PCLKI	
PAPCLK0<6>	H23 P64H2_1_PA_PCLK6	1 R586 2 33
PAPCLK0<5>	H22	
PAPCLK0<4>	H20	
PAPCLK0<3>	H19	
PAPCLK0<2>	J24	
PAPCLK0<1>	J23	
PAPCLK0<0>	J21 P64H2_1_PA_PCLK0_R	1 R996 2 P64H2_1_PA_PCLK0 33D3<
PAPCIRST*	E24 P64H2_1_PA_RST_N	33D7<
PAIRQ<15>	F4 P64H2_1_PA_IRQ15	31A6<>
PAIRQ<14>	E4 P64H2_1_PA_IRQ14	31A6<>
PAIRQ<13>	F5 P64H2_1_PA_IRQ13	31A6<>
PAIRQ<12>	E5 P64H2_1_PA_IRQ12	31A6<>
PAIRQ<11>	D5 P64H2_1_PA_IRQ11	31A6<>
PAIRQ<10>	C5 P64H2_1_PA_IRQ10	31C6<>
PAIRQ<9>	B5 P64H2_1_PA_IRQ9	31C6<>
PAIRQ<8>	A5 P64H2_1_PA_IRQ8	31C6<>
PAIRQ<7>	F6 P64H2_1_PA_IRQ7	31A6<>
PAIRQ<6>	E6 P64H2_1_PA_IRQ6	31C6<>
PAIRQ<5>	D6 P64H2_1_PA_IRQ5	31D6<>
PAIRQ<4>	C6 P64H2_1_PA_IRQ4	31D6<>
PAIRQ<3>	B6 P64H2_1_PA_IRQ3	31D6<>
PAIRQ<2>	A6 P64H2_1_PA_IRQ2	31D6<> 33D3<
PAIRQ<1>	D7 P64H2_1_PA_IRQ1	31C6<> 33D3<
PAIRQ<0>	B7 P64H2_1_PA_IRQ0	31C6<> 33D6<
PAPLOCK*	R23 P64H2_1_PA_PLOCK_N	31B6<> 33C2<>

82870P2 IC 1 OF 5

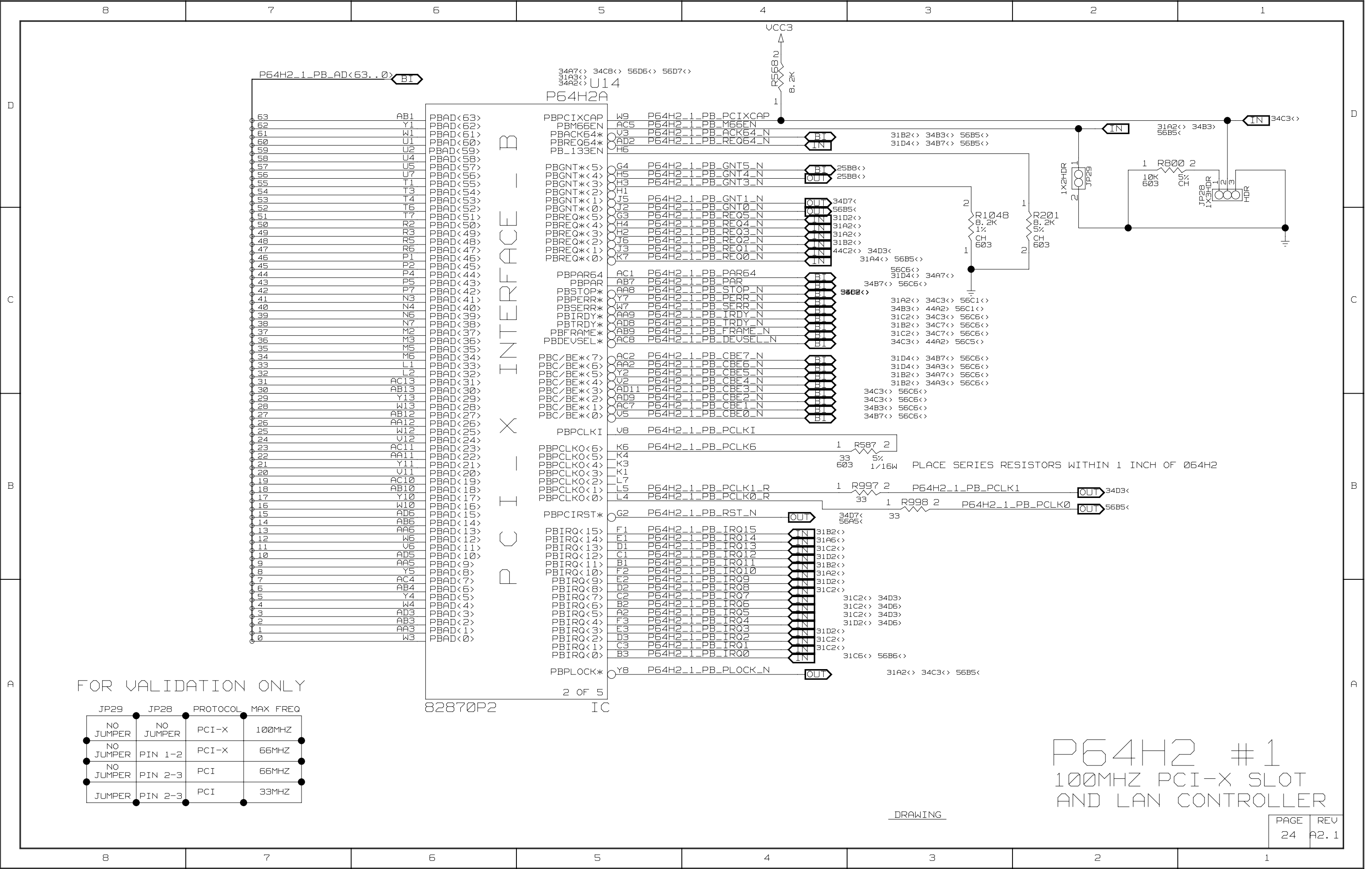
PLACE SERIES RESISTORS WITHIN 1 INCH OF P64H2

FOR VALIDATION ONLY

JP26	JP24	JP25	PROTOCOL	MAX FREQ
NO JUMPER	NO JUMPER	NO JUMPER	PCI-X	133MHZ
NO JUMPER	JUMPER	NO JUMPER	PCI-X	100MHZ
NO JUMPER	JUMPER	PIN 1-2	PCI-X	65MHZ
NO JUMPER	JUMPER	PIN 2-3	PCI	65MHZ
JUMPER	JUMPER	PIN 2-3	PCI	33MHZ

INTEL (R) P64H2 #1
133MHZ SLOT1

DRAWING



PCI-X INTERFACE - B

P64H2_1_PB_AD<63..0>

63	AB1	PBAD<63>
62	Y1	PBAD<62>
61	W1	PBAD<61>
60	U1	PBAD<60>
59	U2	PBAD<59>
58	U4	PBAD<58>
57	U5	PBAD<57>
56	U7	PBAD<56>
55	T1	PBAD<55>
54	T3	PBAD<54>
53	T4	PBAD<53>
52	T6	PBAD<52>
51	T7	PBAD<51>
50	R2	PBAD<50>
49	R3	PBAD<49>
48	R5	PBAD<48>
47	R6	PBAD<47>
46	P1	PBAD<46>
45	P2	PBAD<45>
44	P4	PBAD<44>
43	P5	PBAD<43>
42	P7	PBAD<42>
41	N3	PBAD<41>
40	N4	PBAD<40>
39	N6	PBAD<39>
38	N7	PBAD<38>
37	M2	PBAD<37>
36	M3	PBAD<36>
35	M5	PBAD<35>
34	M6	PBAD<34>
33	L1	PBAD<33>
32	L2	PBAD<32>
31	AC13	PBAD<31>
30	AB13	PBAD<30>
29	Y13	PBAD<29>
28	W13	PBAD<28>
27	AB12	PBAD<27>
26	AA12	PBAD<26>
25	W12	PBAD<25>
24	V12	PBAD<24>
23	AC11	PBAD<23>
22	AA11	PBAD<22>
21	Y11	PBAD<21>
20	V11	PBAD<20>
19	AC10	PBAD<19>
18	AB10	PBAD<18>
17	Y10	PBAD<17>
16	W10	PBAD<16>
15	AD6	PBAD<15>
14	AB6	PBAD<14>
13	AA6	PBAD<13>
12	W6	PBAD<12>
11	V6	PBAD<11>
10	AD5	PBAD<10>
9	AA5	PBAD<9>
8	Y5	PBAD<8>
7	AC4	PBAD<7>
6	AB4	PBAD<6>
5	Y4	PBAD<5>
4	W4	PBAD<4>
3	AD3	PBAD<3>
2	AB3	PBAD<2>
1	AA3	PBAD<1>
0	W3	PBAD<0>

U14
P64H2A

W9	P54H2_1_PB_PCIXCAP	PBPCIXCAP
AC5	P54H2_1_PB_M66EN	PBM66EN
U3	P54H2_1_PB_ACK64_N	PBACK64*
AD2	P54H2_1_PB_REQ64_N	PBREQ64*
H6		PB_133EN
G4	P54H2_1_PB_GNT5_N	PBGNT* < 5 >
H5	P54H2_1_PB_GNT4_N	PBGNT* < 4 >
H3	P54H2_1_PB_GNT3_N	PBGNT* < 3 >
H1	P54H2_1_PB_GNT1_N	PBGNT* < 2 >
J5	P54H2_1_PB_GNT1_N	PBGNT* < 1 >
J2	P54H2_1_PB_GNT0_N	PBGNT* < 0 >
G3	P54H2_1_PB_REQ5_N	PBREQ* < 5 >
H4	P54H2_1_PB_REQ4_N	PBREQ* < 4 >
H2	P54H2_1_PB_REQ3_N	PBREQ* < 3 >
J6	P54H2_1_PB_REQ2_N	PBREQ* < 2 >
J3	P54H2_1_PB_REQ1_N	PBREQ* < 1 >
K7	P54H2_1_PB_REQ0_N	PBREQ* < 0 >
AC1	P54H2_1_PB_PAR64	PBPAR64
AB7	P54H2_1_PB_PAR	PBPAR
AA8	P54H2_1_PB_STOP_N	PBSTOP*
Y7	P54H2_1_PB_PERR_N	PBPERR*
W7	P54H2_1_PB_SERR_N	PBSERR*
AA9	P54H2_1_PB_IRDY_N	PBIRDY*
AD8	P54H2_1_PB_TRDY_N	PBTRDY*
AB9	P54H2_1_PB_FRAME_N	PBFRAME*
AC8	P54H2_1_PB_DEVSEL_N	PBDEVSEL*
AC2	P54H2_1_PB_CBE7_N	PBC/BE* < 7 >
AA2	P54H2_1_PB_CBE6_N	PBC/BE* < 6 >
Y2	P54H2_1_PB_CBE5_N	PBC/BE* < 5 >
V2	P54H2_1_PB_CBE4_N	PBC/BE* < 4 >
AD11	P54H2_1_PB_CBE3_N	PBC/BE* < 3 >
AD9	P54H2_1_PB_CBE2_N	PBC/BE* < 2 >
AC7	P54H2_1_PB_CBE1_N	PBC/BE* < 1 >
U5	P54H2_1_PB_CBE0_N	PBC/BE* < 0 >
V8	P54H2_1_PB_PCLKI	PBPCLKI
K6	P54H2_1_PB_PCLK6	PBPCLK0 < 6 >
K4		PBPCLK0 < 5 >
K3		PBPCLK0 < 4 >
K1		PBPCLK0 < 3 >
L7		PBPCLK0 < 2 >
L5	P54H2_1_PB_PCLK1_R	PBPCLK0 < 1 >
L4	P54H2_1_PB_PCLK0_R	PBPCLK0 < 0 >
G2	P54H2_1_PB_RST_N	PBPCIRST*
F1	P54H2_1_PB_IRQ15	PBIRQ < 15 >
E1	P54H2_1_PB_IRQ14	PBIRQ < 14 >
D1	P54H2_1_PB_IRQ13	PBIRQ < 13 >
C1	P54H2_1_PB_IRQ12	PBIRQ < 12 >
B1	P54H2_1_PB_IRQ11	PBIRQ < 11 >
F2	P54H2_1_PB_IRQ10	PBIRQ < 10 >
E2	P54H2_1_PB_IRQ9	PBIRQ < 9 >
D2	P54H2_1_PB_IRQ8	PBIRQ < 8 >
C2	P54H2_1_PB_IRQ7	PBIRQ < 7 >
B2	P54H2_1_PB_IRQ6	PBIRQ < 6 >
A2	P54H2_1_PB_IRQ5	PBIRQ < 5 >
F3	P54H2_1_PB_IRQ4	PBIRQ < 4 >
E3	P54H2_1_PB_IRQ3	PBIRQ < 3 >
D3	P54H2_1_PB_IRQ2	PBIRQ < 2 >
C3	P54H2_1_PB_IRQ1	PBIRQ < 1 >
B3	P54H2_1_PB_IRQ0	PBIRQ < 0 >
Y8	P54H2_1_PB_PLOCK_N	PBPLOCK*

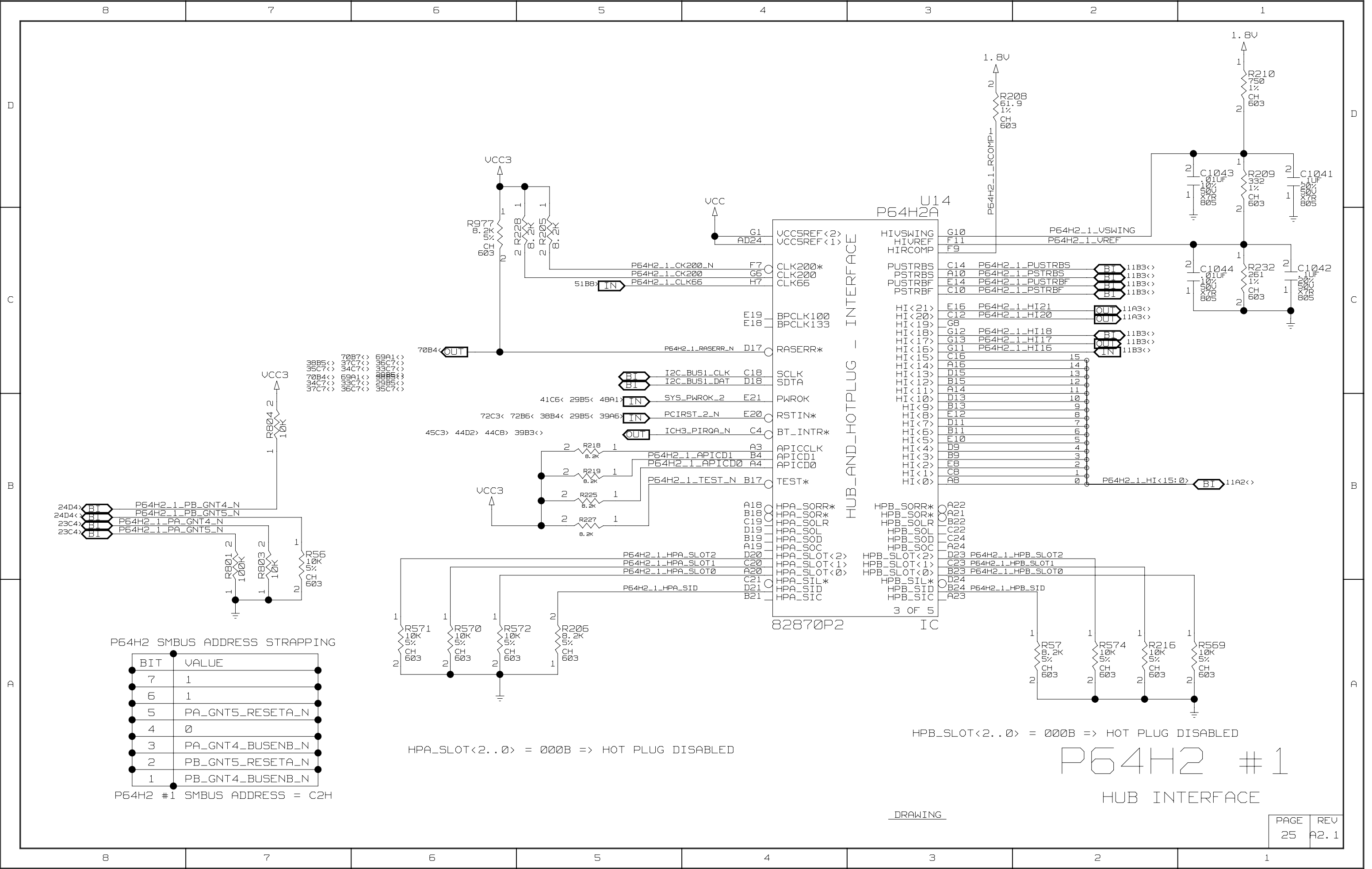
82870P2 IC

FOR VALIDATION ONLY

JP29	JP28	PROTOCOL	MAX FREQ
NO JUMPER	NO JUMPER	PCI-X	100MHZ
NO JUMPER	PIN 1-2	PCI-X	66MHZ
NO JUMPER	PIN 2-3	PCI	66MHZ
JUMPER	PIN 2-3	PCI	33MHZ

P64H2 #1
100MHZ PCI-X SLOT
AND LAN CONTROLLER

DRAWING



38B5<>	70B7<>	69A1<>
35C7<>	37C7<>	36C7<>
70B4<>	69A1<>	36B5<>
34C7<>	33C7<>	29A6<>
37C7<>	36C7<>	35C7<>

P64H2 SMBUS ADDRESS STRAPPING

BIT	VALUE
7	1
6	1
5	PA_GNT5_RESETA_N
4	0
3	PA_GNT4_BUSENB_N
2	PB_GNT5_RESETA_N
1	PB_GNT4_BUSENB_N

P64H2 #1 SMBUS ADDRESS = C2H

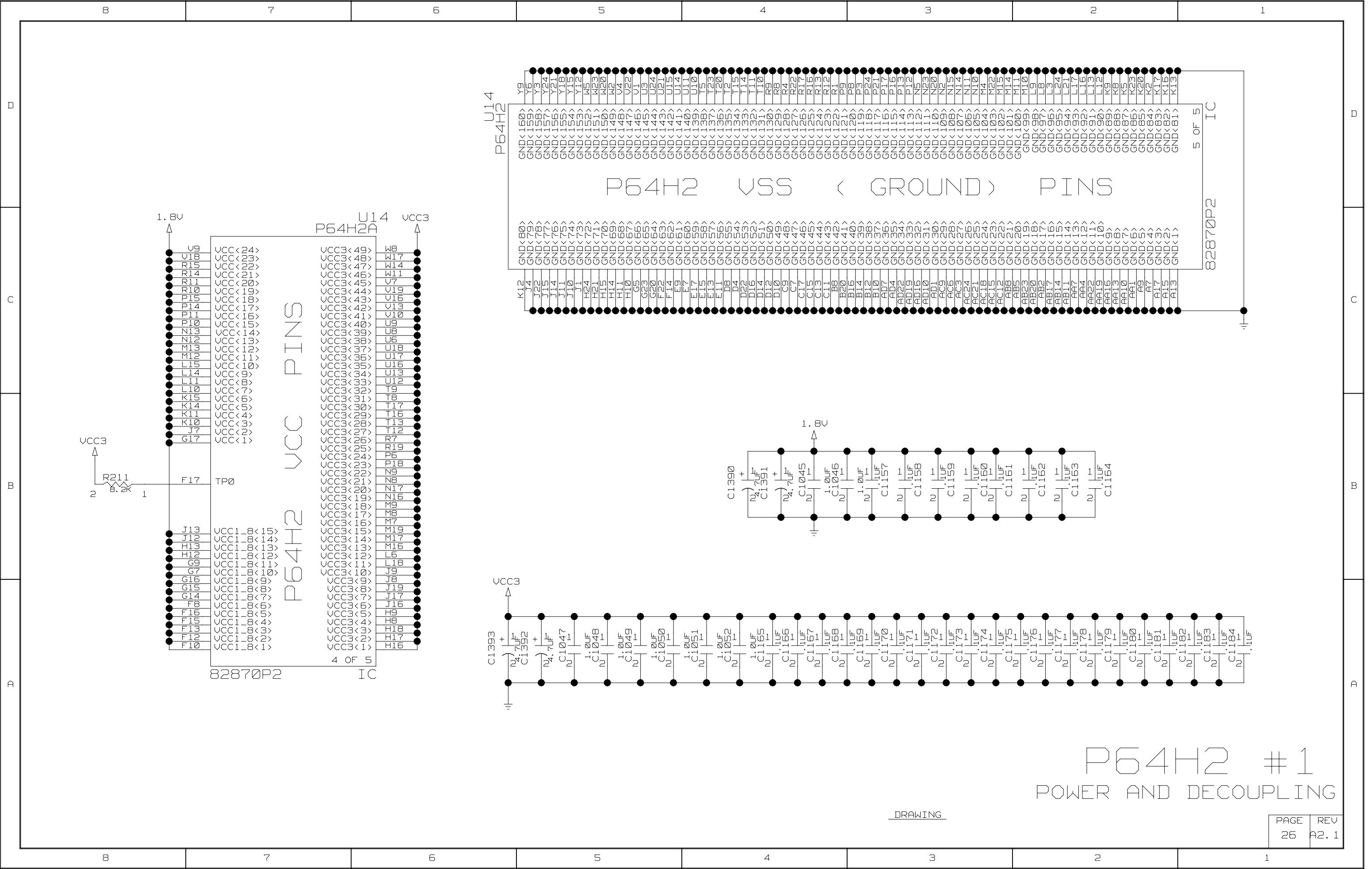
HPA_SLOT<2..0> = 000B => HOT PLUG DISABLED

HPB_SLOT<2..0> = 000B => HOT PLUG DISABLED

P64H2 #1

HUB INTERFACE

DRAWING



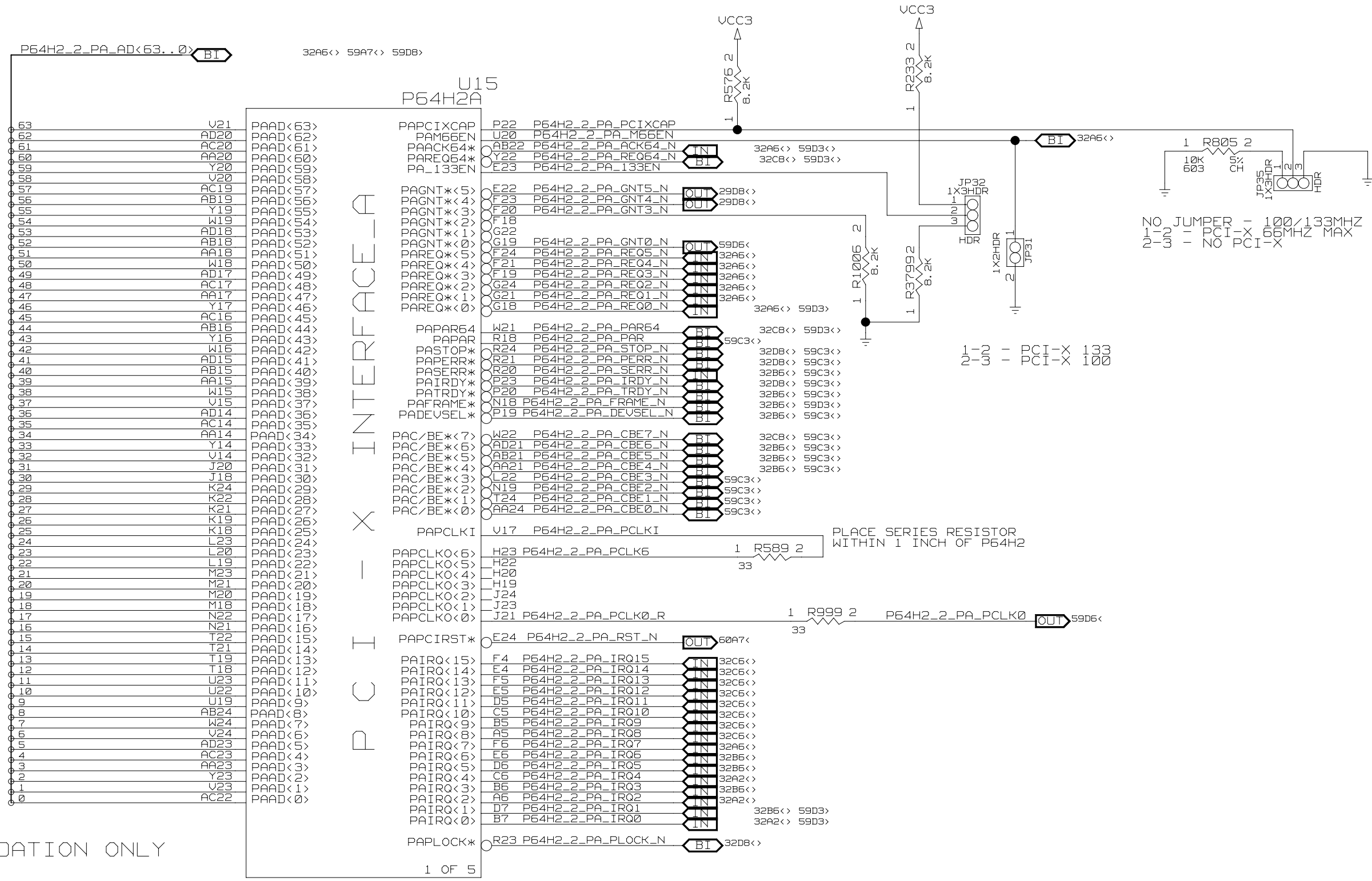
P64H2 VSS < GROUND > PINS

P64H2 #1
POWER AND DECOUPLING

DRAWING

PAGE	REV
26	A2.1

8 7 6 5 4 3 2 1



D
C
B
A

D
C
B
A

FOR VALIDATION ONLY

JP31	JP32	JP27	PROTOCOL	MAX FREQ
NO JUMPER	NO JUMPER	NO JUMPER	PCI-X	133MHZ
NO JUMPER	JUMPER	NO JUMPER	PCI-X	100MHZ
NO JUMPER	JUMPER	PIN 1-2	PCI-X	66MHZ
NO JUMPER	JUMPER	PIN 2-3	PCI	66MHZ
JUMPER	JUMPER	PIN 2-3	PCI	33MHZ

NO JUMPER - 100/133MHZ
1-2 - PCI-X 66MHZ MAX
2-3 - NO PCI-X

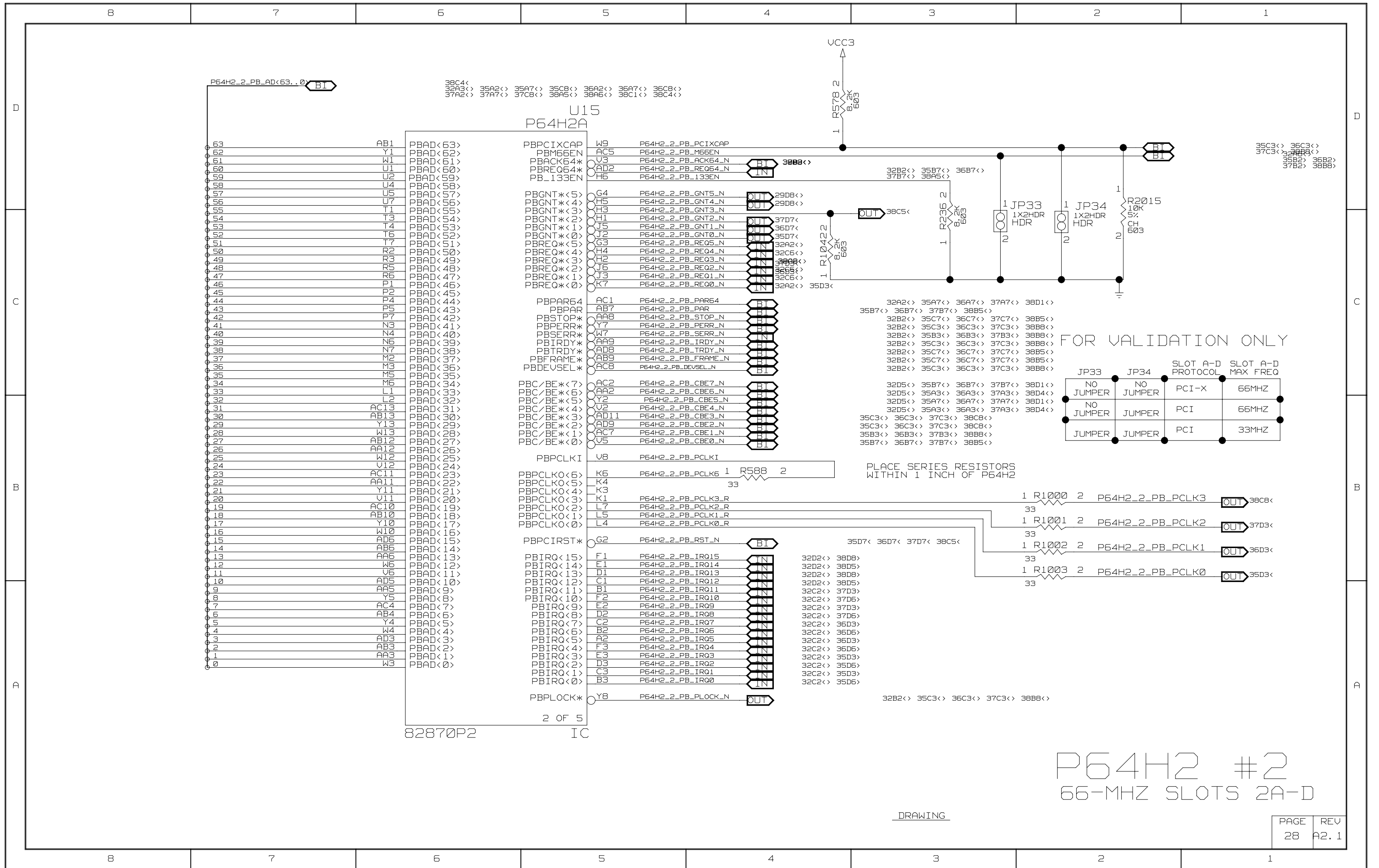
1-2 - PCI-X 133
2-3 - PCI-X 100

PLACE SERIES RESISTOR
WITHIN 1 INCH OF P64H2

P64H2 #2
SCSI CONTROLLER

DRAWING

8 7 6 5 4 3 2 1



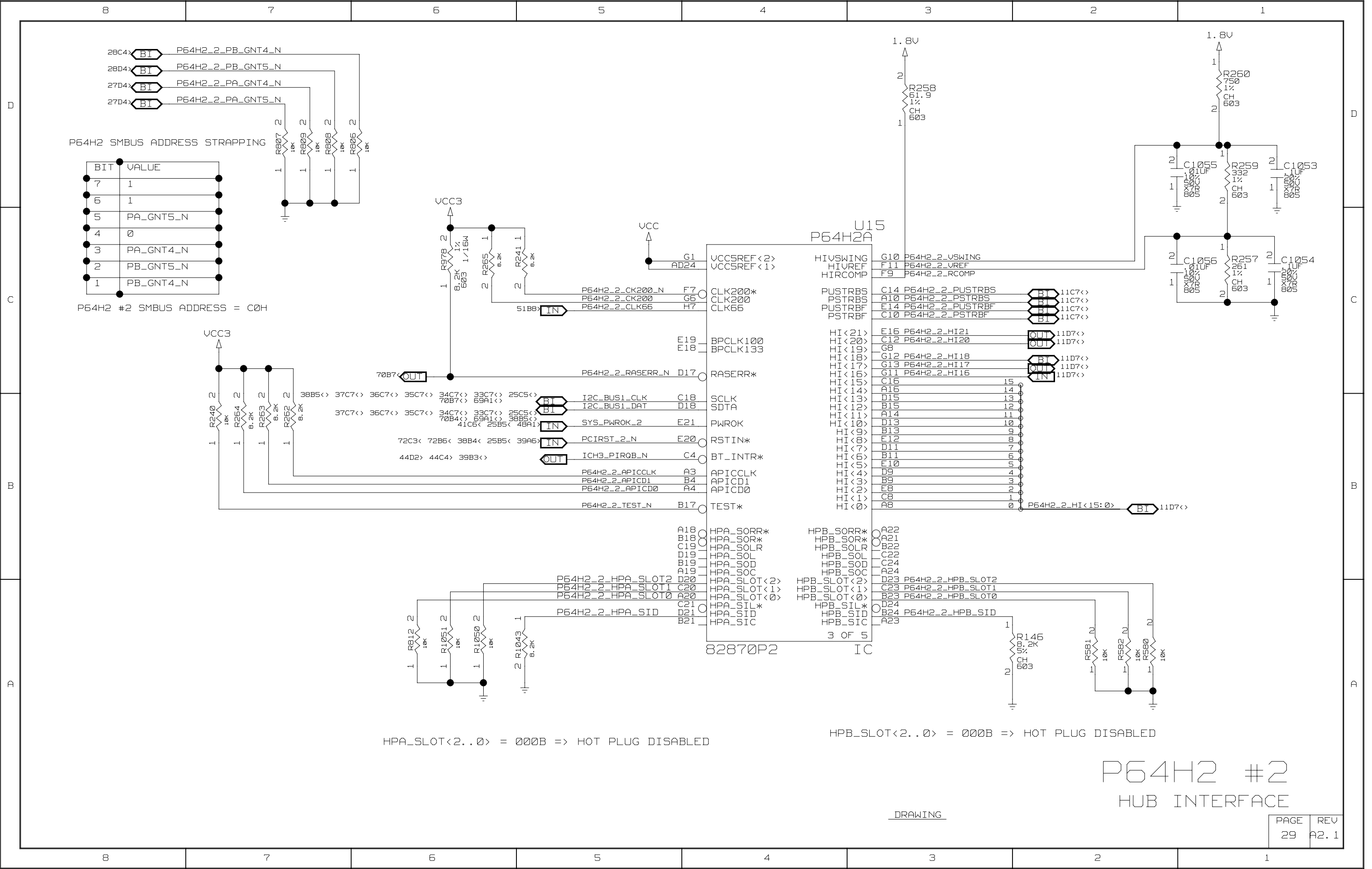
FOR VALIDATION ONLY

JP33	JP34	SLOT A-D PROTOCOL	SLOT A-D MAX FREQ
NO JUMPER	NO JUMPER	PCI-X	66MHZ
NO JUMPER	JUMPER	PCI	66MHZ
JUMPER	JUMPER	PCI	33MHZ

PLACE SERIES RESISTORS WITHIN 1 INCH OF P64H2

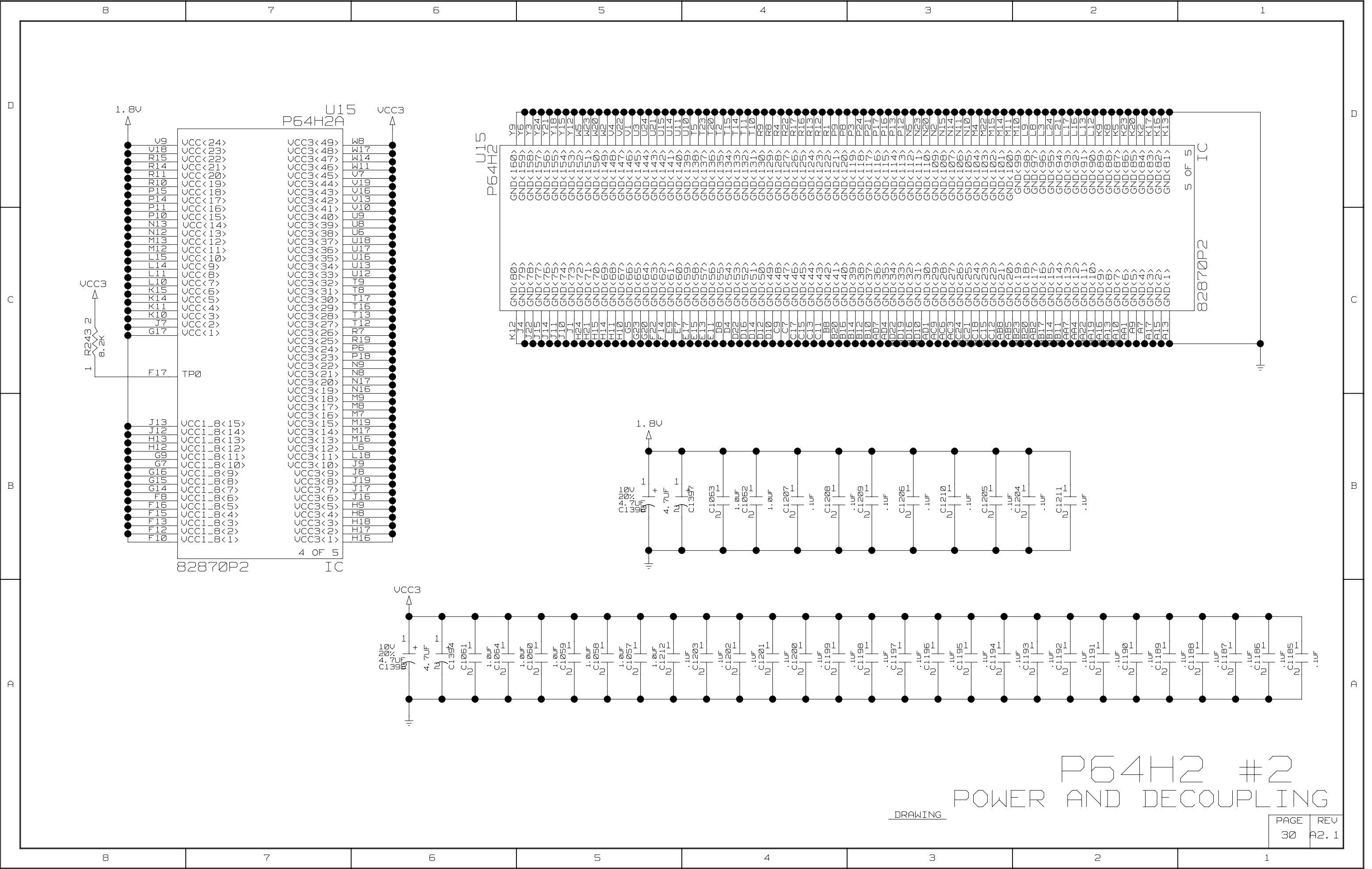
P64H2 #2
66-MHZ SLOTS 2A-D

DRAWING



P64H2 #2 HUB INTERFACE

DRAWING

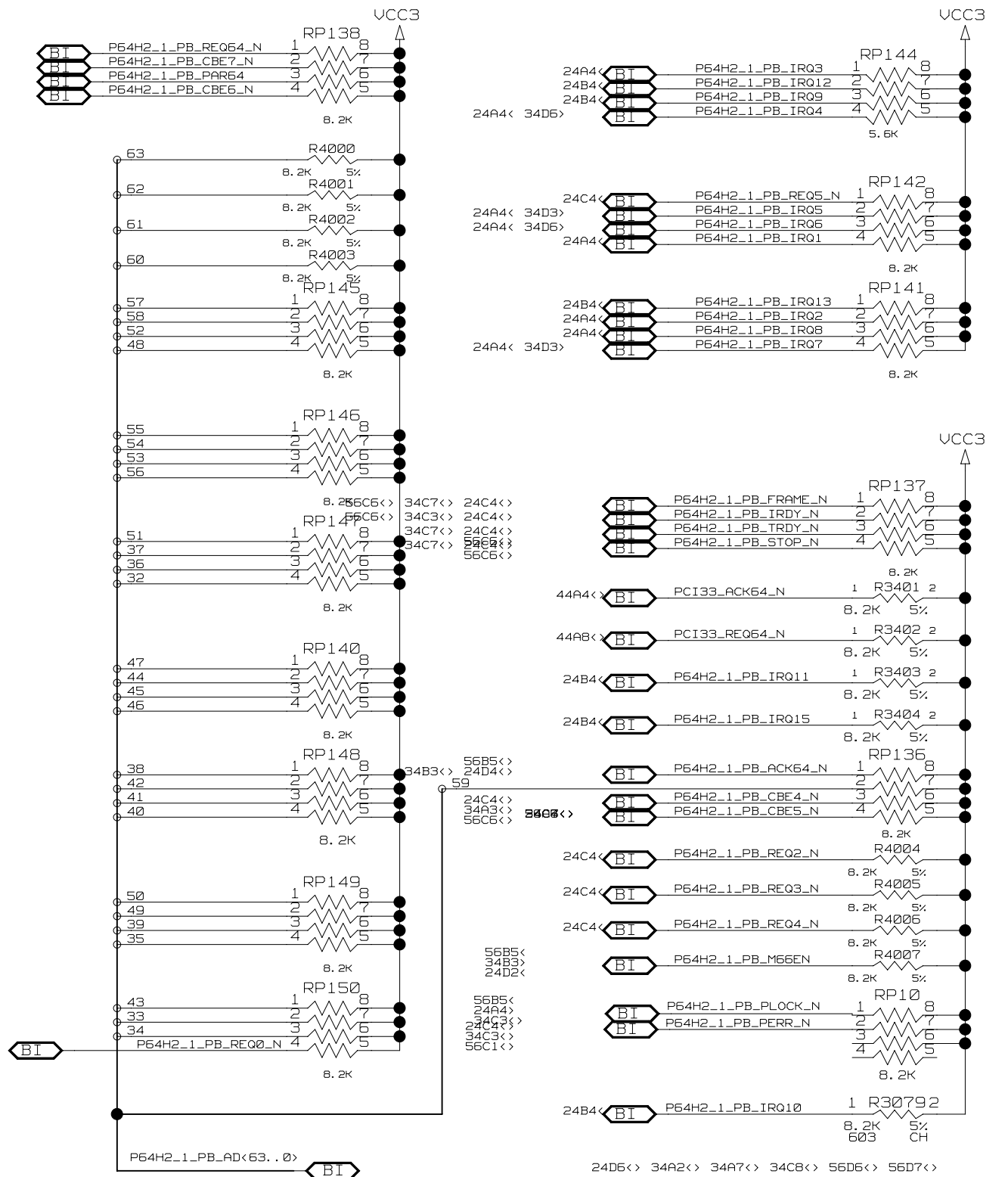
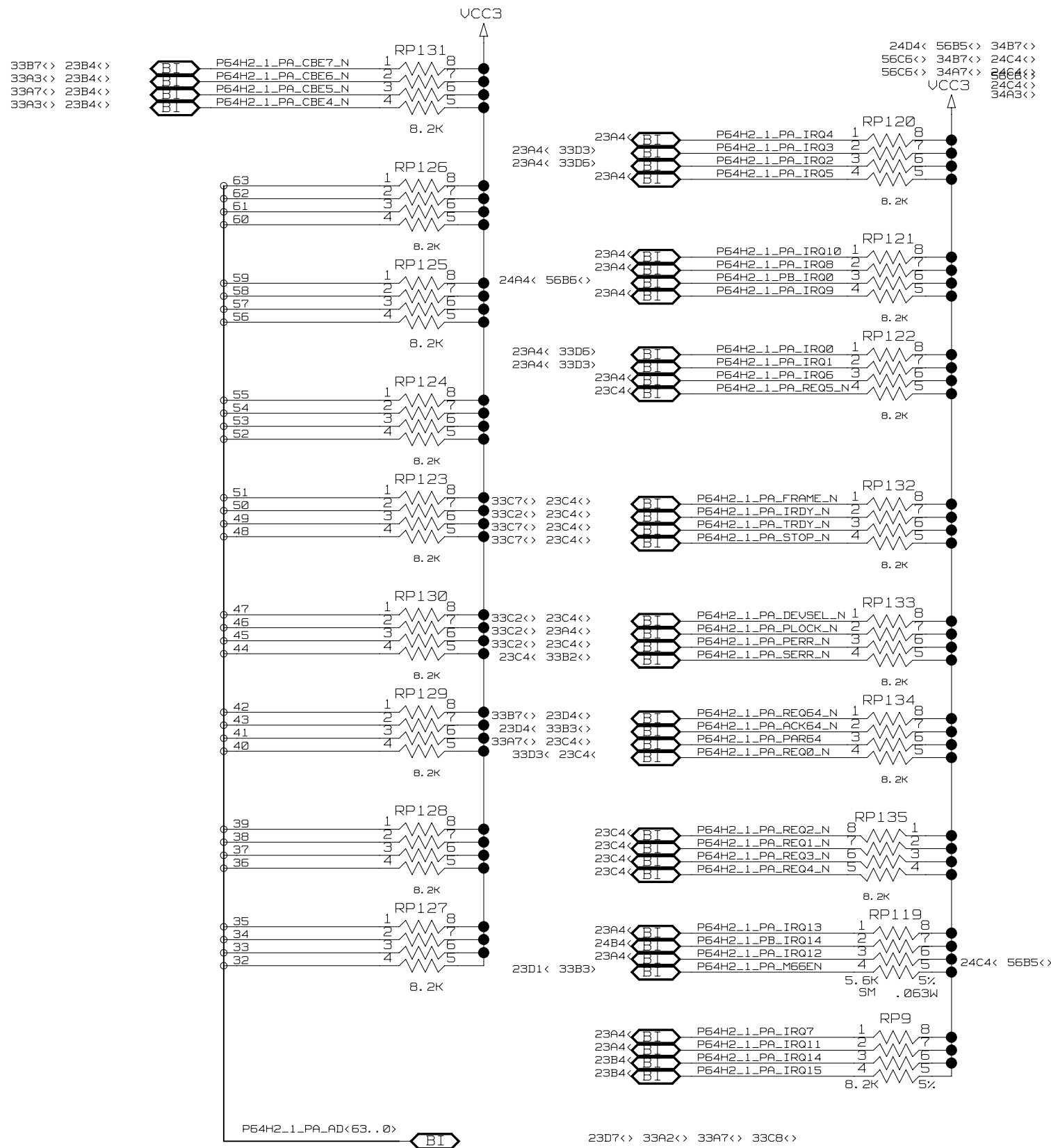


P64H2 #2
POWER AND DECOUPLING

DRAWING

P64H2 #1 PCI BUS A PULL-UPS

P64H2 #1 PCI BUS B PULL-UPS

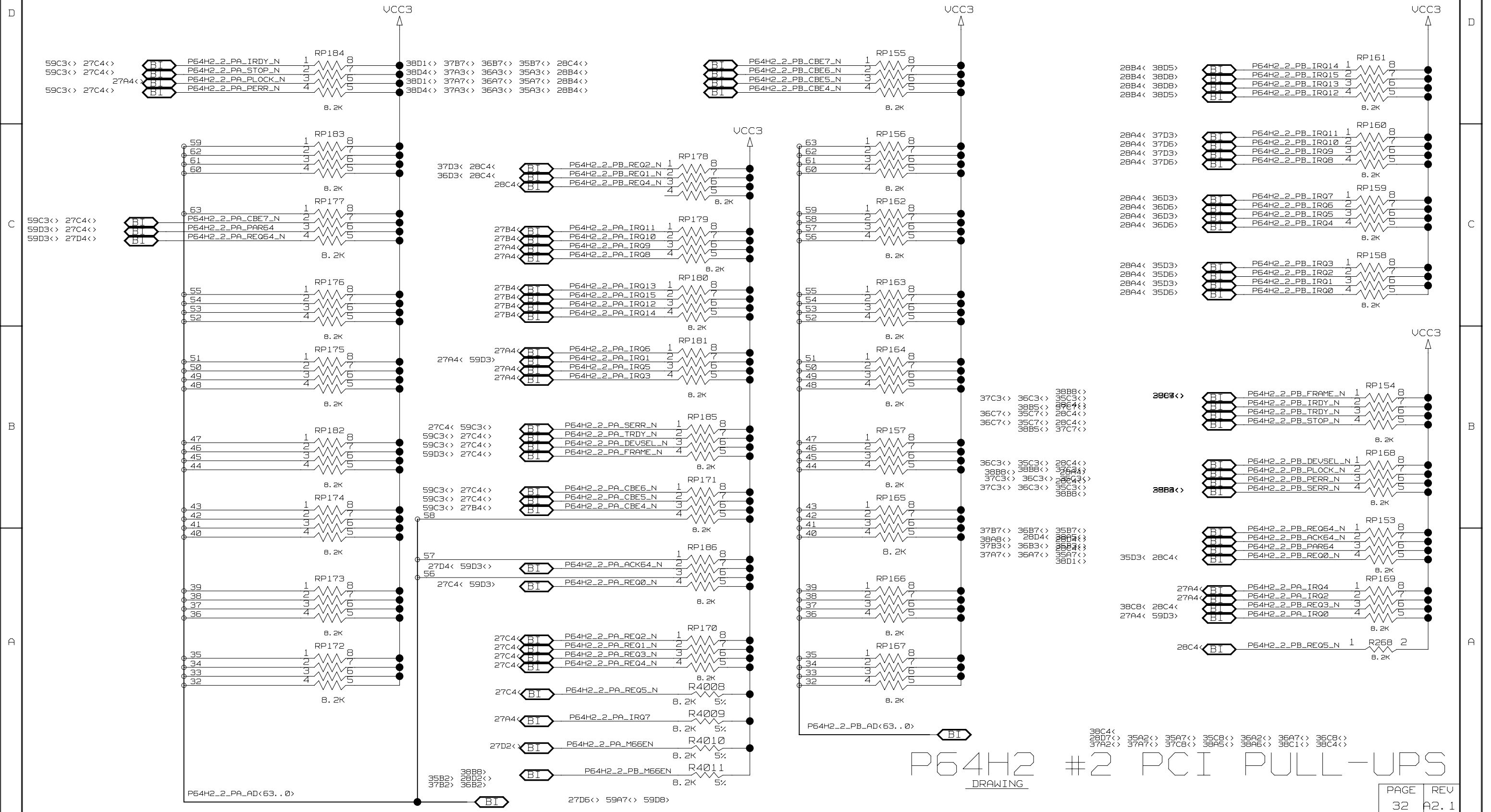


P64H2 #1 PCI PULL-UPS

DRAWING

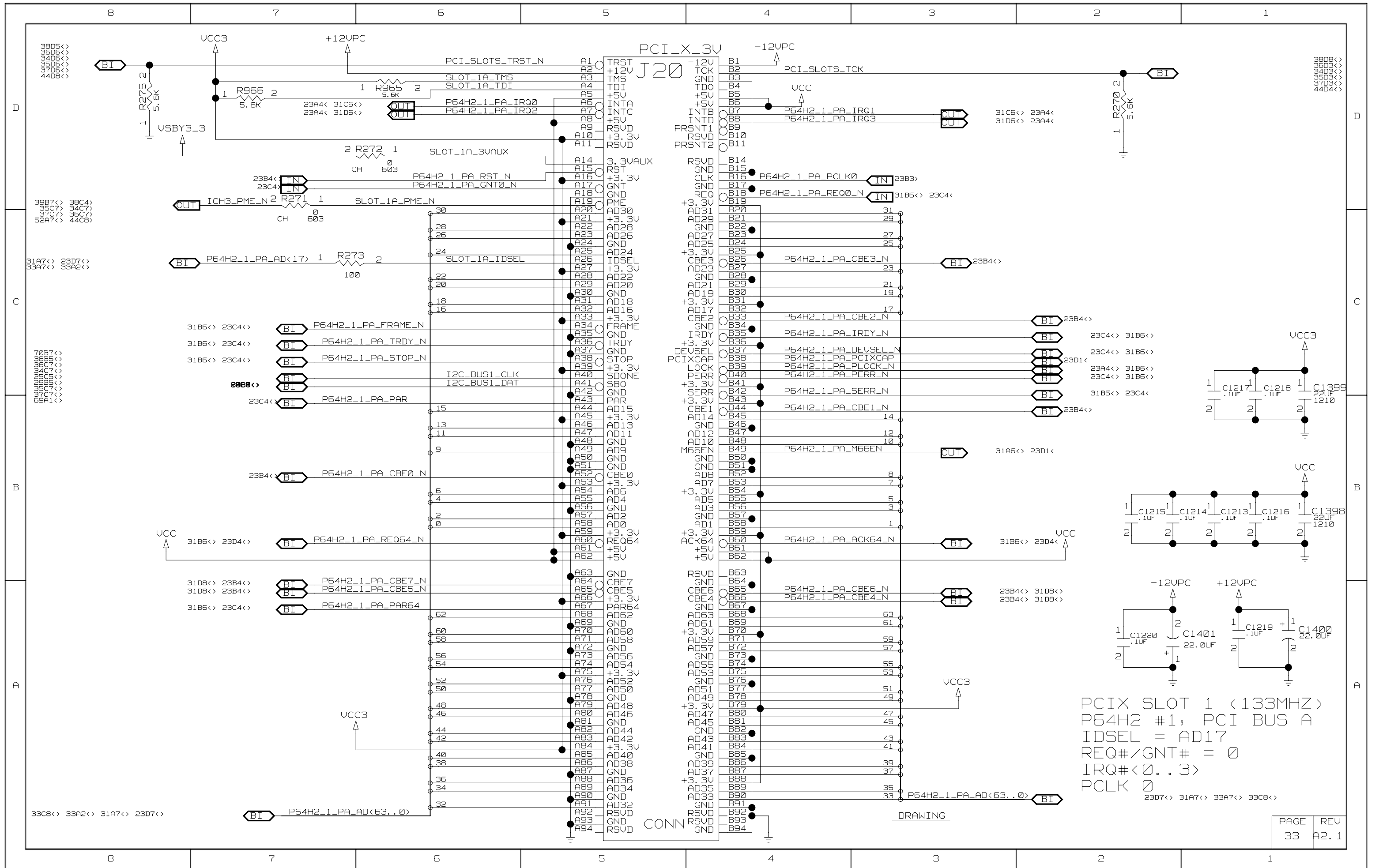
P64H2 #2 PCI BUS A PULL-UPS

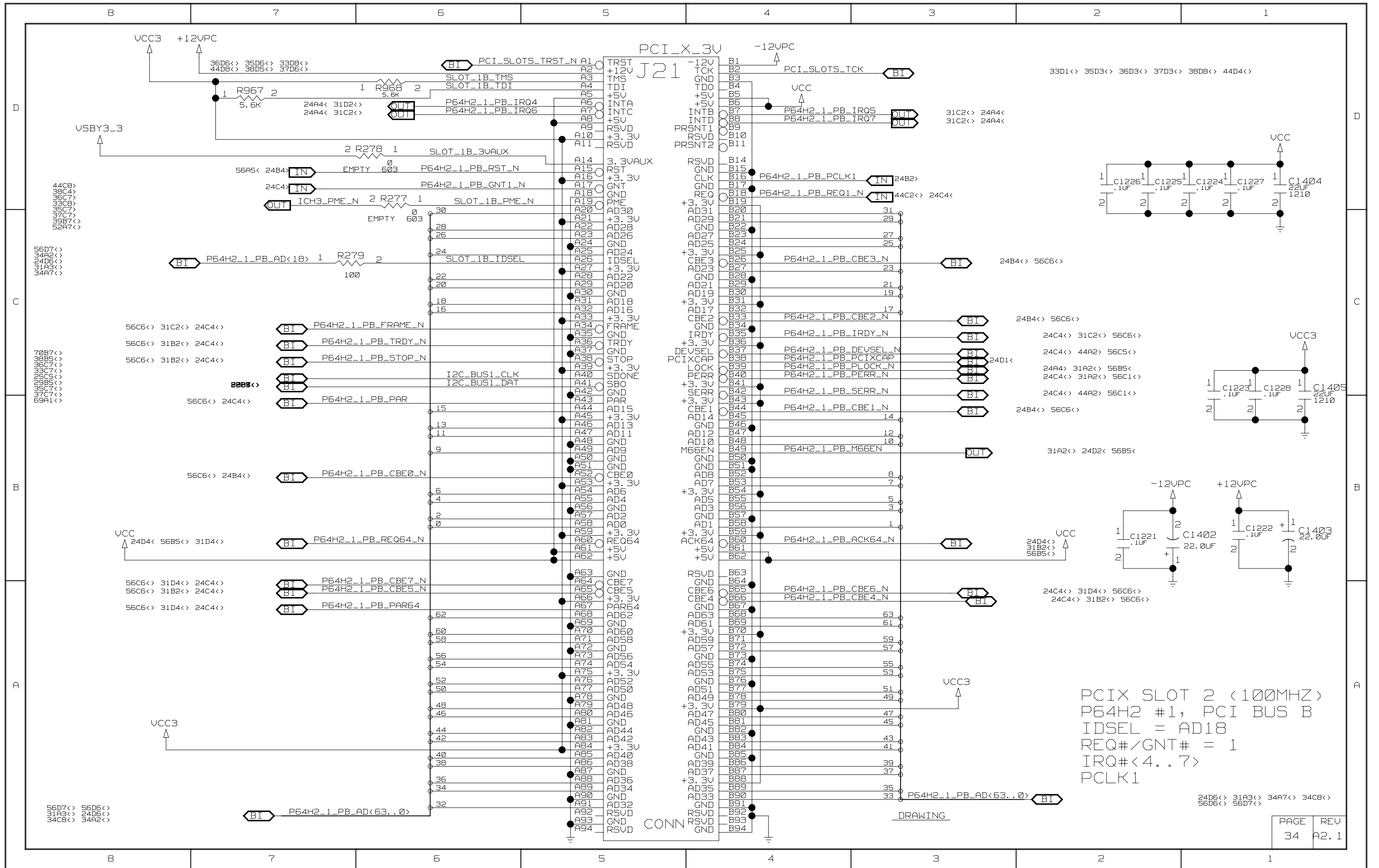
P64H2 #2 PCI BUS B PULL-UPS



P64H2 #2 PCI PULL-UPS

DRAWING





PCIX SLOT 2 (100MHZ)
P64H2 #1, PCI BUS B
IDSEL = AD18
REQ#/GNT# = 1
IRQ#<4..7>
PCLK1

- 44C8<
- 38C4<
- 36C7<
- 33C8<
- 35C7<
- 37C7<
- 39B7<
- 52A7<

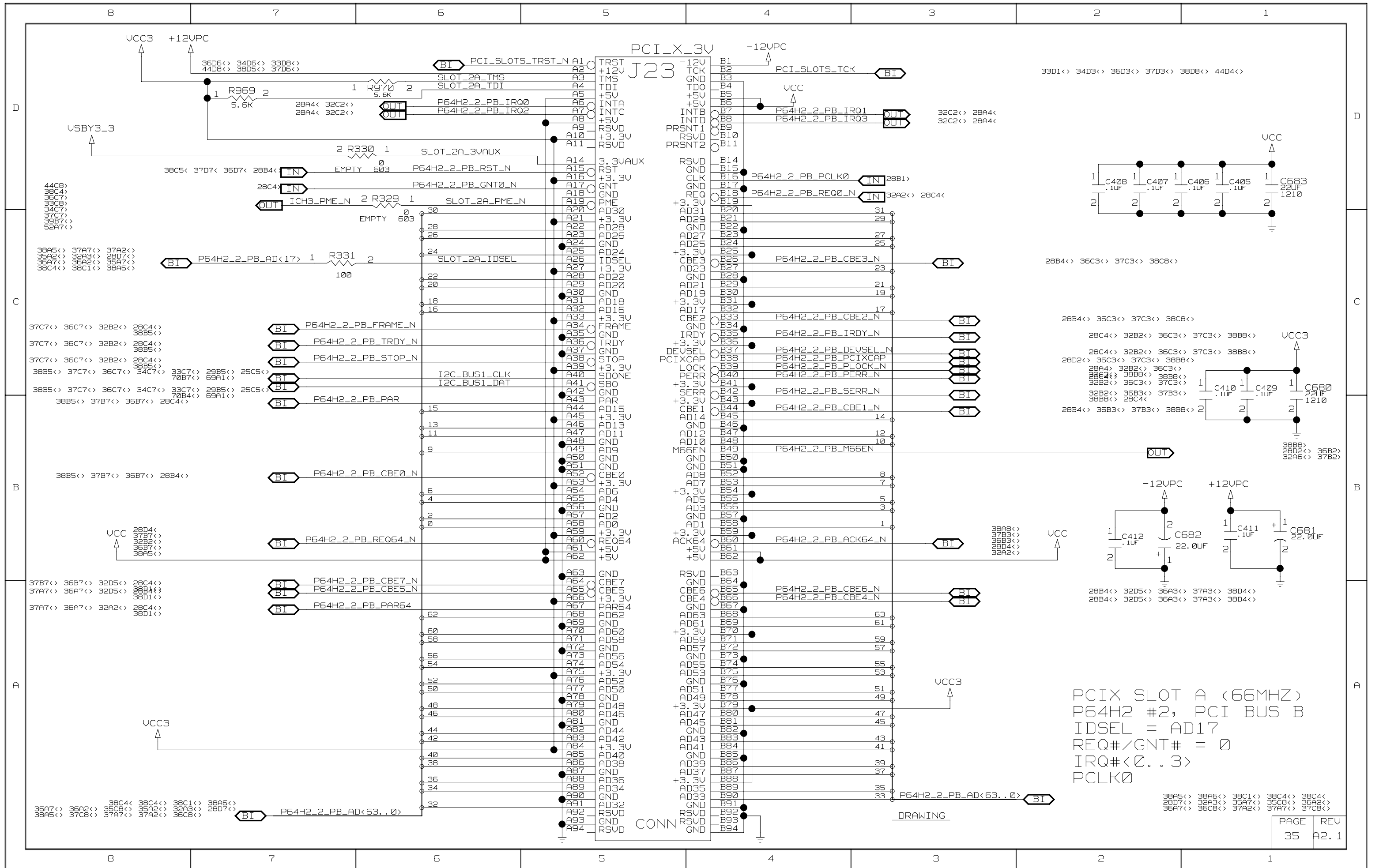
- 56D7<
- 34A2<
- 24D5<
- 31A3<
- 34A7<

- 70B7<
- 38B5<
- 36C7<
- 39C7<
- 29B5<
- 35C7<
- 37C7<
- 69A1<

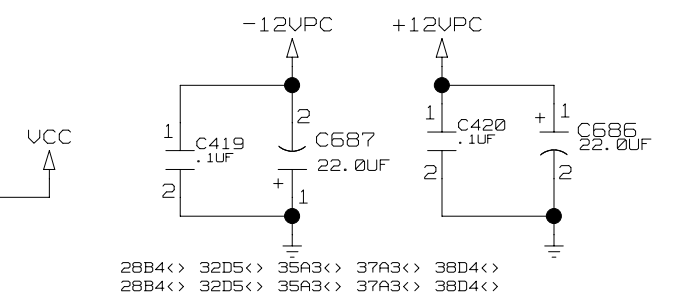
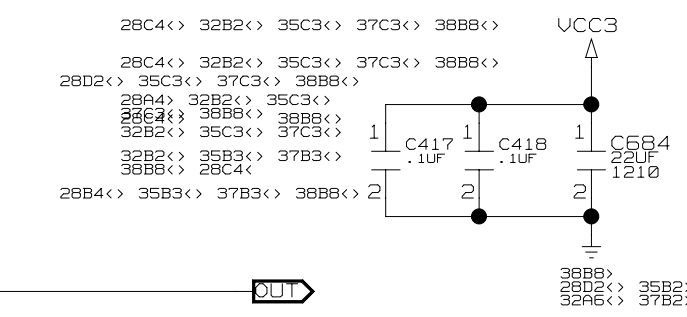
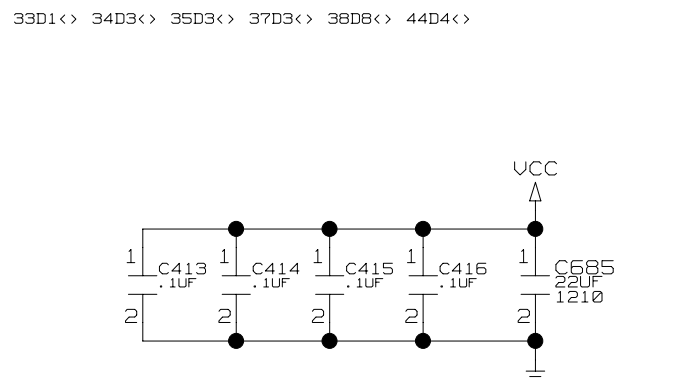
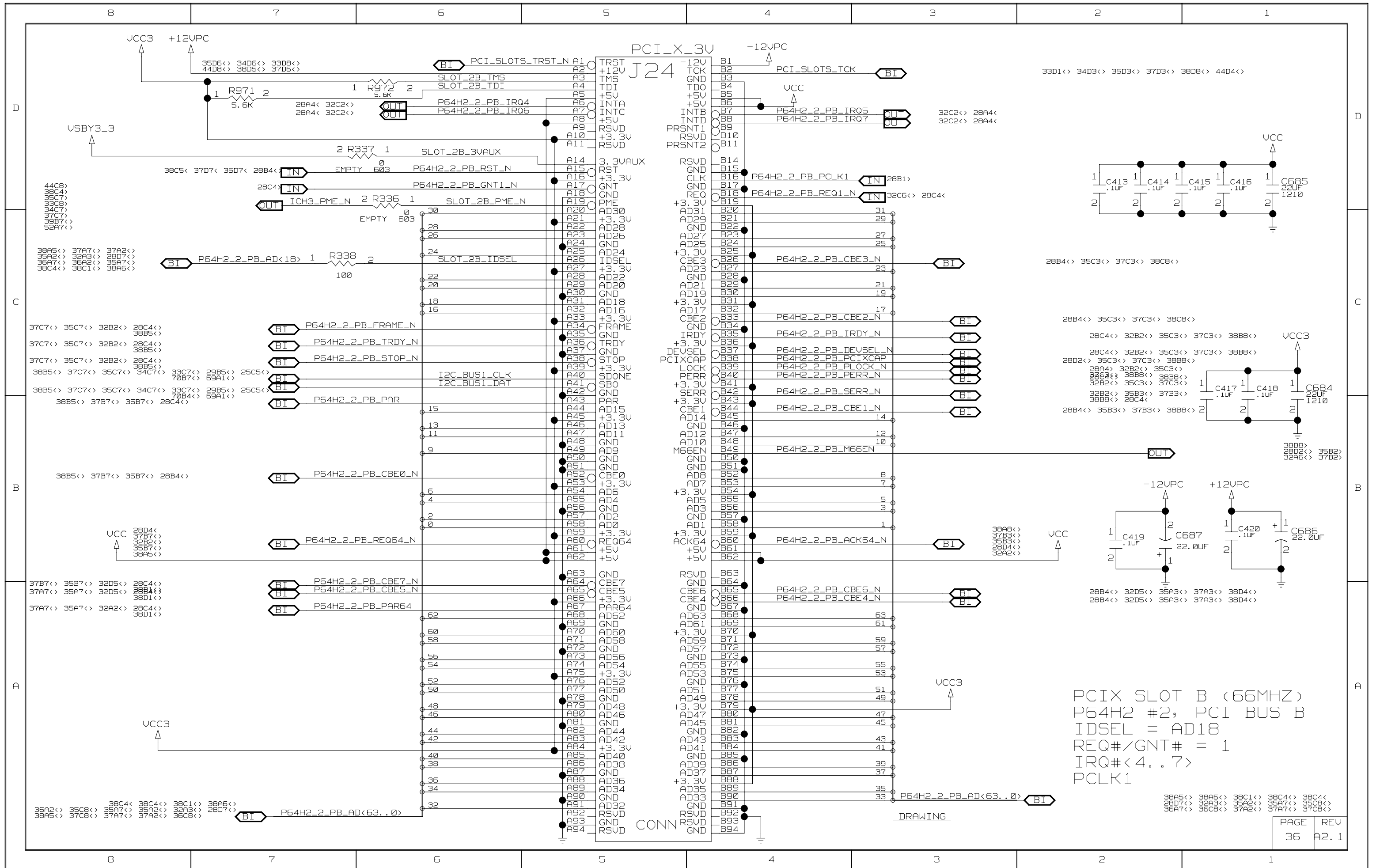
- 56D7<
- 56D6<
- 31A3<
- 34C6<
- 24D6<
- 54A2<

- 24D6<
- 31A3<
- 34A7<
- 34C8<
- 56D6<
- 56D7<

DRAWING

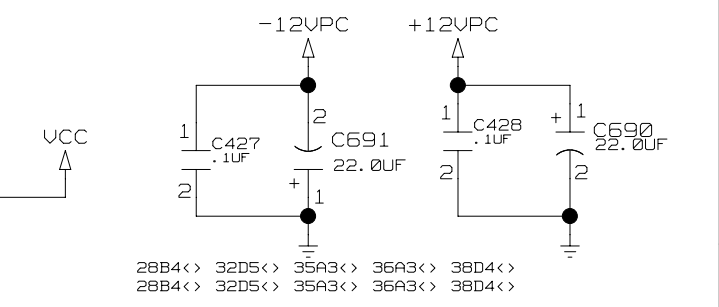
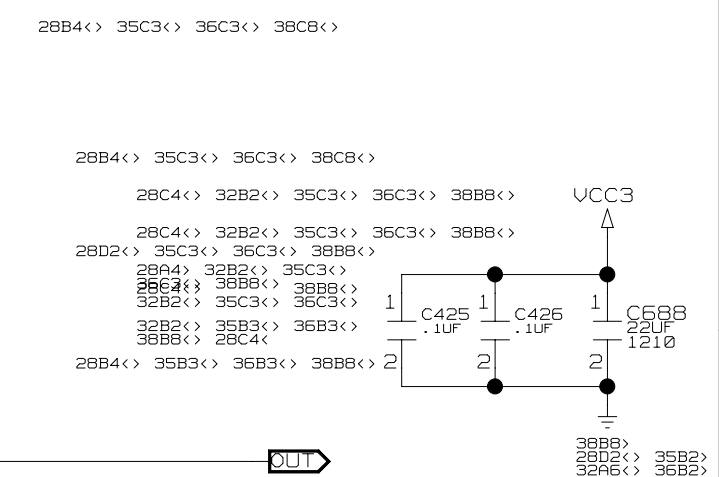
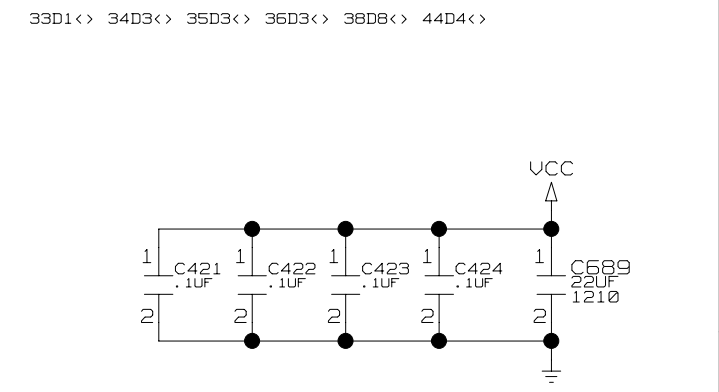
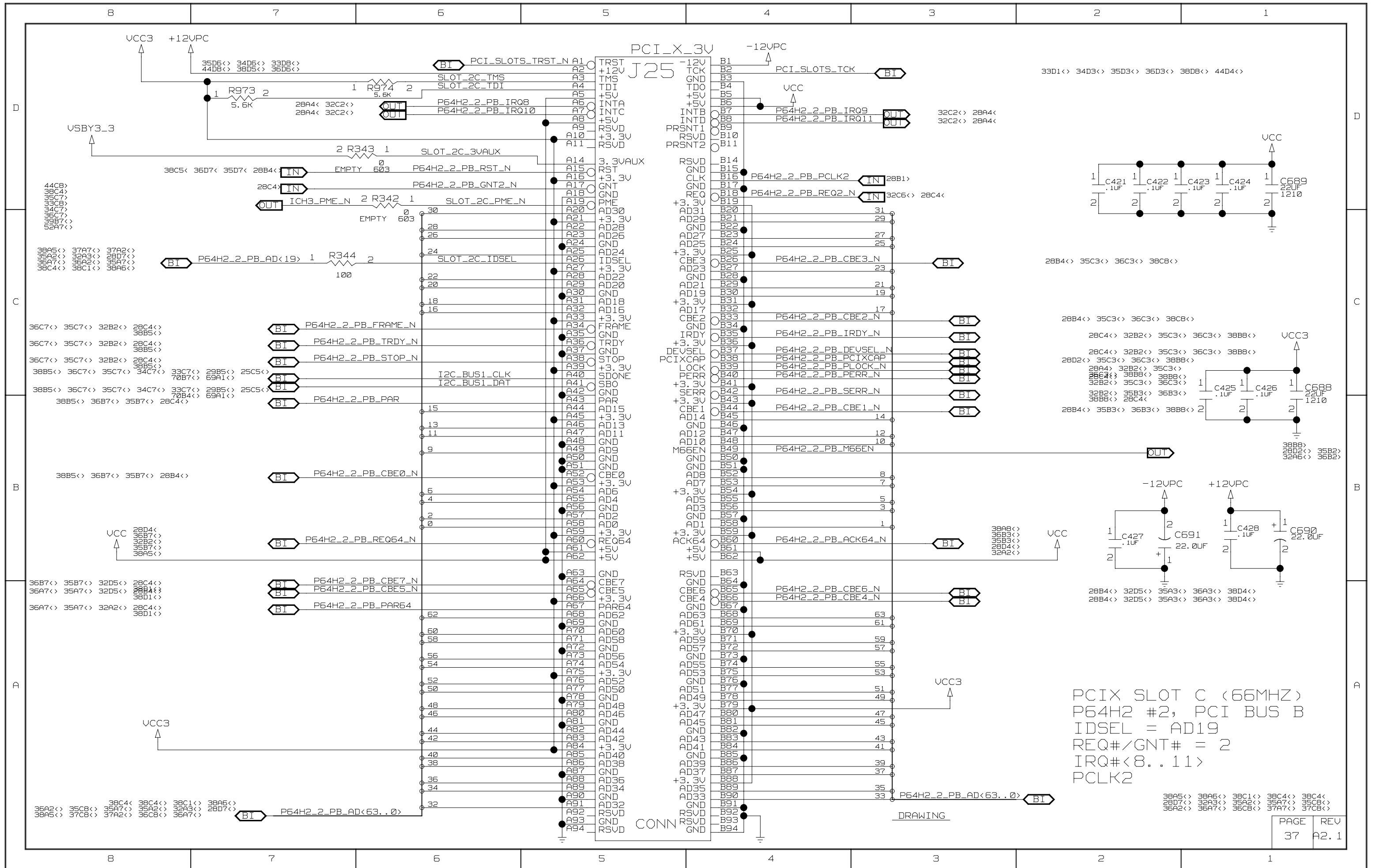


PCIX SLOT A (66MHZ)
P64H2 #2, PCI BUS B
IDSEL = AD17
REQ#/#GNT# = 0
IRQ#<0..3>
PCLK0



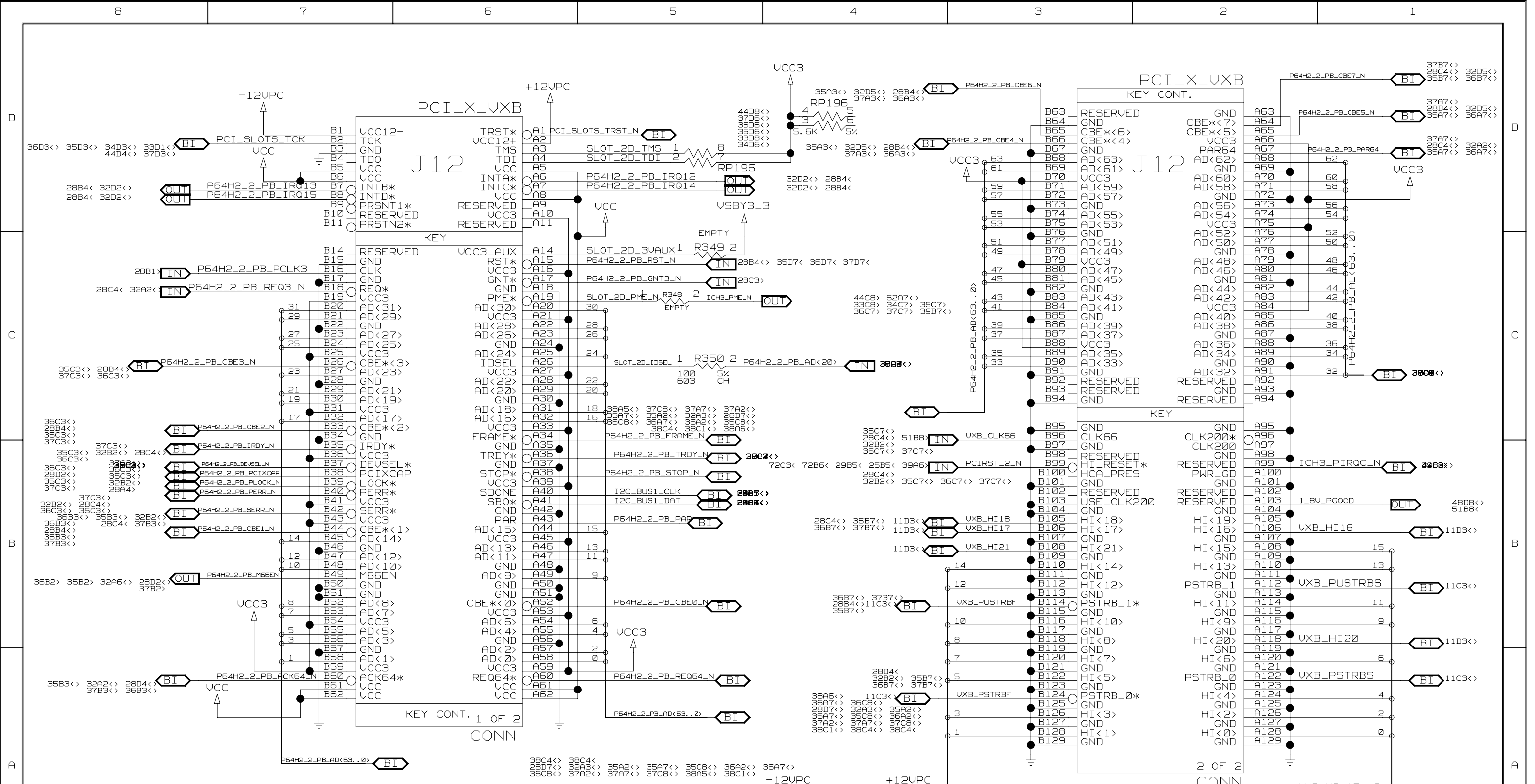
PCIX SLOT B (66MHZ)
P64H2 #2, PCI BUS B
IDSEL = AD18
REQ#/#GNT# = 1
IRQ#<4..7>
PCLK1

38A5<> 38A6<> 38C1<> 38C4<> 38C4<
28D7<> 32A3<> 35A2<> 35A7<> 35C8<>
36A7<> 36C8<> 37A2<> 37A7<> 37C8<>

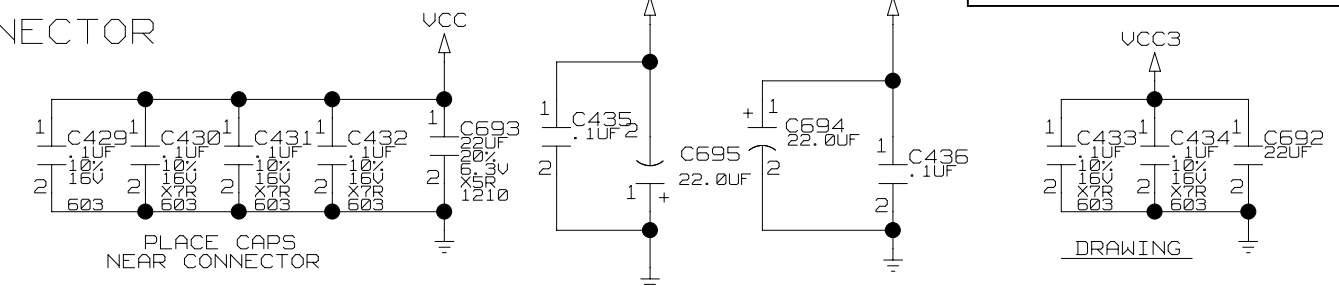


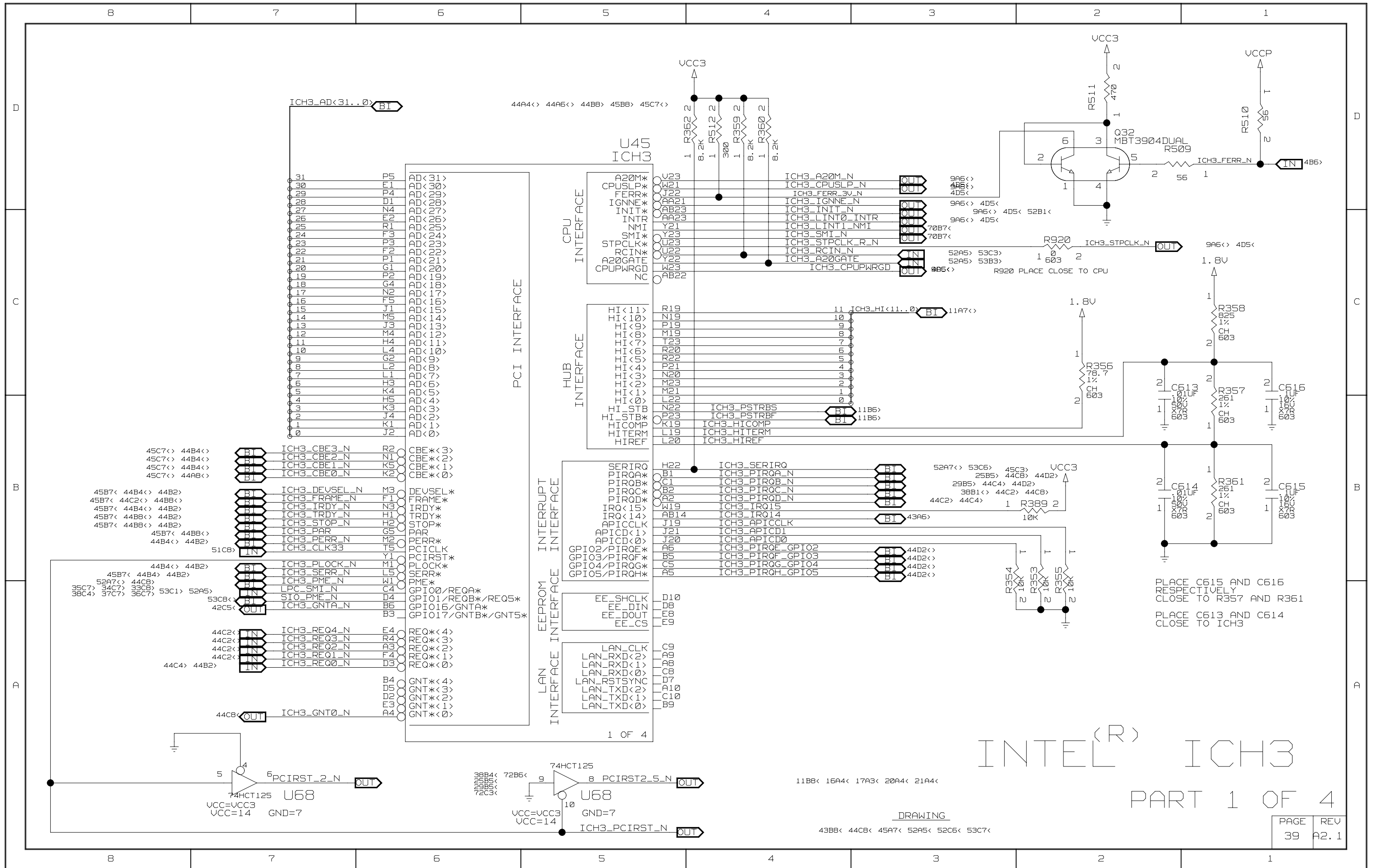
PCIX SLOT C (66MHZ)
P64H2 #2, PCI BUS B
IDSEL = AD19
REQ#/#GNT# = 2
IRQ#<8..11>
PCLK2

38A5<> 38A6<> 38C1<> 38C4<> 38C4<>
28D7<> 32A3<> 35A2<> 35A7<> 35C8<>
36A2<> 36A7<> 36C8<> 36A7<> 37C8<>



PCIX SLOT D (66MHZ) + UXB CONNECTOR
 P64H2 #2, PCI BUS B
 IDSEL = AD20
 REQ#/GNT# = 3
 IRQ# < 12..15 >
 PCLK3





INTEL[®] ICH3

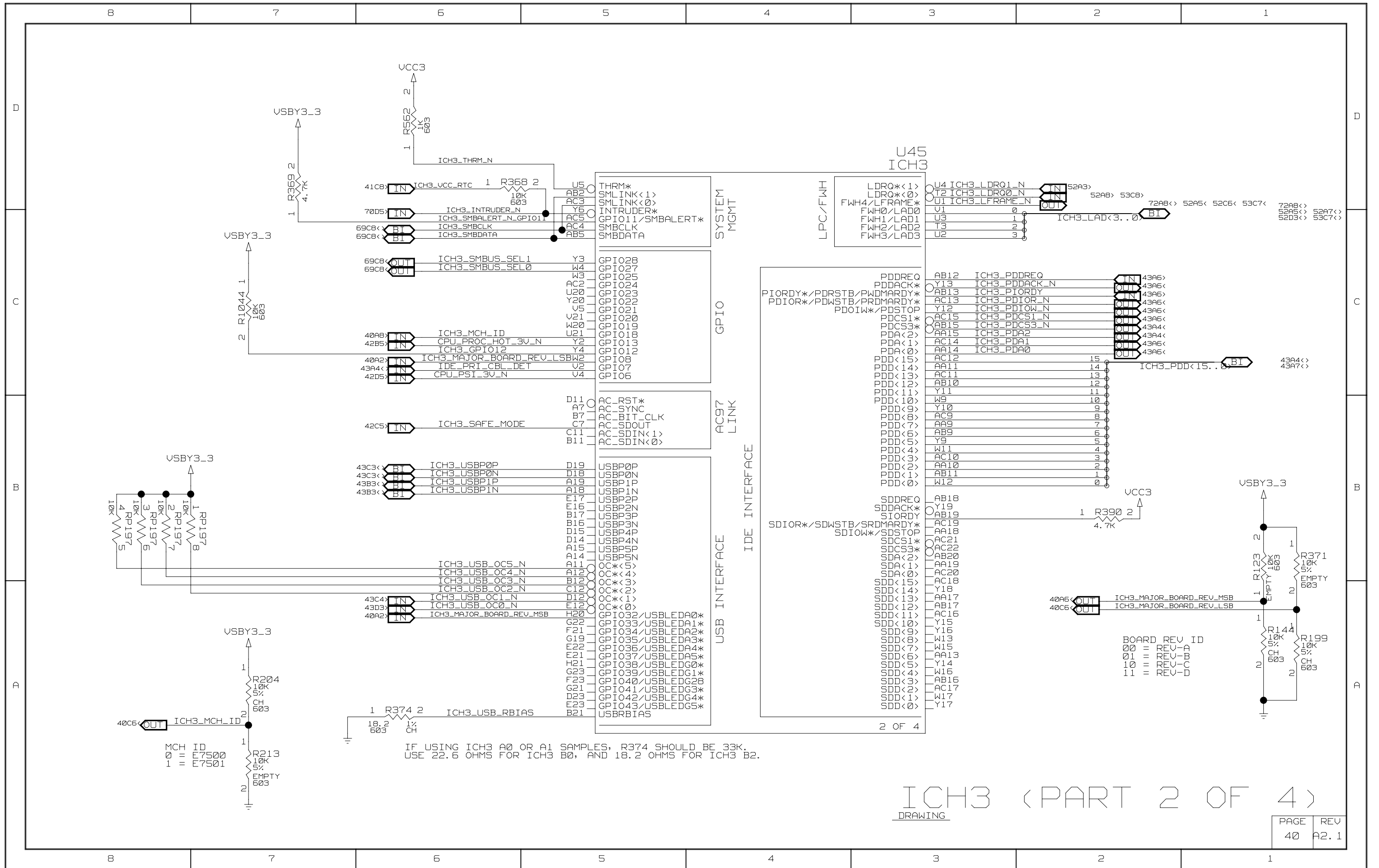
PART 1 OF 4

11B8< 16A4< 17A3< 20A4< 21A4<

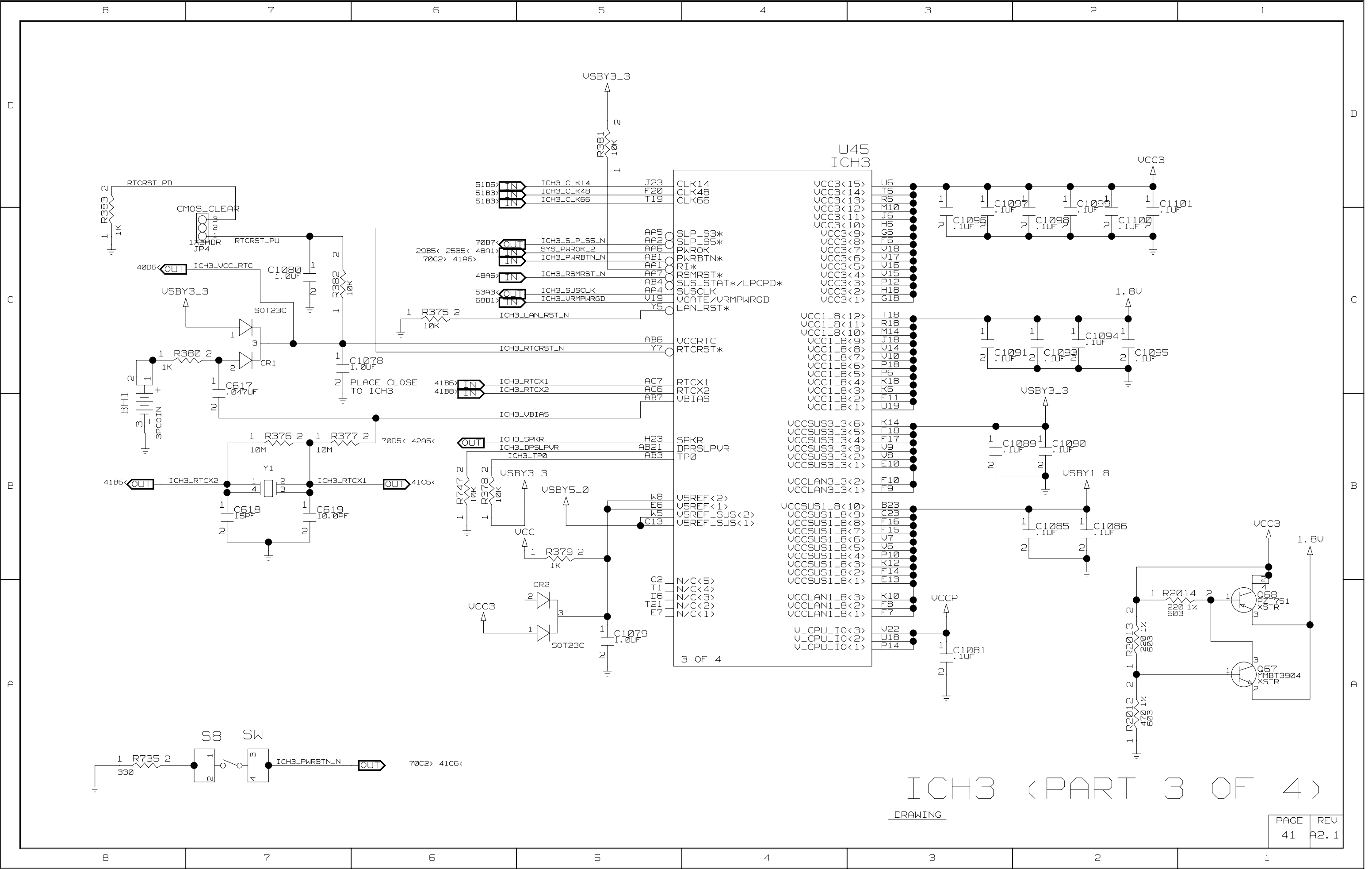
DRAWING

43B8< 44C8< 45A7< 52A5< 52C6< 53C7<

PAGE	REV
39	A2.1



ICH3 (PART 2 OF 4)
DRAWING

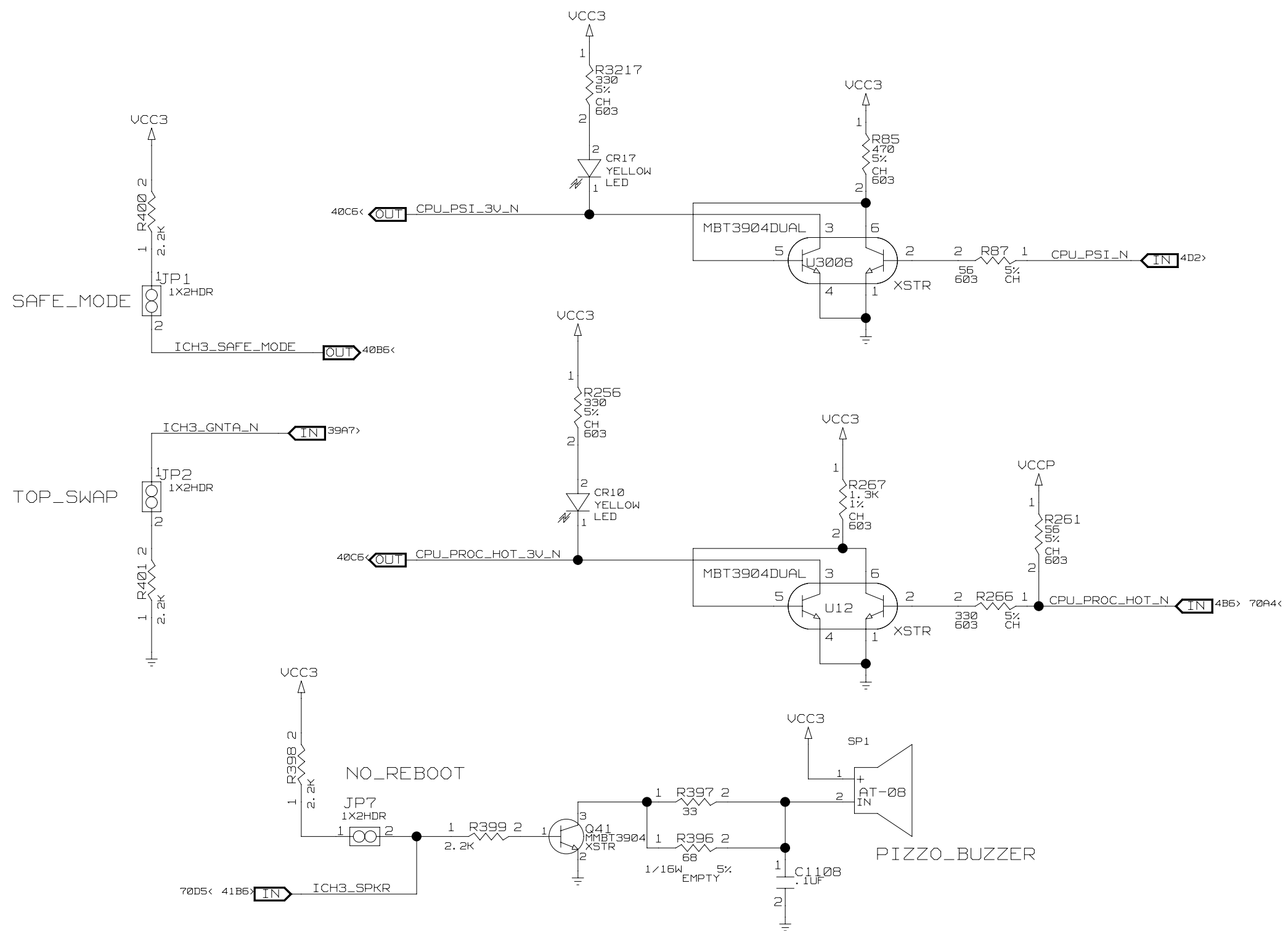


ICH3 (PART 3 OF 4)
DRAWING

U45
ICH3

L3	GND<52>	GND<104>	A22
K23	GND<51>	GND<103>	A21
K22	GND<50>	GND<102>	AC23
K21	GND<49>	GND<101>	AC8
K20	GND<48>	GND<100>	AC1
K13	GND<47>	GND<99>	AB8
K11	GND<46>	GND<98>	AA22
J5	GND<45>	GND<97>	AA20
H19	GND<44>	GND<96>	AA16
G20	GND<43>	GND<95>	AA12
G3	GND<42>	GND<94>	AA8
F22	GND<41>	GND<93>	AA3
F19	GND<40>	GND<92>	Y8
E20	GND<39>	GND<91>	W22
E19	GND<38>	GND<90>	W18
E18	GND<37>	GND<89>	W14
E15	GND<36>	GND<88>	W10
E14	GND<35>	GND<87>	W7
E5	GND<34>	GND<86>	W6
D22	GND<33>	GND<85>	V20
D21	GND<32>	GND<84>	V3
D20	GND<31>	GND<83>	T22
D17	GND<30>	GND<82>	T20
D16	GND<29>	GND<81>	T4
D13	GND<28>	GND<80>	R23
D9	GND<27>	GND<79>	R21
C22	GND<26>	GND<78>	R5
C21	GND<25>	GND<77>	R3
C20	GND<24>	GND<76>	P22
C19	GND<23>	GND<75>	P20
C18	GND<22>	GND<74>	P13
C17	GND<21>	GND<73>	P11
C16	GND<20>	GND<72>	N23
C15	GND<19>	GND<71>	N21
C14	GND<18>	GND<70>	N14
C6	GND<17>	GND<69>	N13
C3	GND<16>	GND<68>	N12
B22	GND<15>	GND<67>	N11
B20	GND<14>	GND<66>	N10
B19	GND<13>	GND<65>	N5
B18	GND<12>	GND<64>	M22
B15	GND<11>	GND<63>	M20
B14	GND<10>	GND<62>	M13
B13	GND<9>	GND<61>	M12
B10	GND<8>	GND<60>	M11
B8	GND<7>	GND<59>	L23
A23	GND<6>	GND<58>	L21
A20	GND<5>	GND<57>	L14
A17	GND<4>	GND<56>	L13
A16	GND<3>	GND<55>	L12
A13	GND<2>	GND<54>	L11
A1	GND<1>	GND<53>	L10

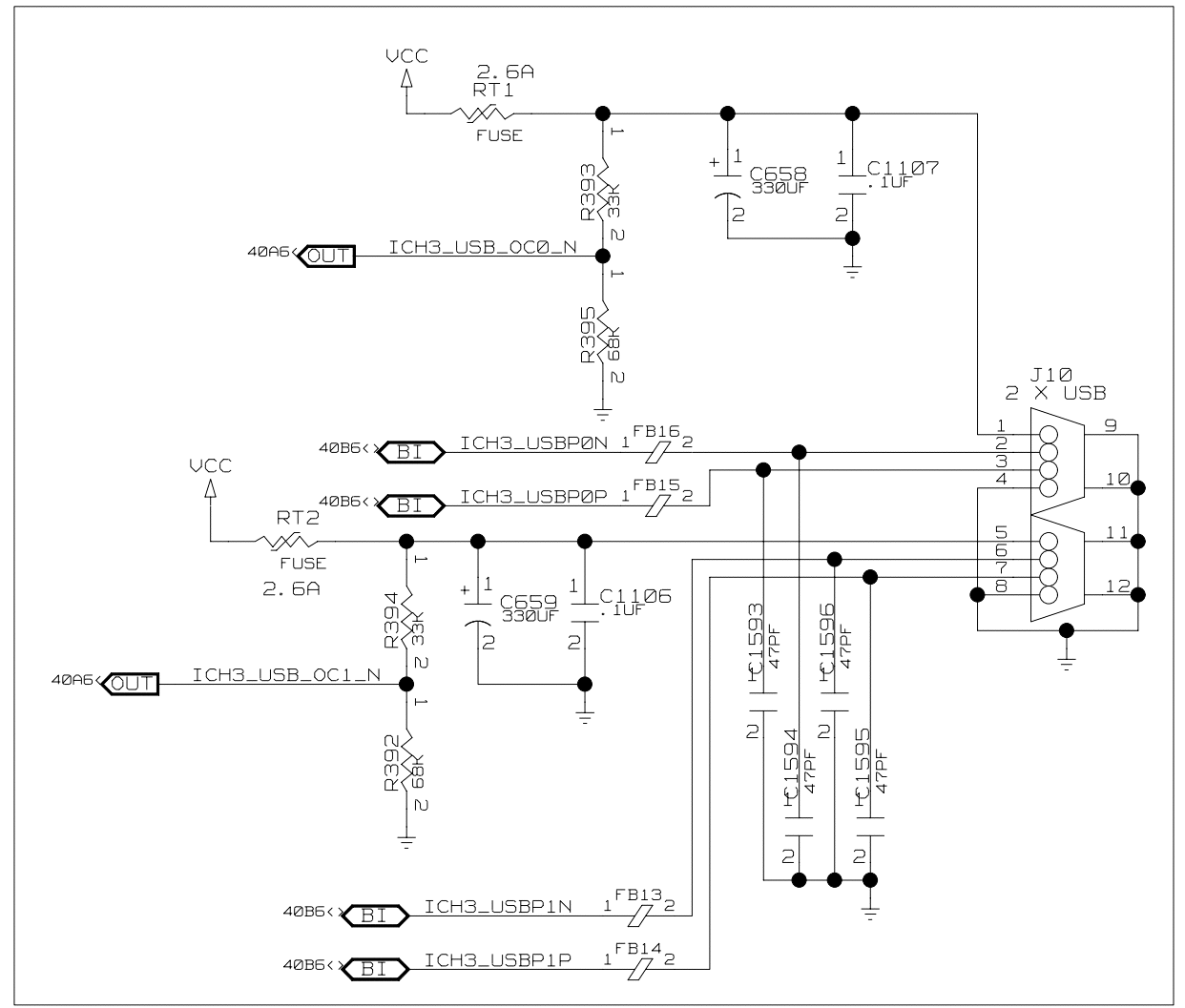
4 OF 4



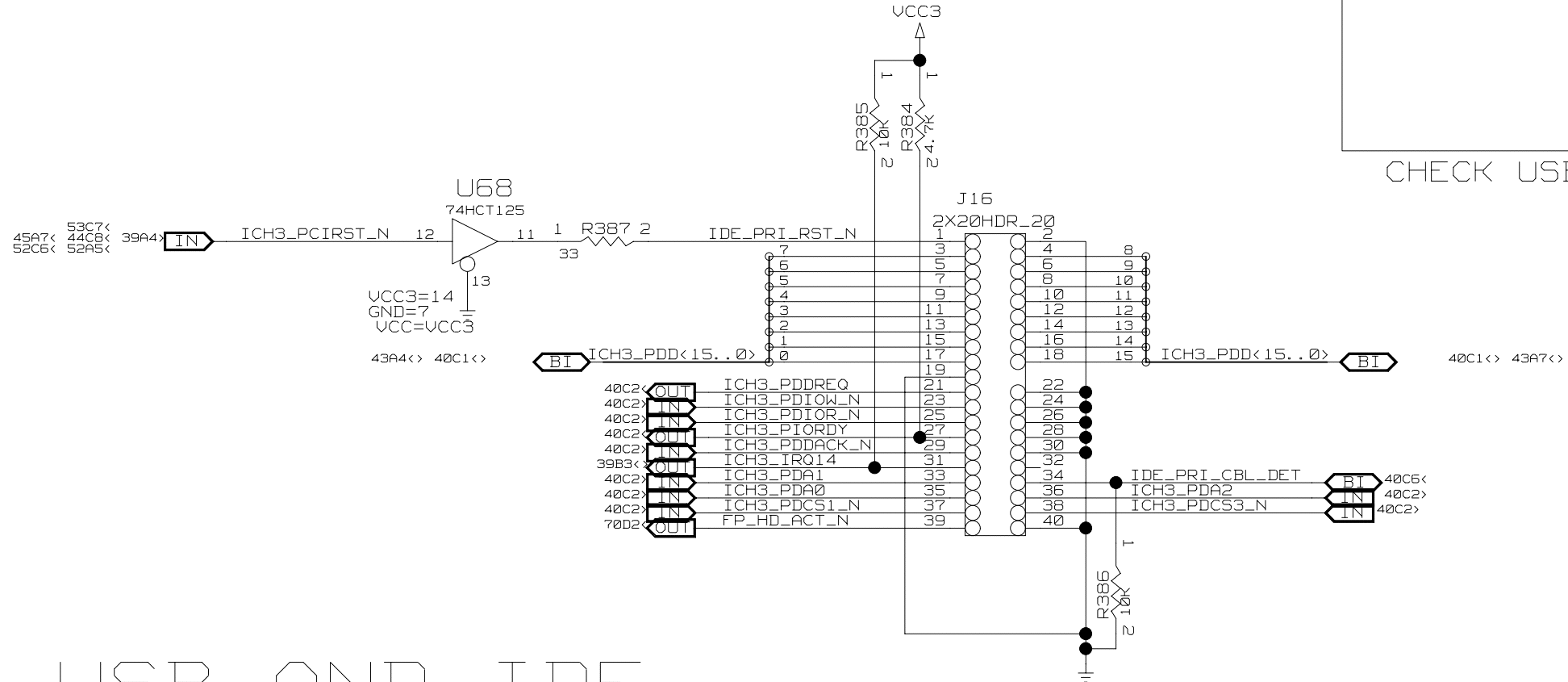
STRAP OPTIONS AND SPEAKER CIRCUITRY

ICH3 (PART 4 OF 4)

DRAWING



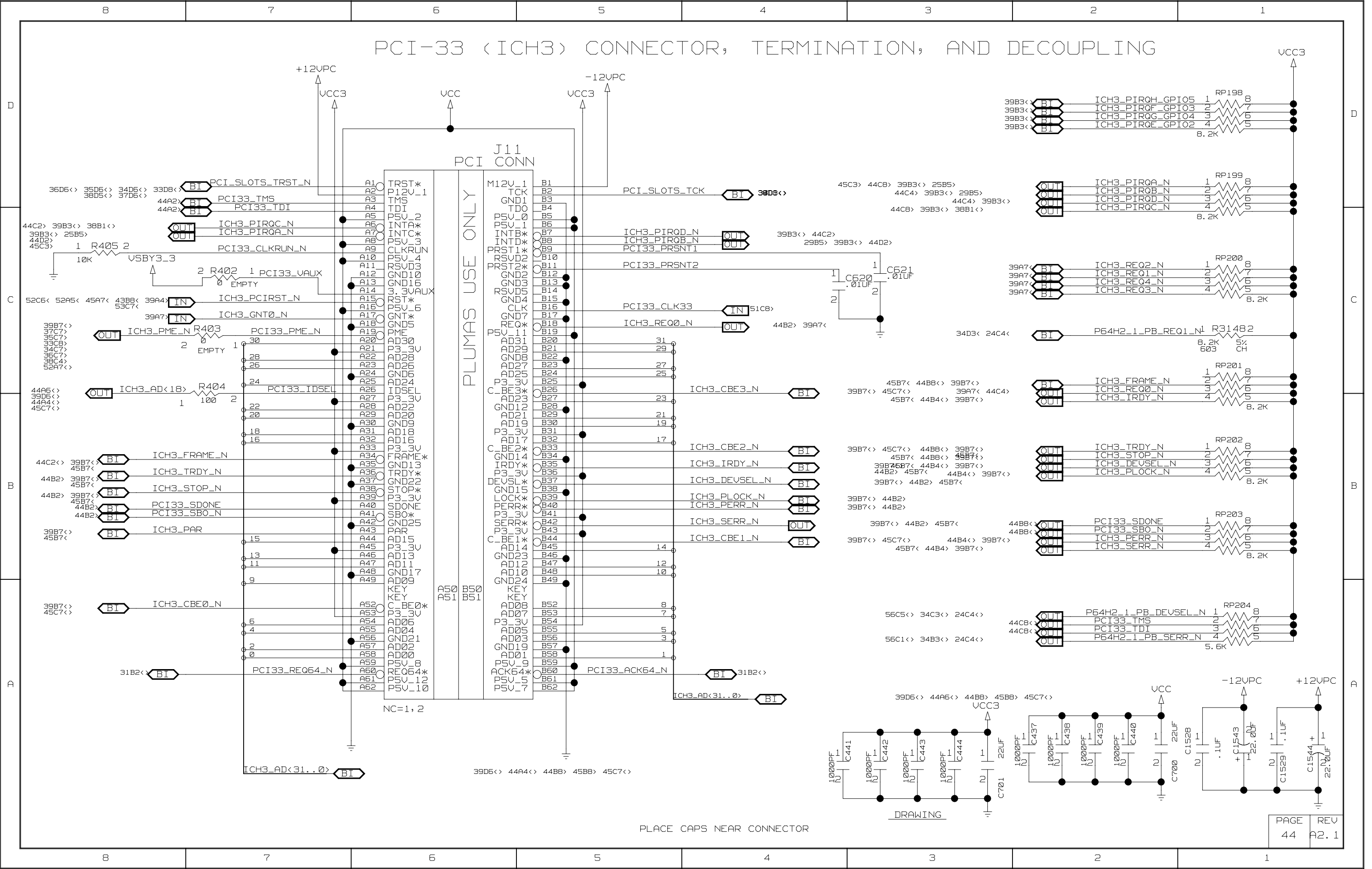
CHECK USB DESIGN GUIDELINES



USB AND IDE

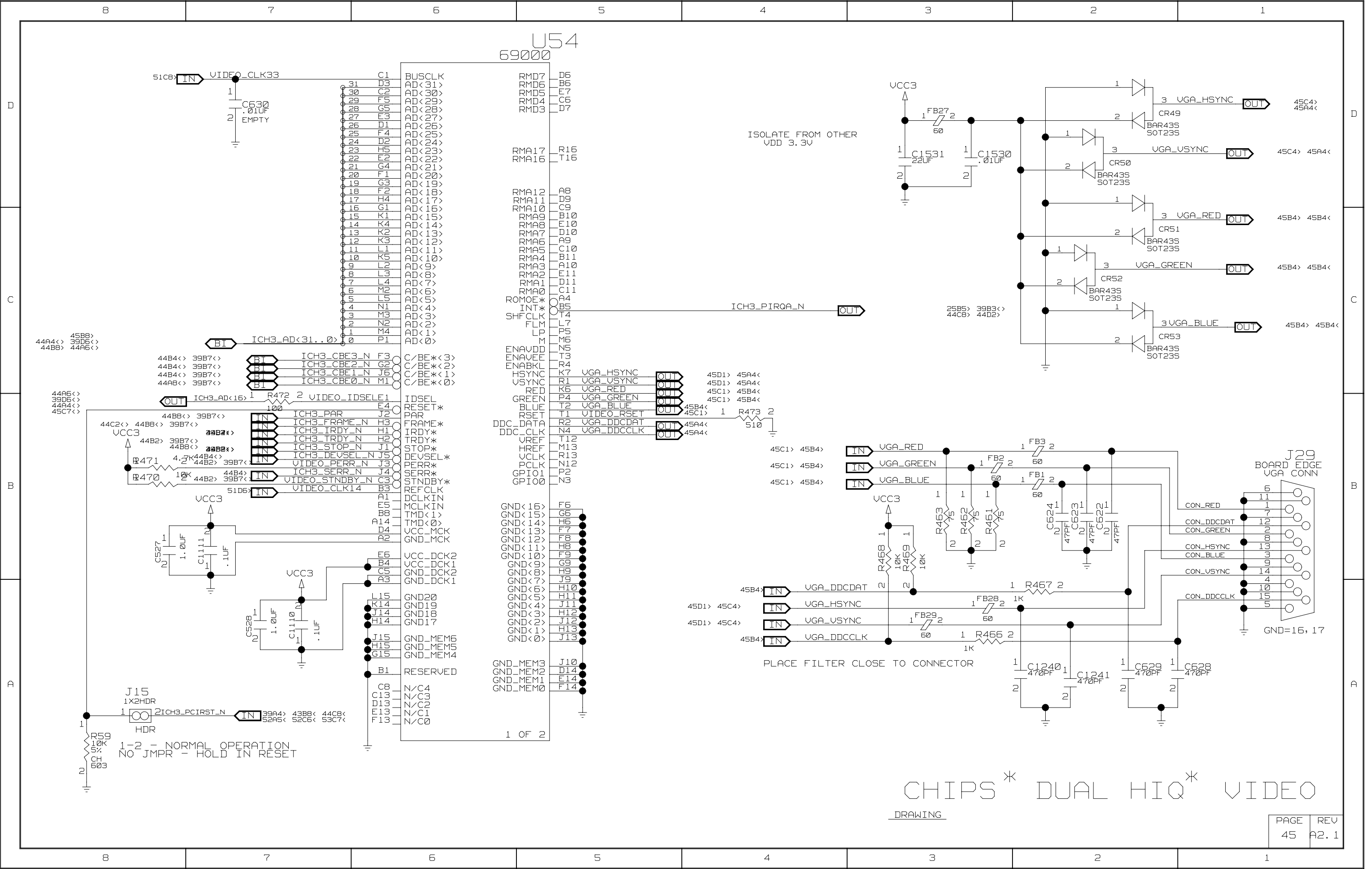
DRAWING

PCI-33 (ICH3) CONNECTOR, TERMINATION, AND DECOUPLING



PLACE CAPS NEAR CONNECTOR

DRAWING

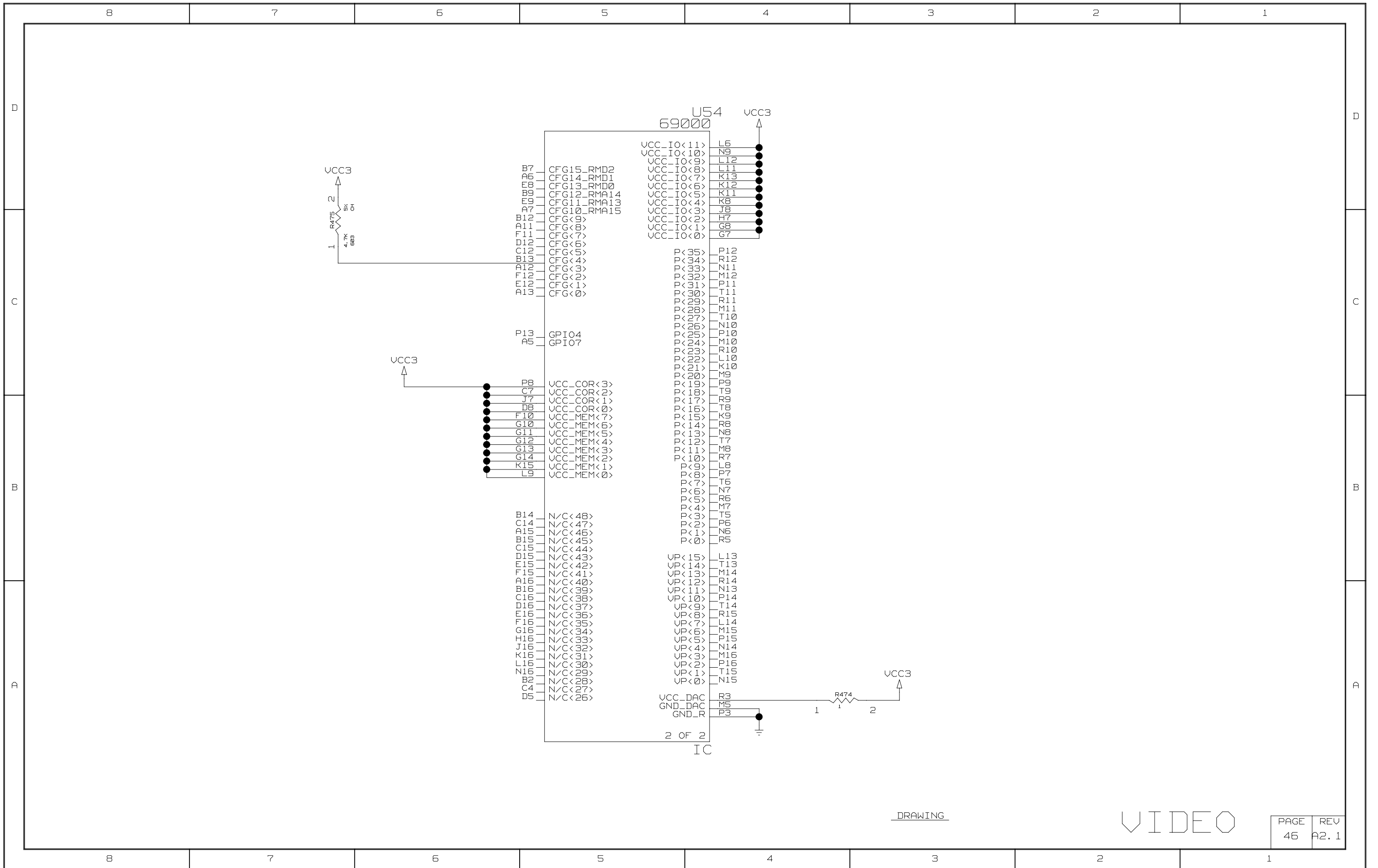


U54
69000

ISOLATE FROM OTHER
VDD 3.3V

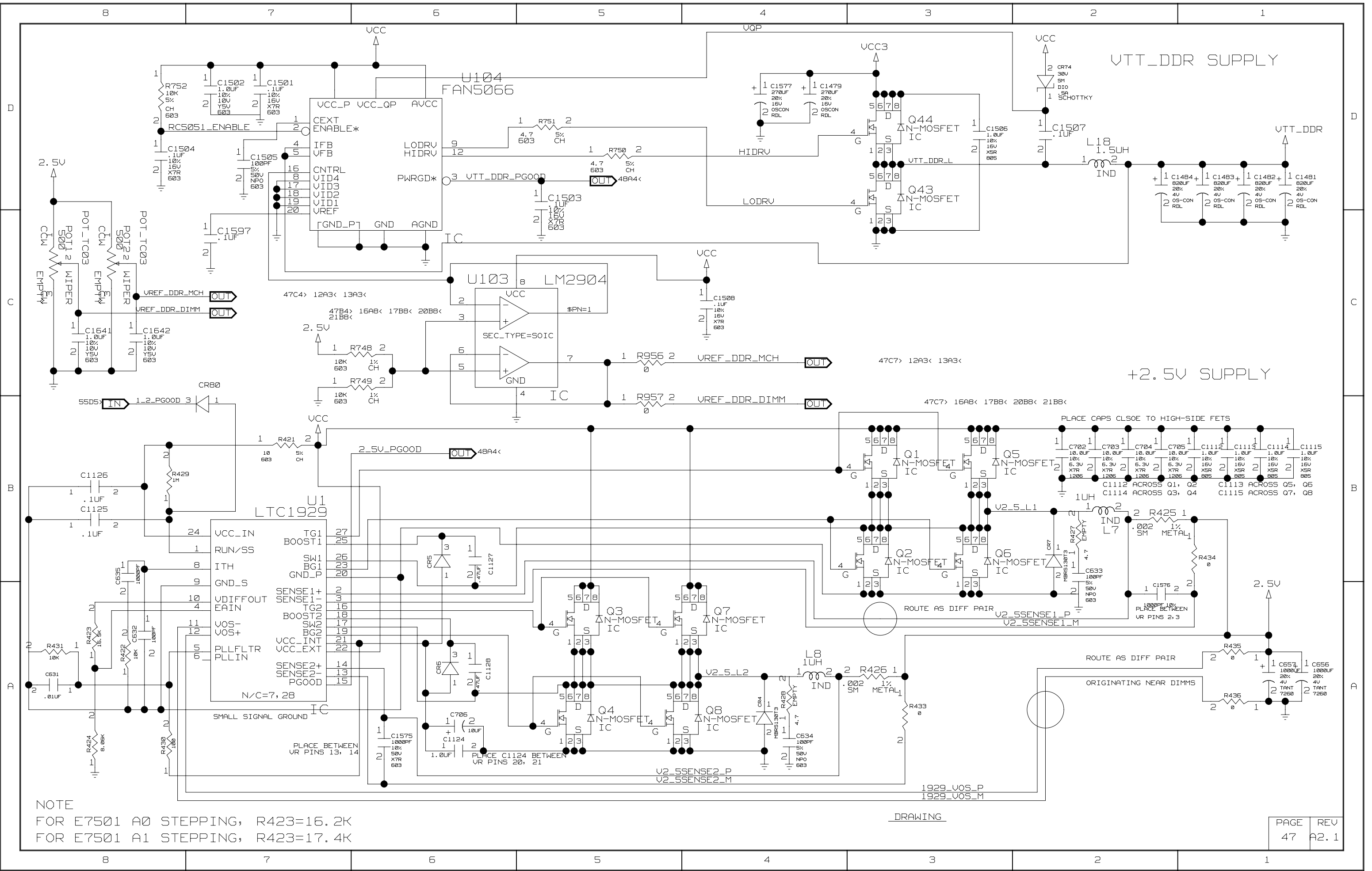
PLACE FILTER CLOSE TO CONNECTOR

CHIPS * DUAL HIQ * VIDEO
DRAWING



DRAWING

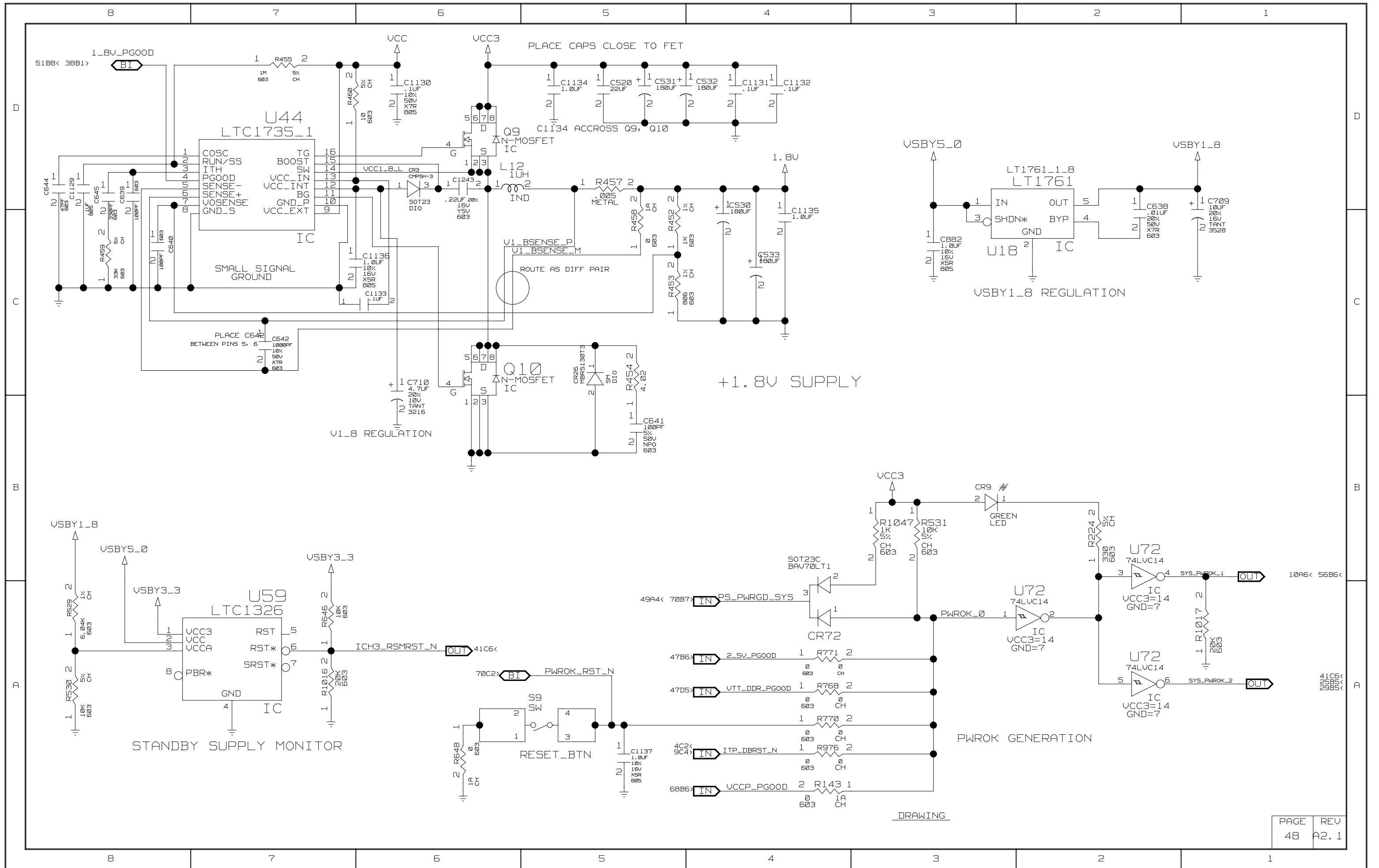
VIDEO



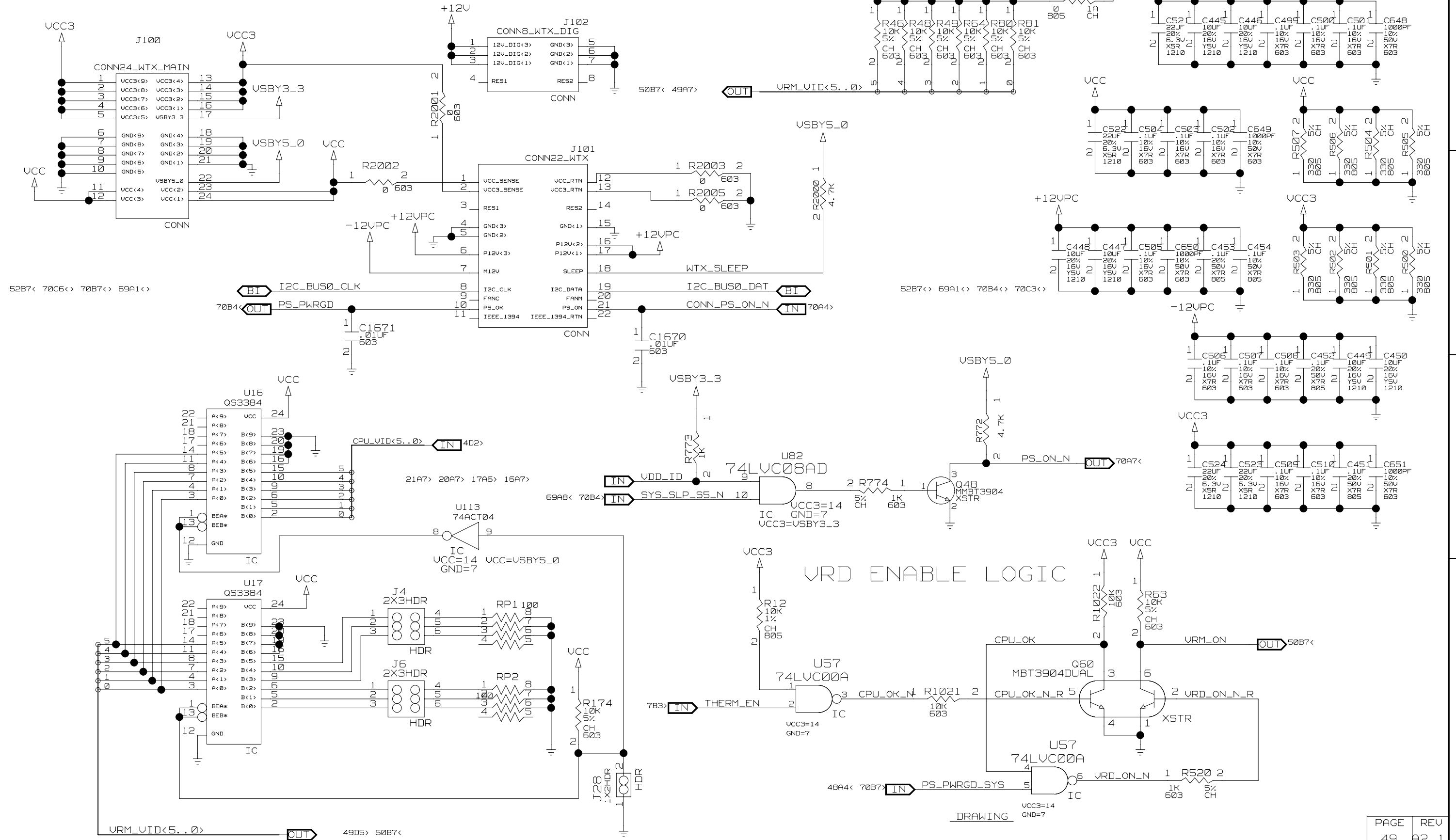
NOTE
 FOR E7501 A0 STEPPING, R423=16.2K
 FOR E7501 A1 STEPPING, R423=17.4K

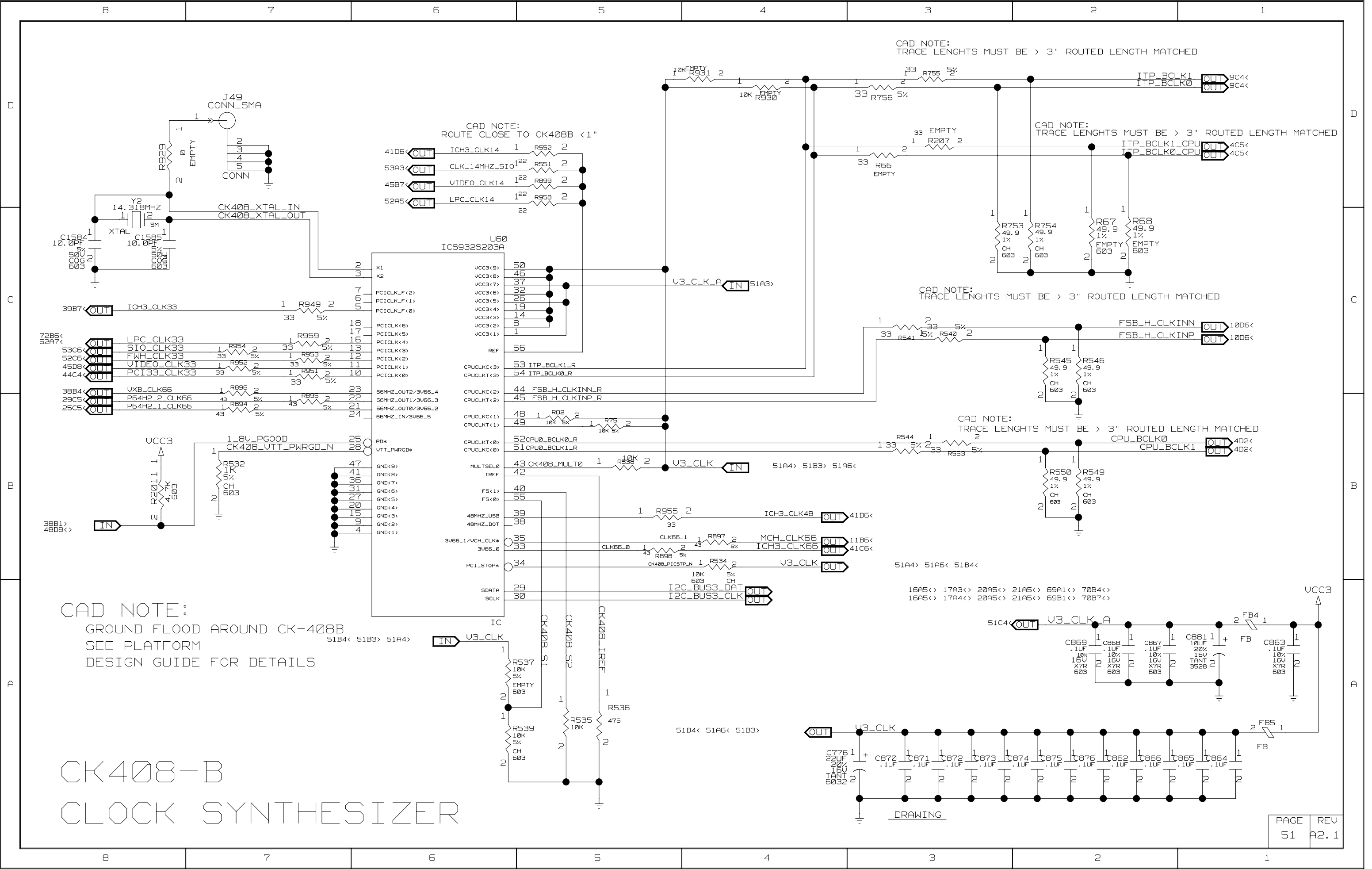
DRAWING

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POWER CONNECTORS





CAD NOTE:
TRACE LENGTHS MUST BE > 3" ROUTED LENGTH MATCHED

CAD NOTE:
ROUTE CLOSE TO CK408B < 1"

CAD NOTE:
TRACE LENGTHS MUST BE > 3" ROUTED LENGTH MATCHED

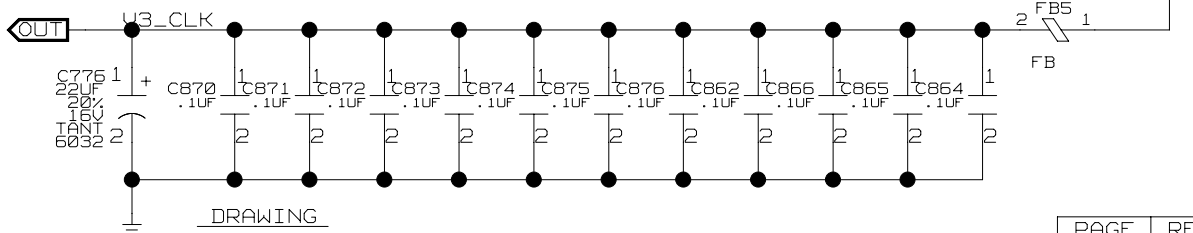
CAD NOTE:
TRACE LENGTHS MUST BE > 3" ROUTED LENGTH MATCHED

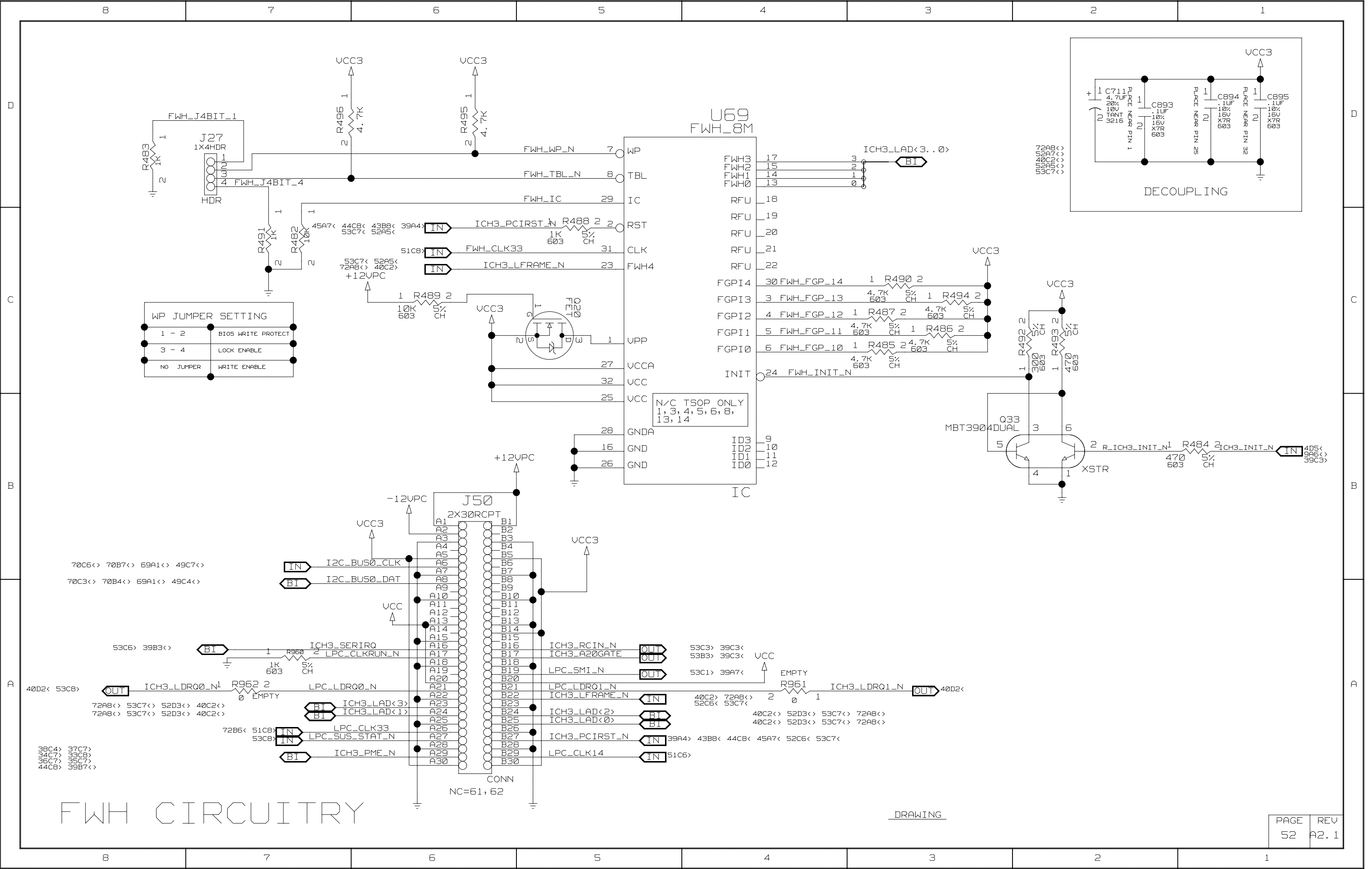
CAD NOTE:
TRACE LENGTHS MUST BE > 3" ROUTED LENGTH MATCHED

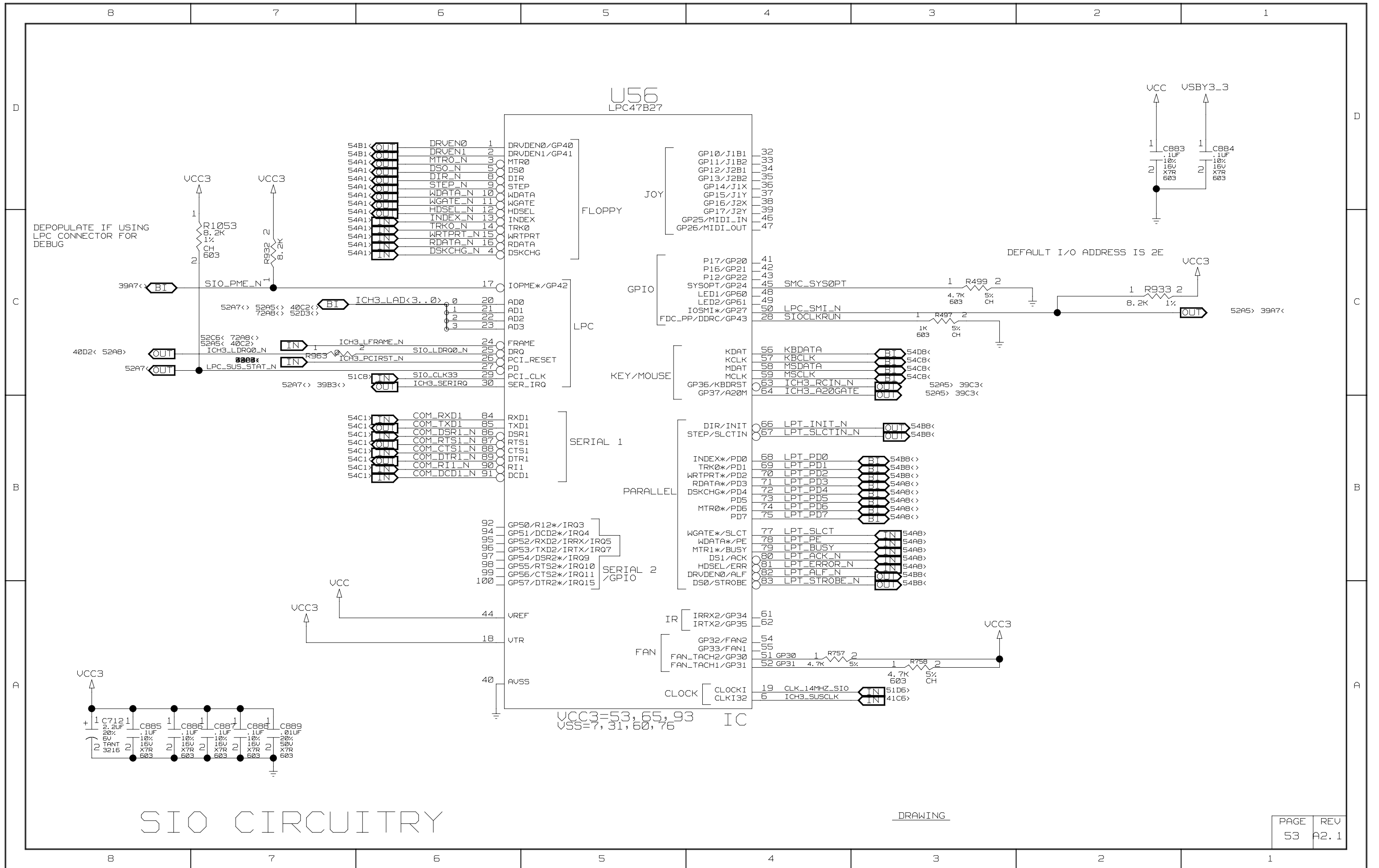
CAD NOTE:
GROUND FLOOD AROUND CK-408B
SEE PLATFORM
DESIGN GUIDE FOR DETAILS

CK408-B CLOCK SYNTHESIZER

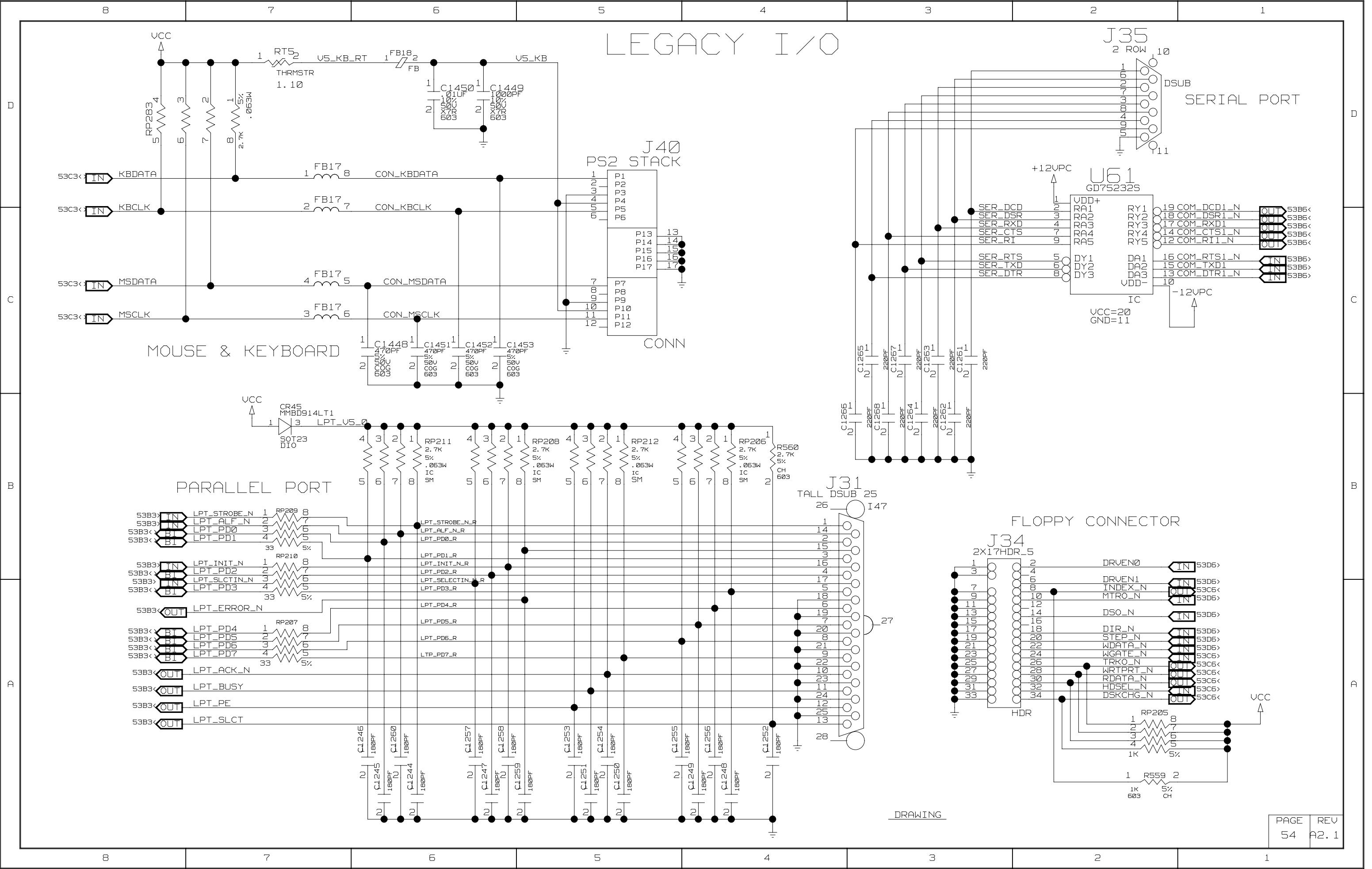
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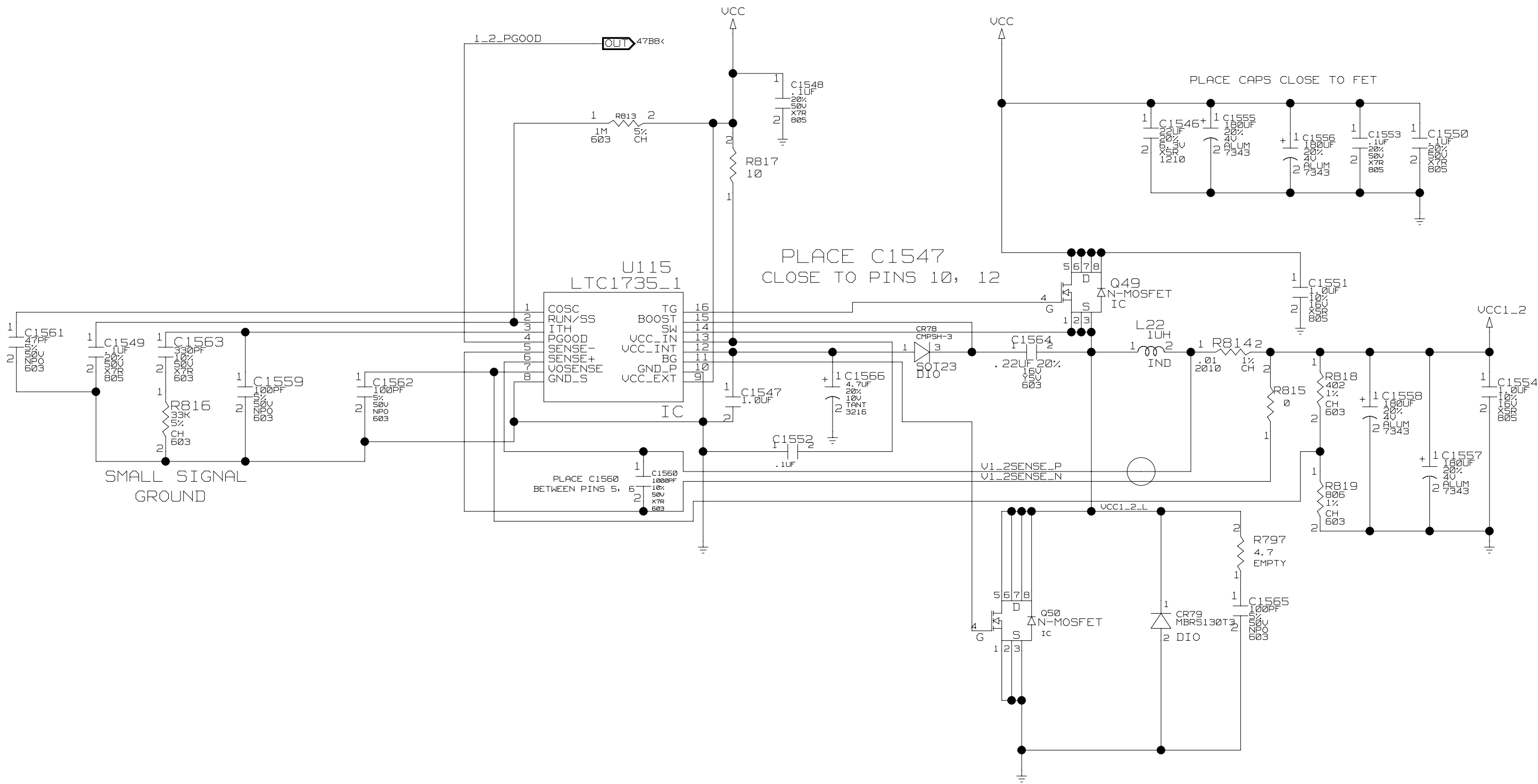
LEGACY I/O



DRAWING

V1.2 REGULATION

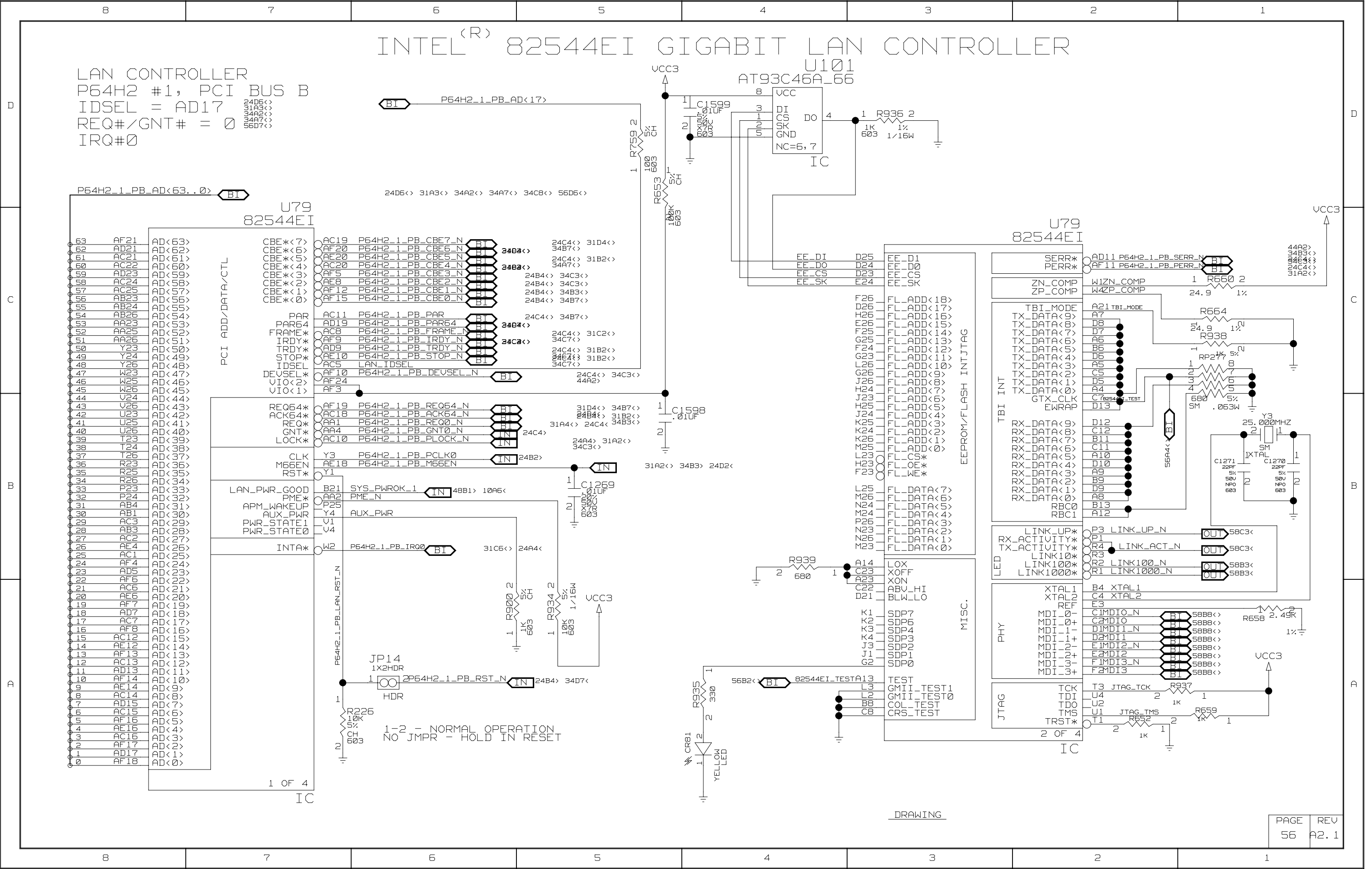
NOTE: ROUTE AS DIFFERENTIAL PAIR



DRAWING

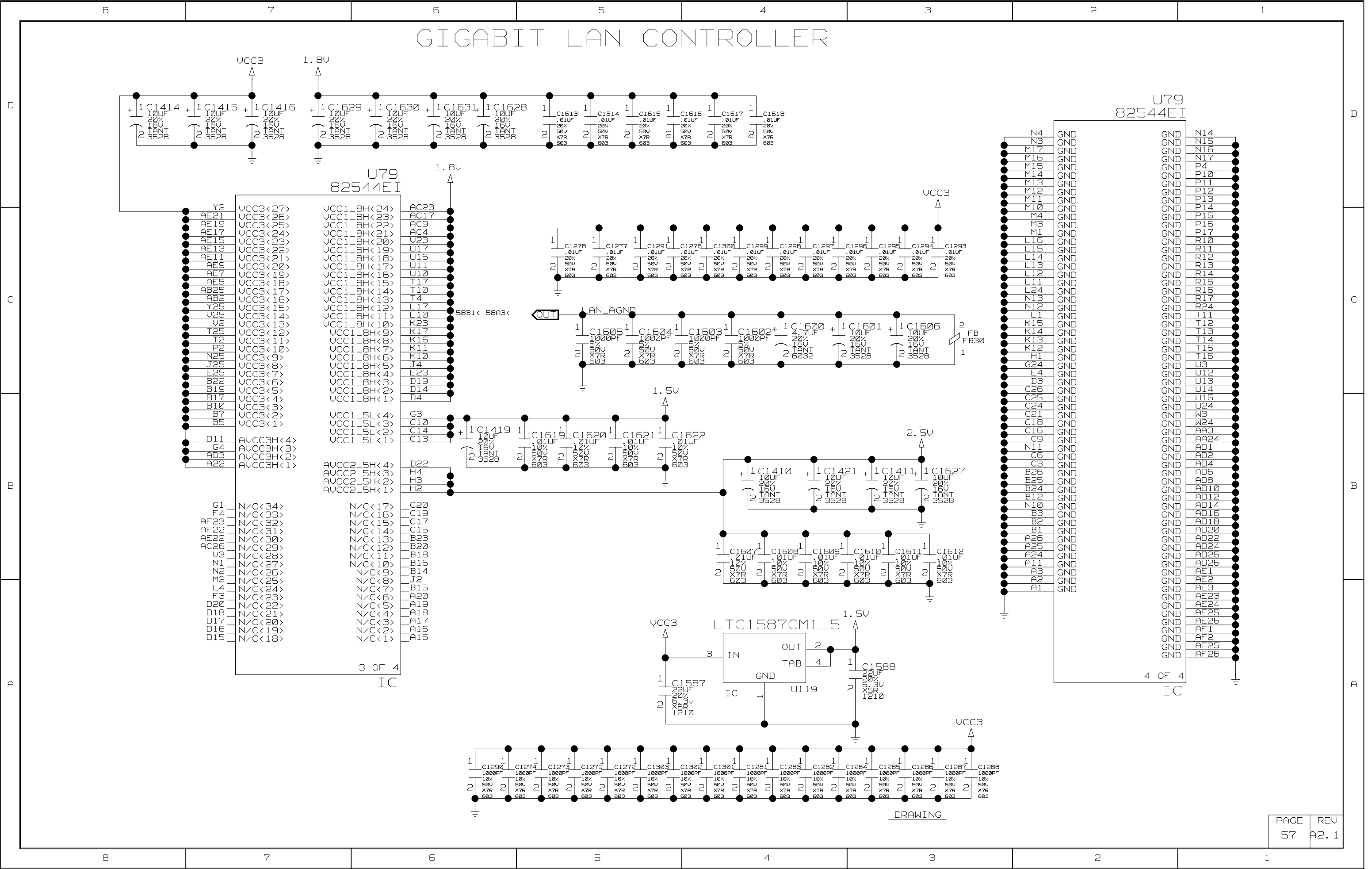
INTEL^(R) 82544EI GIGABIT LAN CONTROLLER

LAN CONTROLLER
 P64H2 #1, PCI BUS B
 IDSEL = AD17
 REQ#/GNT# = 0
 IRQ#0

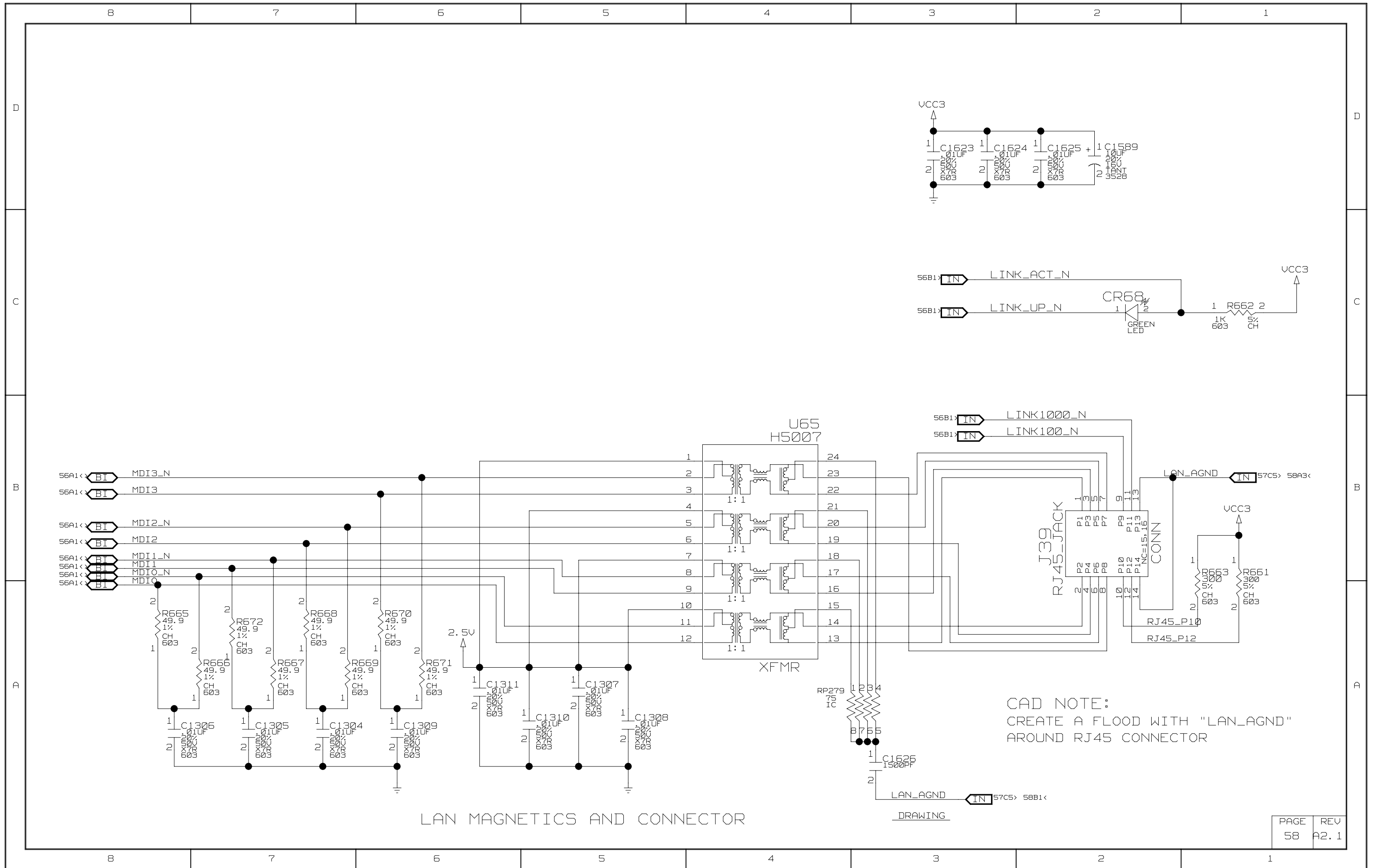


DRAWING

GIGABIT LAN CONTROLLER

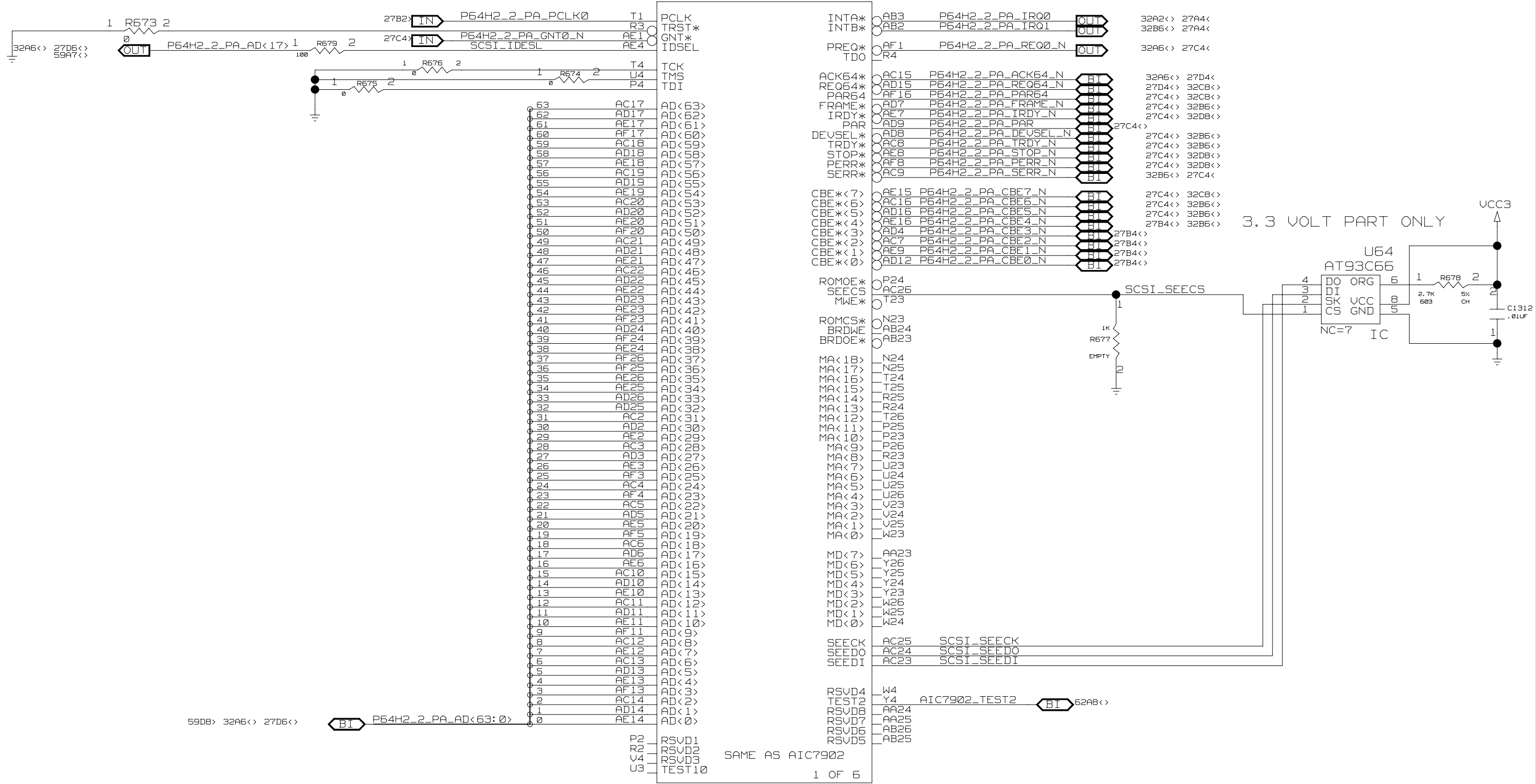


DRAWING



SCSI CONTROLLER

U78
AIC_7902A



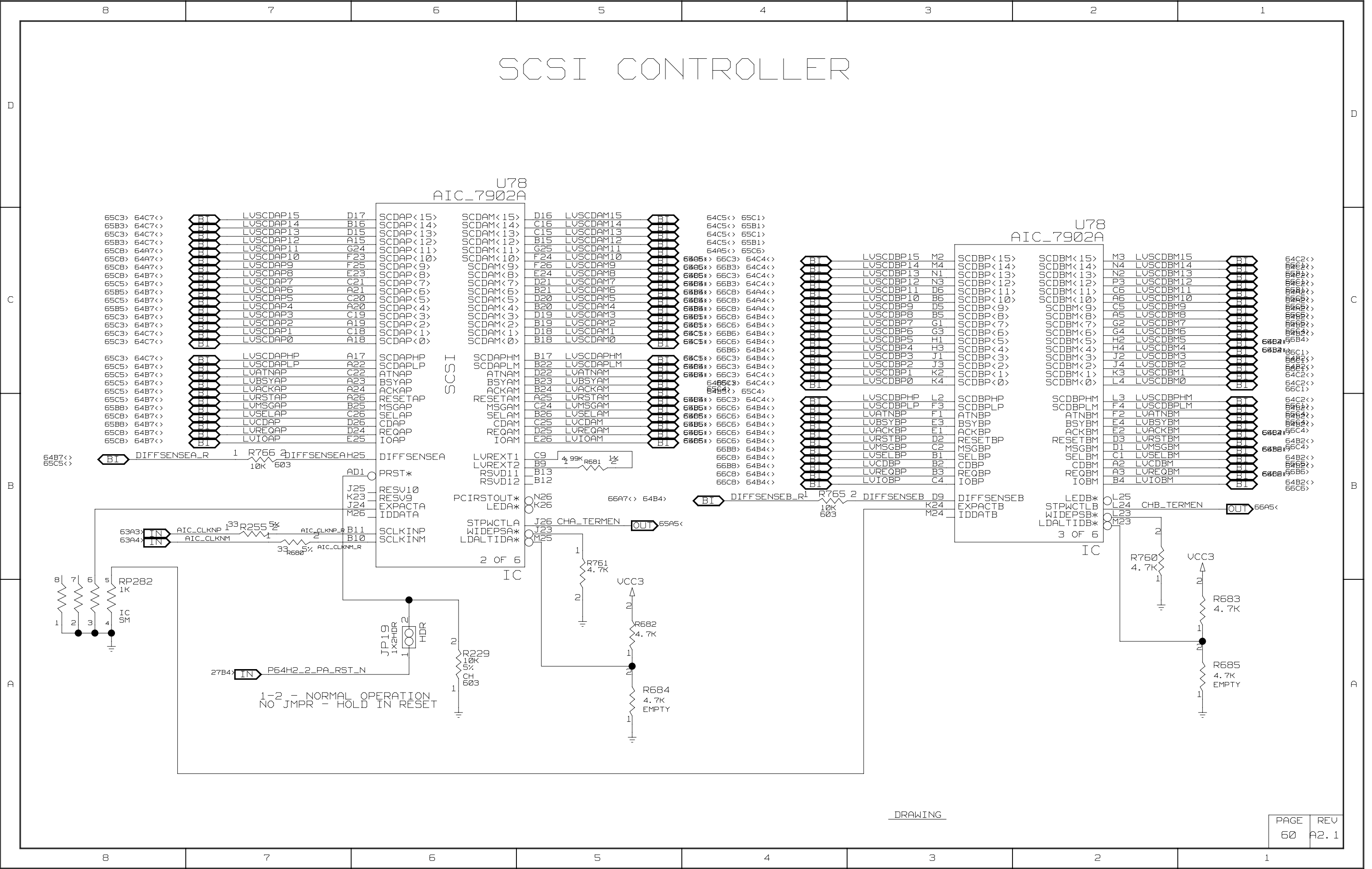
SAME AS AIC7902

1 OF 6

IC

DRAWING

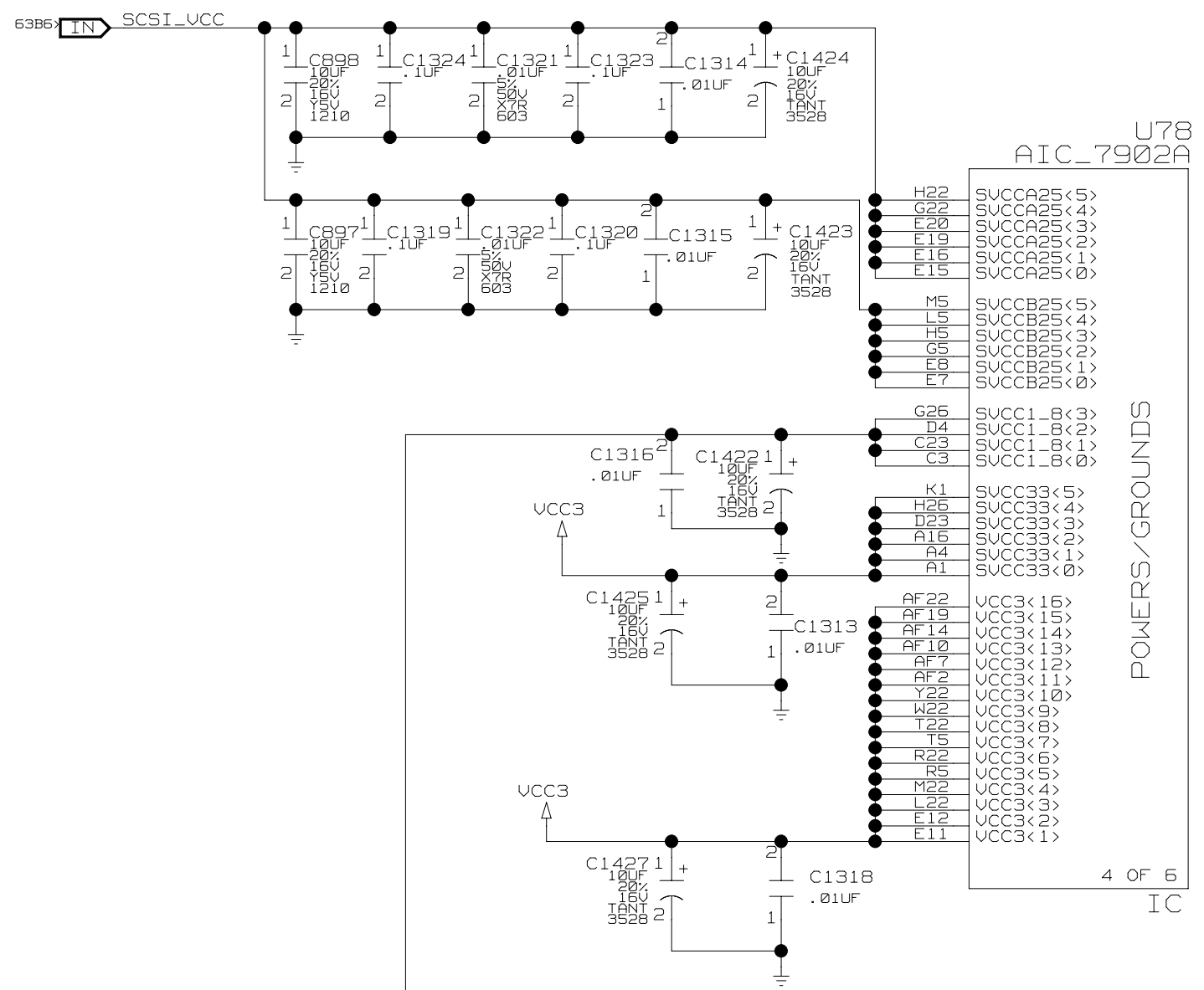
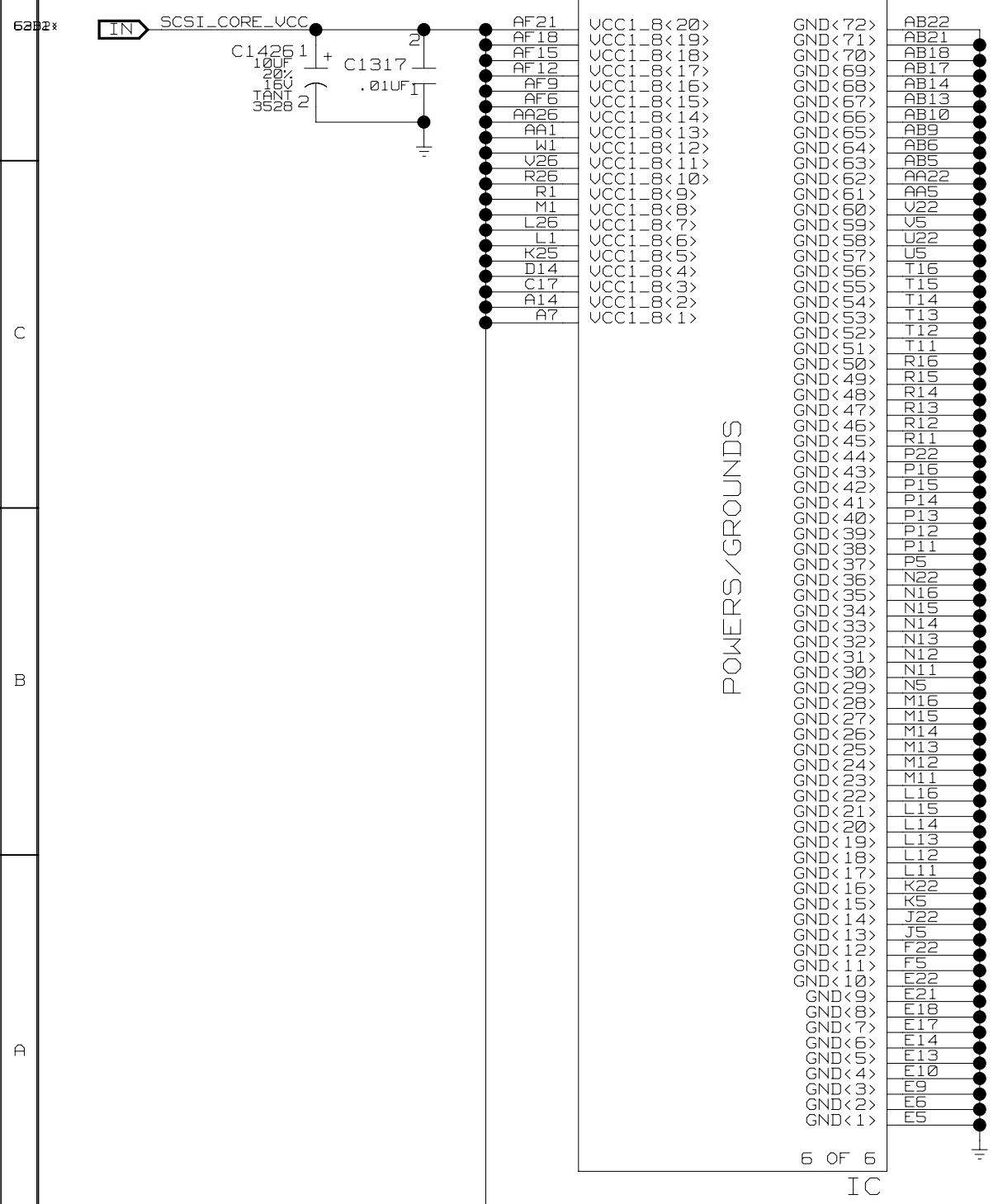
SCSI CONTROLLER



DRAWING

SCSI CONTROLLER

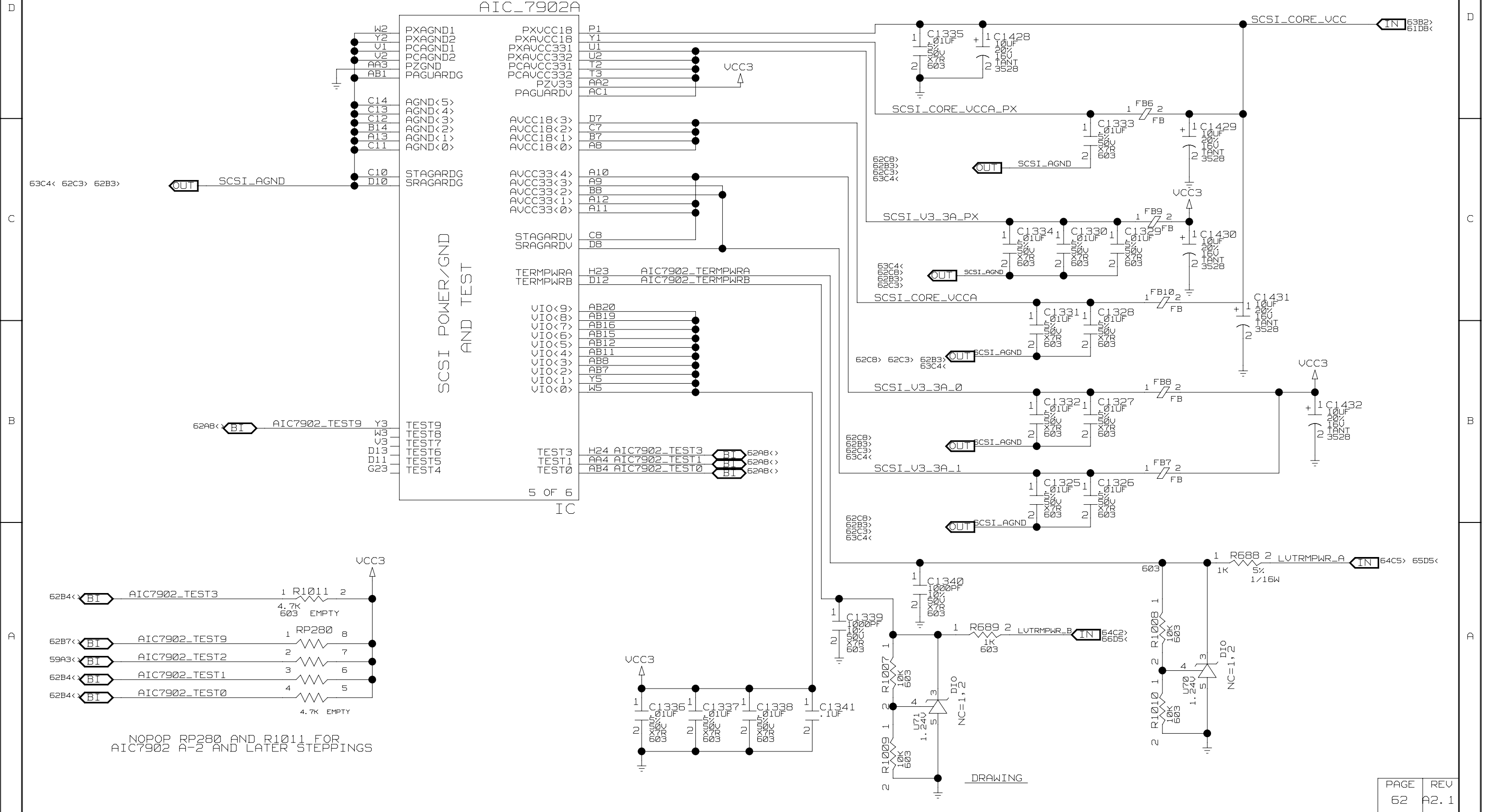
U78
AIC_7902A



DRAWING

SCSI CONTROLLER

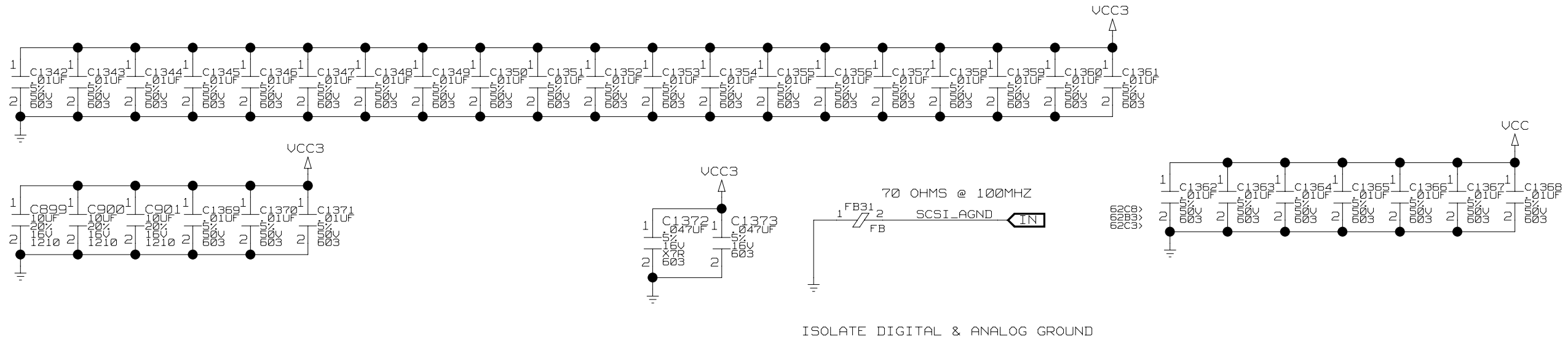
U78
AIC_7902A



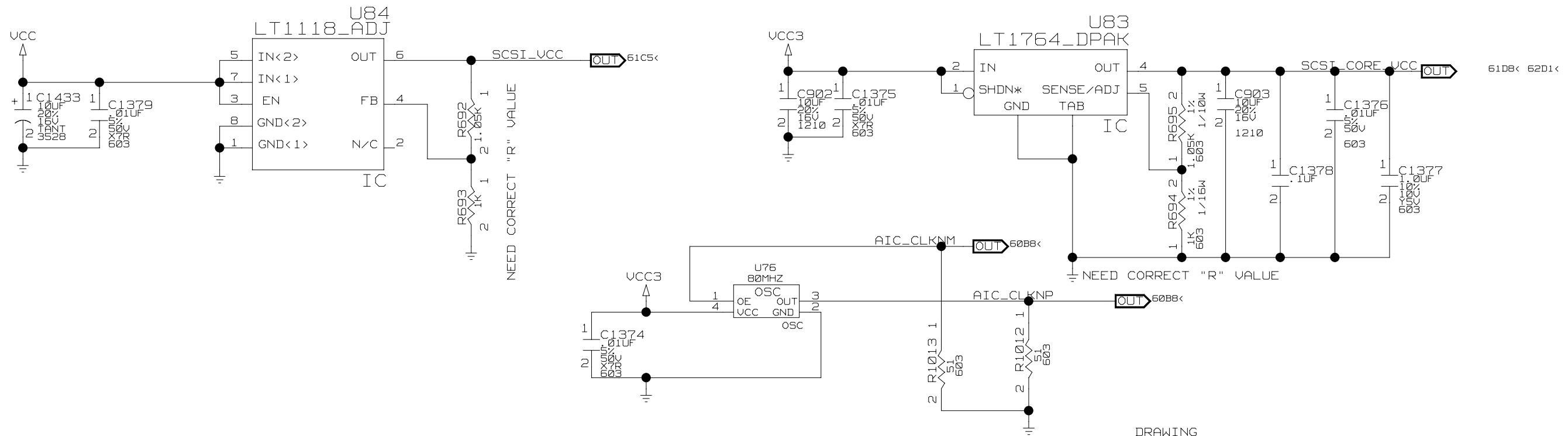
NOPOP RP280 AND R1011 FOR AIC7902 A-2 AND LATER STEPPINGS

DRAWING

AIC - 7902 SCSI DECOUPLING RECOMMENDATION FOR POWER SUPPLIES



VOLTAGE REGULATORS AND SCSI CLOCK



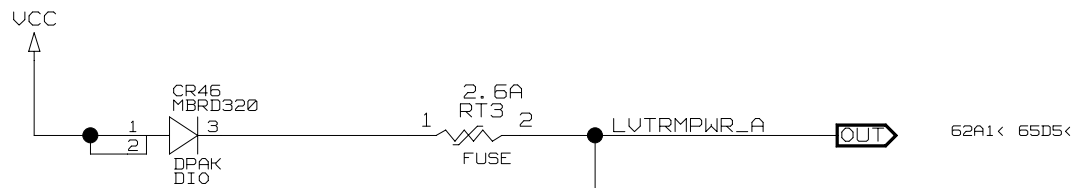
DRAWING

SCSI CONNECTORS A AND B

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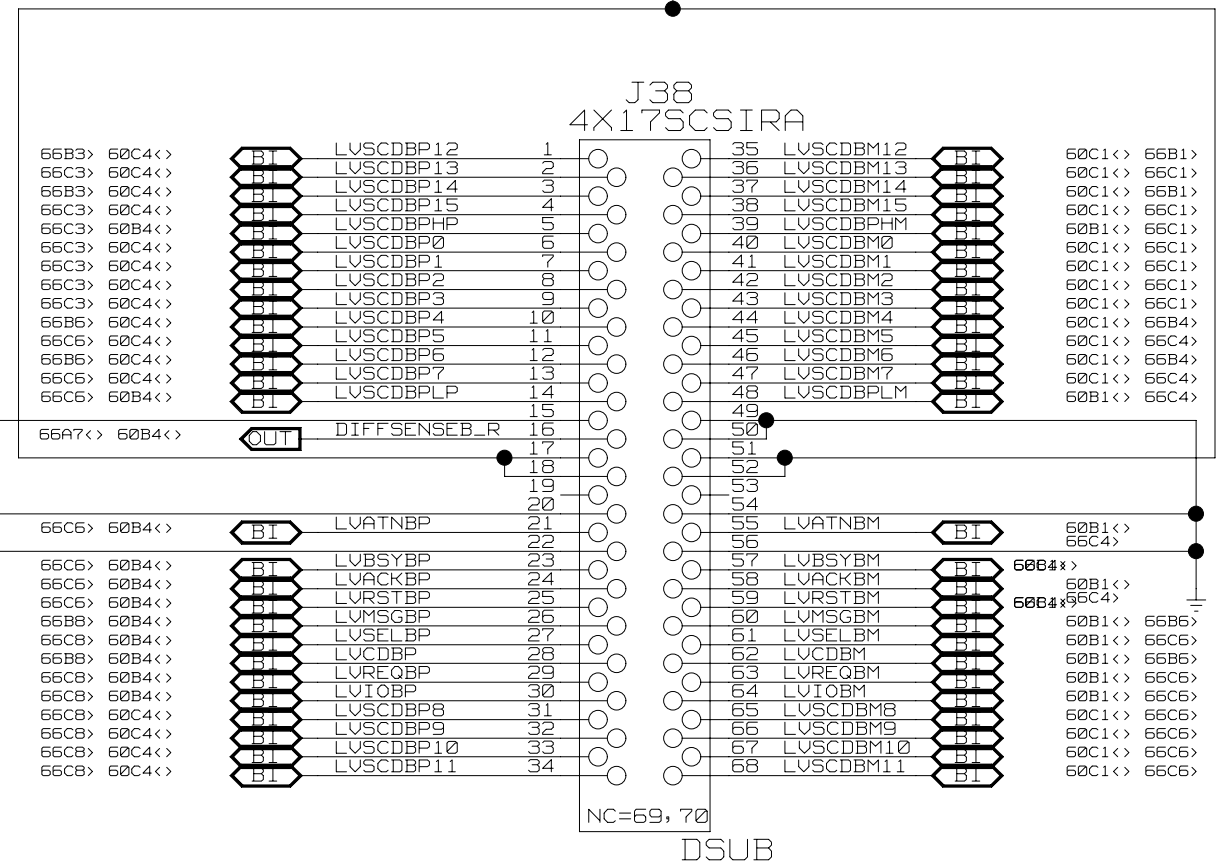
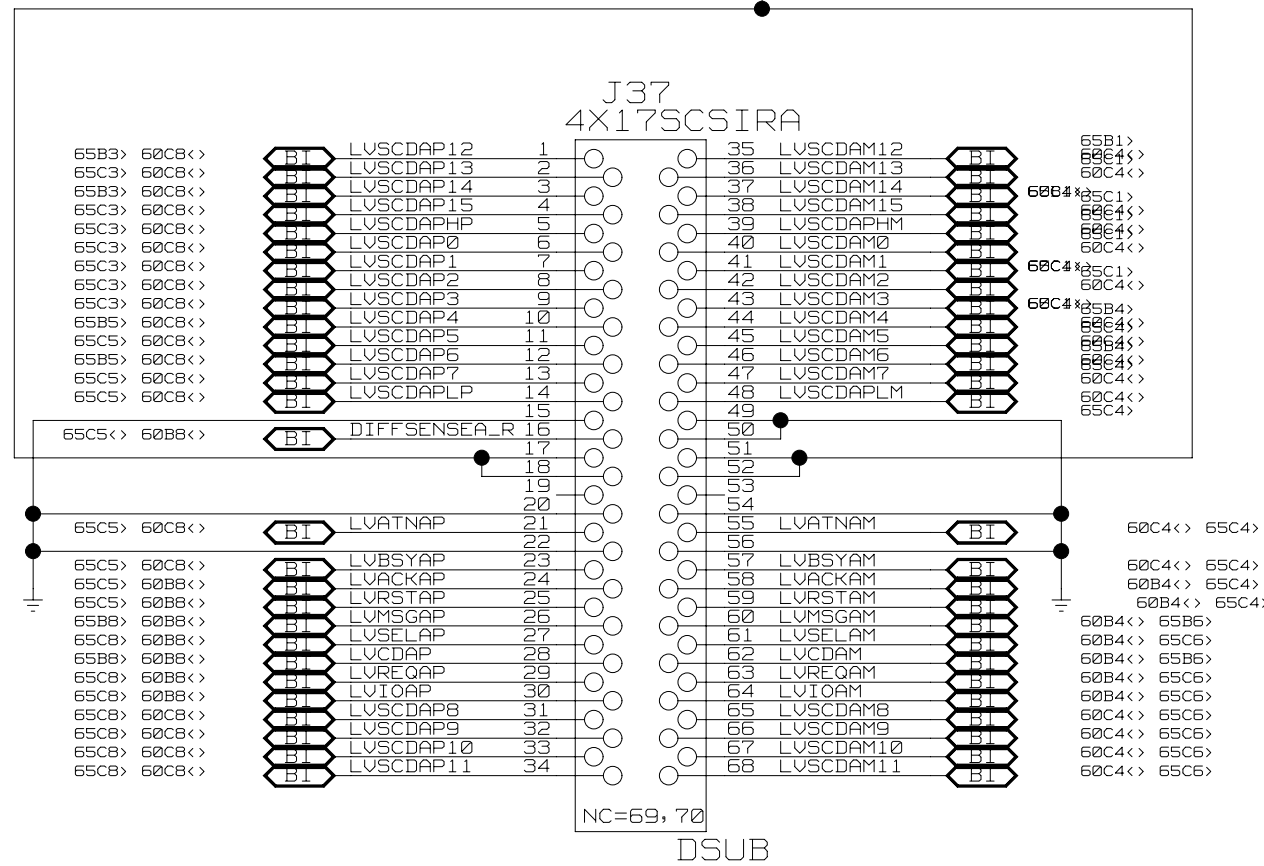
D

D



C

C



B

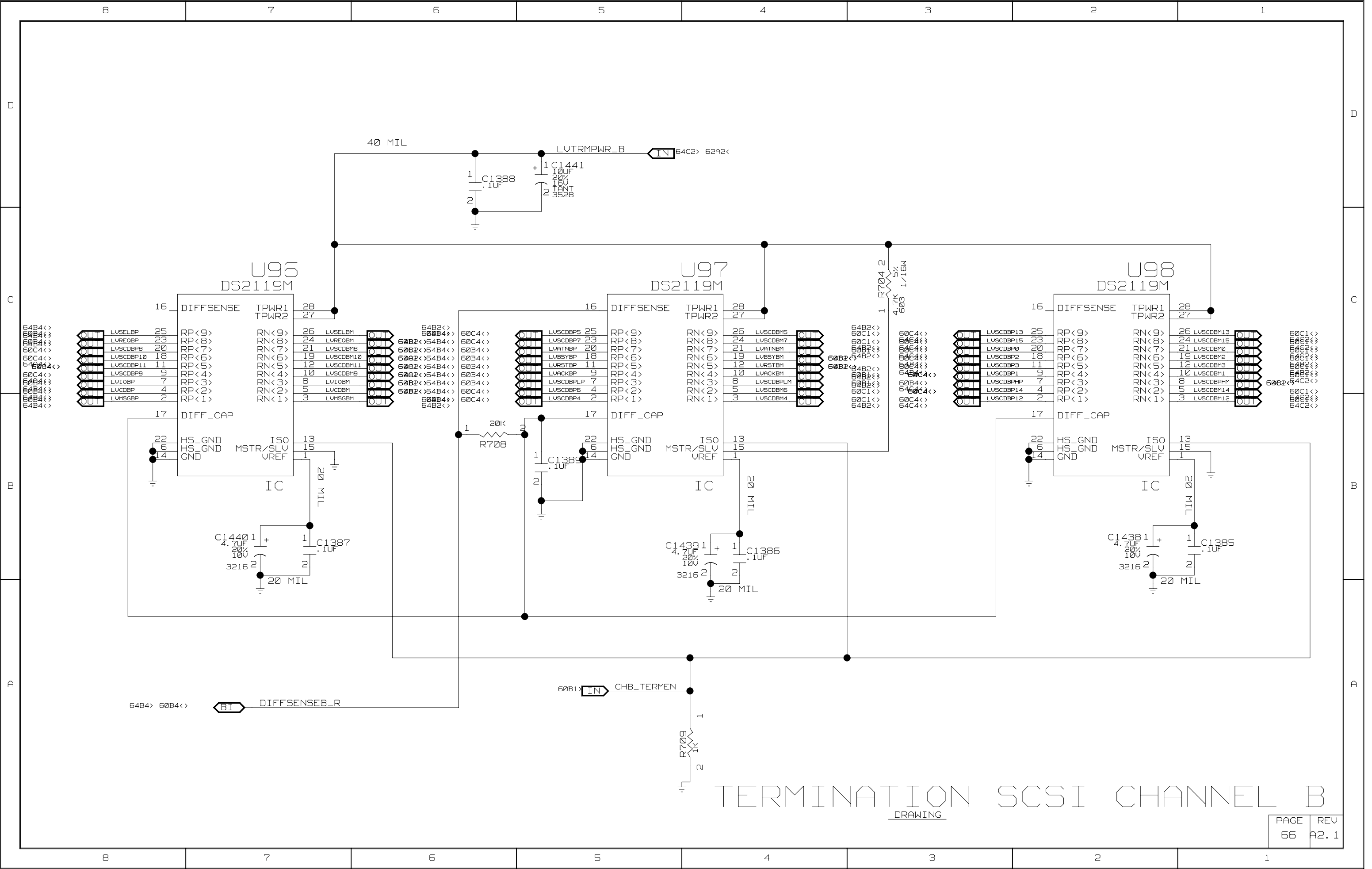
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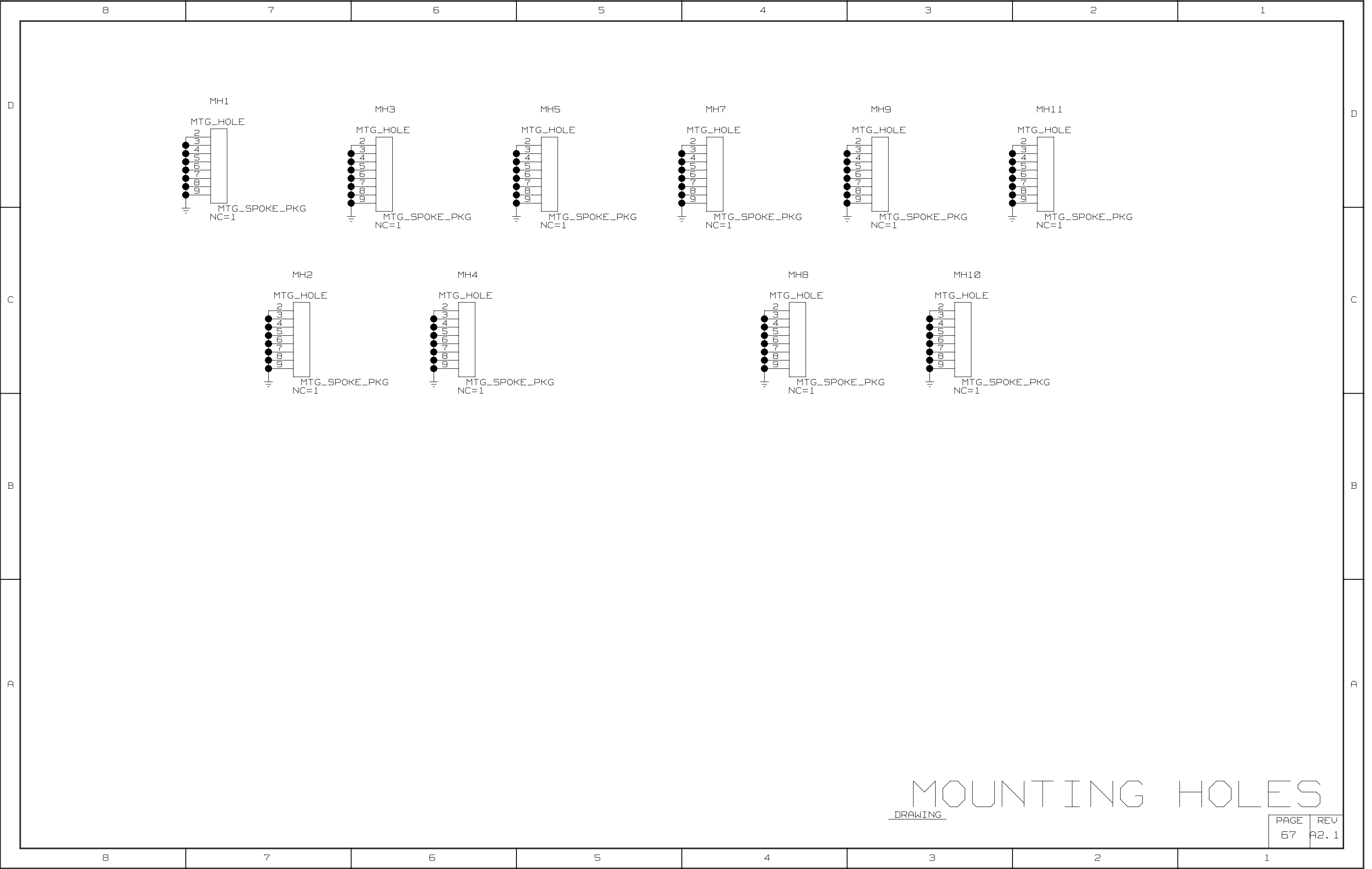
A

A

8 7 6 5 4 3 2 1

DRAWING

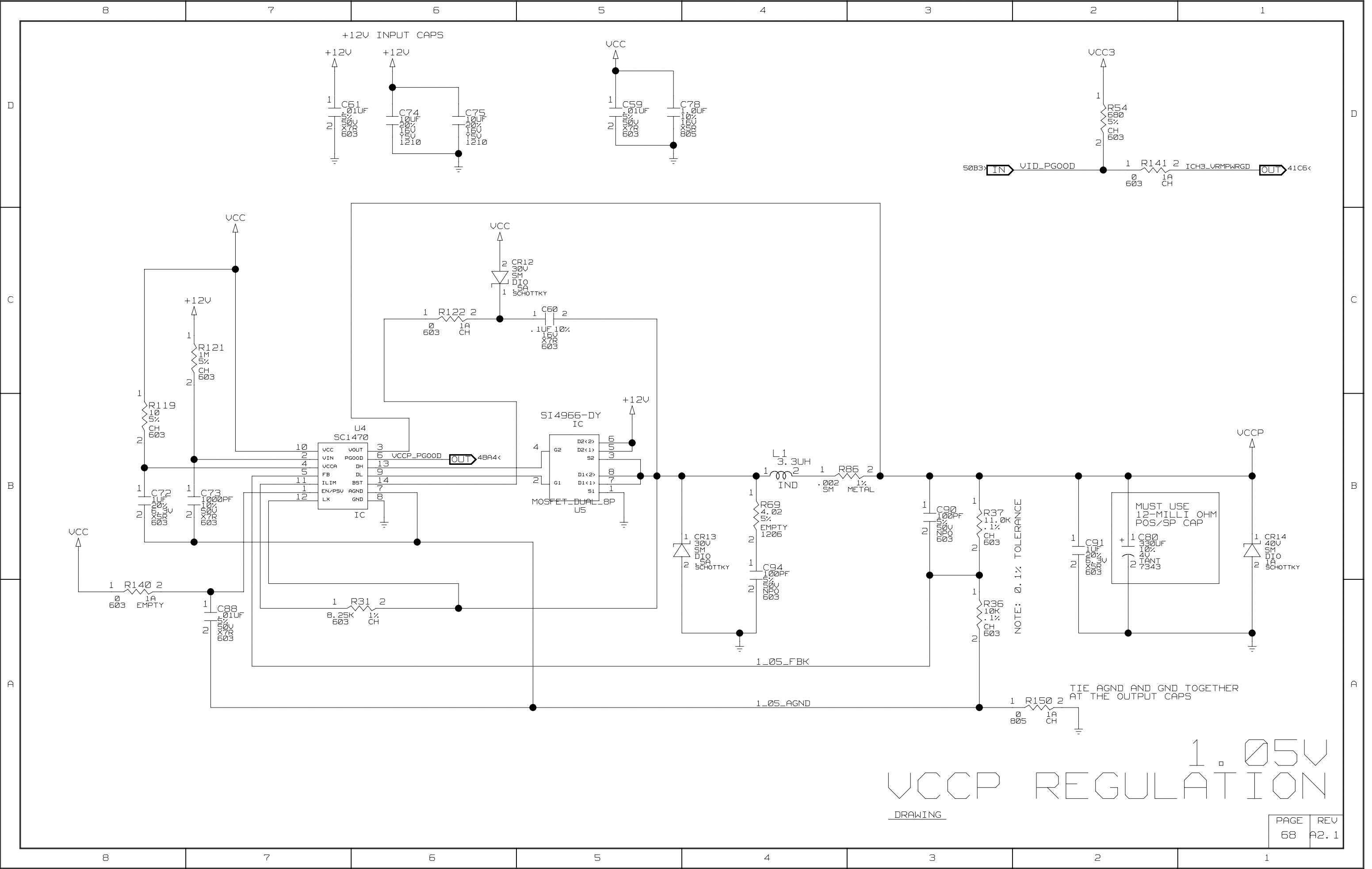




MOUNTING HOLES

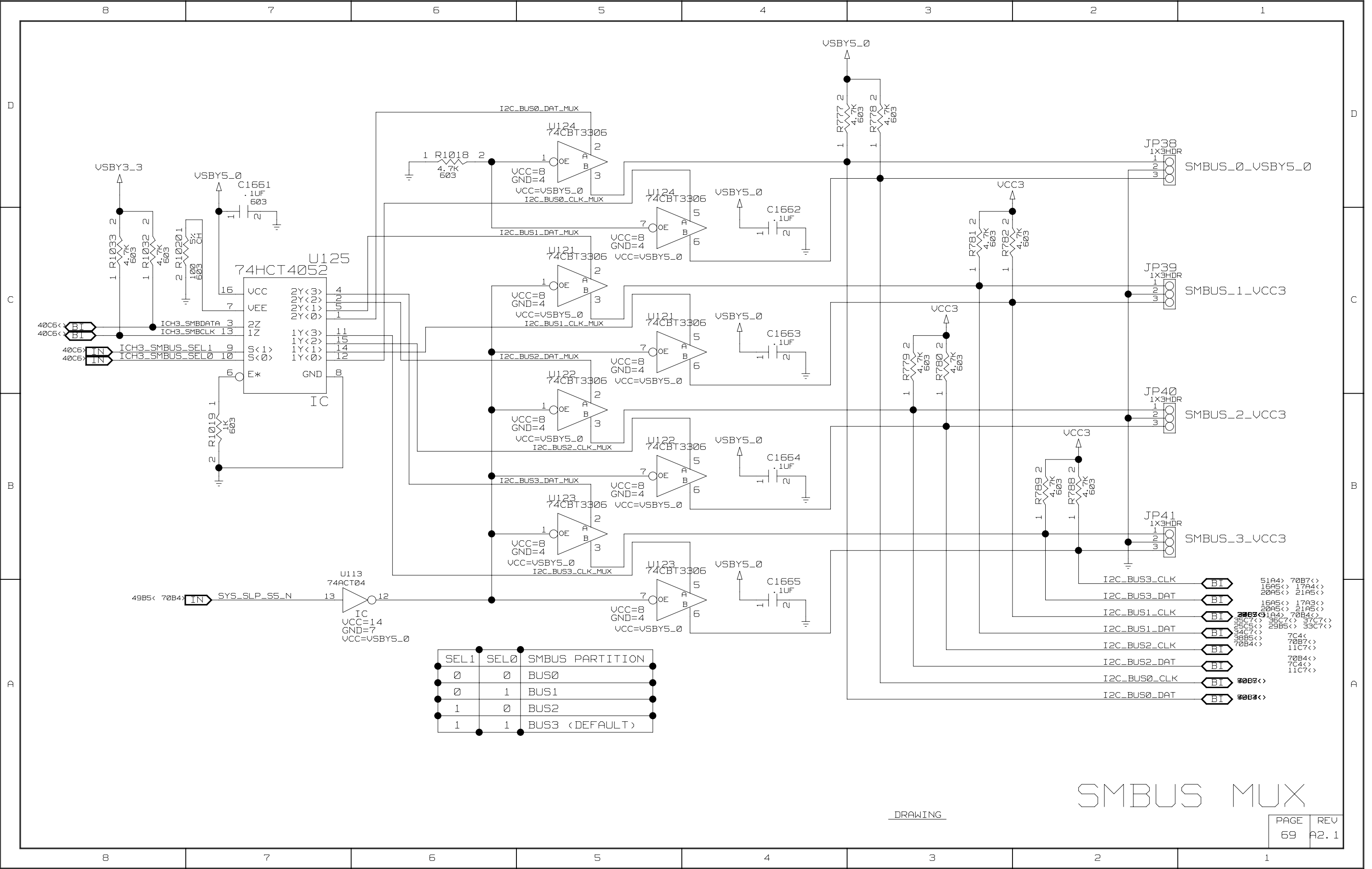
DRAWING

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1.05V VCCP REGULATION

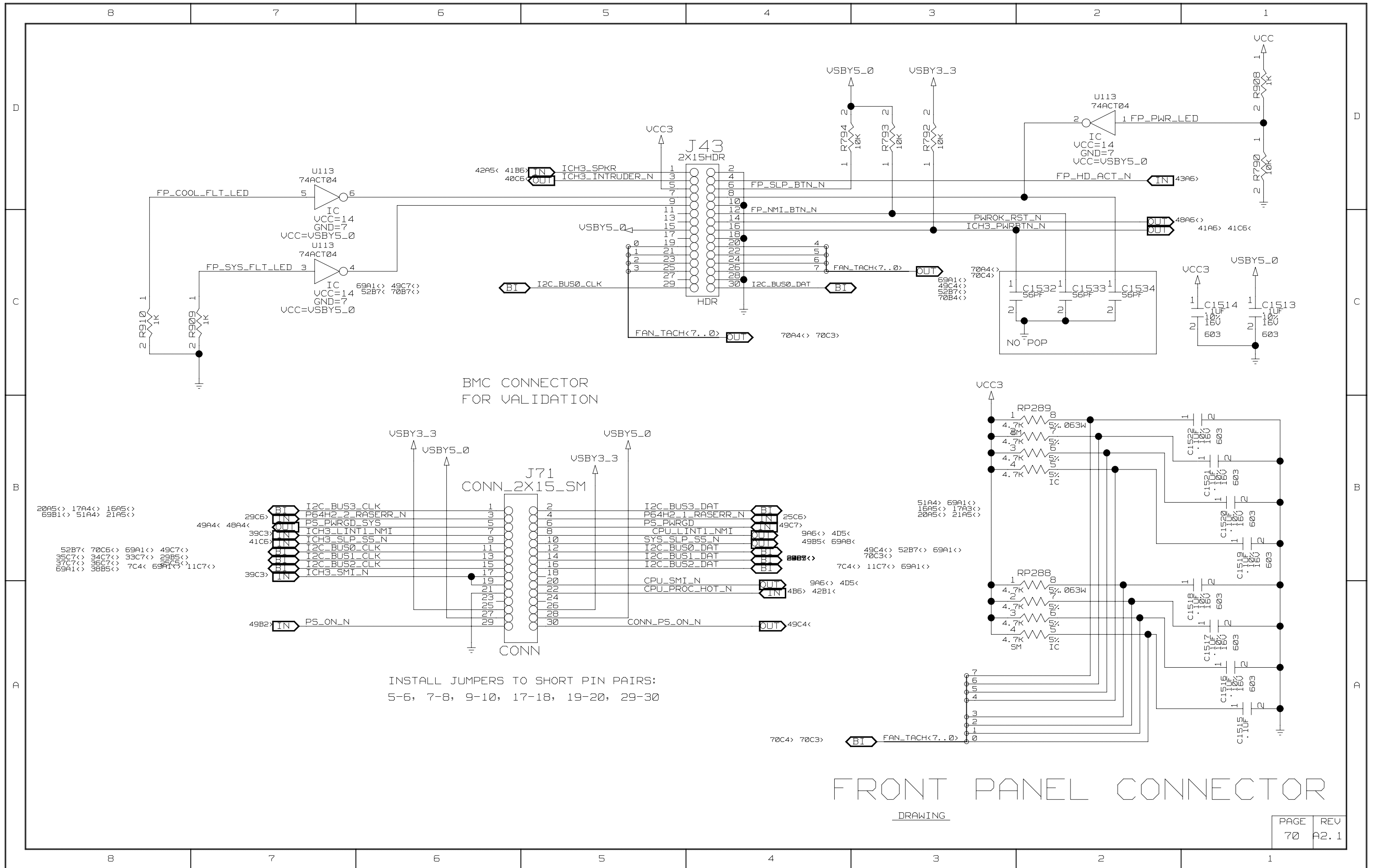
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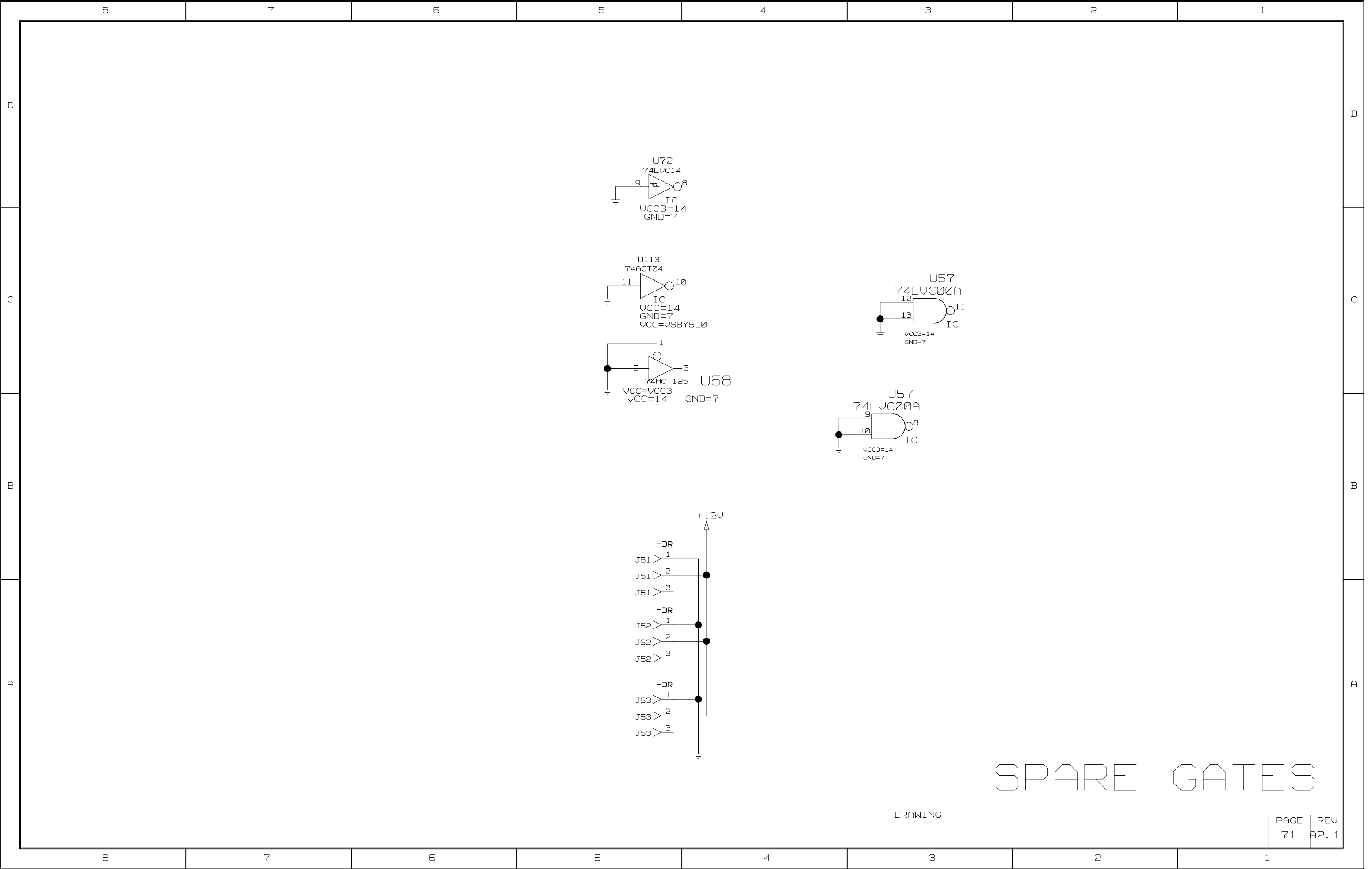


SEL1	SEL0	SMBUS PARTITION
0	0	BUS0
0	1	BUS1
1	0	BUS2
1	1	BUS3 < DEFAULT >

SMBUS MUX

DRAWING

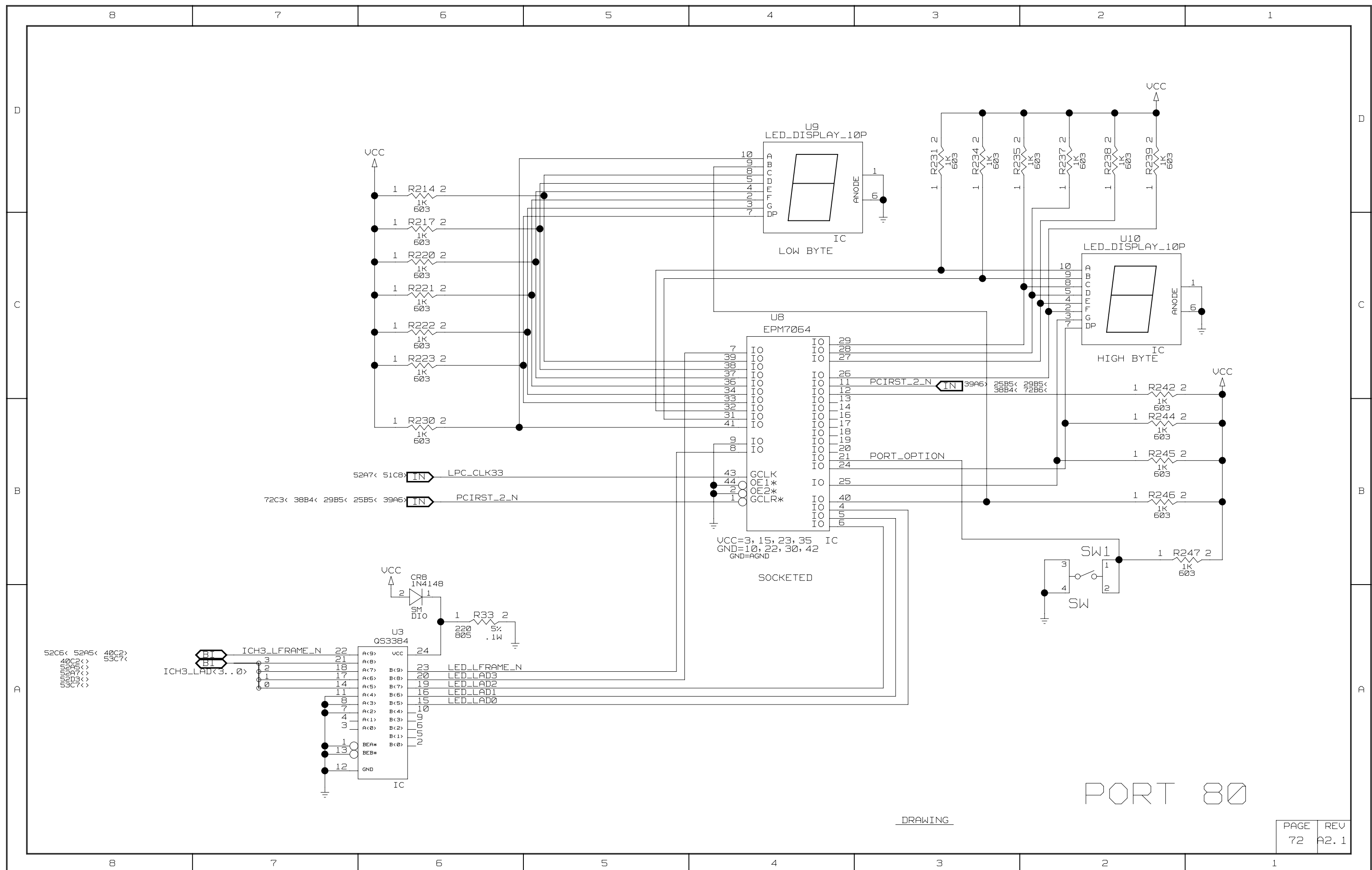




SPARE GATES

DRAWING

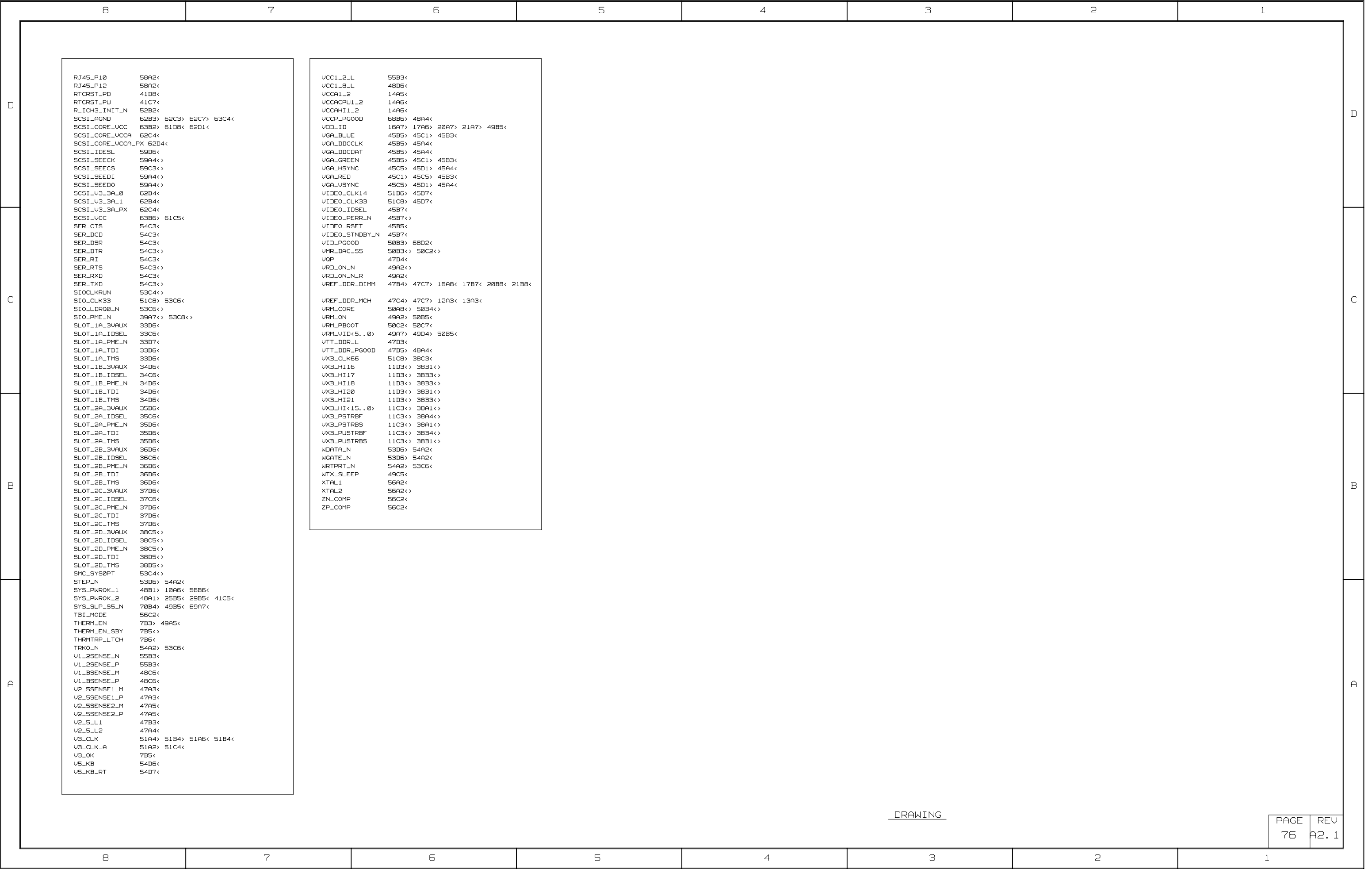
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PORT 80

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C								
B								
A								
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CR5 DIODE 47B6
CR6 DIODE 47A6
CR7 DIODE 47B2
CR8 DIODE 72B6
CR9 LED 48B3
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CR11 SCHOTTKY 50A2
CR12 SCHOTTKY 68C6
CR13 SCHOTTKY 68B4
CR14 SCHOTTKY 68B1
CR15 SCHOTTKY 50A4
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CR18 SCHOTTKY 50C2
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CR46 DIODPAK 64D7
CR47 DIODPAK 64D4
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J5 CONN184_DDR_ECC 17C7
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J16 2X20HDR20 43B5
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J38 4X175CSIRA 64C3
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J40 P52STACK 54D5
J43 2X15HDR 70D4
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L2 INDUCTOR 50C1
L3 INDUCTOR 50B2
L7 INDUCTOR 47B2
L8 INDUCTOR 47A4
L12 INDUCTOR 48D6
L18 INDUCTOR 47D2
L19 INDUCTOR 14A4
L20 INDUCTOR 14A3
L21 INDUCTOR 14A4
L22 INDUCTOR 55C3
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MH2 MTG_HOLE 67C7
MH3 MTG_HOLE 67D6
MH4 MTG_HOLE 67C6
MH5 MTG_HOLE 67D5
MH7 MTG_HOLE 67D4
MH8 MTG_HOLE 67C4
MH9 MTG_HOLE 67D3
MH10 MTG_HOLE 67C3
MH11 MTG_HOLE 67D2

POT1 POT_TC03 47C8
POT2 POT_TC03 47C8
O1 MOSFETN 47B3
O2 MOSFETN 47B3
O3 MOSFETN 47A5
O4 MOSFETN 47A5
O5 MOSFETN 47B3
O6 MOSFETN 47B3
O7 MOSFETN 47A4
O8 MOSFETN 47A4
O9 MOSFETN 48D6
O10 MOSFETN 48C6
O11 MOSFETN 50C3
O20 MGSF1N02LT1 52C5
O21 MOSFETN 50C3
O22 MOSFETN 50B3
O23 MOSFETN 50A3
O24 MOSFETN 50C2
O25 MOSFETN 50A2
O26 MOSFETN 50C2
O27 MOSFETN 50B2
O32 MBT3904DUAL 39D2
O33 MBT3904DUAL 52B2
O41 NPN 42A4
O43 MOSFETN 47D3
O44 MOSFETN 47D3
O48 NPN 49B3
O49 MOSFETN 55C3
O50 MOSFETN 55A3
O60 MBT3904DUAL 49A2
O65 MBT3904DUAL 7A6
O67 NPN 41A1
O68 PZT751 41A1
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R2 RESN 4C6
R3 RESN 4C2
R4 RESN 4C2
R5 RESN 4C2
R6 RESN 4C1
R7 RESN 4C1
R8 RESN 4C1
R9 RESN 4C1
R10 RESN 4B3
R11 RESN 4B3
R12 RESN 49A4
R13 RESN 50C8
R14 RESN 50C8
R15 RESN 50B8
R16 RESN 50C7
R17 RESN 50C7
R18 RESN 50B7
R19 RESN 50C7
R20 RESN 50B7
R21 RESN 50A7
R22 RESN 50A6
R23 RESN 50A6
R24 RESN 50C6
R25 RESN 50B6
R26 RESN 50D6
R27 RESN 50D5
R28 RESN 50D6
R29 RESN 4C5
R30 RESN 68B
R31 RESN 68A6
R32 RESN 50A5
R33 RESN 72A6
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R35 RESN 50D4
R36 RESN 68A3
R37 RESN 68B3
R38 RESN 9D5
R39 RESN 50C8
R40 RESN 50B5
R41 RESN 50B1
R42 RESN 55C1
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R44 RESN 4D5
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R49 RESN 49D3
R50 RESN 13A5
R51 RESN 13A5
R52 RESN 50D6

R53 RESN 50B6
R54 RESN 68D2
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R57 RESN 25A2
R58 RESN 6B3
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R60 RESN 50C2
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R68 RESN 51C2
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R78 RESN 9D4
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R81 RESN 49D3
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R83 RESN 9D5
R84 RESN 9D6
R85 RESN 42D3
R86 RESN 68B3
R87 RESN 42C2
R88 RESN 4C6
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R97 RESN 10D1
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R118 RESN 12A4
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R120 RESN 13D2
R121 RESN 68C7
R122 RESN 68C6
R123 RESN 40B1
R124 RESN 13B5
R125 RESN 7C6
R126 RESN 7C6
R127 RESN 7C6
R128 RESN 16A3
R129 RESN 16A3
R130 RESN 16A3
R131 RESN 16A3
R132 RESN 16A3
R133 RESN 16A3
R134 RESN 7D6
R135 RESN 4B5
R136 RESN 9A4
R137 RESN 4C4
R138 RESN 4C4
R139 RESN 4C4

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REVISIONS

A2 PRODUCTION RELEASE

A2.1 CORRECTED THERMTRIP PAGE 7 RECONNECTED Q65.2 TO GROUND

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