PD67XX — Configuring PCMCIA Sockets for ATA Drive Interface

Application Note

May 2001

As of May 2001, this document replaces the Basis Communications Corp. document *AN-PD5*.

Application Note

Contents

Figures

1.0 Introduction

The PD6710, PD6722, and PD6729 are single-chip PCMCIA interface controllers capable of controlling one or two PCMCIA or compact Flash sockets, respectively. They are designed for use in embedded applications and notebook systems where reduced form factor and low power consumption are critical design objectives.

Current typical application examples include:

- Routers
- Access network servers
- PBXs
- Vending machines
- Portable handheld systems
- Data acquisition systems
- Settop boxes
- Integrated access devices
- DSLAMs
- Terminal servers
- Point of Sale terminals
- Navigation systems
- Measurement equipment

With the PD6710, a complete single-socket PCMCIA solution with power-control circuitry can occupy less than 1.5 square inches (10 square centimeters) of board space. Similarly, with the PD6722 and PD6729, a complete dual-socket PCMCIA solution with power-control circuitry can occupy less than 2 square inches (13 square centimeters) of board space.

The PD67XX controllers are completely compatible with the standards of PCMCIA (Personal Card Memory International Association) Release 2.0 Standard as well as JEIDA (Japan Electronic Industry Development Association) Version 4.1 Standard (PD6729 is compliant with the PCI 2.1 Specification. The PD67XX controllers also offer special power-saving features such as Automatic Low-power Dynamic Mode and Suspend Mode. Both controllers are true mixed-voltage devices that can operate at +5 volts, +3.3 volts, or a combination of these at various interfaces. The controllers have full internal buffering and require no additional circuitry to interface to the ISA (or ISA-like) Bus for the PD6710 and PD6722, and the PCI Bus for PD6729, or to PCMCIA sockets.

Note: In this document, PD67XX represents the PD6710, PD6722, and PD6729.

2.0 Configuring PCMCIA Sockets for ATA Drive Interface

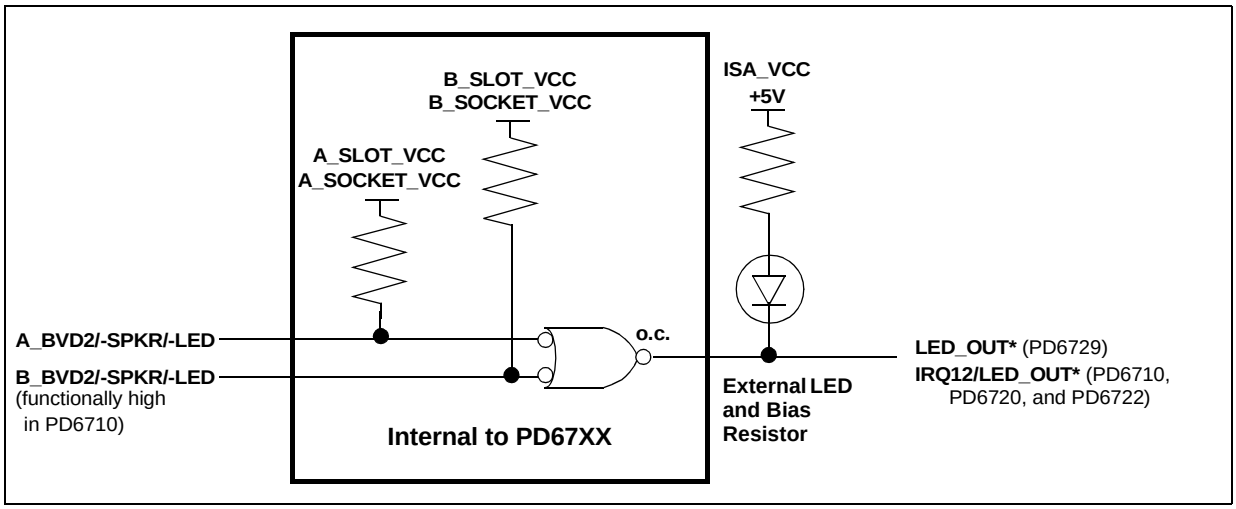
This application note applies to the PD6710, PD6720, PD6722, and PD6729. It describes how to configure the sockets for IDE-type ATA (AT attached) mode and how to set up one socket as the primary ATA interface. The primary ATA interface allows booting from an IDE-type ATA drive using the standard system BIOS routines.

2.1 System Requirements

There are system requirements when configuring for ATA mode:

- The system hard disk controller must be disabled.
- Interrupt request line 14 (IRQ14) from the PD67XX must be connected to system IRQ14.
- The -OE/-ATA pin must be low at power-on reset to initialize the socket for IDE-type ATA mode instead of PCMCIA Card Interface mode (need to set ATA mode, then turn on power to the card and reset).
- If disk-activity LED is required on the PD6710, PD6720, and PD6722, interrupt request line 12 (IRQ12/LED_OUT*) must be used to drive the LED (and the IRQ12 pin can not be used for other purposes). This figure below shows the logic associated with the optional disk-status LED.

Figure 1. Disk-Status LED Logic for ATA Mode



2.2 ATA Pin Cross-reference

The table below shows how the PCMCIA pins function in ATA mode.

PCMCIA Socket Pin Number	Function	
	PCMCIA Card Interface	ATA Interface
1	Ground	Ground
2	D3	D3
3	D4	D4
4	D5	D5
5	D6	D6
6	D7	D7
7	-CE1	-CS0
8	A10	n/c
9	-OE	-ATA (always low)
10	A11	n/c
11	A9	CS1*
12	A8	n/c
13	A13	n/c
14	A14	n/c
15	-WE	n/c
16	-IREQ	IREQ
17	VCC	VCC
18	VPP1	n/c
19	A16	n/c
20	A15	n/c
21	A12	n/c
22	A7	n/c
23	A6	n/c
24	A5	n/c
25	A4	n/c
26	A3	n/c
27	A2	A2
28	A1	A1
29	A0	A0
30	D0	D0
31	D1	D1
32	D2	D2
33	-IOIS16	-IOIS16
34	Ground	Ground

PCMCIA Socket Pin Number	Function	
	PCMCIA Card Interface	ATA Interface
35	Ground	Ground
36	-CD1	-CD1
37	D11	D11
38	D12	D12
39	D13	D13
40	D14	D14
41	D15	D15
42	-CE2	-CS1
43	VS1	VS1
44	-IORD	-IORD
45	-IOWR	-IOWR
46	A17	n/c
47	A18	n/c
48	A19	n/c
49	A20	n/c
50	A21	n/c
51	VCC	VCC
52	VPP2	n/c
53	A22	n/c
54	A23	VU
55	A24	-M/S
56	A25	CSEL
57	VS2	VS2
58	RESET	RESET*
59	-WAIT	IOCHRDY
60	-INPACK	DREQ [1]
61	-REG	-DACK [1]
62	-SPKR	-LED
63	-STSCHG	-PDIAG [1]
64	D8	D8
65	D9	D9
66	D10	D10
67	-CD2	-CD2
68	Ground	Ground

NOTE:
1. Not supported by the PD67XX.

2.3 Register Settings for ATA

The table below lists register values to be used to configure socket 0 for primary ATA, with ATA-compatible timing and operation. See the "Sample Code" later in this application note for the sequence of register programming.

Register Index	Value	Register Name	Description
05h	00h	Management Interrupt Configuration	No management interrupt is needed
06h	C0h	Mapping Enable	Enables I/O windows 0 and 1
07h	22h	I/O Window Control	Enables auto-size for data path for I/O windows 0 and 1
08h	F0h	System I/O Map 0 Start Address Low	Sets I/O window 0 to 1F0h–1F7h and I/O window 1 to 3F6h–3F7h (defines primary address space)
09h	01h	System I/O Map 0 Start Address High	
0Ah	F7h	System I/O Map 0 End Address Low	
0Bh	01h	System I/O Map 0 End Address High	
0Ch	F6h	System I/O Map 1 Start Address Low	
0Dh	03h	System I/O Map 1 Start Address High	
0Eh	F7h	System I/O Map 1 End Address Low	
0Fh	03h	System I/O Map 1 End Address High	
1Eh	32h[1]	Misc Control 2	Sets IRQ12 for driving LED and three-states bit 7 at I/O addresses 3F7h and 377h
26h	03h[2]	ATA Control	Sets ATA mode and sets PCMCIA -SPKR pin to be used to drive IRQ12 pin for LED
02h	B0h	Power Control	Turns on card power and enables outputs to the card
03h	6Eh	Interrupt and General Control	Sets card type to I/O, removes reset, and sets IRQ level to IRQ14

NOTES:
1. This is a typical value. For the PD6710, PD6720, and PD6722, bit 5 must be '1', bit 4 must be '1' for disk-status LED, bit 2 must be '0', and other bit settings depend on system configuration. For the PD6729, bit 2 must be '0' and other bit settings depend on system configuration.
2. This is a typical value. Bit 0 must be '1'; bit 1 must be '1' for disk-status LED; and bits 7:3 depend on the vendor-specific drive requirements.

2.4 Sample Code

This sample code is for the PD6710, PD6720, and PD6722. The code may need to be modified, depending on the system configuration.

```
#define    67xxbase     0x3e0
#define    67xxindex    67xxbase
#define    67xxdata     67xxindex + 1
#define    miscntrl2    0x1e

// This code need to be modified to fit your hardware and software system
environment

// Disable Memory and I/O windows and turn off power to the socket
outp (67xxindex, 0x02);
outp (67xxdata, 0x00);

// Disable IRQ lines
outp (67xxindex, 0x03);
outp (67xxdata, 0x00);

// Disable memory and I/O windows
outp (67xxindex, 0x06);
outp (67xxdata, 0x00);

// Reset card, configure for I/O, and set IRQ line to IRQ14
outp (67xxindex, 0x03);
outp (67xxdata, 0x6e);

// Set ATA mode and enable LED
outp (67xxindex, 0x26);
outp (67xxdata, 0x03);

// Set I/O window 0 for 1F0-1F7h
outp (67xxindex, 0x08);
outp (67xxdata, 0xf0);

outp (67xxindex, 0x09);
outp (67xxdata, 0x01);

outp (67xxindex, 0x0a);
outp (67xxdata, 0xf7);

outp (67xxindex, 0x0b);
outp (67xxdata, 0x01);

// Set I/O window 1 for 3F6-3F7h
outp (67xxindex, 0x0c);
outp (67xxdata, 0xf6);

outp (67xxindex, 0x0d);
outp (67xxdata, 0x03);

outp (67xxindex, 0x0e);
outp (67xxdata, 0xf7);

outp (67xxindex, 0x0f);
outp (67xxdata, 0x03);
```

```
// Set I/O width  for Auto-Data width
outp (67xxindex, 0x07);
outp (67xxdata, 0x22);

// Enable I/O window 0 and 1
outp (67xxindex, 0x06);
outp (67xxdata, 0xc0);

// Drive LED and enable three-state bit 7
outp (67xxindex, 0x1e);
outp (67xxdata, 0x32);

// Apply power and enable outputs
outp (67xxindex, 0x02);
outp (67xxdata, 0xb0);

// Add some delay.  The delay time depends on the drive specifications.
Delay_function (some_delay)

// Activate the reset pin
outp (67xxindex, 0x03);
outp (67xxdata, 0x2e);

// Add some delay.  The delay time depends on the drive specifications.
Delay_function (some_delay)

// Remove the reset signal
outp (67xxindex, 0x03);
outp (67xxdata, 0x6e);

// Add some delay.  The delay time depends on the drive specifications.
Delay_function (some_delay
```