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# Intel® 2xOC-3/16xT1/E1 ATM RAN Application Kit for UTRAN

**Speed development of wireless infrastructure devices based on the Intel® IXP23XX product line of network processors**

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## Product Highlights

- Demonstrates transport functions for ATM-based Radio Access Networks (RANs) up to full duplex OC-3/1 Gbps line rates
- Provides specific instructions for rapidly assembling Intel® software modules to build 3G wireless infrastructure components such as Radio Network Controllers (RNCs), Node Bs, and Node B/RNC aggregation units
- Includes software building blocks, documentation, training and support

## Product Overview

Intel network processors provide robust network processing performance to support value-added network services at line rate, and design flexibility to meet specific application requirements. Built on a fully programmable architecture, these network processors feature a highly modular, flexible programming environment that helps OEMs maximize development productivity.

## Enhanced Intel® Network Processor Development Environment

Using tested software building blocks called microblocks, developers can quickly assemble functional sequences, or pipelines, that perform specific network functions. These pipelines are portable and can be reused in multiple products, further accelerating development and time-to-market.
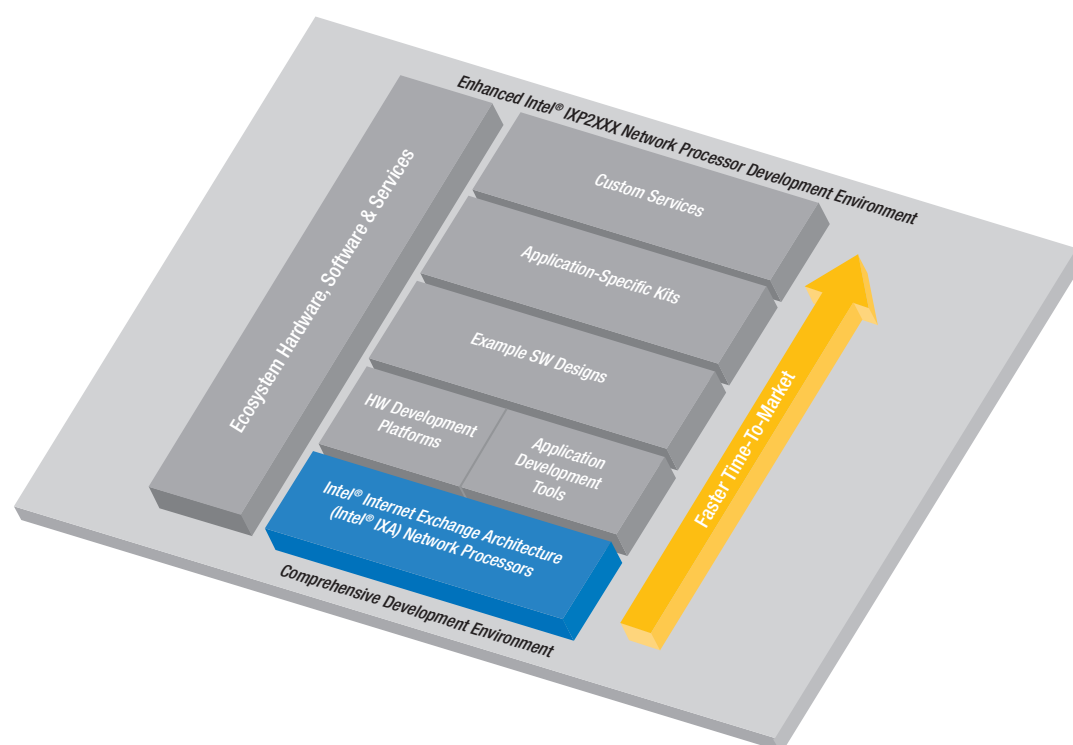
The Intel® ATM RAN Application Kit demonstrates the use of the Intel® IXP2325 and Intel® IXP2350 network processors for processing ATM transport-level functions in an ATM-based RAN. This ATM RAN Application Kit is intended for use in the RAN network and is directed at the UMTS Terrestrial Radio Access Network (UTRAN) and the CDMA2000 Access Network. These networks connect radio transceivers and a service provider's core network.

The application is written in C language using the Intel® C Compiler and supports two configurations:

• 2xOC-3 configuration typically used in a RNC application. The application uses external SRAM and CPP DRAM to store packets, packet information and various data structures.
• 16xT1/E1 configuration typically used in a Node B application. The application uses MSG SRAM and XSI DRAM to store packet, packet information and various data structures.

This application kit is designed for 3G wireless applications, but it can be used in other applications, and many of its core functions are applicable to any ATM-based deployment of the Intel® IXP23XX network processor product line.
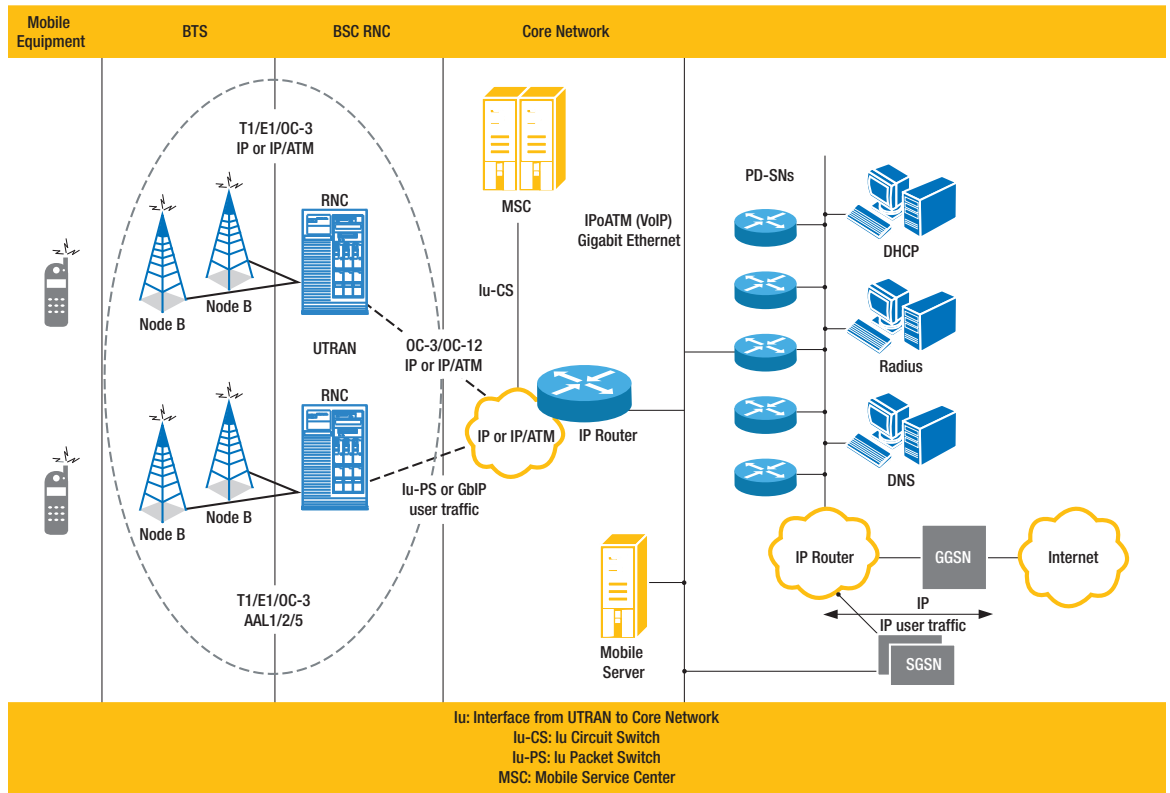


**Figure 1: Generalized 3G Wireless Network Architecture**

The UTRAN consists of a radio network and a core network. The radio network subsystem comprises RNCs and Node Bs, while the core network comprises both circuit switched (PSTN) and packet switched (Internet) services.

The logical UTRAN interfaces relevant to this application kit are:

- Iu—Representing the interconnection point between a RNC and core network
- Iur—Representing interconnection between RNCs
- Iub—Representing interconnection between RNCs and Node Bs

Voice and data received from the user equipment travels from Node B to RNC over T1/T3 links. Higher data rate links such as OC-3/STM1 can be supported using other, higher performance Intel network processors with minimal change in the software architecture. Both ATM- and IP-based transport are included in the 3GPP UTRAN specifications.

ATM Adaptation Layers (AAL2 and AAL5) are used to carry the voice, data and signaling packets in ATM-based transport. For IP-based voice transport, data and signaling messages are contained in IP packets.
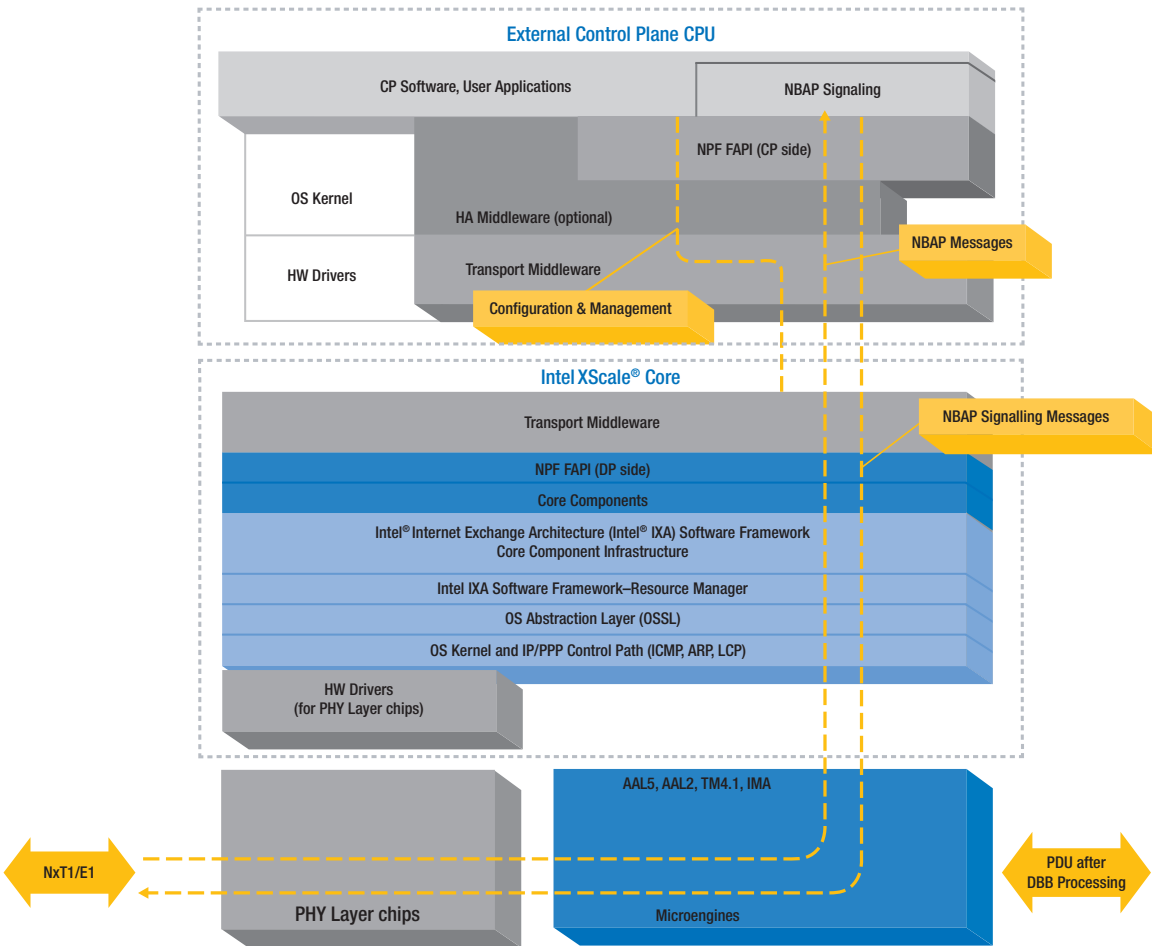
**External Control Plane CPU**

CP Software, User Applications

NBAP Signaling

NPF FAPI (CP side)

OS Kernel

HA Middleware (optional)

NBAP Messages

HW Drivers

Transport Middleware

Configuration & Management

**Intel XScale® Core**

Transport Middleware

NBAP Signalling Messages

NPF FAPI (DP side)

Core Components

Intel® Internet Exchange Architecture (Intel® IXA) Software Framework Core Component Infrastructure

Intel IXA Software Framework–Resource Manager

OS Abstraction Layer (OSSL)

OS Kernel and IP/PPP Control Path (ICMP, ARP, LCP)

HW Drivers (for PHY Layer chips)

AAL5, AAL2, TM4.1, IMA

NxT1/E1

PHY Layer chips

Microengines

PDU after DBB Processing

**Figure 2: Software Framework**

This software framework illustrates the scope of the ATM RAN Application Kit within the Intel® Internet Exchange Architecture Software Development Kit (Intel® IXA SDK).

## Data Plane Block Diagrams

The data plane diagrams in Figure 3 and Figure 4 illustrate how the Intel® ATM RAN Application Kit microblocks running on microengines can be assembled into pipelines for processing upstream and downstream traffic.
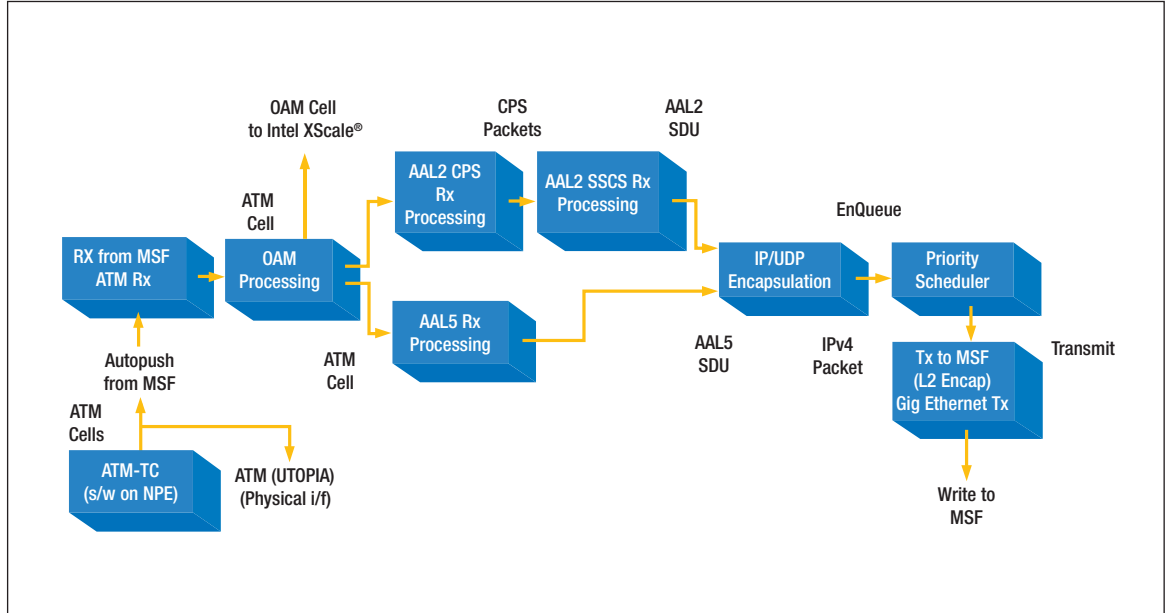


**Figure 3: Iu* to RNL Data Flow**
ATM cells are received via the media switch fabric from either the 16xT1/E1 lines or 2xOC-3 ports. The cells are reassembled into either AAL5 or AAL2 SDUs, encapsulated into UDP/IP datagrams and transmitted over a Gigabit Ethernet link.
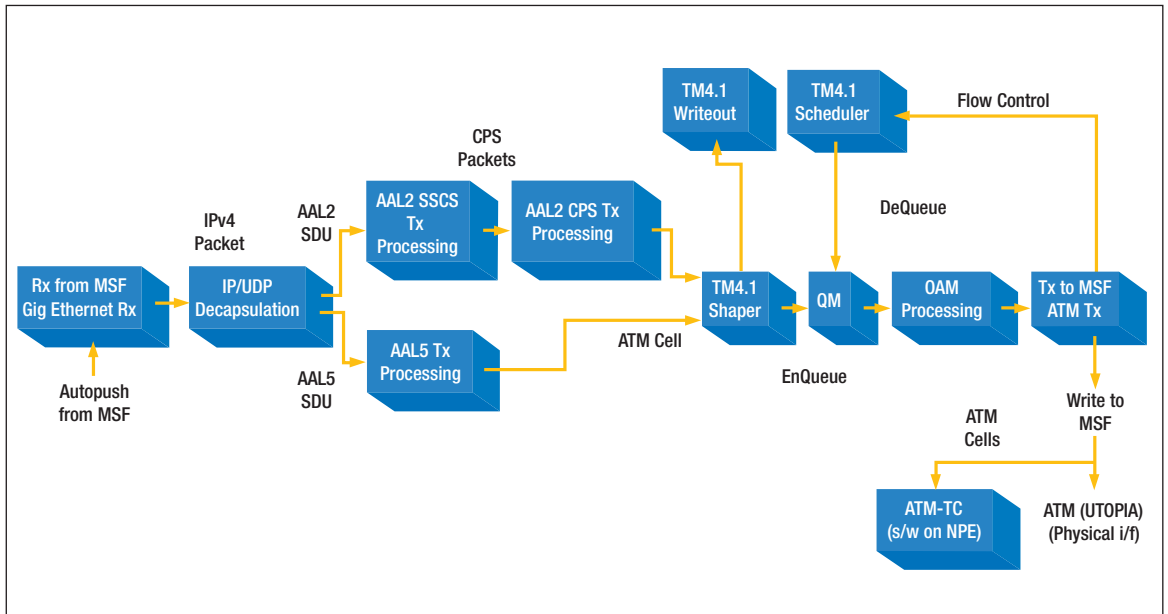


**Figure 4: RNL to Iu* Data Flow**
Ethernet frames are received from a Gigabit Ethernet fabric. The Ethernet frames contain AAL2 or AA-5 SDUs in UDP/IP datagrams.
The UDP/IP header is decapsulated and the underlying AAL2/AAL5 SDUs are transmitted as ATM cells into the media switch fabric.

*Either Iu-CS, Iu-PS, or Iub

## Supported Features

- ATM Features
    - AAL2 CPS
    - AAL2 SSSAR
    - AAL2 SSTED
    - AAL5 SAR
    - AAL5 SSCS
    - IMA
    - ATM-TC
    - OAM
- UDP/IP Framing
- Scheduling/Traffic Management
    - IEEE 802.1p Scheduler
    - TM 4.1 Traffic Management
- Physical Interface
    - 2xOC-3 ATM Unchannelized
    - 2xOC-3 ATM Channelized (i.e. with IMA)
    - 16 xT1/E1

## Performance and Specifications

Using an Intel® IXP2350 network processor with both the Intel XScale® core and microengines running at 900 MHz, the application kit supports processing of minimum size packets at full line rate for the 2xOC-3 configuration. In this application, the IXP2350 network processor retains about 30% processing headroom for additional application work. For the 16xT1/E1 configuration, the Intel® IXP2325 network processor (with the XScale core running at 600 MHz and the microengines at 300 MHz), supports line rate connectivity with more than 50% processing headroom.

## Software Framework

The Intel® 2xOC-3/16xT1/E1 ATM RAN Application Kit is based on the modular Intel® Internet Exchange Architecture (Intel® IXA) Software Framework, which enables flexible application partitioning across processing elements (microengines and threads), and facilitates the integration of customer-developed and third-party software modules, as well as software modules supplied by Intel.

The Intel IXA Software Framework includes a suite of code libraries to:

- Simplify interoperability, integration and reusability of Intel microblocks across multiple hardware configurations
- Facilitate development of modular components in the Intel XScale core
- Enhance portability among multiple operating environments

## Intel® Application Kits & Custom Solutions

Intel® IXP2XXX application kits are production-quality implementations of specific network devices. Pre-assembled, integrated and optimized on Intel network processors, these application kits simplify development and free up resources for developers to focus on value-added services and features for product differentiation. Intel can also extend or modify the application kits to meet developers' specific requirements, port to unique hardware or perform integration with existing software.

The Intel® IXP2325 and Intel® IXP2350 network processors are offered in various speeds and temperature options to support a range of wireless applications.

| Features | Specifications | |
|---|---|---|
| 2xOC-3 Pipeline | Number of AAL5 VCs | 16K |
| | Number of AAL2 VCs | 672 |
| | Concurrent AAL2 flows | 8K* |
| 16xT1/E1 Pipeline | Number of AAL5 VC | 16 |
| | Number of AAL2 VCs | 32 |
| | Concurrent AAL2 flows | 512** |
| Protocols | AAL2 CPS, SSSAR, SSTED | I.363.2, I.366.1 |
| | OAM | ITU-T I.610 |
| | AAL5 SSCS and SAR | ITU I363.5 |
| QOS | ATM CBR, rtVBR, nrtVBR and UBR | ATMF TM4.1 |
| Interfaces | Ethernet | IEEE 802.3 |
| | ATM | ITU-T I.361 |

*Architecturally the reference code can support up to 64K concurrent AAL2 flows. However, the use of 8Mb of SRAM limits the current reference design to 8K flows.

** The 16xT1/E1 application utilizes128Kb of MSG SRAM.

## Intel® Internet Exchange Architecture (Intel® IXA)

Intel® IXA is a packet processing architecture that provides a foundation for software portability across multiple generations of network processors. Intel IXA is based on programmable microengines, Intel XScale® technology and the Intel IXA Software Framework. Additional information on Intel IXA and the Intel network processor product line is available at the addresses listed below.

## Intel Access

| | |
|---|---|
| Intel® Network Processors Web page | http://www.intel.com/go/networkprocessors |
| Intel in Communications | http://intel.com/communications |
| Other Intel Support: | |
| Intel® Technical Document Center | http://intel.com/go/techdoc<br>(800) 548-4725   7 a.m. to 7 p.m. CST (U.S. and Canada)<br>International locations please contact your local sales office. |
| General Information Hotline | (800) 628-8686 or (916) 356-3104   5 a.m. to 5 p.m. PST |

For more information, visit the Intel web site at: **developer.intel.com**

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