



Intel® 82546EB Dual Port Gigabit Ethernet Controller

*Two Integrated Gigabit Connections
for High-Density Designs*

Product Brief

The Intelligent Way to Connect

- Dual port single-chip configuration simplifies designs
- Footprint compatibility for flexible designs
- Enhanced manageability and system health monitoring

Product Description

The Intel® 82546EB Dual Port Gigabit Ethernet Controller incorporates two full Gigabit Ethernet MAC and PHY layer functions on a single, compact component. Packaged in a very small 21x21mm PBGA, the 82546EB Dual Port Gigabit Ethernet Controller provides dual port functionality without requiring additional board space for the component.

The Intel 82546EB integrates Intel's fourth-generation Gigabit MAC design, with fully integrated, physical-layer circuitry, to provide two standard IEEE 802.3 Ethernet interfaces for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, 802.3ab). For fiber-optic applications, the Intel 82546EB's two integrated SERDES support 1000BASE-SX and 1000BASE-LX (802.3z). In addition, the controller provides a single, direct Peripheral Component Interconnect (PCI) 2.2 and PCI-X 1.0a compliant bus that operates as a single multi-function device on the bus at clock frequencies up to 133MHz.

The Intel 82546EB on-board SMBus port enables enhanced manageability and system health monitoring via the LAN. With SMBus, management packets can be routed to or from a management processor. The SMBus port enables industry standards such as IPMI (Intelligent Platform Management Interface) to be implemented with the 82546EB. In addition, ASF 1.0 (Alert Standard Format) circuitry provides alerting and remote-control capabilities with standardized interfaces.

The Intel 82546EB Gigabit Ethernet Controller architecture is optimized to deliver both high-performance networking and PCI/PCI-X bus efficiency. Using state logic design with a pipelined DMA Unit and 128-bit-wide buses for the fastest performance, the 82546EB controller handles Gigabit Ethernet traffic with low network latency and minimal internal processing overhead. The controller's architecture includes independent transmit and receive queues to limit PCI bus traffic, and a PCI interface that maximizes the use of bursts for efficient bus usage. The Intel 82546EB Gigabit Ethernet Controller prefetches up to 64 packet descriptors in a single burst for efficient PCI-bandwidth usage. Two 64KB on-chip packet buffers maintain superior performance as available PCI bandwidth changes. Advanced interrupt moderation hardware manages interrupts generated by the 82546EB controller to further improve system efficiency. In addition, using hardware acceleration, the controller also offloads tasks from the host processor, such as TCP/UDP/IP checksum calculations and TCP segmentation.

Applications

The Intel® 82546EB Gigabit Ethernet Controller is designed for use in the following applications:

- LAN on Motherboard (LOM) in dense, space-constrained systems such as rack-mounted servers and high-density blade servers
- Communications platform using dual Gigabit Ethernet on the backplane (PICMG 2.16 compliant or 1000BASE-X)
- Internet infrastructure devices with high-speed requirements and limited board real estate, such as switches, routers and load balancers

Features

PCI/PCI-X Features

- 133MHz PCI-X bus
- Multi-function PCI device
- PCI revision 2.2, 32/64-bit, 33/66MHz

MAC Specific Features

- Dual 64KB configurable RX and TX packet FIFOs
- Low-latency transmit and receive queues
- IEEE 802.3x compliant flow control support with software controllable pause times and threshold values
- Caches up to 64 packet descriptors in a single burst
- Programmable host memory receive buffers (256B to 16KB); Programmable cache line size from 16B to 256B

Gigabit PHY Specific Features

- Two integrated PHYs for 10/100/1000Mb/s full- and half-duplex operation
- IEEE 802.3ab Auto-Negotiation
- Proven PHY compatible with IEEE 802.3ab
- State-of-the-art DSP architecture implements digital adaptive equalization, echo, cross-talk and baseline wander cancellation
- PHY detects polarity, MDI-X, 2 pair vs. 4 pair cables, and cable length
- Dual Internal Serializer-Deserializers (SERDES)

Host Offloading Features

- Transmit TCP segmentation IP, TCP, and UDP checksum off-loading capabilities on RX and TX
- Advanced packet filtering
- IEEE 802.1Q VLAN support with VLAN tag insertion and stripping and packet filtering for up to 4096 VLAN tags
- Descriptor ring management hardware for TX and RX
- Jumbo frame support up to 16KB
- Interrupt moderation controls

Manageability Features (available on both ports)

- On-chip SMBus 2.0 port
- ASF 1.0 alerting
- Compliance with PCI Power Management v1.1/ACPI v2.0
- Wake on LAN (WoL) support
- Automatic link speed switching from 1000Mb/s down to 10 or 100Mb/s in standby

Additional Device Features

- Eight programmable LED outputs
- Internal PLL for clock generation using a 25MHz crystal or a 25MHz oscillator
- On-chip power regulator control circuitry

Benefits

- Supports bandwidth to allow wire-speed performance of two Gigabit Ethernet connections
- Lowest latency solution – a PCI/PCI-X bridge component is not required to implement a dual port design
- Application flexibility in LOM or embedded use
- 64-bit addressing for systems with more than 4GB of physical memory

- No external FIFO memory requirements
- FIFO size tunable to the application
- Network packets handled without waiting or buffer overflow
- Reduced frame loss due to receive FIFO overrun
- Efficient PCI-bandwidth usage
- Efficient usage of PCI bandwidth

- Reduced board space and lower power dissipation
- Automatic link configuration including speed, duplex, and flow control
- Robust operation over CAT-5 twisted-pair cabling at lengths over 100m
- Robust 1000Mb/s performance in noisy environments and despite severe cable installation problems
- Easier network installation and maintenance
- Solution for server blade backplane connections and Fiber Gigabit Ethernet

- Increased throughput and lower CPU utilization. Compatible with large send offload feature found in Windows® 2000 and Windows® XP
- 16 exact matched (unicast or multicast)
- Promiscuous (unicast/multicast) transfer mode
- Enables IT staff to easily create multiple virtual LAN segments
- Optimized fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage
- High throughput for large data transfers on networks supporting jumbo frames
- Reduces the number of interrupts generated by receive and transmit operations

- Enables IPMI, and ASF implementations
- Provides alerting and remote-control capabilities with standardized interfaces
- PCI power management capability requirements for PC and embedded applications
- Packet recognition and wakeup for network adapter and LOM applications
- Low power in standby states
- Supports power-down states without software assistance

- Indications for link speed, activity, duplex, collisions, pause by flow control, PCI speed, PCI width, and port ID on each port
- Allows design customization without affecting software drivers
- Lower component count and cost
- Simplified power supply design

Characteristics

Electrical

- PCI Signaling 3.3V and 5V
- Power Dissipation 3.5W (1.75W/port) (typical)

Environmental

- Operating temperature 0°C to 55°C (maximum); Does not require a heat sink or forced airflow.
- Storage temperature -65°C to 140°C

Physical

- Package 364-pin PBGA. 1mm ball pitch, 21 x 21mm (Saves critical space on LOM board designs).
- Footprint-compatible with Intel® 82544GC and Intel® 82545EM Gigabit Ethernet Controllers Enables a single-port or dual-port implementation on the same board.

For more information, contact your Intel® sales representative.

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