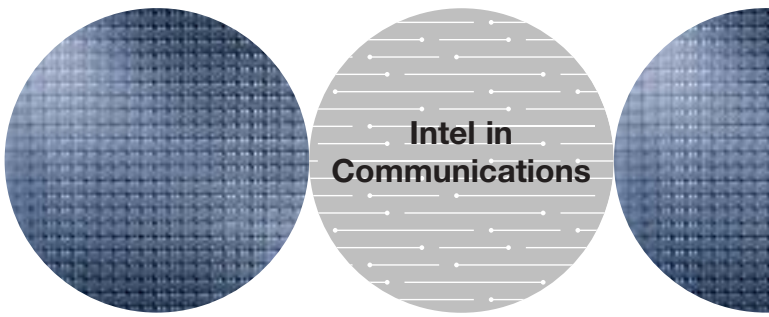
White Paper

Communication Streaming Architecture

Reducing the PCI Network Bottleneck

Intel® PRO Network Connections



Contents

Executive Summary

With the increasing computing capabilities of today's PCs and the Internet economy, demands on PCI bus capacity have outgrown PCI throughput. Network traffic at Gigabit speeds has become a substantial burden on the PCI bus, potentially degrading user experiences. By creating a new communications interface that directly connects the Memory Controller Hub (MCH) to the network controller, Intel has created Communication Streaming Architecture (CSA). With CSA-based motherboards, network data can be transferred at a much higher rate with lower latency. This new interface performs networking tasks more efficiently, achieves bi-directional Gigabit speeds and eliminates network traffic through the PCI bus. The Intel® 82547EI Gigabit Controller and Intel® 865 and 875 chipsets for the Intel® Pentium® 4 processor form the foundation for CSA-based LOM designs in next-generation motherboards.

Demand for More PC Bandwidth

The processing capacity of the PC continues to grow according to Moore's Law[1], giving users more resources at their fingertips. In business communications, users incorporate sophisticated elements into their documents, increasing the file size and thus the volume of each data transfer. High-resolution graphics and video are now ubiquitous and can be found in presentations, Web pages and e-mail. Large and media-rich documents, and data from the tools used to create them – IEEE 1394-based digital video cameras, scanners, 5.1 Sound – must traverse the PCI bus on its journey through the PC. While the PCI bus offers large capacity, our networked world adds to the burden on the PC's I/O bus.

The network has become the center of the company, keeping users connected and collaborating with one another over great distances and enabling IT departments to provide more productive management of networked clients. IT administrators leverage the network to keep systems healthy and running by deploying critical software updates and new applications "on the wire." The size of these updates is often relatively small, but the increasing frequency of releases creates more network traffic. To help speed this traffic, more and more desktops are migrating to faster network connections. Gigabit Ethernet is quickly becoming the standard in new PC deployments from OEMs.

[1] Moore's Law: The number of transistors able to be placed on a computer chip will double every two years. http://www.intel.com/pressroom/kits/bios/moore.htm

In our PC and network-centric world, we depend on the continuing advancement of the PC to provide us with more productive resources, and we rely on the network to leverage the effectiveness of PC technologies. The PCI bus is where all our data aggregates. Can it handle the load without degrading user experiences as more desktops migrate to faster and faster network connections? Or is it a potential bottleneck?

The PCI Bottleneck

Data arriving through a PCI network adapter must traverse several buses before it is presented to the user. These buses operate at different speeds. Figure 1 illustrates the typical PC's architecture and the bandwidth between each of the various components of the 32-bit Intel® Architecture.[2]

Most interconnect speeds exceed a Gigabit per second (Gbps). The 32-bit/33 MHz PCI bus's maximum speed is 1.06 Gbps, which cannot support full-duplex Gigabit speed through the network interface. Any other traffic that is generated on or directed to the PCI bus will also be limited by bus contention.

Figure 2 illustrates a typical network transaction, showing the path that data traverses when being sent from a local hard drive to the network, and from the network to a local hard drive.

In this transaction, the data traverses the HubLink* interface, from I/O Controller Hub (ICH) to Memory Controller Hub (MCH), four times and the PCI bus twice. This transmission is bottlenecked in two ways:

- The HubLink interface has a maximum throughput of 266 MB per second, roughly 2.2 Gbps.[3] This bandwidth will not be fully utilized because the 32-bit PCI bus, running at 33 MHz, limits the data transfer rate to 1.06 Gbps. Plus, the data must complete operations serially: from the PCI bus to memory, then from memory to the ATA interface. Serial transmission increases latency. While the HubLink interface has plenty of bandwidth, the serial nature of the traffic forces much of that bandwidth to go unutilized.
- A PCI-based network adapter will never achieve true full-duplex Gigabit speeds of 2 Gbps, because of the bandwidth limitation of the PCI bus. The best achievable rate is 1 Gbps unidirectionally.

Figure 1. Intel® 32-bit chipset architecture

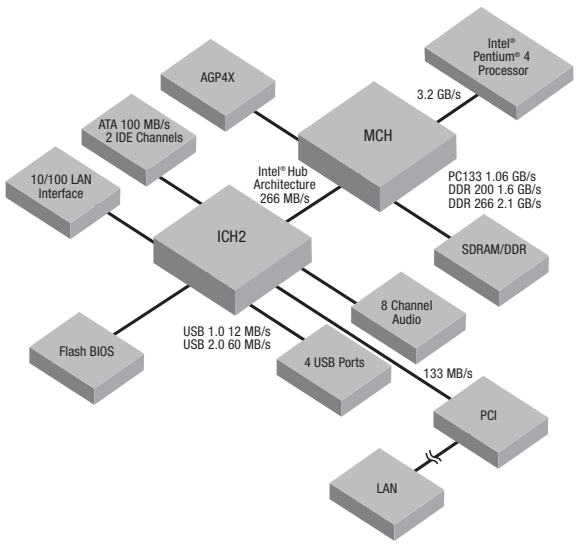
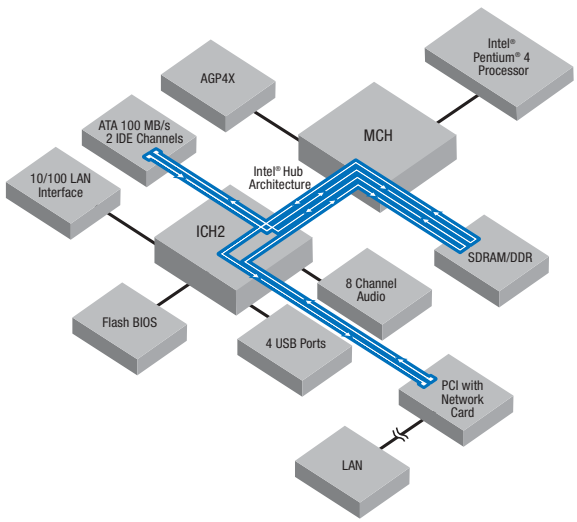


Figure 2. Network datapath



[2] From the Intel® 815, 845, and 850 Chipset data http://www.intel.com/design/chipsets/

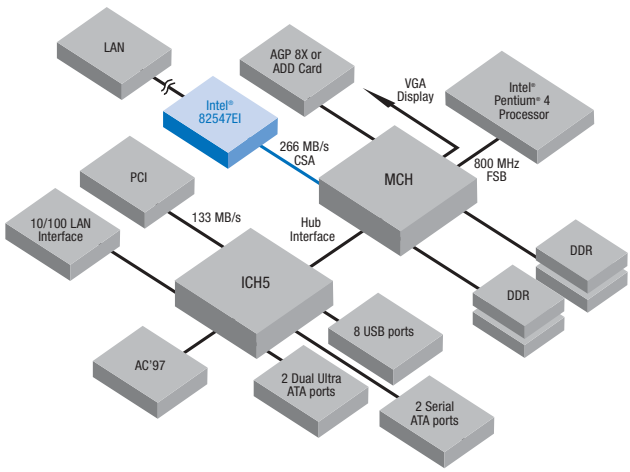
[3] Bytes to bits conversion. 1024*1024=1048576 bytes or 1 MB. 1 Mb=1 million bits. 1 Mb is not equal to 1 MB. 266 MB=266*1024*1024 or 2,231,369,728 bits.

Reducing the Bottleneck – Communication Streaming Architecture

Communication Streaming Architecture (CSA) from Intel is a new communications architecture that creates a dedicated link from the MCH to the network interface (Figure 3), offloading network traffic from the PCI bus. CSA, based on HubLink Architecture, provides a throughput of 266 MB per second, making it twice as fast as the PCI bus interface.

Direct attachment to the MCH affords a double benefit. Memory read and write operations have lower latencies, because data moves directly from the network interface to RAM. CSA also reduces the number of traverses across the HubLink interface to the ICH by half, further reducing the latency of the network transmission. Network-sourced traffic is sent from the network controller via CSA to the MCH and RAM, then to the ICH via the HubLink interface and local storage. This architecture eliminates the latencies inherent to PCI-based network traffic.

Figure 3. CSA-based architecture



Since the PCI bus is eliminated from the data's path and data moves directly from the network interface to RAM, the network controller no longer competes with other devices for PCI or ICH bandwidth. The PCI bus becomes available for the devices that today's users employ, such as scanners, digital cameras and IEEE 1394 cards. Additionally, other devices connected to the ICH, such as USB, Serial ATA hard drives, optical drives and AC'97, can utilize bandwidth formerly used by networking.

Intel offers the devices to easily implement CSA-based LOM designs. The Intel® 82547EI Gigabit Controller and the Intel® 865 and 875 chipsets for the Intel® Pentium® 4 processor form the foundation for next-generation LOM designs based on CSA. These devices enable full-duplex Gigabit networking while making the PCI bus more available.

Conclusion

Is the PCI bus able to handle additional network loads without degrading user experiences as more desktops migrate to faster and faster network connections? No. The PCI bus impedes the performance of network traffic at a time when users critically depend on the network and more desktops connect at Gigabit speeds. Communication Streaming Architecture, based on the Intel® 82547EI Gigabit Controller and Intel® 865 and 875 chipsets, enables full-duplex Gigabit networking by using a direct connection between the MCH and the network interface. CSA eliminates the PCI bottleneck and frees the HubLink interface to the ICH from network-sourced transactions. CSA-based network connections deliver true wirespeed Gigabit connectivity.

CSA offers the following benefits:

- Provides more efficient use of data paths
- Frees the PCI bus for other devices
- Delivers true full-duplex Gigabit speeds for the LAN connection without draining the resources of the system

CSA, the next evolution of bus technology, allows a desktop system to run more efficiently. CSA implementations allow users to take advantage of the increasing power of the PC without degrading their network experience.

0503/OC/PL/PDF

252451-002