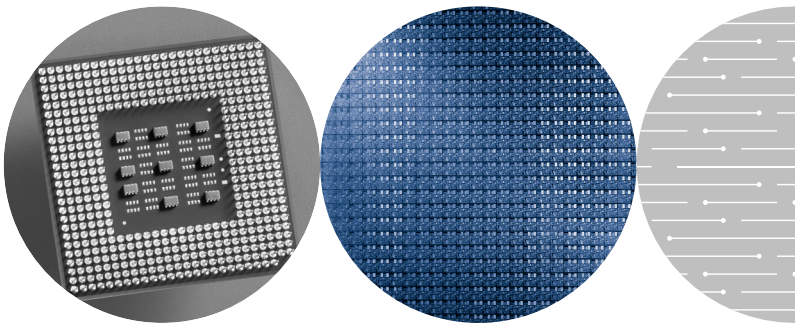
White Paper

Accelerating the Convergence of Computing & Communications

Intel® 90nm Communications Technology

Intel in Communications



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Abstract

For more than 30 years, "Moore's Law" has accurately predicted that the number of transistors on a chip would double approximately every two years. The resulting exponential increases in performance led to worldwide computerization of nearly every business and life function, and in effect defined our whole economy as we know it today. Through relentless advancements and extensive investment in process technology, Intel has the capability to ensure that Moore's Law will hold true at least through this decade.

The next increment on this growth curve – Intel's industry-leading 90 nanometer (nm) manufacturing technology – will be no less revolutionary, especially when Intel optimizes key features for communications later this year. Through this process of integrating certain analog functions on Intel's 90nm digital CMOS process, the communications industry will finally be able to ride the accelerated performance curve predicted by Moore's Law.

It's all good news for communications manufacturers. Integrated computing and communications functions (mixed-signal technology and heterojunction bipolar transistors) on a small, 90nm-based form factor will accelerate industry convergence and result in higher performance, true system-on-a-chip solutions. In addition, Intel's manufacturing capabilities will enable volume production of highly integrated communications building blocks, thereby reducing manufacturers' need for costly, proprietary ASIC development. And tight coupling between Intel's design and manufacturing resources can help reduce time-to-market for both Intel and its customers.

Intel's 90nm logic technology has been demonstrated successfully with the highest capacity SRAM in the industry (52 Mbits). Intel plans to apply this leading-edge technology to wireless, Ethernet, optical and network processing solutions, with the first silicon available in the second half of 2003. This white paper examines the acceleration of convergence in computing and communications made possible by the Intel® 90nm process – as well as the new, specialized features optimized by Intel specifically for integrated, high-performance communications functions on chip.

Communications Features

For this paper, "communications functions" or "communications features" include mixed-signal technology – both analog and digital – and Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs). See sidebar on page 6.

The Path to Convergence

As advancements in technology drive the convergence of computing and communications, Intel is developing new technologies that can accelerate this process. Accordingly, Intel has predicted that the time is not far off in which all computers will communicate and all communication devices will compute.

To deliver such devices, manufacturers of computers and handhelds will require standards-based silicon that enables the seamless migration of communications capabilities into the computing platform. In addition, communications manufacturers will require new levels of computing and system integration in their products.

Although existing silicon technology enables integration of many of these functions through multi-chip or multi-die designs, the manufacturing processes for computing and communications silicon have traditionally been optimized separately, resulting in longer and more costly development cycles for integrated solutions.

For example, computing industry silicon manufacturing has been driven by the need for the highest performance logic and the smallest CMOS memory cell size (for SRAM cache) while controlling drive and leakage currents. Meanwhile, communications industry silicon manufacturing processes must enable high-speed analog I/O at radio frequencies. In addition, communications-optimized silicon puts a higher priority on voltage threshold and linear transconductance direct current (DC) parameters. In other words, distinct differences in functional requirements have resulted in unique design strategies and manufacturing processes for these industries. To facilitate true convergence without driving up costs, these two disparate silicon processes must be optimized together.

Convergence at 90nm

Intel has brought these two processes together at 90nm – the first in the industry to do so. With experience in building both computing and communications devices, Intel design engineers were able to take advantage of shrinking lithography to erase the performance differences designed into these unique processes. At the same time, Intel's 90nm process technology uses the corresponding increase in transistors provided by the shrinking lithography to substantially increase the number of possible functions – including both analog and digital – that can be performed on chip.

One Vision – Many Benefits

Intel's integration of computing and communications functions at 90nm – using a digital CMOS-based manufacturing process – results in no degradation in CMOS performance. This will enable optimization of both computing and communications features on the same accelerated growth curve predicted by Moore's Law, thereby providing the communications industry with all of the accompanying benefits, including exponential performance increases, reduced power consumption, and lower development costs.

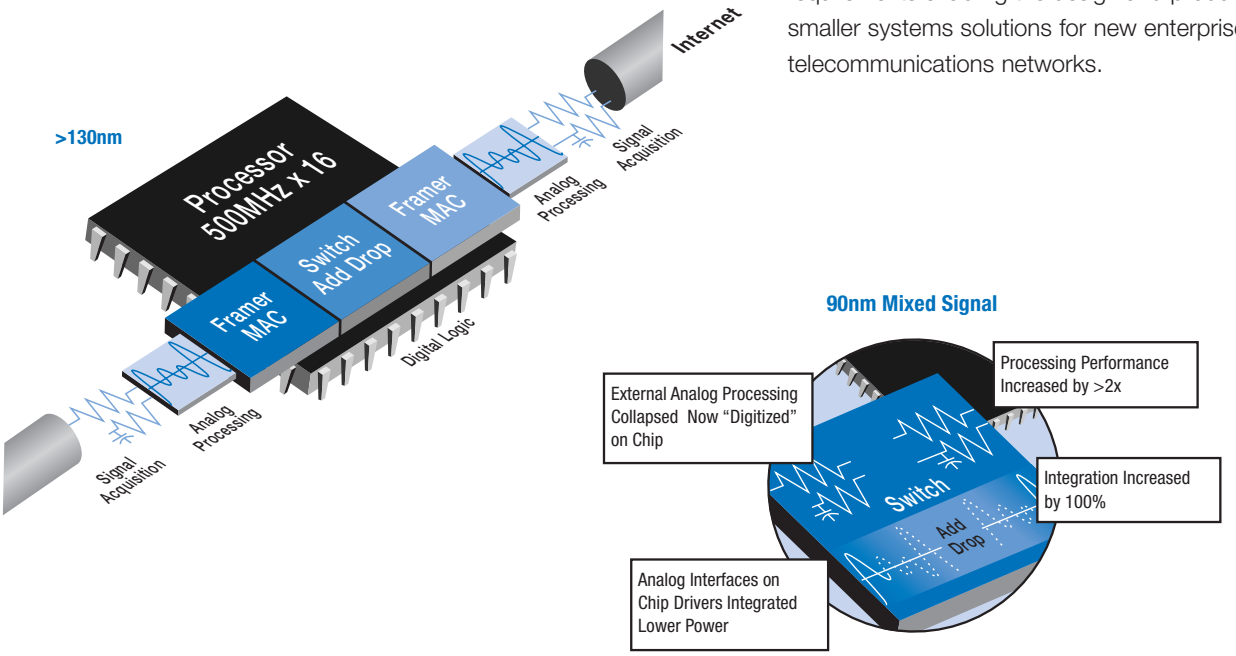
For truly converged solutions, silicon processes must be optimized to meet four essential development metrics. The Intel 90nm communications process meets all four criteria and is currently unmatched in the industry:

Acceleration

As predicted by Moore's Law, the Intel 90nm process more than doubles processing speeds, resulting in an exponential increase in performance. This increase in processing power provides the performance needed to build highly integrated communications systems on a single chip. As a result, the development of truly converged solutions will become more time and cost efficient, enabling OEMs to utilize modular, fully integrated building blocks for accelerated delivery of more robust solutions.

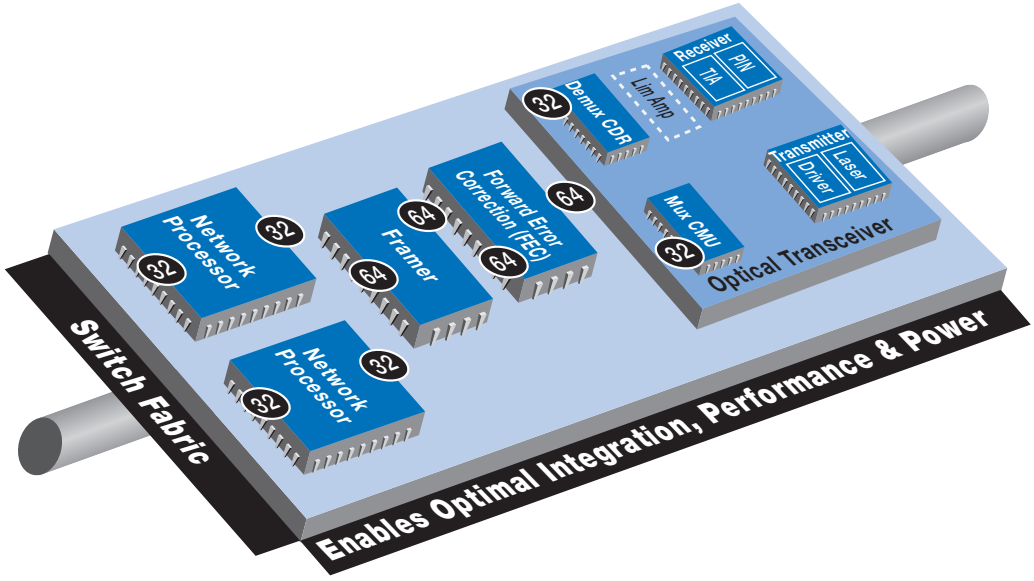
Integration

Through analog and digital integration and technical manufacturing advancements, Intel's communications design can be produced on a chip that is 2.5 times smaller than existing 130nm processes (see figure 1). This leads to more power-efficient product designs enabling longer battery life, simpler cooling processes and lower operating expenses. In addition, the combination of computing and communications on a single die at 90nm can help reduce system-level power consumption by reducing the number of chips required for an integrated solution. At the same time, the smaller form factor reduces space requirements enabling the design and production of increasingly smaller systems solutions for new enterprise and telecommunications networks.



Mixed Signal Integration

figure 1



Intelligent Fiber-Optic Line Card ≥ *130nm*

figure 2

Using Intel 90nm process technology, all of these functions can be integrated on a chip, eliminating the need for components and their corresponding pin counts, thereby reducing the size requirements for the printed circuit board.

Digitization

The Intel 90nm process technology allows some ingress analog signals to be converted to digital signals, processed in the digital domain, and converted back into analog on egress. This allows communications development to begin tracking the Moore's Law curve for exponential performance improvements every two years. By providing the necessary analog building block libraries in 90nm technology, analog signals can be converted on the same silicon die as digital signals. Enabling scalability of mixed-signal designs in tandem with logic functions provides customers with an integration path that could help lower development costs and optimize the design process, resulting in new products being developed more quickly for faster time-to-market. At the same time, lower power usage is likely to result from smaller transistor sizes.

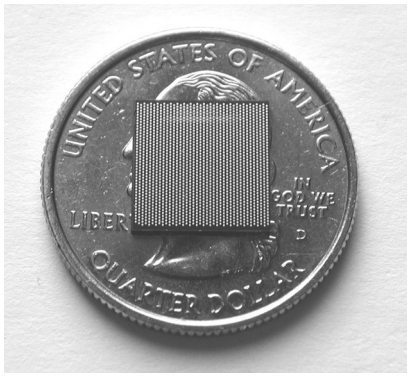
Serialization

Intel's 90nm technology makes it possible to incorporate an entire design on a single chip. In the board example shown in figure 2, an entire optical transceiver - with signals passing from the fiber to the error/correction device to the framer to the network processor to the switch fabric - can be implemented on a single chip. Smaller transistor sizes at 90nm allow more circuitry in a smaller area, allowing the discreet component implementation shown in figure 2 on a single piece of silicon. With seven metal layers of interconnect at 90nm, all of the component interfaces could be connected on chip, reducing the external pin count significantly. This in turn would reduce the size requirements for the printed circuit board.

Industry–Leading Technology Intel's 90nm Logic Process

Intel's breakthrough 90nm communications technology builds on its industry-leading 90nm logic process. In early 2002, Intel demonstrated fully functional chips with a record-setting SRAM (cache) of 52 Mbits. Packing six transistors in an area of 1 square micron, and 330 million transistors on a chip, Intel's new technology illustrates the tremendous density and performance enhancements that will be available through its 90nm manufacturing process.

1.0 µm2 SRAM Cell



52 Mbit SRAM on a 90nm process

The technology behind these achievements features 50nm transistor gate lengths, a gate oxide only 1.2 nm thick (less than five atomic layers) and a performance-enhancing technique called strained silicon (see sidebar below). Through the corresponding increase in speed and density, these technologies will enable more functions to be performed on chip. For example, Intel's unique strained silicon technology increases electron and hole mobility resulting in a 10-20 percent increase in transistor drive current, for higher performance and lower power consumption than processors based on the existing 130nm logic technology.

The Intel 90nm process also features faster, denser interconnects with seven copper layers (metallization) – one more layer than the 130nm generation of chips – providing cost-effective improvement in logic density routing. A new low-K dielectric reduces wire-wire capacitance, speeding up intra-chip communication and potentially reducing power consumption.

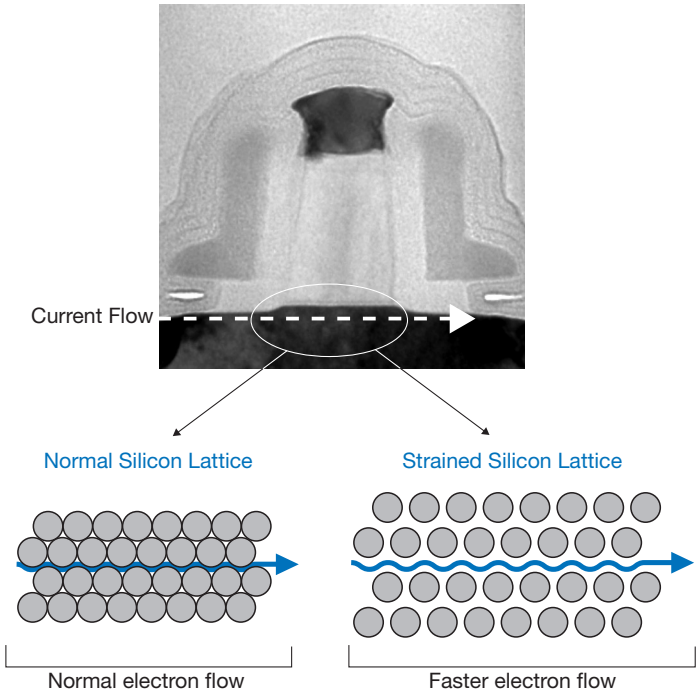
These technical achievements will be combined with Intel's industry leading manufacturing capabilities, enabling early and cost-effective volume production of Intel 90nm logic chips in the second half of 2003.

Strained Silicon

In strained silicon, germanium atoms are inserted into a chip's silicon lattice, effectively "stretching" the distance between the silicon atoms in transistors. Moving these atoms slightly farther apart eases the movement of electrons through the transistors, leading to better performance and lower energy consumption for the chip. In addition, Intel's unique strained silicon process results in no detriments to short channel behavior or junction leakage. (*figure 3)*

Strained Silicon comparison to Normal Silicon Lattice

figure 3



Cost-Efficient Manufacturing & Solutions

Because all of the Intel 90nm manufacturing will be done on 300mm wafers – a process already employed at many of Intel's Fabs – Intel can quickly and cost-effectively begin high-volume production. Using the increased number of transistors to significantly increase the number of possible functions performed on chip – including both analog and digital functions – Intel design engineers and customers can more quickly and cost-effectively develop highly integrated system-level solutions. By virtue of their efficiency, these solutions can then help customers reduce capital and operating expenditures by reducing the need for costly, proprietary ASIC development.

Time-to-Market

Intel's manufacturing expertise has been demonstrated through its successful implementation of the Intel 130nm process technology. Using many of the same tools as the 130nm manufacturing process will help Intel engineers and Fabs ramp quickly to volume manufacturing of the new 90nm process chips. In addition, tight integration between design and manufacturing will help shorten the time it takes Intel to get to market with volume production of new 90nm process-based chips, thereby helping customers get to market more quickly with their highly integrated solutions. In fact, Intel expects to deliver 90nm process-based chips well ahead of other leading manufacturers.

Performance

With extensive investment in manufacturing R&D, Intel has become an industry leader in process technology. Utilizing performance-enhancing materials – such as strained silicon, low-K dielectric and copper interconnects between layers – Intel's 90nm communications process will offer industry-leading performance for converged solutions.

Communications Enhancements to 90nm Process

Intel will add bipolar transistors and other communications-optimized technology to its industry-leading 90nm logic process later this year. One of the more significant achievements of Intel's 90nm communications technology is the addition of analog functions with no degradation in CMOS performance. To accomplish this, Intel optimized some of the 90nm logic process features specifically for communications and added specialized analog device elements to enable digitization of key analog functions.

Communications enhancements to Intel's 90nm process include:

- Silicon Germanium (SiGe) (see sidebar on the right) heterojunction bipolar transistors (HBTs) provide higher frequency, higher voltage swing and lower noise than CMOS transistors, enabling uninterrupted current flow necessary for analog functions on chip.
- Thicker gate oxide for the high voltage radio frequency (RF) analog CMOS transistors improves the signal-to-noise ratio (dynamic range) in communications functions. At the same time, thick-oxide variant reduces power consumption through less leakage.
- Extra masking steps for precision capacitors and resistors used in analog circuits provide precise control and matching for conditioning and converting analog signals.
- High-Q inductors and varactors allow for building the precise filters needed when conditioning analog signals before and after digital processing.

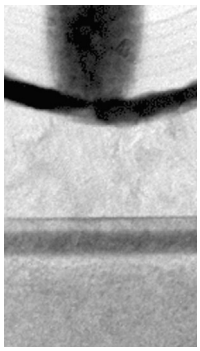
Silicon Germanium (SiGe)

For the 90nm communications process, Intel will add a layer of silicon germanium into the transistor bed to create high-frequency circuits optimized for communications functions. SiGe will also be used to build the strained silicon channels giving CMOS transistors higher drive current, which translates into higher clock frequencies.

In several ways, the Intel 90nm logic process also contributes to exceptional performance metrics for communications functions. For example, the combination of copper and low-K dielectric now meets or exceeds performance and manufacturing goals.

Same Toolset

Intel will use most of the same toolset developed for the 130nm process in both the logic and communications versions of its 90nm chips ensuring faster time-to-market and early high-volume production. Tight coupling between design and process manufacturing also reduces the need for retooling, saving time and resources as Intel moves to production at 90nm. Using the same toolset also increases the opportunity for design reuse, allowing designers to reuse libraries and components from the 130nm process at 90nm, further shortening customers' time-to-market.



SiGe HBT Transistors

What's Next? 90nm Communications Solutions

As seen in the earlier diagrams, there is enormous development potential made possible by the integrated Intel 90nm communications process. Network processing, wireless devices, Ethernet and optical components all stand to benefit from this highly efficient technology. Having demonstrated one square micron SRAM cell sizes, 52 Mbit capacity and the highest drive current in the industry, the Intel 90nm mixed signal process will offer developers a lot of performance in a very small package.

Wireless and Optical Components

Strong demand for integrated computing and communications in mobile devices will make wireless and optical components early candidates to take advantage of this process. With mobile communications devices requiring high-performance density and low power consumption, the 90nm communications technology will be a key contributor to new, more efficient designs. Intel's addition of SiGe HBTs to the 90nm process will enable analog functions performed on chip to benefit from higher frequency, higher voltage swing and lower noise, which in turn will allow the integration of signal conditioning, antenna driver and input-amplifier functions in wireless components.

It then becomes feasible and efficient to integrate wireless functions on chip. Although today's high-performance Intel® Pentium® 4 processor at 3 GHz offers tremendous capacity, wireless communications functions performed on chip would utilize as much as 10 percent of the processor's performance capacity. However, on a chip with 300-500 million transistors – quite possible with 90nm manufacturing – integrating wireless functions on chip will not only be feasible, but desirable from a manufacturing and design efficiency standpoint.

Network Processors

Network processors too can become more powerful and efficient at 90nm. With such high transistor density provided through 90nm process technology, network processors could provide integrated aggregation, control and packetization. Performance-intensive applications, such as advanced security functions requiring deep packet inspection at line rate speed (like Denial of Service prevention), can potentially be performed on chip. A 90nm network processor might include an intelligent server network interface, immunizing the server from common resource attacks, while the network processor software detects and identifies new attacks and isolates the attack signature. Network processors could also benefit from the integration of computing and communications, enabling manufacturers to lower development costs and carriers to reduce operating expenses.

Conclusion

Clearly there are numerous exciting potential applications made possible by an integrated 90nm silicon platform. Intel customers can begin now to take advantage of this breakthrough technology through early design discussions for new communications solutions. It's happening now: computing and communications are converging. And Intel's industry-leading 90nm communications process will be the catalyst to accelerate this process in 2003.

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