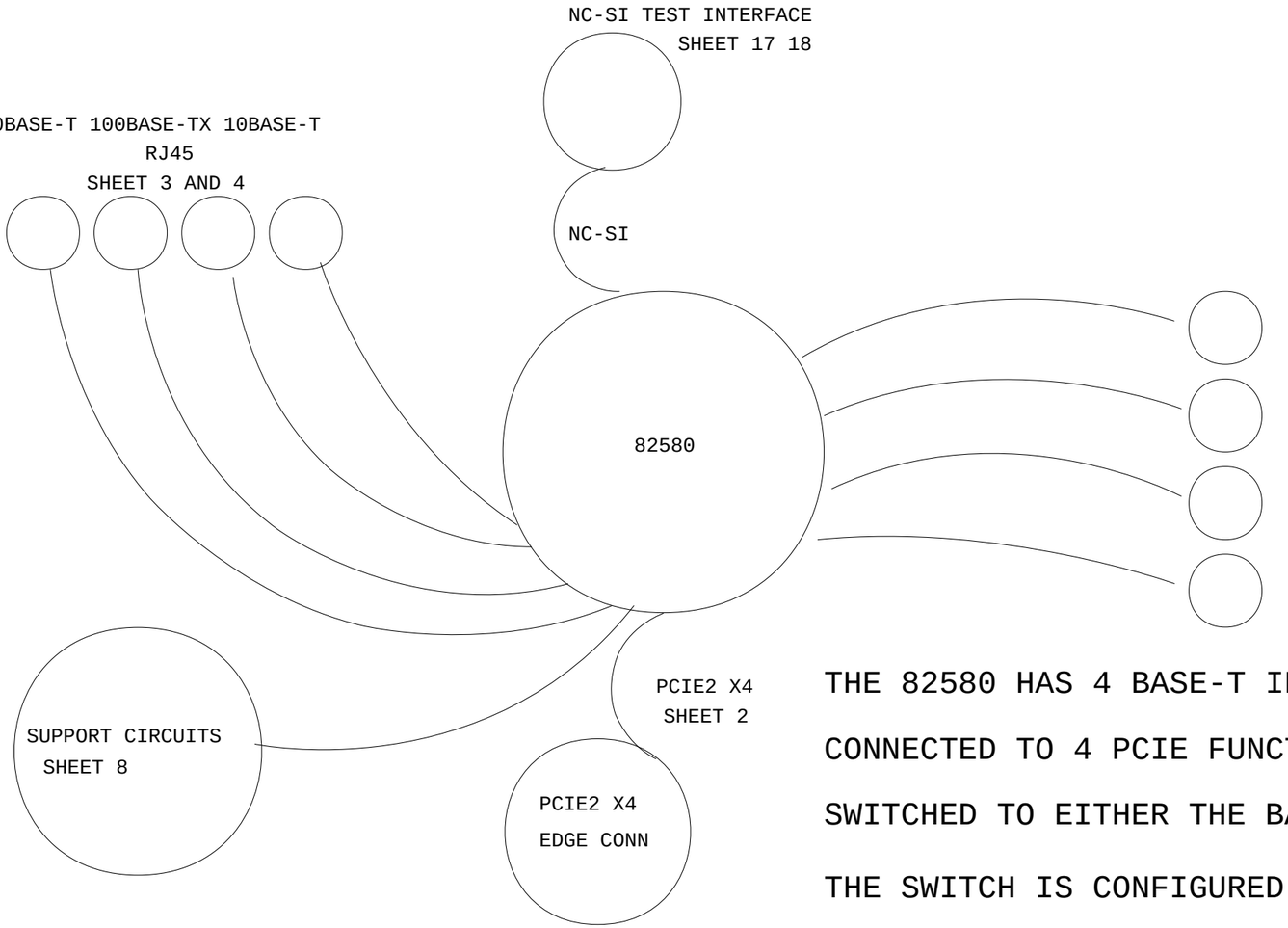
82580 REFERENCE DESIGN

HISTORY:
2.0 FIRST RELEASE
2.1 CORRECT OFF PAGE REFERENCES
ADD CURRENTS TO POWER FILTER PAGE



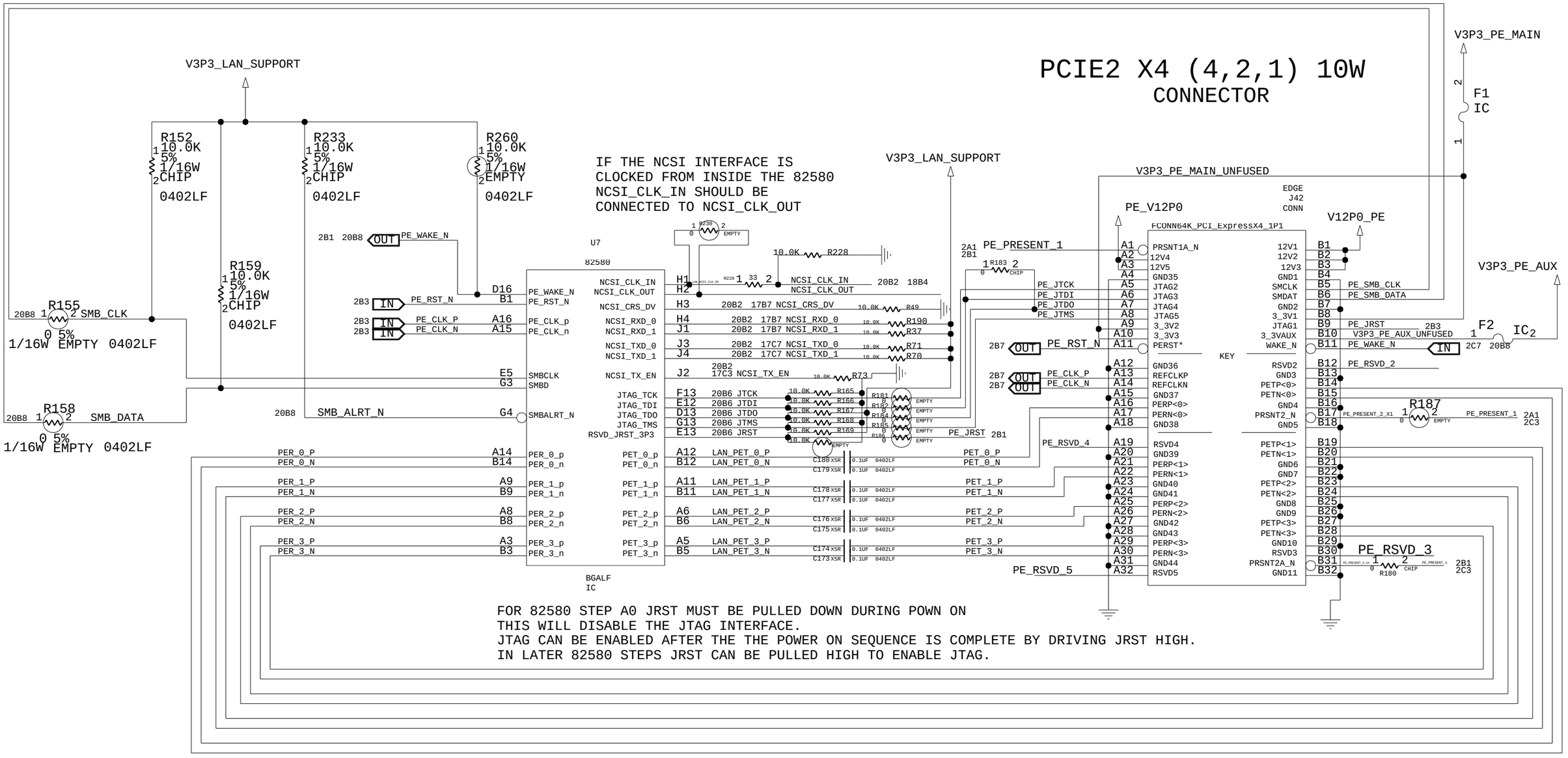
THE 82580 HAS 4 BASE-T INTERFACES AND 4 SERDES INTERFACES CONNECTED TO 4 PCIE FUNCTIONS. EACH PCIE FUNCTION CAN BE SWITCHED TO EITHER THE BASE-T INTERFACE OR THE SERDES INTERFACE.

THE SWITCH IS CONFIGURED WITH A STATIC EEPROM SETTING OR DYNAMICALLY THROUGH A REGISTER SETTING.

UNKNOWN

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 1

PCIE NC-SI SMB JTAG



INTEL CONFIDENTIAL

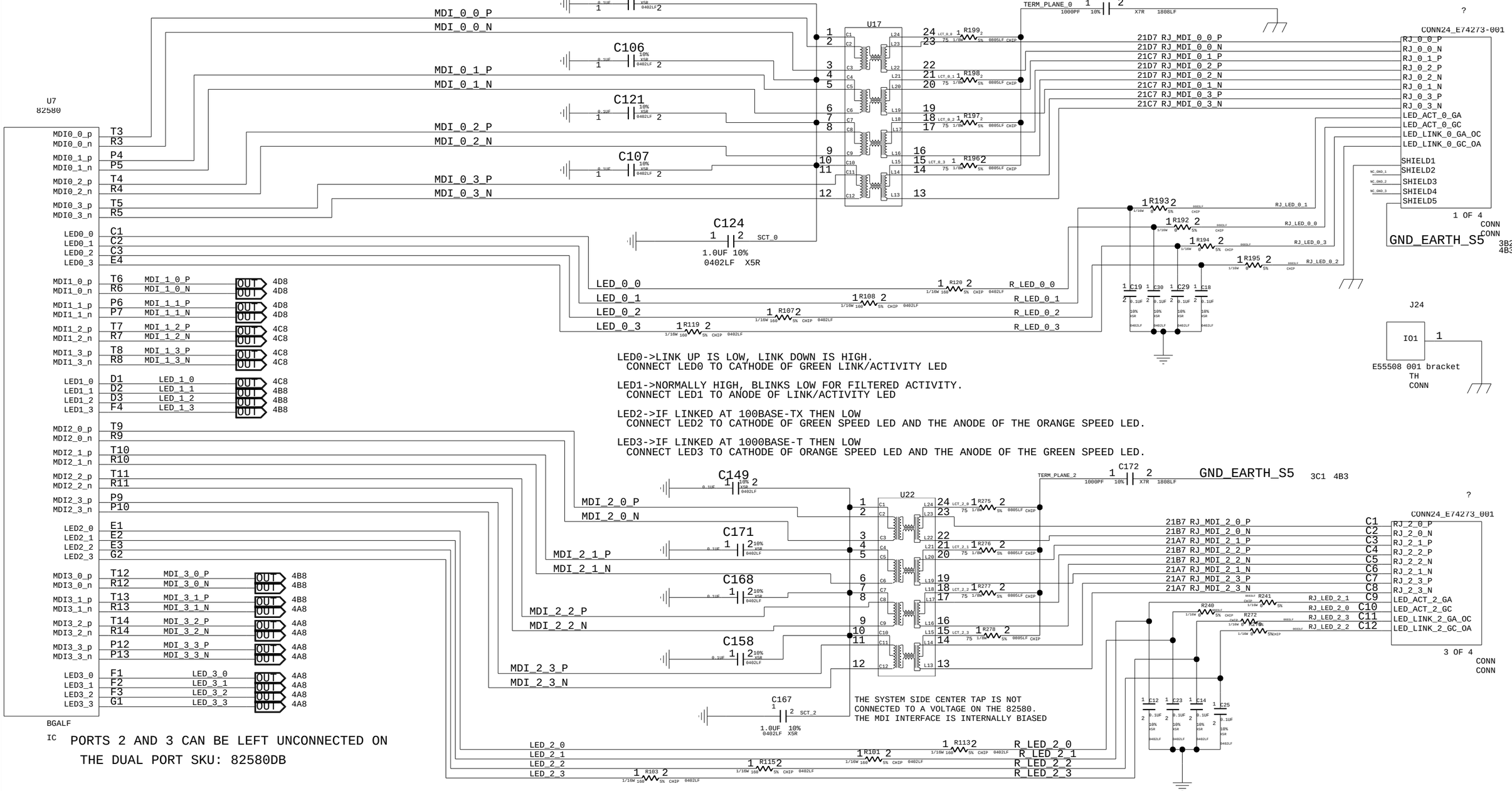
UNKNOWN

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 2

MDI 10BASE-T/100BASE-TX/1000BASE-T

THE MDI INTERFACE ON THE 82580 IS INTERNALLY TERMINATED.
EXTERNAL MDI TERMINATION IS NOT REQUIRED

THE SYSTEM SIDE CENTER TAP IS NOT CONNECTED TO A VOLTAGE ON THE 82580. THE MDI INTERFACE IS INTERNALLY BIASED



LED0->LINK UP IS LOW, LINK DOWN IS HIGH.
CONNECT LED0 TO CATHODE OF GREEN LINK/ACTIVITY LED

LED1->NORMALLY HIGH, BLINKS LOW FOR FILTERED ACTIVITY.
CONNECT LED1 TO ANODE OF LINK/ACTIVITY LED

LED2->IF LINKED AT 100BASE-TX THEN LOW
CONNECT LED2 TO CATHODE OF GREEN SPEED LED AND THE ANODE OF THE ORANGE SPEED LED.

LED3->IF LINKED AT 1000BASE-T THEN LOW
CONNECT LED3 TO CATHODE OF ORANGE SPEED LED AND THE ANODE OF THE GREEN SPEED LED.

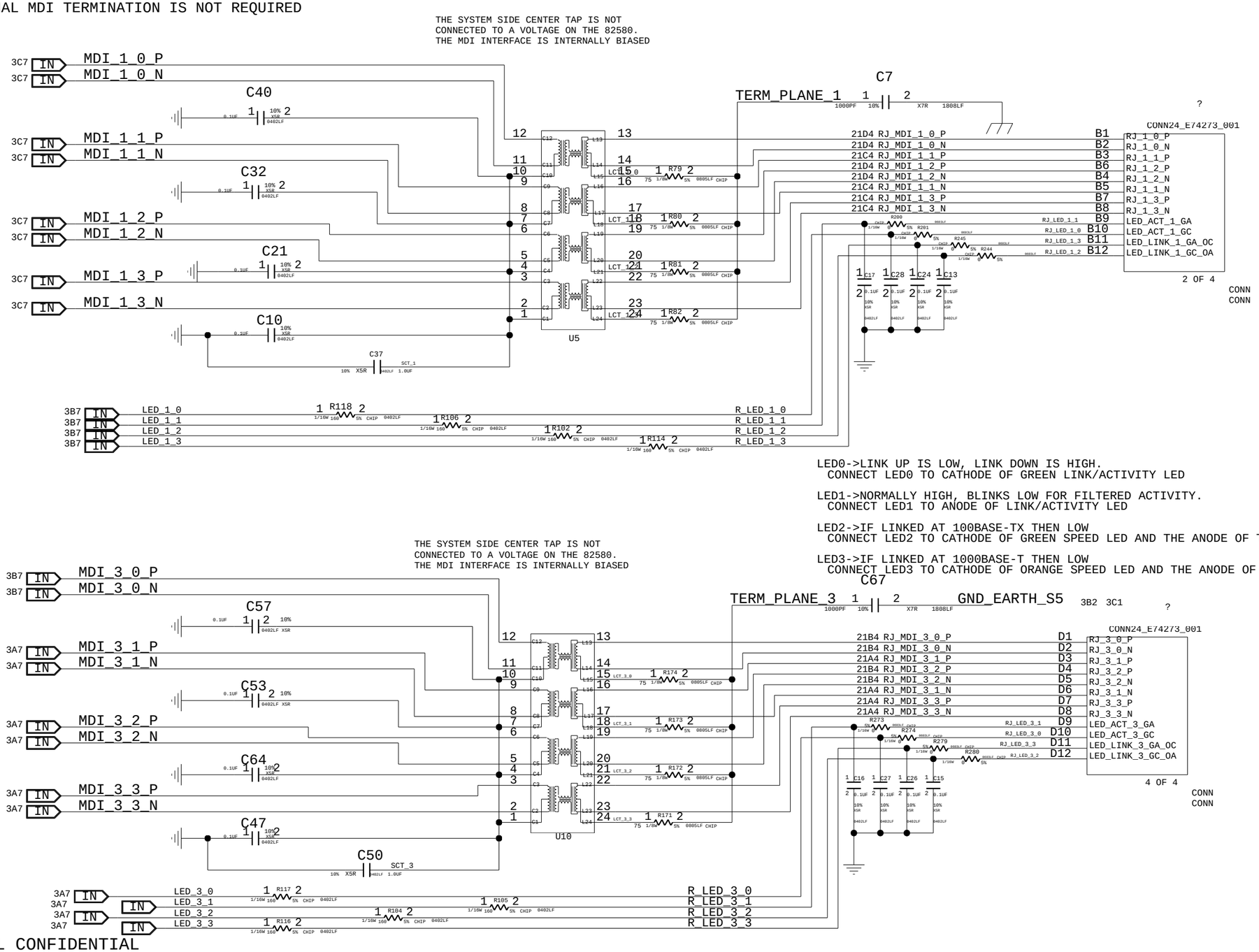
INTEL CONFIDENTIAL

UNKNOWN

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 3

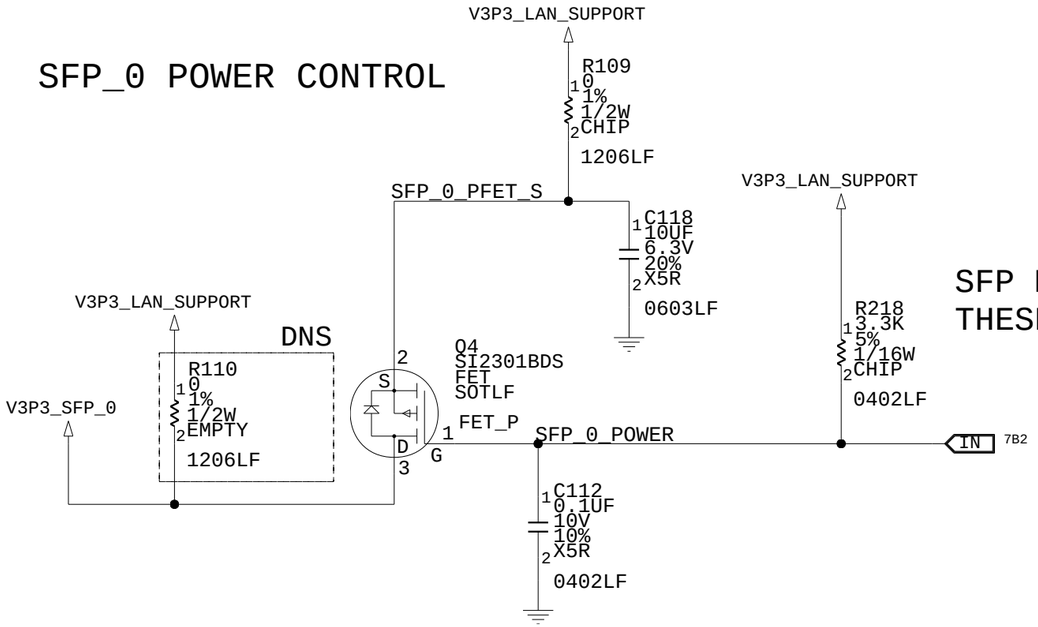
MDI 10BASE-T/100BASE-TX/1000BASE-T

THE MDI INTERFACE ON THE 82580 IS INTERNALLY TERMINATED.
EXTERNAL MDI TERMINATION IS NOT REQUIRED



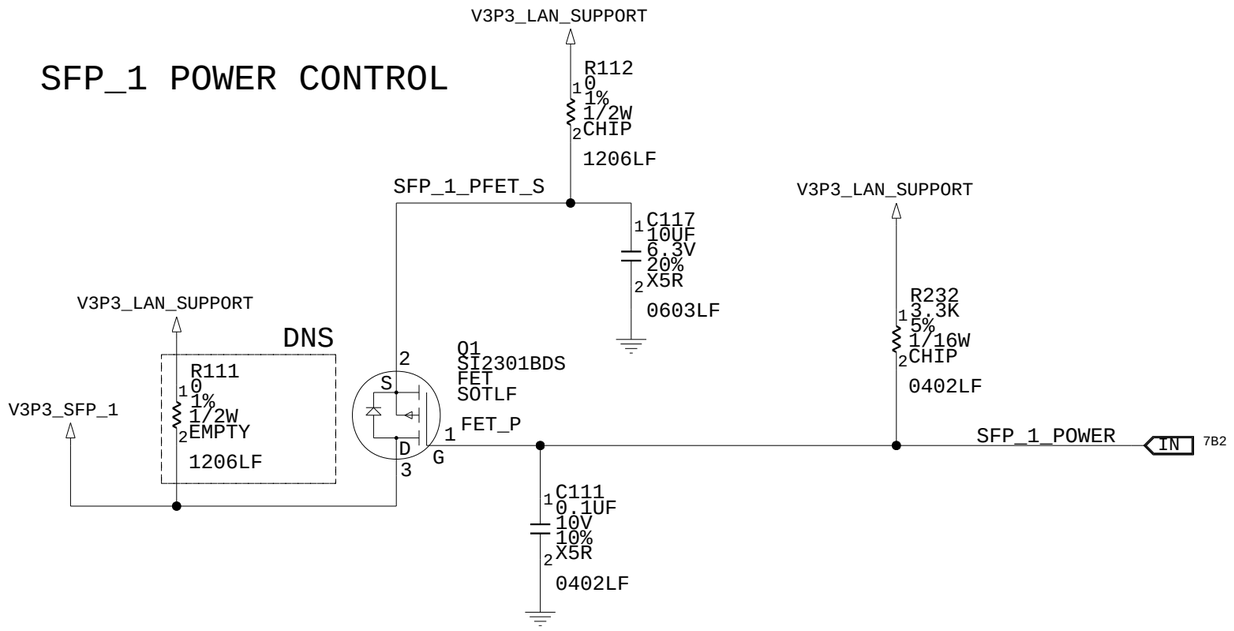
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: 82580 REFERENCE DESIGN	SIZE: B	CODE	DOCUMENT NUMBER: 322445-007EN	REV: 2.2	DATE: 2010-06-25	SHEET: 4

SFP_0 POWER CONTROL



SFP MODULES MAY NEED TO BE SHUT DOWN WHILE IN LOW POWER STATES
THESE FETS ALLOW SOFTWARE TO CONTROL THE SFP MODULE POWER.

SFP_1 POWER CONTROL

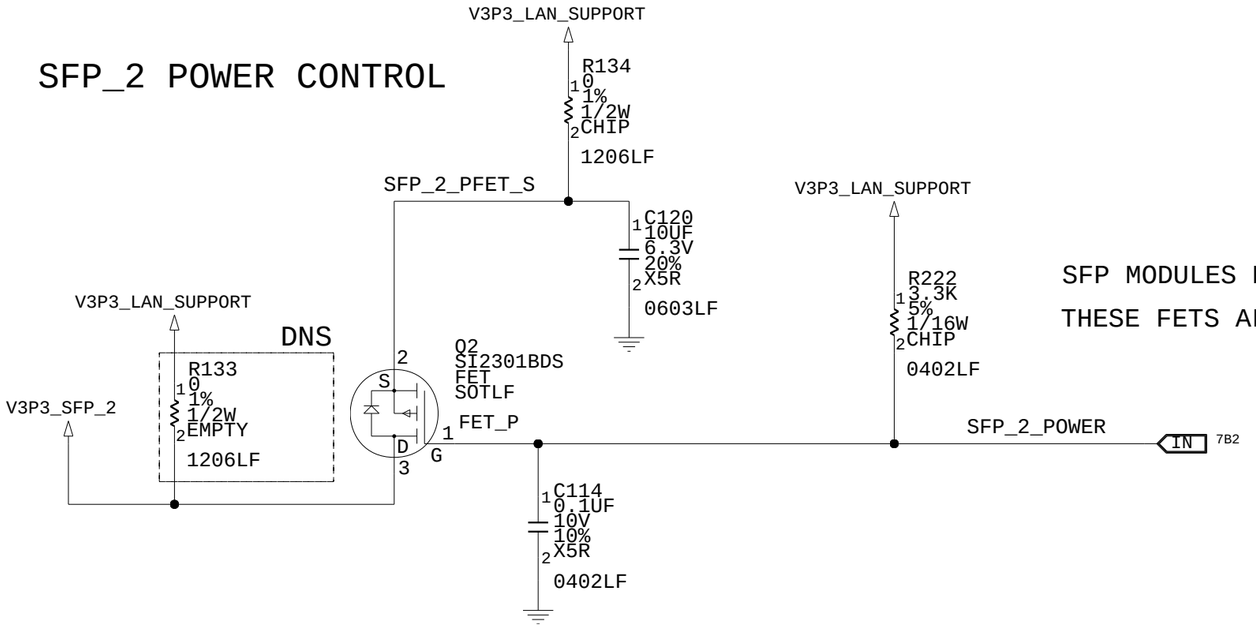


INTEL CONFIDENTIAL

UNKNOWN

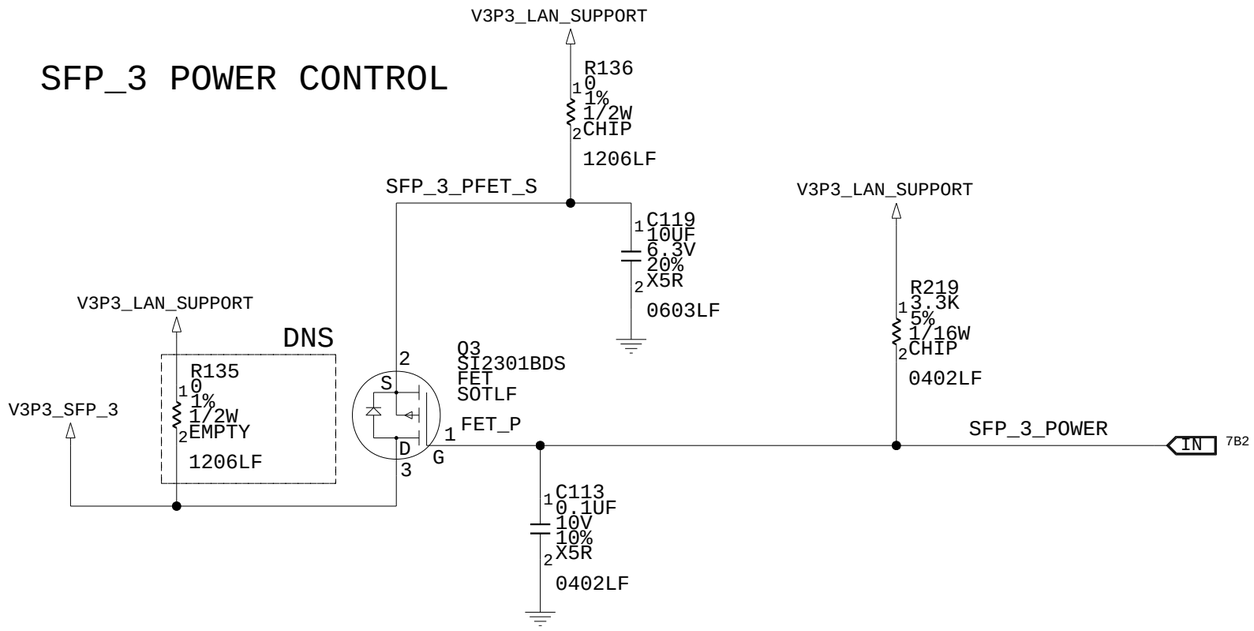
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 5

SFP_2 POWER CONTROL



SFP MODULES MAY NEED TO BE SHUT DOWN WHILE IN LOW POWER STATES
THESE FETS ALLOW SOFTWARE TO CONTROL THE SFP MODULE POWER.

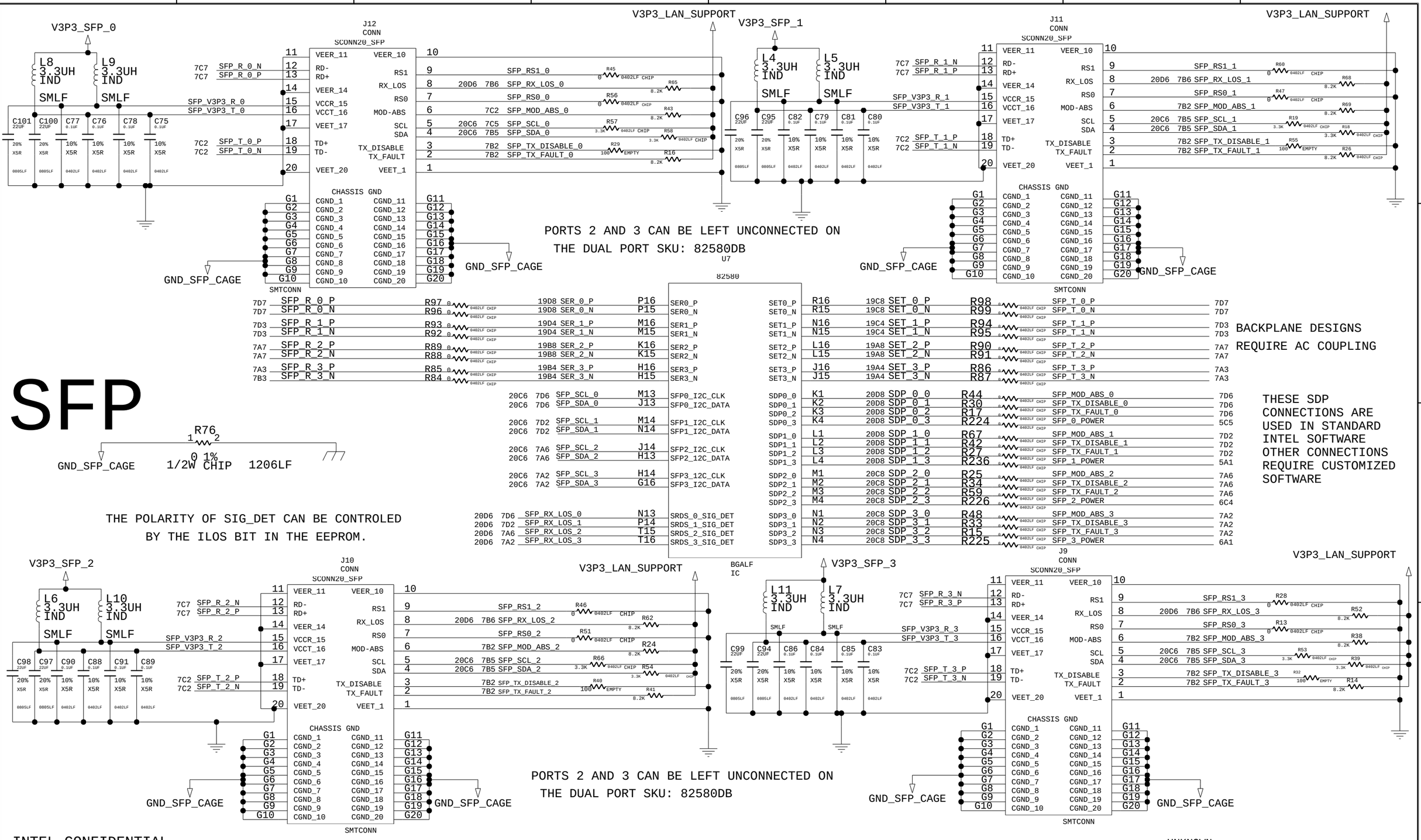
SFP_3 POWER CONTROL



UNKNOWN

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 6

SFP



INTEL CONFIDENTIAL

UNKNOWN

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: 82580 REFERENCE DESIGN	SIZE: B	CODE	DOCUMENT NUMBER: 322445-007EN	REV: 2.2	DATE: 2010-06-25	SHEET: 7

SUPPORT CIRCUITS

THE CAPACITORS BETWEEN THE CRYSTAL AND GROUND
MAY NEED TO BE ADJUSTED BASED ON PARASITIC CAPACITANCE
OF TRACES ON THE BOARD. 33 PF MAY BE A BETTER CHOICE FOR A SMALL CRYSTAL WITH VERY SHORT TRACES.

C110 27.0PF 50V 5%COG 0402LF
Y1 25.000MHZ IC
C108 27.0PF 50V 5%COG 0402LF
XTAL_IN 1 2 XTAL_OUT

R231 0 5% 1/16W CHIP 0402LF

C109 10.0PF 50V 5% COG 0402LF

THIS IMPLEMENTATION IS REQUIRED FOR PROPER CRYSTAL LOADING

ON THE 82580 THE LANX_DIS_N SIGNALS ARE INPUTS WHILE THEY ARE SAMPLED BUT BECOME OUTPUTS WHEN INITIALIZATION IS COMPLETE. A SERIES RESISTER SHOULD BE USED TO DRIVE THESE PINS.

THLF J43

CONN

R128 0 5% 1/16W CHIP 0402LF

V3P3_LAN_SUPPORT

V3P3_PE_MAIN

V3P3_LAN

R234 1.50K 1% CHIP 0402LF 1/16W

R238 3.3K 5% CHIP 0402LF 1/16W

R237 3.3K 5% CHIP 0402LF 1/16W

MAIN_PWR_OK IS HIGH WHEN FULL DEVICE POWER IS AVAILABLE
AND LOW WHEN ONLY AUX POWER IS AVAILABLE

R265 3.3K 5% CHIP 0402LF 1/16W
R254 3.3K 5% CHIP 0402LF 1/16W
R257 3.3K 5% CHIP 0402LF 1/16W
R252 3.3K 5% CHIP 0402LF 1/16W
R253 3.3K 5% CHIP 0402LF 1/16W
R239 3.3K 5% CHIP 0402LF 1/16W
R258 2.37K 1% 1/16W CHIP 0402LF

U7
82580
BGALF IC

	XTAL_CLK_OUT	P2	XTAL_CLK_O
20C2	XTAL_CLK_IN	P1	XTAL_CLK_I
20B6	AUX_PWR	D15	AUX_PWR
20B4	LAN0_DIS_N	F14	LAN0_DIS_N
20B4	LAN1_DIS_N	E14	LAN1_DIS_N
20B4	LAN2_DIS_N	D14	LAN2_DIS_N
20B4	LAN3_DIS_N	C14	LAN3_DIS_N
20B8	DEVICE_OFF_N	C4	DEVICE_OFF_N
	SE_RSET	K13	SE_RSET
	TSENSP	D5	TSENSP
	TSENSZ	C5	TSENSZ
	PE_TRIM1	A2	PE_TRIM1
	PE_TRIM2	A1	PE_TRIM2
20B8 11A1	LAN_PWR_GOOD	D4	LAN_PWR_GOOD
20B8	MAIN_PWR_OK	B2	MAIN_PWR_OK

FLSH_CE_N	C16	FLASH_CS_N
FLSH_SCK	B16	FLASH_SCK
FLSH_SI	B15	FLASH_SI
FLSH_SO	C15	FLASH_SO
EE_CS_N	F16	EEPROM_CS_N
EE_DI	E15	EEPROM_SI
EE_DO	F15	
EE_SK	E16	EEPROM_SCK
RSVD_ATST_p	R2	
RSVD_ATST_n	T1	
RSVD_TX_TCLK	R1	
GE_REXT3K	T2	REXT3K
RSVD_TP_5	C13	
RSVD_TP_6	D12	
RSVD_TP_7	G14	
RSVD_TP_8	G15	
RSVD_TE_VSS	C12	

THE TSENSEP AND TSENSEZ ARE CONNECTED TO AN INTERNAL THERMAL DIODE. THIS IS PRIMARILY INTENDED FOR LAB MEASUREMENTS. FUTURE PIN COMPATABLE DESIGNS WILL CHANGE THIS FUNCTION.

20B6 TEST_ENABLE
R247 3.3K 5% 1/16W CHIP 0402LF

A FLASH DEVICE IS NOT REQUIRED IF PXE AND/OR ISCSI BOOT CODE IS INTEGRATED INTO THE BIOS

U13 M25P40 SOICLF IC
5 D, 6 C, 1 S_N, 3 W_N, 7 HOLD_N, 8 VCC, 4 GND, 2 Q

V3P3_LAN_SUPPORT

FLASH_HOLD_N
FLASH_WP_N

R266 3.3K 5% CHIP 0402LF 1/16W
R268 3.3K 5% CHIP 0402LF 1/16W
R269 3.3K 5% CHIP 0402LF 1/16W
R267 3.3K 5% CHIP 0402LF 1/16W

EEPROM_WP_N

U12 IC AT25256
CS_N, WP_N, SI, SCK, HOLD_N, SO

VCC=V3P3_LAN_SUPPORT
GND=GND_POWER

EEPROM_HOLD_N
EEPROM_SO

ATEST_P
ATEST_N
J25 CONN THLF

REXT3K
R235 3.01K 1% CHIP 0402LF 1/16W

TX_TCLOCK
J27 CONN THLF

V3P3_LAN_SUPPORT

R160 3.3K 5% 1/16W CHIP EMPTY 0402LF
R161 3.3K 5% 1/16W CHIP EMPTY 0402LF
R162 3.3K 5% 1/16W CHIP EMPTY 0402LF
R163 3.3K 5% 1/16W CHIP EMPTY 0402LF

20B4 TP5 R251 3.3K 5% 1/16W 0402LF EMPTY
20B4 TP6 R249 3.3K 5% 1/16W 0402LF EMPTY
20B4 TP7 R262 3.3K 5% 1/16W 0402LF EMPTY
20B4 TP8 R264 3.3K 5% 1/16W 0402LF EMPTY

UNKNOWN

INTEL CONFIDENTIAL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 8

POWER SUPPLIES

V1P8_LAN

MAX VCC1P8 = ~0.2 A

FB3 — 330 FB SMLF

R131 — 0.39 1% 1/10W CHIP 0603LF

C134 1.0UF 6.3V 10% X5R 0402LF

C152 0.01UF 25V 10% X7R 0402LF

C122 1000PF 50V 10% X7R 0402LF

C135 1000PF 50V 10% X7R 0402LF

V1P8_LAN_PE_TXVTERM

V1P8_LAN_APE

FB7 — 330 FB SMLF

R144 — 0.39 1% 1/10W CHIP 0603LF

C156 1.0UF 6.3V 10% X5R 0402LF

C144 0.01UF 25V 10% X7R 0402LF

C157 1000PF 50V 10% X7R 0402LF

C33 47UF 6.3V 20% X5R 1206LF

C22 10UF 6.3V 20% X5R 0805LF

V3P3_LAN

MAX VCC3P3 = ~0.3 A

FB10 — 330 FB SMLF

R125 — 0.39 1% 1/10W CHIP 0603LF

C123 1.0UF 6.3V 10% X5R 0402LF

C116 0.01UF 25V 10% X7R 0402LF

C115 1000PF 50V 10% X7R 0402LF

FB5 — 330 FB SMLF

R139 — 0.39 1% 1/10W CHIP 0603LF

C130 1.0UF 6.3V 10% X5R 0402LF

C141 0.01UF 25V 10% X7R 0402LF

C126 1000PF 50V 10% X7R 0402LF

C150 1000PF 50V 10% X7R 0402LF

V3P3_LAN_AGE

V3P3_LAN_A

V3P3_LAN

U7
82580

C6	PE_TXVTERM1	VCC1P0_K11	K11
C8	PE_TXVTERM2	VCC1P0_J11	J11
C9	PE_TXVTERM3	VCC1P0_H11	H11
C11	PE_TXVTERM4	VCC1P0_G11	G11
		VCC1P0_E11	E11
C7	VCC1P8_APE_C7	VCC1P0_M11	M11
C10	VCC1P8_APE_C10	VCC1P0_E6	E6
		VCC1P0_G6	G6
		VCC1P0_H6	H6
		VCC1P0_J6	J6
L5	VCC3P3_AGE_L5	VCC1P0_K6	K6
M6	VCC3P3_A_M6	VCC1P0_N12	N12
M7	VCC3P3_A_M7	VCC1P0_AGE_L7	L7
M8	VCC3P3_A_M8	VCC1P0_AGE_L8	L8
M9	VCC3P3_A_M9	VCC1P0_AGE_L9	L9
M10	VCC3P3_A_M10	VCC1P0_AGE_L10	L10
P8	VCC3P3_A_P8		
P11	VCC3P3_A_P11	VCC1P0_APE_D6	D6
F5	VCC3P3_F5	VCC1P0_APE_D8	D8
F12	VCC3P3_F12	VCC1P0_APE_D9	D9
H5	VCC3P3_H5	VCC1P0_APE_D11	D11
H12	VCC3P3_H12		
K5	VCC3P3_K5	VCC1P0_ASE_L14	L14
K12	VCC3P3_K12	VCC1P0_ASE_K14	K14
L12	VCC3P3_L12	VCC1P0_ASE_L13	L13

BGALF IC

U7
82580

M5	VSS_M5	VSS_M12	M12
G10	VSS_G10	VSS_N5	N5
G9	VSS_G9	VSS_P3	P3
G8	VSS_G8	VSS_N11	N11
G7	VSS_G7	VSS_N10	N10
G5	VSS_G5	VSS_N9	N9
F11	VSS_F11	VSS_N8	N8
F10	VSS_F10	VSS_N7	N7
F9	VSS_F9	VSS_N6	N6
F8	VSS_F8	VSS_L11	L11
F7	VSS_F7	VSS_L6	L6
F6	VSS_F6	VSS_K10	K10
E10	VSS_E10	VSS_K9	K9
E9	VSS_E9	VSS_K8	K8
E8	VSS_E8	VSS_K7	K7
E7	VSS_E7	VSS_J12	J12
D10	VSS_D10	VSS_J10	J10
D7	VSS_D7	VSS_J9	J9
B13	VSS_B13	VSS_J8	J8
B10	VSS_B10	VSS_J7	J7
B7	VSS_B7	VSS_J5	J5
B4	VSS_B4	VSS_H10	H10
A13	VSS_A13	VSS_H9	H9
A10	VSS_A10	VSS_H8	H8
A7	VSS_A7	VSS_H7	H7
A4	VSS_A4	VSS_G12	G12

BGALF IC

V1P0_LAN

MAX VCC1P0 = ~1.1 A

C151 1000PF 50V 10% X7R 0402LF

C143 1000PF 50V 10% X7R 0402LF

C125 1000PF 50V 10% X7R 0402LF

C132 1000PF 50V 10% X7R 0402LF

C128 0.01UF 25V 10% X7R 0402LF

C129 1.0UF 6.3V 10% X5R 0402LF

V1P0_LAN_AGE

MAX VCC1P0_AGE = ~0.8 A

C139 1000PF 50V 10% X7R 0402LF

C140 1000PF 50V 10% X7R 0402LF

C131 0.01UF 25V 10% X7R 0402LF

C154 1.0UF 6.3V 10% X5R 0402LF

FB6 — 330 FB SMLF

R143 — 0.39 1% 1/10W CHIP 0603LF

V1P0_LAN_APE

MAX VCC1P0_APE = ~0.9 A

C138 1000PF 50V 10% X7R 0402LF

C137 1000PF 50V 10% X7R 0402LF

C127 0.01UF 25V 10% X7R 0402LF

C142 1.0UF 6.3V 10% X5R 0402LF

FB4 — 330 FB SMLF

R138 — 0.39 1% 1/10W CHIP 0603LF

V1P0_LAN_ASE

MAX VCC1P0_ASE = ~0.2 A

C155 1000PF 50V 10% X7R 0402LF

C162 1000PF 50V 10% X7R 0402LF

C165 0.01UF 25V 10% X7R 0402LF

C166 1.0UF 6.3V 10% X5R 0402LF

FB8 — 330 FB SMLF

R149 — 0.39 1% 1/10W CHIP 0603LF

C45 10UF 6.3V 20% X5R 0805LF

C60 47UF 6.3V 20% X5R 1206LF

C55 47UF 6.3V 20% X5R 1206LF

C105 10UF 6.3V 20% X5R 0805LF

C145 1.0UF 6.3V 10% X5R 0402LF

C146 0.01UF 25V 10% X7R 0402LF

C164 1000PF 50V 10% X7R 0402LF

C163 1000PF 50V 10% X7R 0402LF

THIS POWER SUPPLY FILTERING DESIGN IS KNOWN TO WORK
OTHER DESIGNS MAY BE POSSIBLE

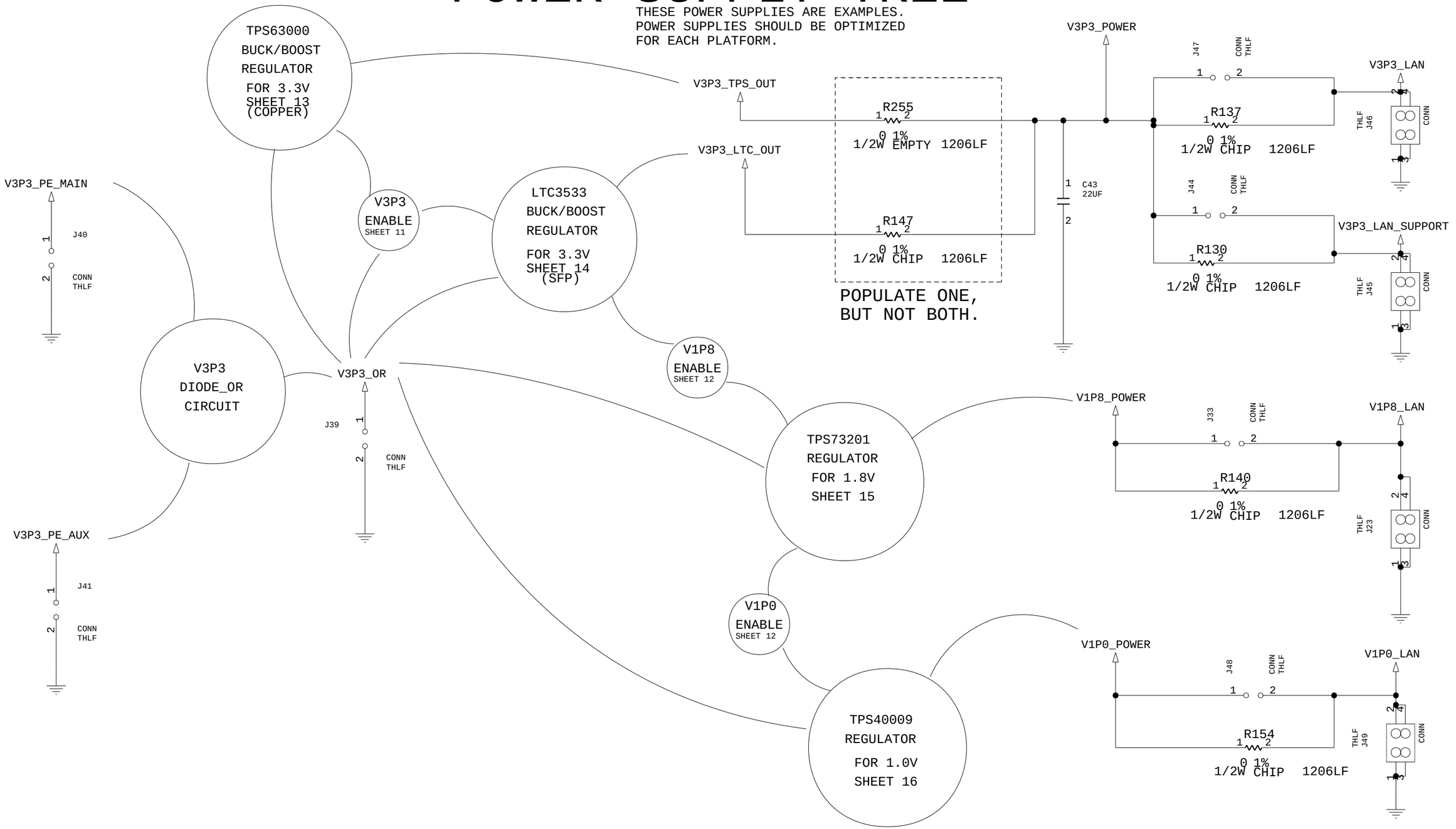
INTEL CONFIDENTIAL

UNKNOWN

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: 82580 REFERENCE DESIGN	SIZE: B	CODE:	DOCUMENT NUMBER: 322445-007EN	REV: 2.2	DATE: 2010-06-25	SHEET: 9

POWER SUPPLY TREE

THESE POWER SUPPLIES ARE EXAMPLES.
POWER SUPPLIES SHOULD BE OPTIMIZED
FOR EACH PLATFORM.

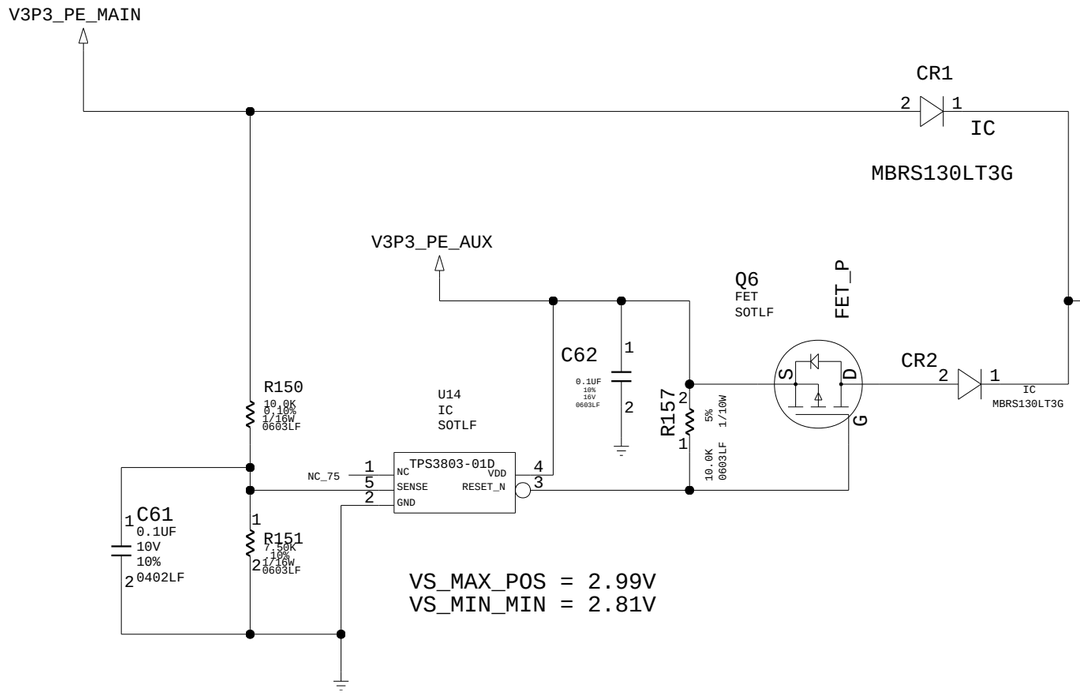


INTEL CONFIDENTIAL

UNKNOWN

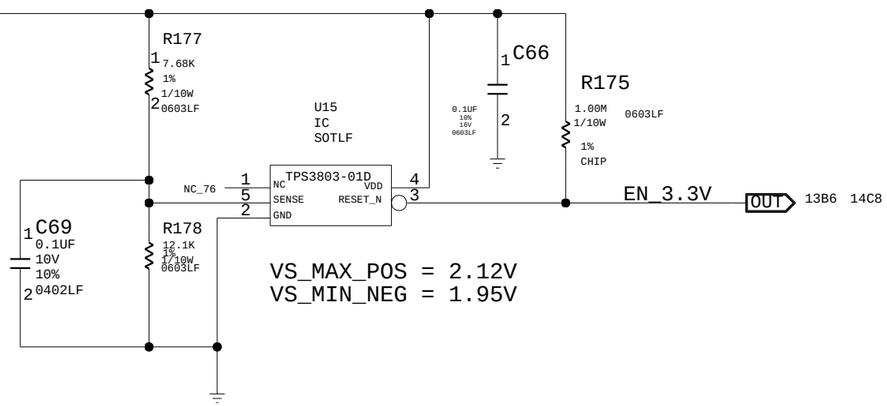
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 10

DETECT AND VAUX DISABLE CIRCUIT WITH DIODE "OR" OUTPUT



VS_MAX_POS = 2.99V
VS_MIN_MIN = 2.81V

3.3V ENABLE CIRCUIT

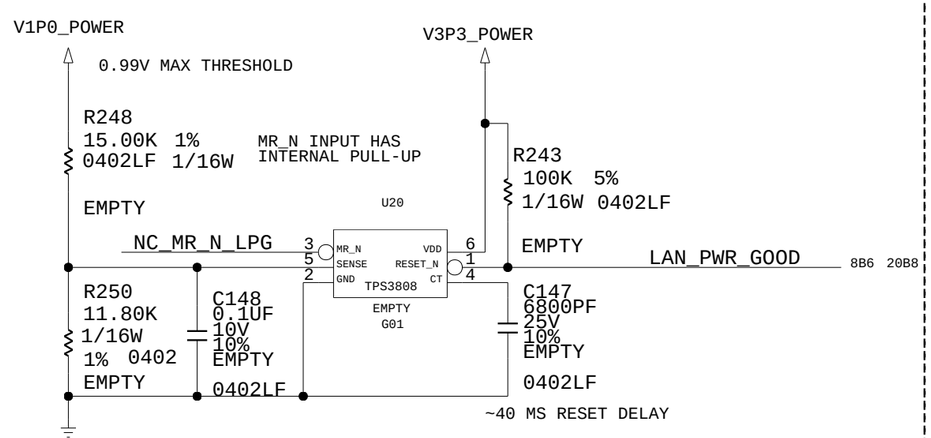


VS_MAX_POS = 2.12V
VS_MIN_NEG = 1.95V

82580 LAN_PWR_GOOD GENERATOR

EXTERNAL LAN_PWR_GOOD GENERATION IS NOT REQUIRED IN MOST DESIGNS

82580 INTERNAL POWER GOOD INDICATION IS A LOGICAL AND OF THE EXTERNAL LAN_PWR_GOOD PIN AND AN INTERNAL POWER ON RESET CIRCUIT.



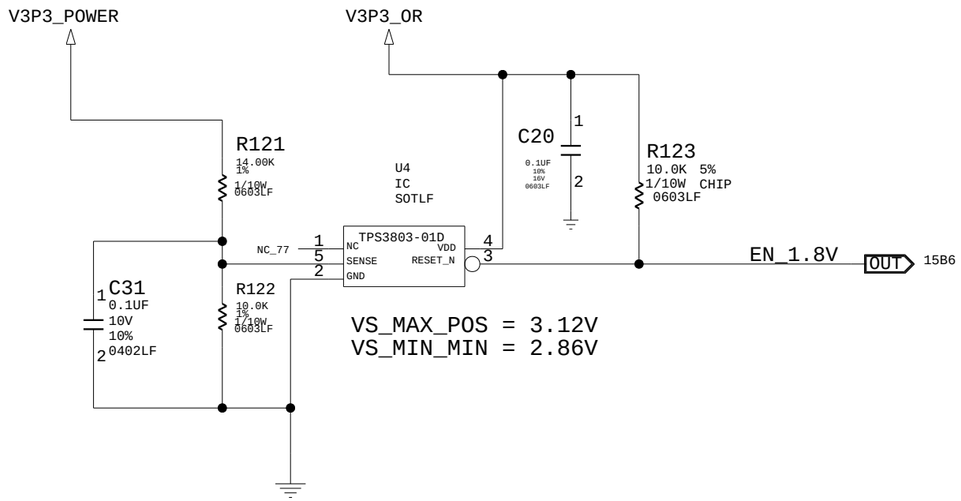
DNS

11 - DETECT, DIODE "OR" AND 3.3V ENABLE CIRCUIT

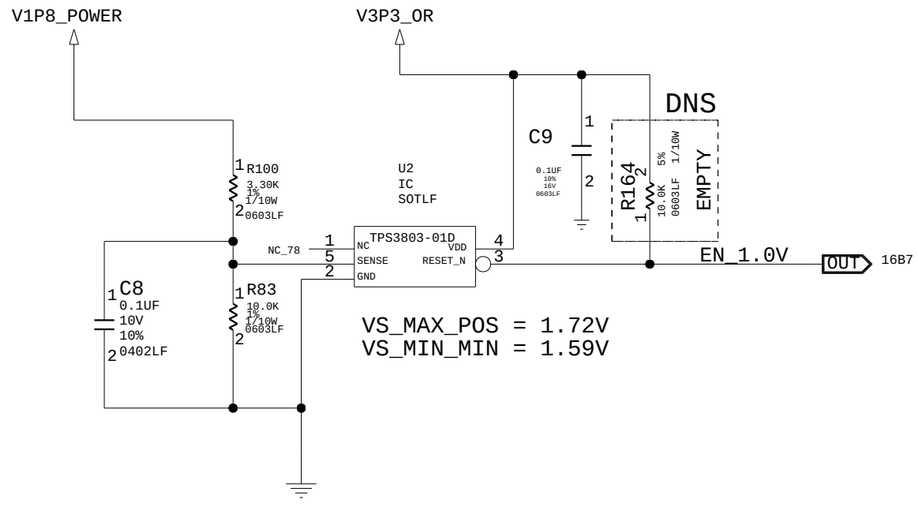
INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: 82580 REFERENCE DESIGN	SIZE: B	CODE	DOCUMENT NUMBER: 322445-007EN	REV: 2.2	DATE: 2010-06-25 / SHEET: 11

1.8V ENABLE CIRCUIT



1.0V ENABLE CIRCUIT



13 - 1.8V AND 1.0V ENABLE CIRCUITS

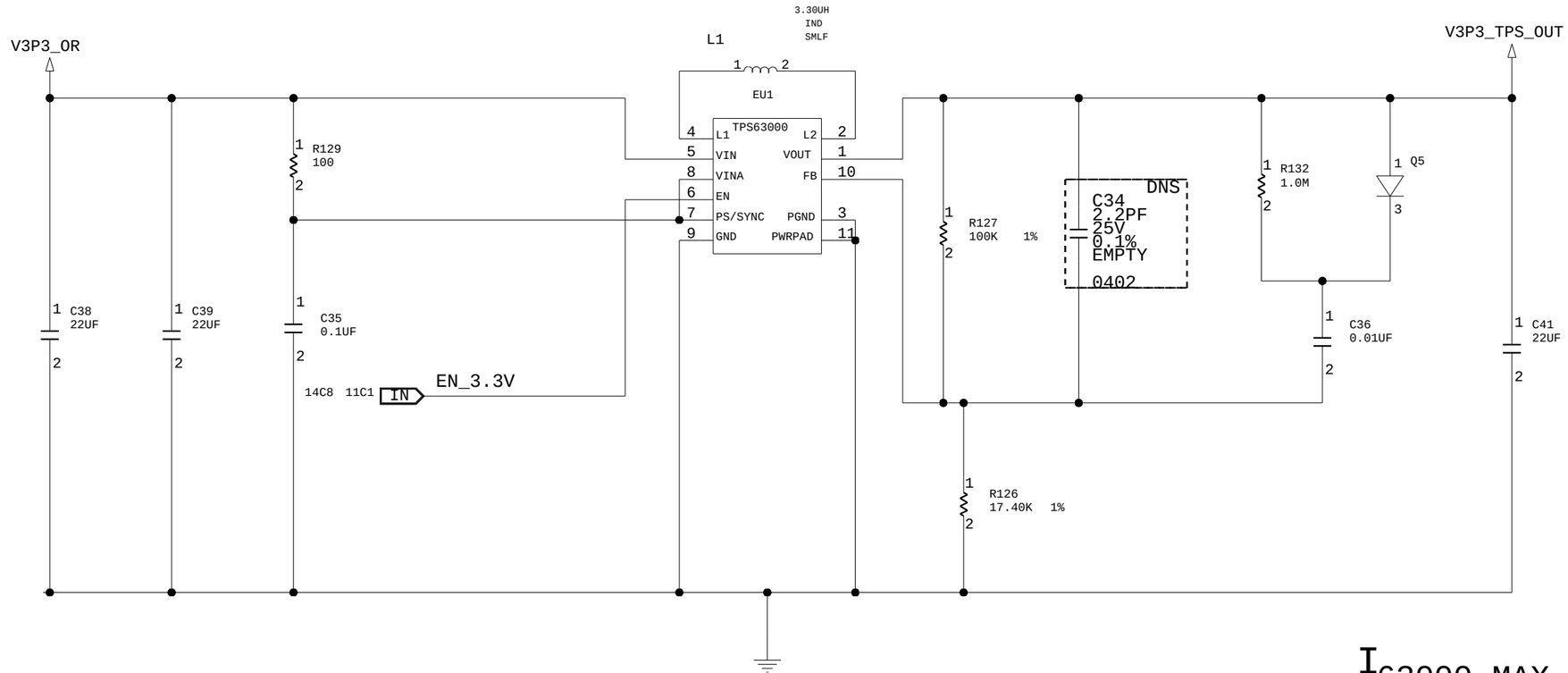
INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 12

TPS63000 BUCK/BOOST REGULATOR FOR 3.3V

VOLTAGE BOOST REQUIRED TO COMPENSATE FOR
VOLTAGE DROP FROM DIODE OR CIRCUIT. MANY DESIGNS MAY NOT REQUIRE A BOOST CIRCUIT.

VOUT_MAX = 3.47V
VOUT_MIN = 3.28V

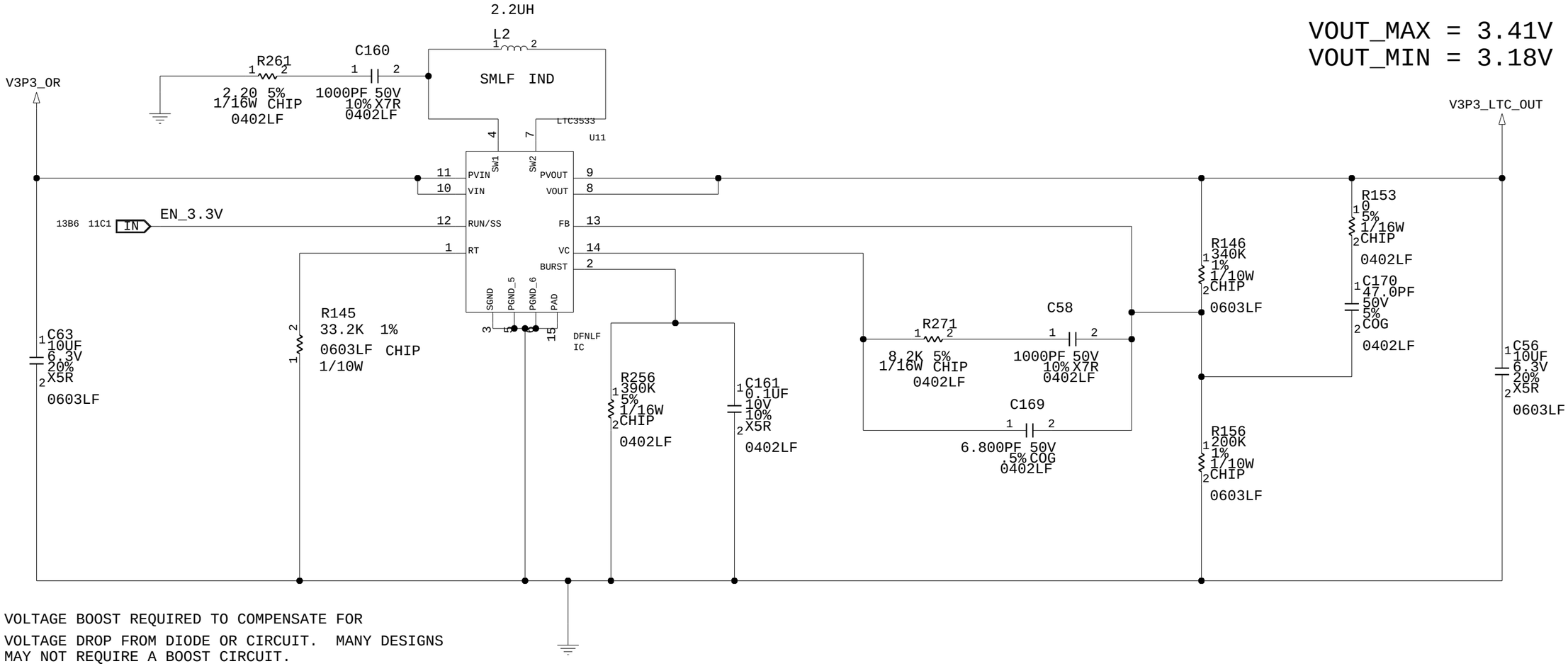


$I_{63000\text{-}MAX}$ = 0.800A

13 - 3.3V REGULATOR
INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 13

LTC3533 BUCK/BOOST REGULATOR FOR 3.3V (REQUIRED FOR 4-PORT SFP OPERATION)



VOUT_MAX = 3.41V
VOUT_MIN = 3.18V

VOLTAGE BOOST REQUIRED TO COMPENSATE FOR
VOLTAGE DROP FROM DIODE OR CIRCUIT. MANY DESIGNS MAY NOT REQUIRE A BOOST CIRCUIT.

$I_{3533\text{-}MAX}$ = 1.5A

14 - 3.3V REGULATOR

INTEL

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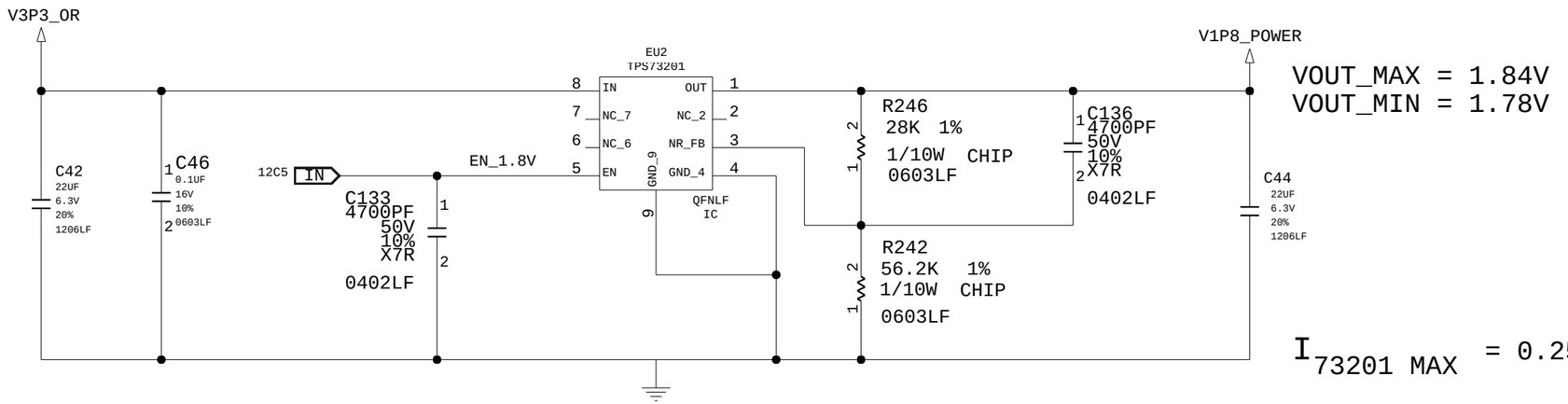
TPS73201 REGULATOR FOR 1.8V



VOUT_MAX = 1.84V
VOUT_MIN = 1.78V

$I_{73201\ MAX} = 0.25A$

15 - 1.8V REGULATOR

INTEL

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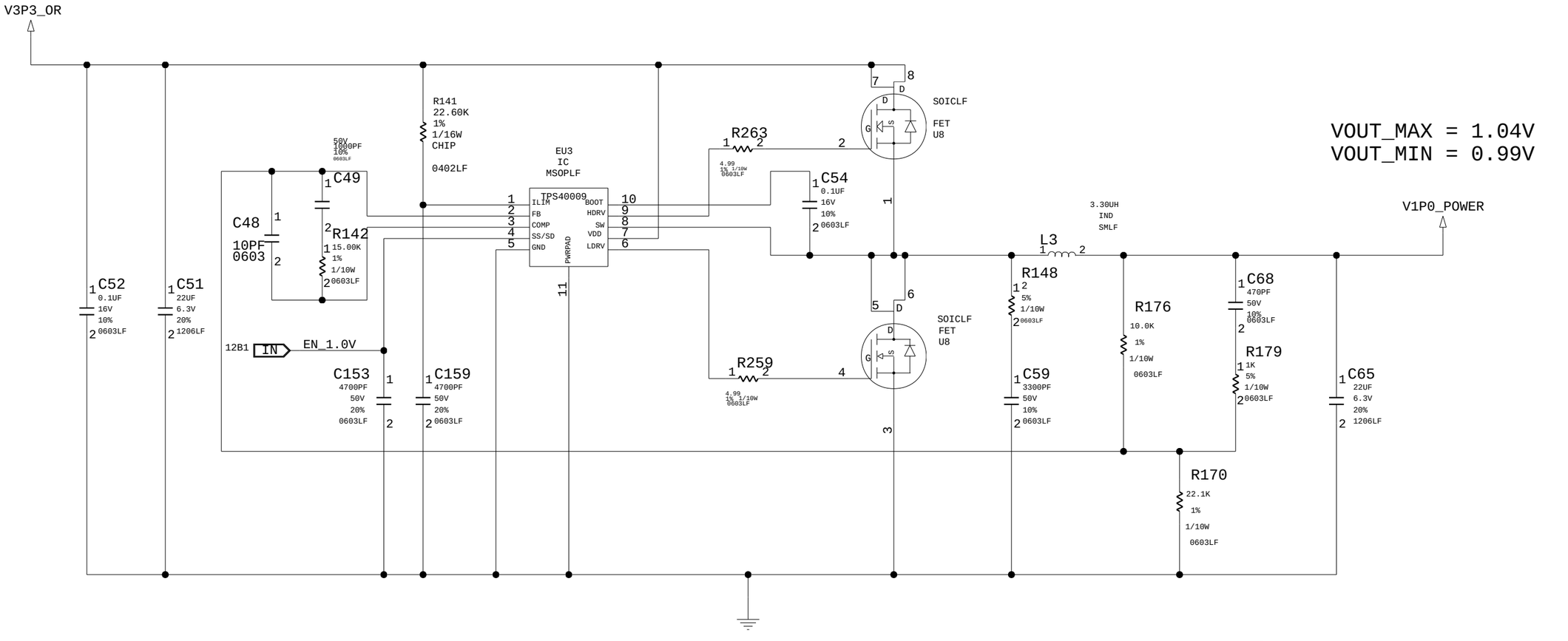
TPS40009 REGULATOR FOR 1.0V



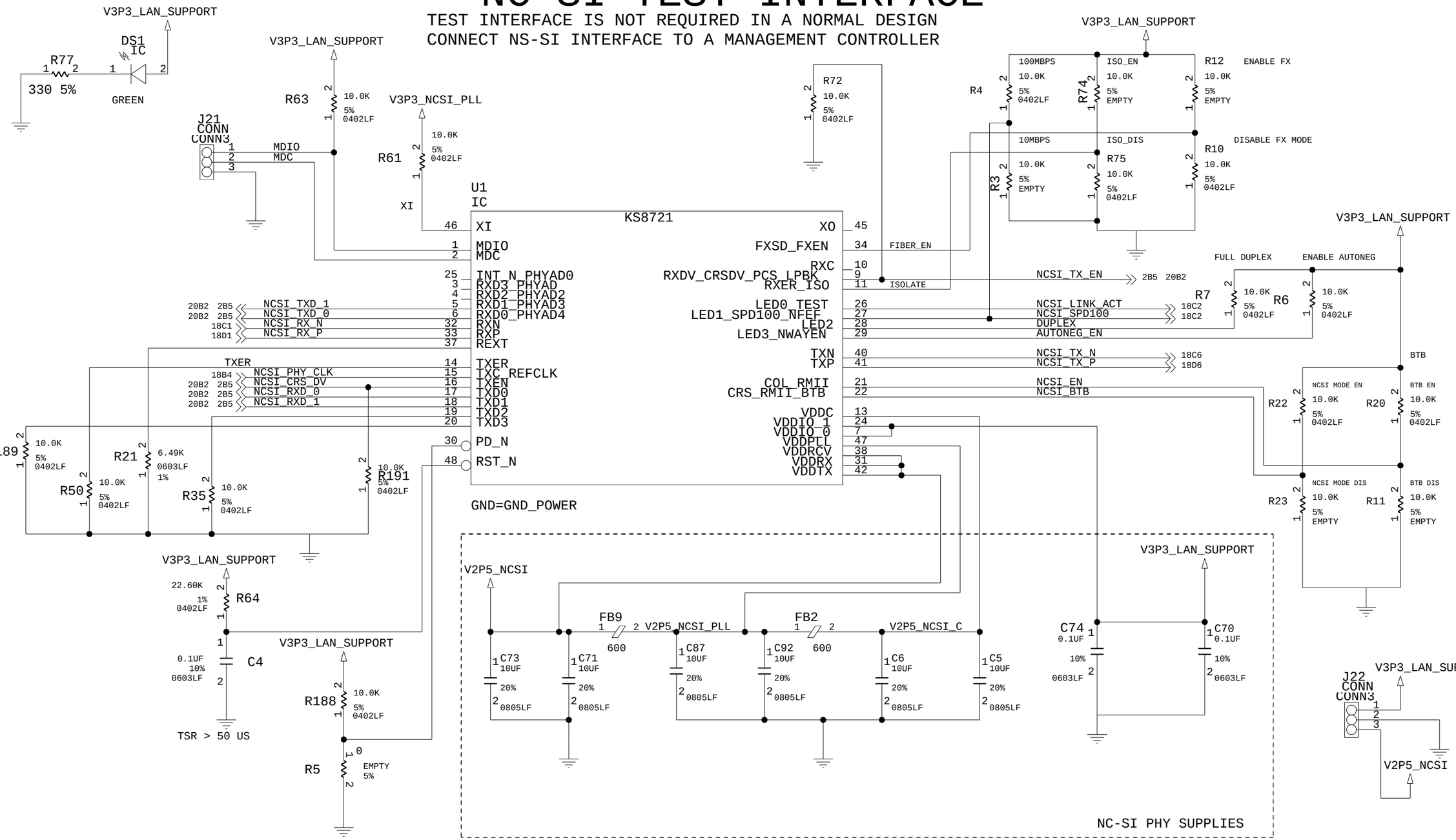
16 - 1.0V REGULATOR

INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 16

NC-SI TEST INTERFACE

TEST INTERFACE IS NOT REQUIRED IN A NORMAL DESIGN
CONNECT NS-SI INTERFACE TO A MANAGEMENT CONTROLLER



INTEL CONFIDENTIAL

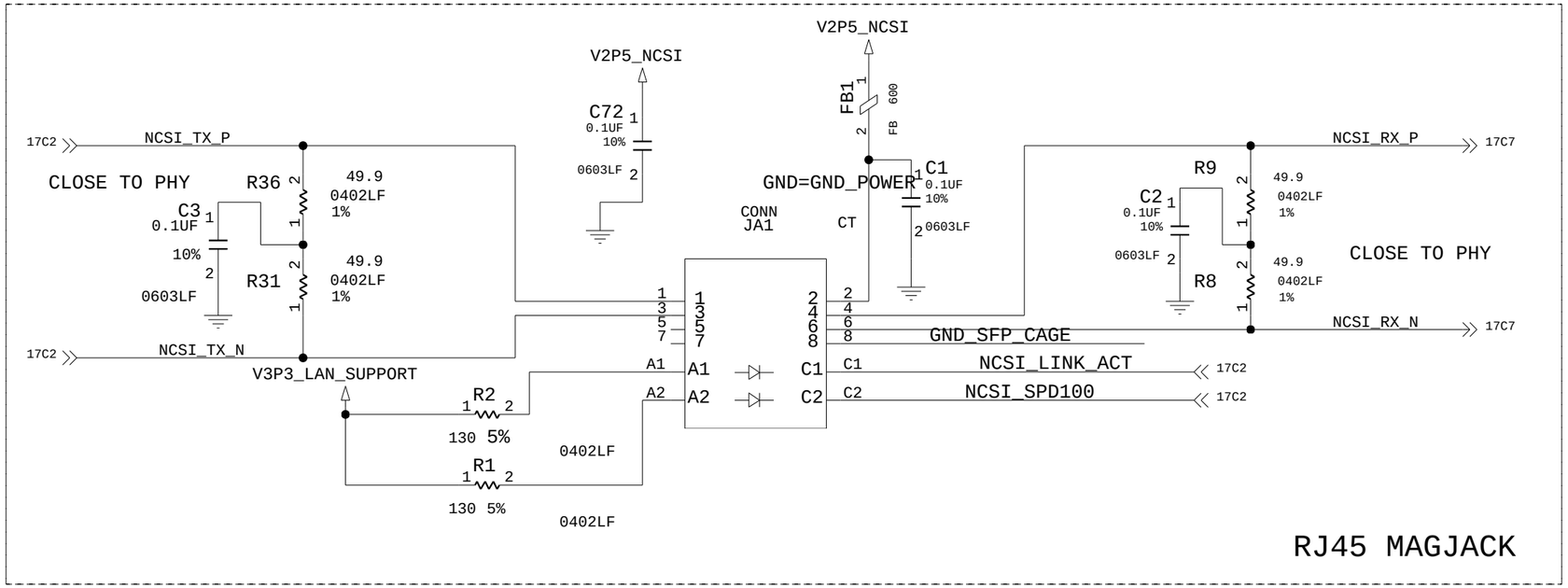
UNKNOWN

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 17

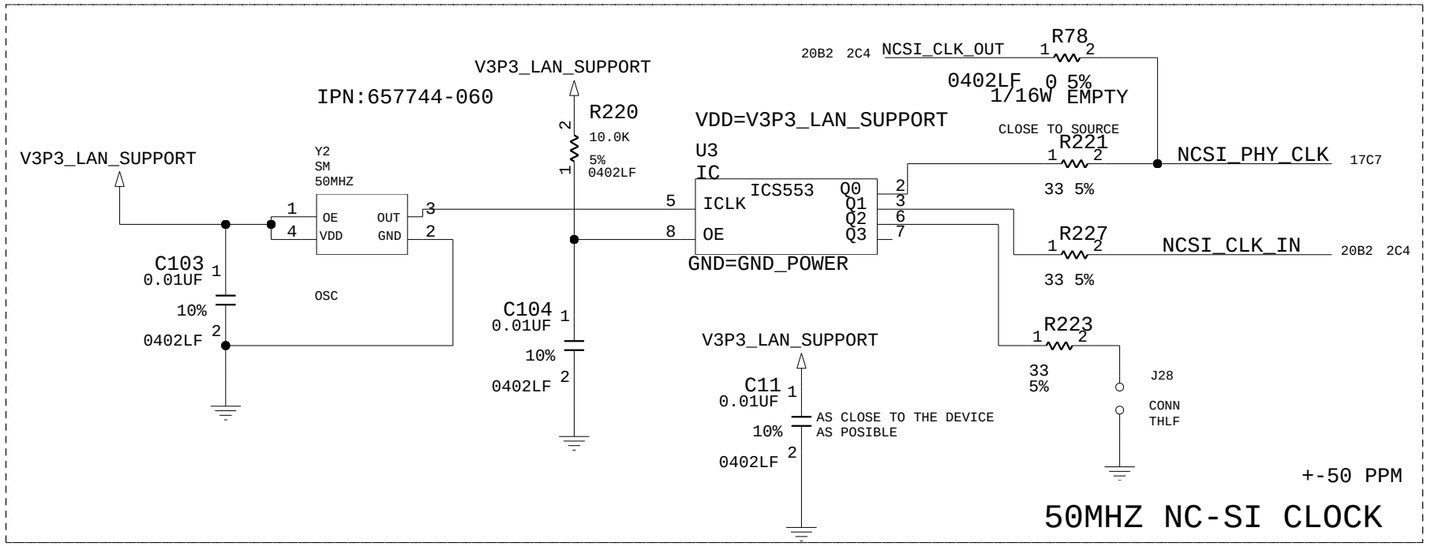
NC-SI TEST INTERFACE

TEST INTERFACE IS NOT REQUIRED IN A NORMAL DESIGN

CONNECT NS-SI INTERFACE TO A MANAGEMENT CONTROLLER



RJ45 MAGJACK



50MHZ NC-SI CLOCK

INTEL CONFIDENTIAL

UNKNOWN

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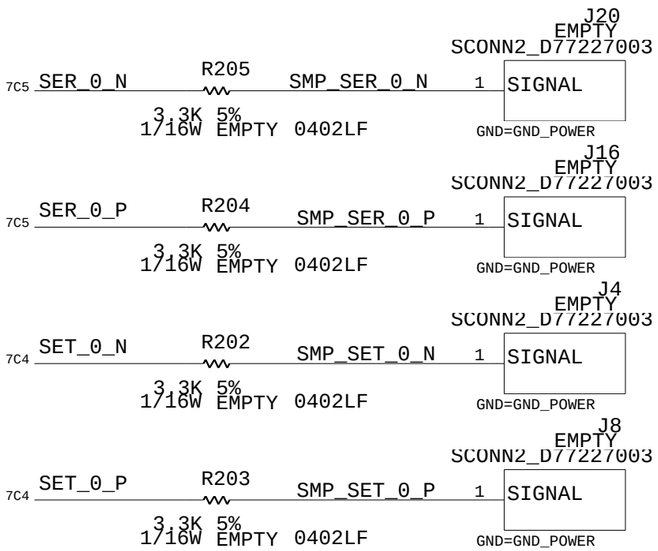
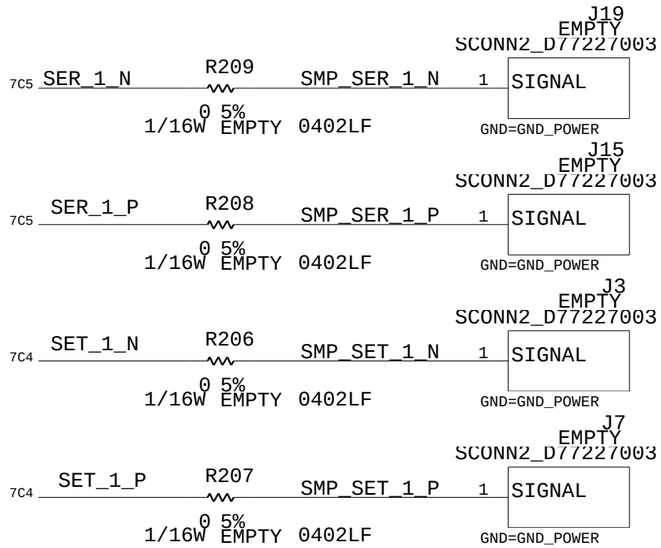
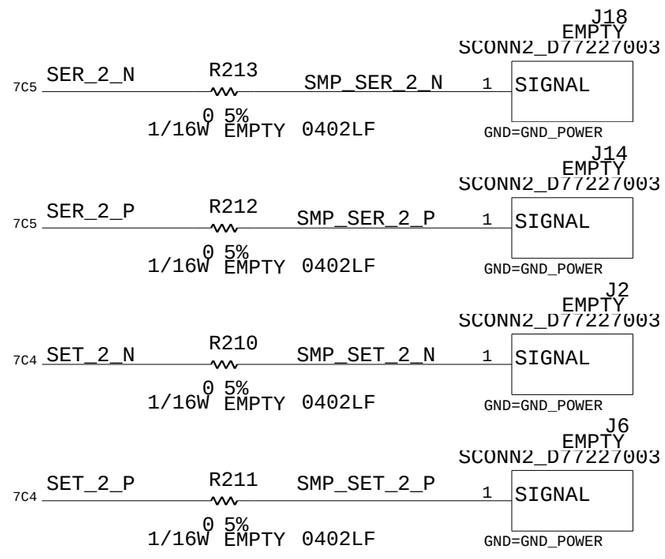
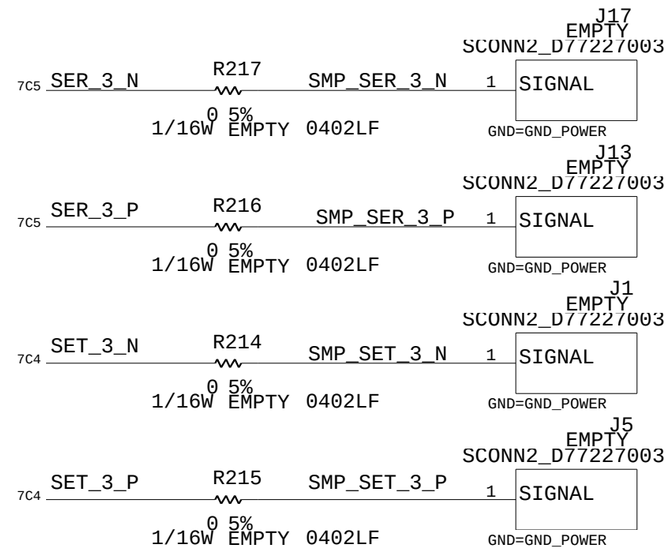
TEST CONNECTORS SE







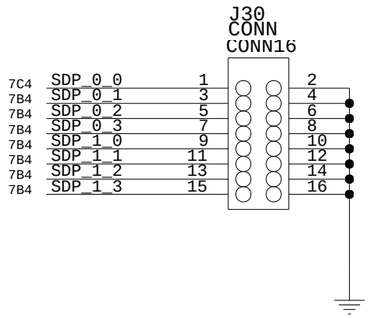


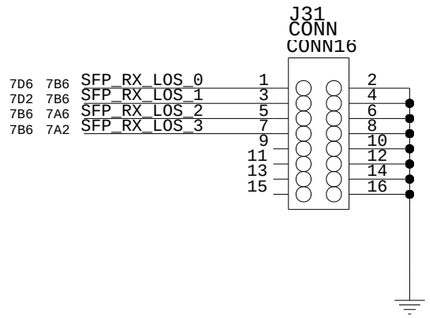
TEST INTERFACE IS NOT REQUIRED IN A NORMAL DESIGN

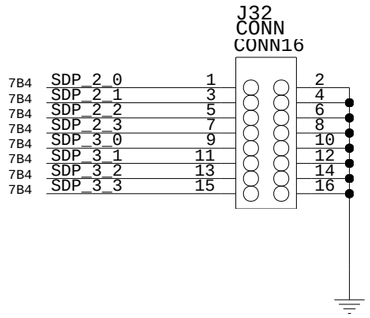
UNKNOWN

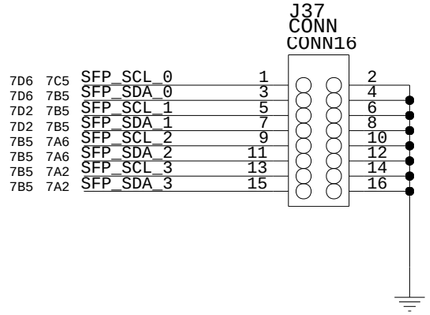
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82580 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 322445-007EN	REV 2.2	DATE 2010-06-25	SHEET 19

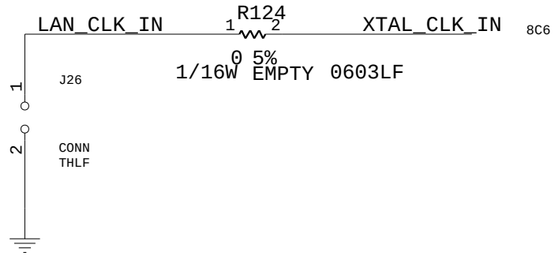
TEST CONNECTORS IO

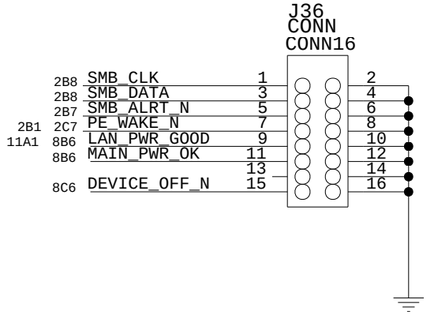


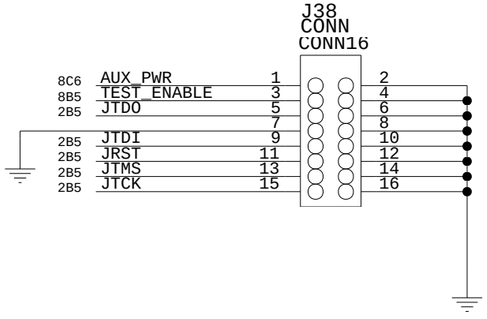


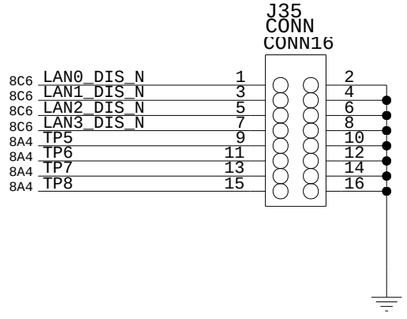


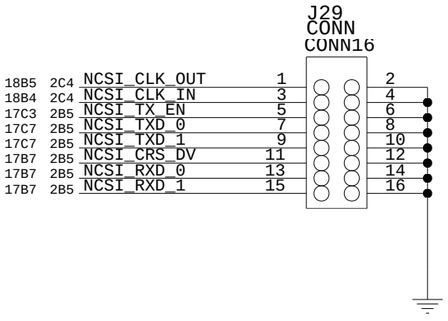












TEST INTERFACE IS NOT REQUIRED IN A NORMAL DESIGN

INTEL CONFIDENTIAL

UNKNOWN

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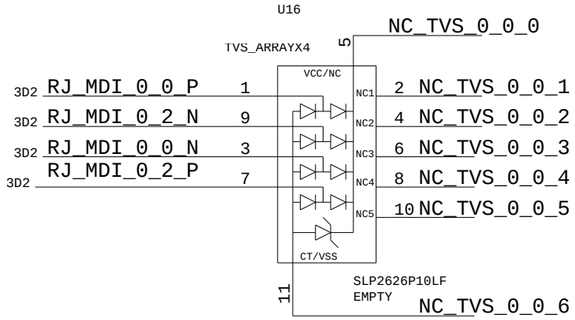
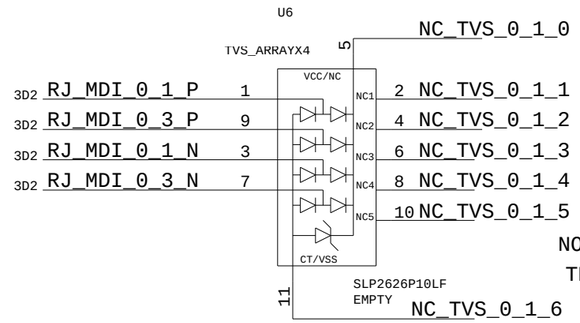
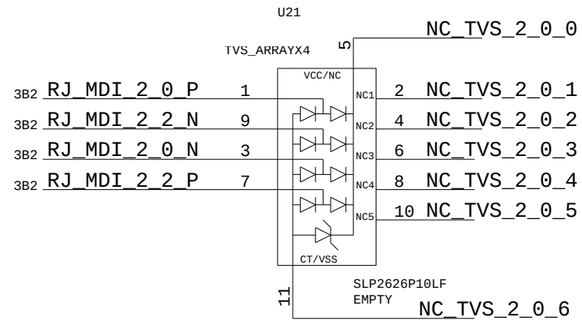
MDI TVS DIODES

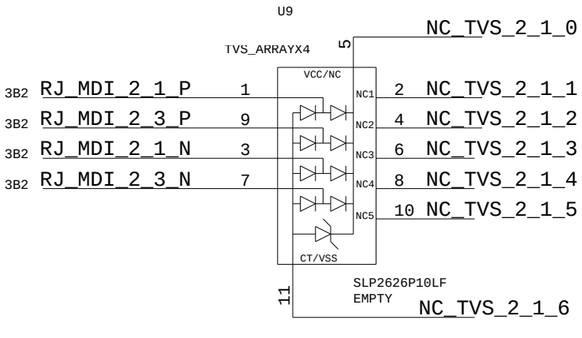
THESE DIODES ARE NOT REQUIRED IN MOST DESIGNS.
THEY ARE ONLY REQUIRED IN DESIGNS
WITH HIGH RISK FOR TRIBOELECTRIC CHARGING
SOME MOBILE DESIGN MIGHT REQUIRE THESE DIODES.

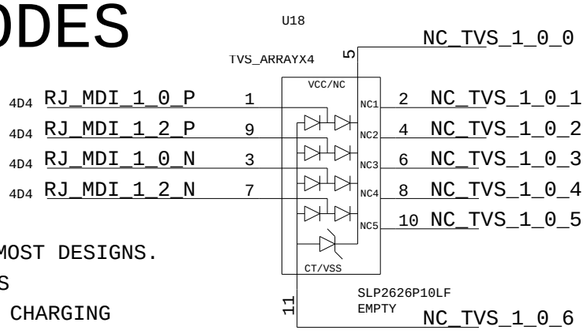
NOTE THAT THE PAIRS ARE GROUPED 1 WITH 3 AND 0 WITH 2.
THIS IS TO PREVENT A PROBLEM WITH POWER-OVER-ETHERNET
IMPLEMENTATIONS

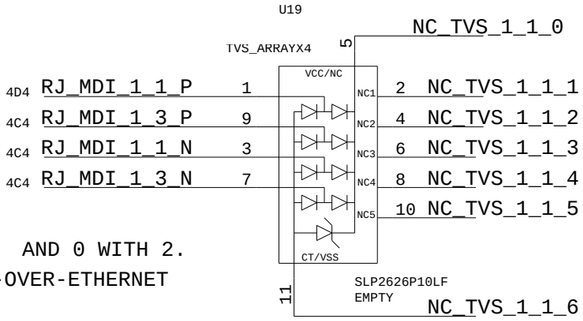


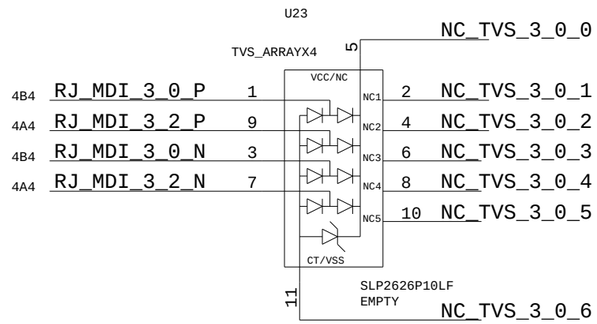


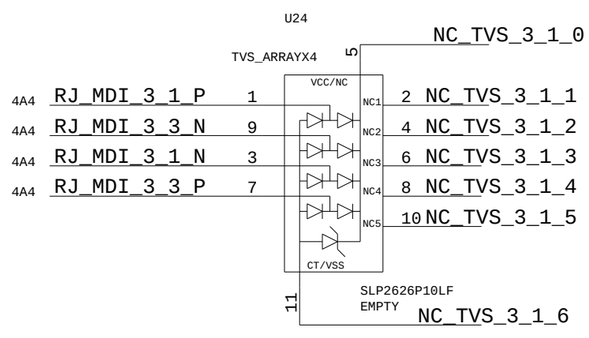












UNKNOWN

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