intel®

AP-522

APPLICATION NOTE

Implementation Guidelines for 3.3V Pentium® Processors with VRE Specifications

for Desktop and Server Designs

June 1997

Order Number: 242687-003

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect IL 60056-7641

or call 1-800-879-4683
or visit Intel's website at http:\\www.intel.com

CONTENTS

1.0. INTRODUCTION

In addition to standard 3.3V Pentium® processors, Intel is offering 3.3V Pentium processors with VRE specifications to enable quicker time-to-market cycles, and higher-performance desktop and server systems. This document will explain the voltage specifications, recommend solutions for supplying consistent power, and suggest validation techniques to ensure robust 3.3V Pentium processor-based desktop or server systems. VRE (Voltage Regulated Extension) components have stricter supply voltage specifications than standard components, and as such VRE-based designs bring additional challenges to power regulation. Although this document focuses on VRE designs, the system design and voltage measurement concepts also apply to designs for standard components.

This document contains five key sections:

Chapter 2.0 discusses the standard and VRE specifications. The VRE and standard voltage ranges have been adjusted for the C2-step and all subsequent processors. These changes are reflected in the chapter (and the entire document). Chapter 2.0 also gives an overview of some important system design and voltage measurement considerations associated with VRE components. The consequences of specification violations are also discussed.

Chapter 3.0 deals with the power supply and regulation. It contains power implementation recommendations to ensure a robust system design. In addition, this chapter contains detailed low cost bulk and high speed decoupling recommendations for Socket 5, Socket 7, and standard 3.3V designs.

Chapter 4.0 explains the proper measurement techniques to verify that systems meet their respective voltage specifications. These measurement techniques apply to all Pentium processors. Measurement results from the *Pentium® Processor Flexible Motherboard Reference Design* are shown in this chapter.

Appendices A and B provide information about tools to assist in both simulating decoupling solutions, and in taking voltage measurements. Specifically, information is provided about obtaining SPICE* source files and simulation results. This section also contains information on how to obtain and use the recommended “stress” code for voltage noise measurement.

Finally, Appendix C provides a list of third party vendors. These vendors include suppliers of regulators, resistors, capacitors, and sockets.

2.0. SPECIFICATIONS

2.1. The VRE Specification

The only difference between the VRE, and standard 3.3V specifications are the voltage supply requirements. Since the VRE specification has a stricter V_{CC} requirement than the standard voltage specification, VRE-based systems are very sensitive to voltage supply noise and transients. Any overshoot or undershoot beyond the voltage range (at a measurement bandwidth of 20MHz) is not permitted. Any transient excursion beyond the specified voltage range may result in unstable system behavior. Note that socket type and measuring techniques are also specified and should be followed to ensure consistent and accurate measurements.

Complete S-Specs, and availability of the Pentium processor family may be found in the latest Pentium processor stepping information or *Pentium® Processor Specification Update* (Order Number 242480).

The complete specifications shown above must be met to ensure a robust VRE-based platform. All measurements must be made and guaranteed at the back of the motherboard at the CPU socket pins. The voltage specifications assume an oscilloscope measurement bandwidth of 20MHz. Socket 5 or Socket 7 (or an equivalent socket of less than 5nH) should be used to ensure upgradability to future Pentium OverDrive® processors and to ensure accurate transient measurements.

Note that standard voltage range encompasses the VRE range, hence standard parts will operate in VRE systems.

2.1.1. The VRE Supply Voltage Range

VRE components allow less transient tolerance than standard components. To compensate for the smaller transient tolerance, VRE-based platforms must use accurate voltage regulators and adequate local decoupling capacitors. During worst-case transient conditions (transition into and out of Stop Grant Mode or Halt Power Down Mode), current supplied to the processor can change by several amperes in tens of nanoseconds (Appendix B provides information about obtaining simulation models for accurately determining current change). Since power supply units and voltage regulators can at best respond in a time frame on the order of milliseconds, bulk decoupling capacitors are required to act as current reservoirs until the power supply unit or voltage regulators regulate to the new load. Due to the high operation speed of the internal core of the Pentium processor, high frequency capacitors are also required to filter the excessive noise components. Failure to provide adequate power regulation during this transition may result in undershoot and overshoot beyond the voltage specifications of the processor.

2.2. Typical Appication Behavior

Poorly designed desktop and server systems will violate VRE specifications during normal operation. An unusual application instruction mix can cause large current spikes from clock cycle to clock cycle. Figure 2 shows the rapid fluctuations of system power during execution of a BAPCo93* benchmark trace (BAPCo93 is a system benchmark used for measuring system performance). These quick transitions in current occur in a shorter time frame than that in which the power supply unit or voltage regulator may be able to respond.

Worst-case transients occur during power management. Figure 3 shows an oscilloscope trace of a system leaving the low-power Stop Grant State (via a deassertion of STPCLK#). The supply voltage "droops" due to ESL and ESR effects (see section 3.4), and because the voltage regulator cannot respond quickly enough to the large, instantaneous change in current. Droops and surges also occur in systems with proper decoupling, but to a lesser extent. The system also has high frequency noise due to high operation speed of the internal core. Figure 3 shows the "droop" due to ESR/ESL effects when exiting the Stop Grant state. The longer term voltage variations (on the order of milliseconds) are not shown in this plot. Violating the VRE specifications by undershooting or overshooting the voltage range will result in unreliable and unstable behavior. The consequences of voltage specification violations are explained in the next section. Chapter 3.0 will recommend techniques for providing accurate regulation and proper decoupling to ensure a robust VRE-based platform.

2.3. Voltage Specification Violations

Overshooting the voltage specification can cause certain signals to violate their Minimum Valid Delay timing specifications. This timing violation will in turn lead to a failure in the system. Excessive and sustained overshooting can also cause hot electron related effects which can compromise the reliability of the part.

Undershooting causes a reduction in the performance of the component, and may also lead to timing related failures. The processor will not function properly at its correct clock frequency. The effects of undershooting are aggravated by improper cooling mechanisms.

Extensive die probing experiments show that high frequency overshooting and undershooting of the voltage specification are filtered by the processor's package parasitics, and are accounted for during the testing of the processor. As a result, the recommended oscilloscope measurement bandwidth has been adjusted to 20MHz (see section 4.2 for details).

Table 1. Comparison of Standard Specifications to VRE Specifications

Specifications	Standard	VRE
V_{CC}	**3.135V[1] to 3.6V** No overshoot or undershoot allowed	**3.4V[2] to 3.6V** No overshoot or undershoot allowed
Timings	Standard and MD	MD only
Thermals	Same Maximum I_{CC} and Maximum Power Dissipation	
Socket	Pentium OverDrive® Processor Upgrade Socket 5 or Socket 7	
Measurement	Transients must be measured and guaranteed at the back of the motherboard at the CPU socket pins. The measurement should be taken with a bandwidth of at least 20MHz (see section 4.2)	

[1]Applies to the C2 stepping, and all subsequent Pentium processors.
[2]Applies to the C2 stepping, and all subsequent Pentium processors with the VRE specification.

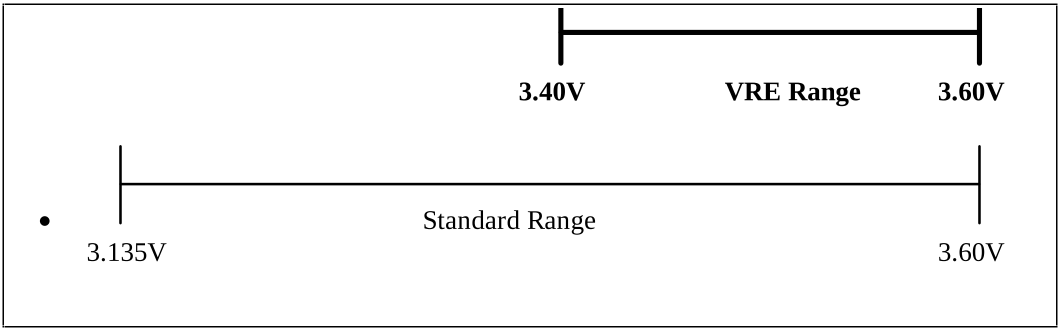

Figure 1. A Comparison of Standard and VRE Specifications

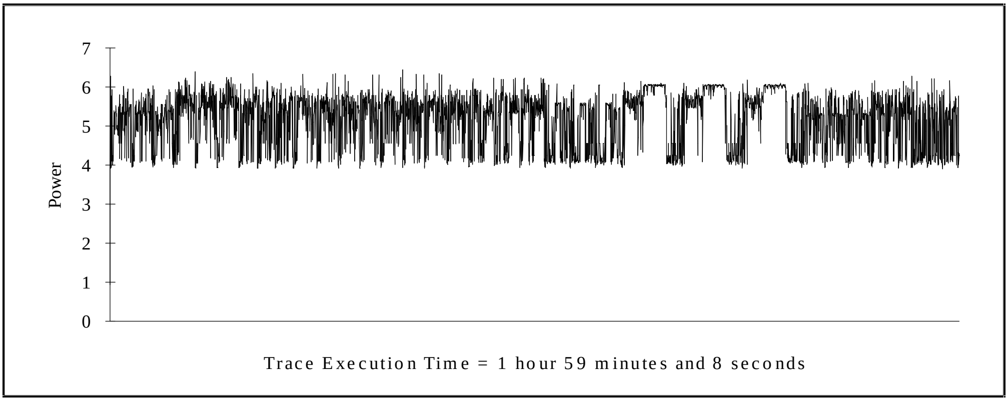

Figure 2. Rapid Fluctuations of System Power While During Active Operation (BAPCo93)

3.0. THE POWER SUPPLY

Until traditional power supply units with 3.3V DC outputs are widely available, supplying power to the 3.3V Pentium processor requires a 5V-to-3.3V voltage regulator. In addition, robust local decoupling must be provided to accommodate the transition to and from low-power modes. It is important to select the components to be as accurate as possible. A platform based on an inaccurate power supply unit must be compensated with a more accurate regulator and extra local decoupling. Similarly, a platform based on an inaccurate regulator requires accurate supporting components and additional decoupling capacitors. As shown next, selecting accurate components will maximize the voltage transient allowed.

VRE Specifications =	Σ Voltage Regulator Accuracy
+	Support Component Accuracy
+	Thermal Drift and Aging Effects
+	**Measured Voltage Transient**

The VRE specification allows a total voltage budget of 200mV. It is important to understand the voltage budget must include any deviation in the voltage regulator, the inaccuracy of its supporting components, and other non-ideal behavior of real components. When designing for a VRE-based platform, these DC factors must be subtracted from

the total VRE budget. The remaining allowance should be targeted when measuring the voltage transient. It is hence important to select accurate voltage regulators and precise support components to allow maximum voltage transients.

3.1. Selecting an Accurate Power Supply Unit

The power supply unit must provide a minimum setpoint equal to, or higher than the minimum input voltage required by the regulator. Off-the-shelf 5V power supply units with a 5% accuracy specification can meet the typical 4.75V requirement of most regulators. However, a 5V power supply unit with an accuracy of 10% may provide a setpoint as low as 4.5V and fail the minimum input requirement. Similarly, an accurate power supply unit may also fail if the voltage regulator has minimum input voltages higher than 4.75V. If using a less accurate power supply unit, the minimum setpoint must be raised to meet or exceed the minimum input voltage required by the voltage regulator. If a voltage regulator requires an input voltage higher than 4.75V, consider choosing a more accurate power supply unit to raise the minimum setpoint.

Sufficient decoupling must be provided between the power supply unit and the voltage regulator to minimize any noise. The disturbance on the 5V power supply unit may exceed the specification of TTL logic devices if the decoupling capacitance is insufficient.

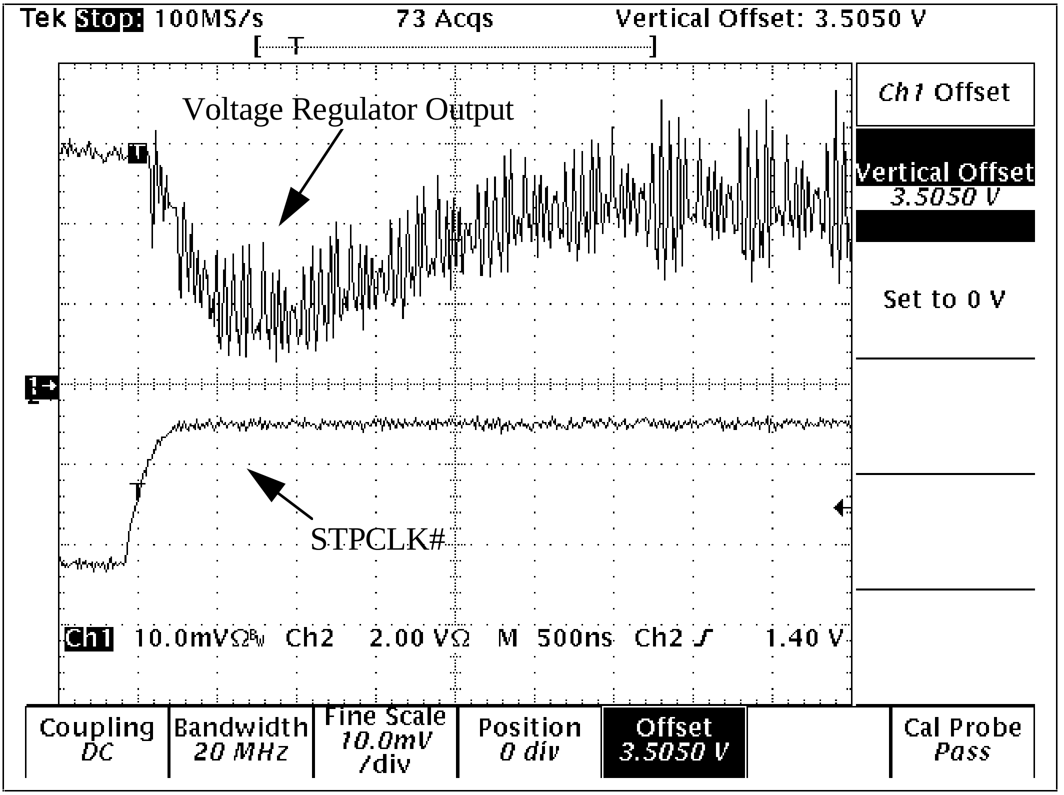

Figure 3. Voltage "Droop" when Exiting Stop Grant State

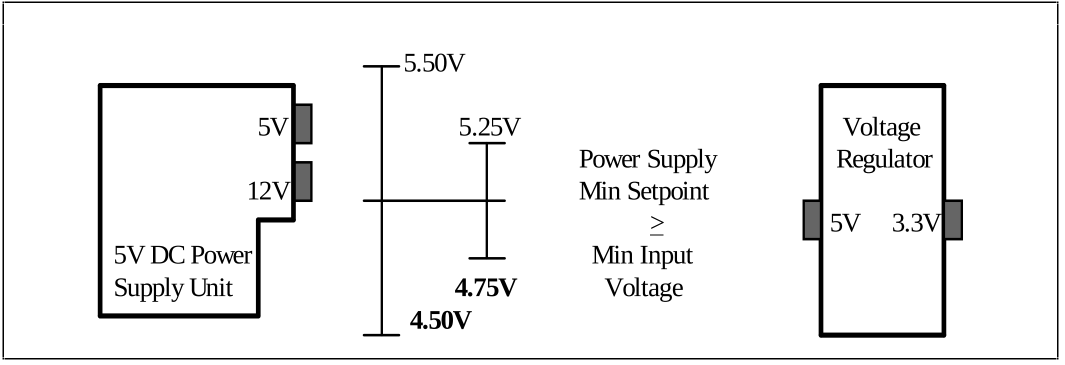

Figure 4. Setpoint Requirement of Power Supply

3.2. Selecting an Accurate Voltage Regulator

There are two types of voltage regulators: switching and linear. Switching regulators provide power by pulsing the voltages and currents to the load, thus resulting in lower heat dissipation and higher efficiency. Switching regulators are however generally more expensive and require more supporting components than linear regulators. Linear regulators essentially are voltage dividers and provide power by "dividing down" the 5V inputs to 3.3V outputs. Linear regulators dissipate more power, but are less expensive and typically require only two additional (feedback) resistors. Unless the system has strict thermal requirements, linear regulators generally are suited for high-volume designs. Both types of regulators can meet the VRE voltage range if they have accurate outputs and precise supporting components. Table 2 below compares the two types of voltage regulators:

An inaccurate regulator leaves little room for transient tolerance. For example, VRE specifications allow a voltage regulator solution to deviate only two percent (3.4V to 3.6V) from the desired regulator setpoint of 3.5V. Static specifications such as line regulation, temperature drift, and the initial setpoint must be held to 1% if any transient is to be permitted at all. Table 3 recommends the voltage regulator module accuracy required to ensure a robust VRE-based platform.

There are direct tradeoffs between the accuracy of the regulator and the amount of local decoupling. Using an inaccurate regulator requires more accurate dividing resistors and more decoupling. Conversely, using high-ESR, quick-aging capacitors necessitates accurate regulators. The next section recommends the bulk and high-speed decoupling required to ensure a robust VRE-based platform. The recommendations were based on extensive simulations and empirical measurements.

Table 2. Comparison of Voltage Regulators

Characteristics (Typical)	Linear Regulator	Switching Regulator
Maximum Efficiency	67%	95%
Maximum Power Dissipation	33%	5%
Supporting Components	2 to 6 (feedback resistors)	5 to 12 (feedback resistors, MOSFET switches, inductor, diode, caps)
Approximate Total Cost	Moderate	Moderately High

Table 3. Recommendations for Linear Voltage Regulator

Parameters	Total Accuracy	Maximum Deviation
Voltage Regulator Setpoint +	± 1 % (VRE)	±35mV (VRE)
Feedback Resistors +	± 2% (STD)	± 66mV (STD)
Thermal Drift, Aging Effects		

3.3. Bulk Decoupling Recommendations

The Pentium processor can be shut down and restarted very quickly with either the STPCLK# signal, or the HALT instruction. Switching the supply current on and off in very short time may cause serious power supply surges and droops in systems with inadequate bulk decoupling. Adequate bulk decoupling capacitors, located between the power and ground planes, near the processor, are necessary to filter these surges and droops. Adequate bulk capacitance is necessary to provide a current reservoir until the regulator can respond to the new load. It is important to use tantalum capacitors to minimize any aging effect. Electrolytic capacitors age faster, are inaccurate and are not stable over a wider temperature range. Capacitors with long leads add inductance and increase transients. Figure 5 shows the bulk decoupling required and a layout example to ensure the effectiveness of bulk decoupling.

Table 4 shows the decoupling recommendations for Socket 5, Socket 7 and standard 3.3V designs. Socket 7 is compatible with Socket 5, and in addition it allows for upgradability to a P6-based processor. Note that the recommendations in Table 4 have already been optimized for cost efficiency.

3.4. High Speed Decoupling Recommendations

Due to its high speed core activity, the Pentium processor generates high frequency noise components and higher current spikes in the power supply. High frequency capacitors between the power and ground planes and near the processor, are required to filter these high frequency noise components. Since the inductive effects of circuit board traces and component leads become more critical at higher frequencies, it is critical to place high frequency capacitors as near as possible to the processor, using short traces to minimize inductance. Surface mount capacitors should be placed inside and around the socket cavity as shown in Figure 6.

The reccomendations shown in Table 4 and Table 5

Table 4. Bulk Decoupling Recommendations for 3.3V Platforms

Design	Qty	Value	Type	Maximum ESR	Maximum ESL
Socket 5	4	100 μF	Tantalum	25 mΩ (100 mΩ/cap)	0.68 nH (2.7 nH/cap)
Socket 7	4	100 μF	Tantalum	25 mΩ (100 mΩ/cap)	0.68 nH (2.7 nH/cap)
Standard (low cost, non -VRE)	4	100 μF	Tantalum	25 mΩ (100 mΩ/cap)	0.68 nH (2.7 nH/cap)

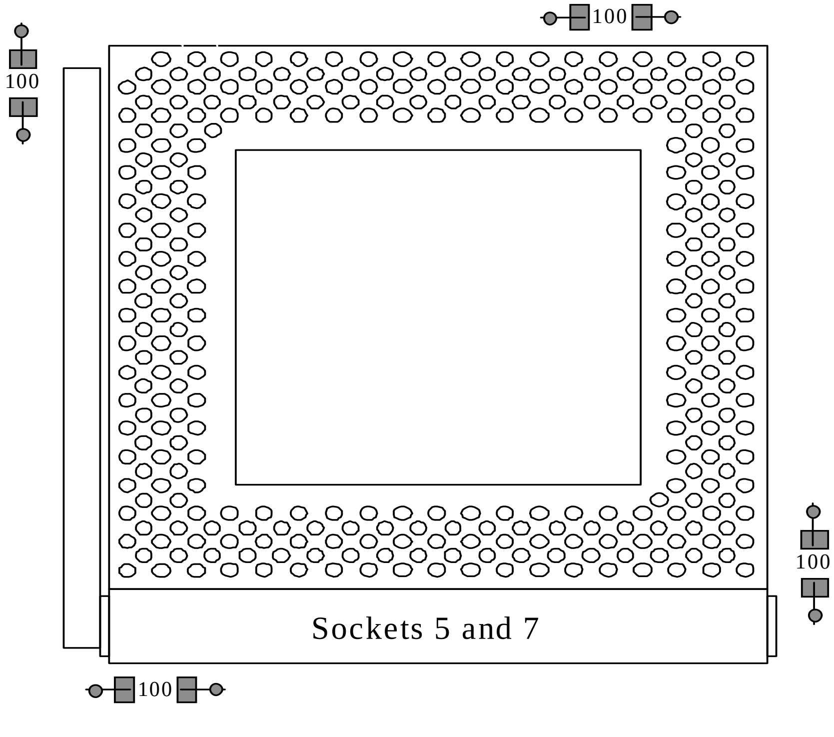

Figure 5. Recommended Bulk Decoupling Capacitor Values and Layout for VRE-based Design

Table 5. High Speed Decoupling Recommendations for 3.3V Platforms

Socket	Qty	Value	Type	Maximum ESR	Maximum ESL
Socket 5	18	1 µF	**X7R/X7S ceramic caps**	**0.83 mΩ** (15 mΩ/cap)	**0.117 nH** (2.1 nH/cap)
Socket 7	25	1 µF	**X7R/X7S ceramic caps**	**0.6 mΩ** (15 mΩ/cap)	**0.084 nH** (2.1 nH/cap)
Standard (Low Cost)	12	1 µF	**X7R/X7S ceramic caps**	**1.25mΩ** (15 mΩ/cap)	**0.175 nH** (2.1 nH/cap)

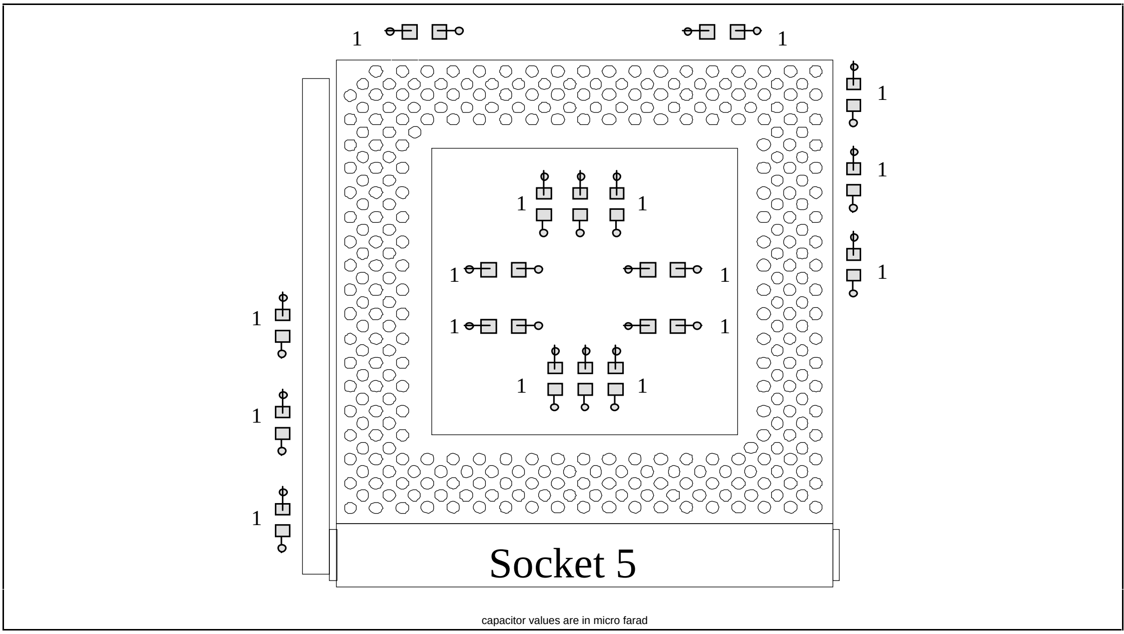

Figure 6. Recommended High Speed Decoupling Capacitors and Layout for VRE-based Unified-Plane Designs

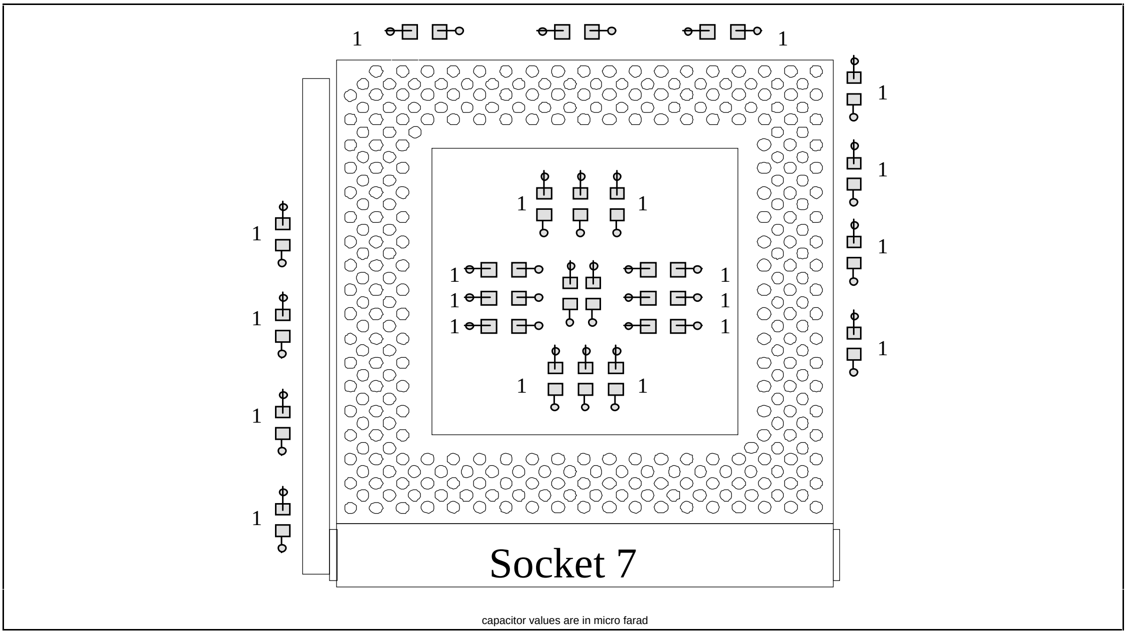

Figure 7. Recommended High Speed Decoupling Capacitors and Layout for VRE-based Unified-Plane Designs

were based on extensive simulations and experiments. They provide a robust, low cost solution to accommodate various Pentium processors and Pentium Overdrive processors. During system design cycles, questions may arise about reducing cost by reducing the amount of decoupling, substituting with different capacitor dielectrics, and using less accurate resistors. Before committing to any deviations from the recommendations, it is highly recommended that the solution be simulated and certified for the variety in components, temperatures, and lifetime degradations. The use of fewer, and / or lower quality decoupling than indicated in this section is discouraged, even if voltage measurements indicate that the margin exists at 20MHz[1].

Endnotes

1 The product test environment assumes a certain minimum amount of decoupling.

ESR and ESL: Why Less is Better?
Effective Series Resistance (ESR) and Effective Series Inductance (ESL) are elements of non-ideal behavior of real components. The ESR and ESL determine how quickly a capacitor can source current to regulate a new load. More importantly, the ESR must be low enough at high frequencies to not offset the desired filtering effects of bulk decoupling capacitors. For a given current transient, the voltage transient is proportional to the ESL and ESR. The use of capacitors with high ESR and ESL hence contributes to higher voltage transients and may cause overshooting or undershooting. Aluminum electrolytic capacitors degrade at a relatively low frequency. Low ESR tantalum caps can retain ESR specifications up to about 1-10 MHz. Low ESR ceramic capacitors can retain ESR specifications up to 100MHz. Do not reduce the quantity of capacitors shown in Table 4 and Table 5 if substituting with capacitors with a larger value. When placed in parallel, two 220µF tantalum capacitors may have higher ESR than four 100 µF capacitors. Placing capacitors in parallel reduces the maximum overall ESR. The maximum overall ESR specifications listed in Table 4 are the same for capacitors with values of 100µF, 220µF, and 330µF.

3.5. Decoupling Recommendations for Split-Plane Designs

A split-plane design using Socket 7 should have all the decoupling capacitors recommended for Socket 7 (in Tables 4 and 5) placed on the core power plane. In addition 12 capacitors, each with a value of 0.1µF, should be used to decouple the I/O power plane.

4.0. TAKING VOLTAGE MEASUREMENTS

4.1. Creating Worst-Case Transient Excursion

The recommendations for regulators and local decoupling can be validated by creating worst-case supply transient conditions and measuring accurately. Worst-case transients may be generated by executing the “stress” program on a Pentium processor test sample (refer to Appendix A for directions on obtaining test samples and the “stress” program). The table below explain the steps to create the worst-case transient conditions

It is necessary to assert and deassert the STPCLK# signal while executing the “stress” program to create the worst-case transient conditions. Asserting the STPCLK# signal will place the processor into the Stop Grant mode (consuming about 15% of active current). Deasserting the STPCLK# signal will return the processor to the Normal state. To simulate actual system behavior, V_{CC} should be stabilized before asserting or deasserting STPCLK# as shown below. Asserting and deasserting STPCLK# too rapidly may generate unrealistic voltage transients. There are no minimum time specifications required to stabilize V_{CC} since the estimated time is highly dependent on the system (length of current instruction, outstanding write cycles, response time of voltage regulator, and accuracy and quantity of decoupling). However, based on experiments from the Pentium Processor Flexible Motherboard Reference Design, STPCLK# should be asserted and deasserted at a rate of 10-100KHz. As part of their power saving features, certain BIOS are able to assert/deassert STPCLK# during execution of a batch file (such as described in Table 6).

Table 6. Directions to Generate Worst-Case Transient

Step One	A	Install Pentium® processor
Step Two	B	Insert diskette containing the "stress" program
Step Three	C	Copy "STR4Y.EXE" to the C drive
Step Four	D	Create a batch file with an infinite loop that executes "STRY4.EXE" once in every loop. See Appendix A.
Step Five	E	Run the batch file created in step four.
Step Six	F	Measure V_{CC} and set oscilloscope as shown in Table 8 to obtain the voltage transient. The voltage transient must not overshoot 3.6V, or dip lower than 3.4V fo VRE systems.
Step Seven	G	Assert and deassert STPCLK# while the "stress" program is executing.

Table 7. Measurement Technique Summary

Measurement Bandwidth[1]	≥ 20 MHz
Probe Bandwidth	≥ 250 MHz
Board Location	At the back of the board, at Socket pins
Pin Locations	12 Pins (listed above)

[1] Signals should be attenuated by no more than 3dB at 20MHz, and 6dB at 40MHz.

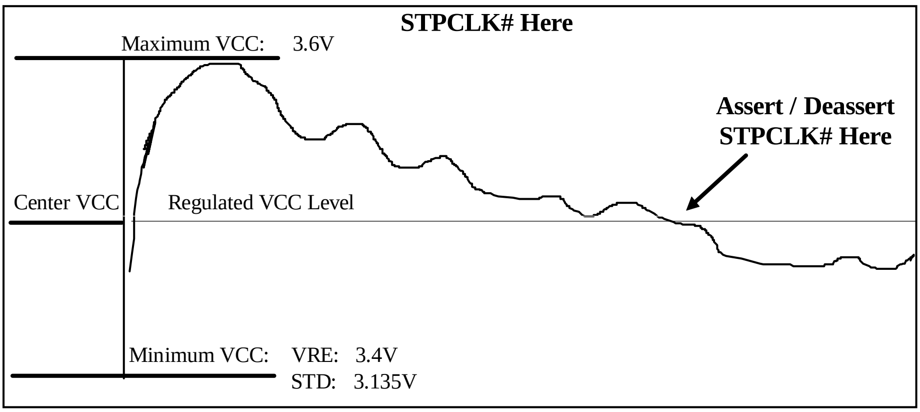

Figure 8. Method for Generating Worst-Case Transient via STPCLK#

4.2. Measurement Technique

All transient measurements must be taken at the back of the motherboard at the socket pins on an iPSL-certified Socket 5, Socket 7, or an equivalent socket of 5nH or less. Measuring transients on an unspecified socket or at a different location will result in inaccurate readings. For accurate readings, all probe connections must be clean. Shorten the ground lead of the probe to minimize any extra inductance. A specially-made probe as shown in Figure 9A will ensure accurate readings by connecting the probe tip directly to the V_{SS} signal and connecting four standoffs to the V_{SS} plane. Figure 9B proposes an alternate solution by providing a short loop of wire around the ground shield of the probe. Figure 9C is not a good example of how to perform measurements. The ground cable of the probe will add significant noise to the transient measurements.

The following V_{CC}/V_{SS} pairs should be measured, and must all meet the voltage specification: AN13/AM10, AN21/AM18, AN29/AM26, AC37/Z36, U37/R36, L37/H36, A25/B28, A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2. These pins are a subset of all V_{CC}/V_{SS} pairs, and hence should not be singled out when placing decoupling capacitors.

The scope settings shown in Table 8 are recommended for accurate measurements. Although the measurement bandwidth of the scope should be set at 20MHz, a probe with a bandwidth of at least 250MHz should be used. This high bandwidth probe ensures a total effective bandwidth of 20MHz. The trigger point should be set in the middle of the range and slowly moved to both the high and low ends of the VRE range.

Table 8. Recommended Oscilloscope Configurations to Capture Voltage Transient

Bandwidth[1]	20 MHz[2]
Sampling Rate	≥ 100 Million Samples / Second
Vertical Reading	≤ 20 mV/division
Horizontal Reading	≥ 500 nS/division
Display	Infinite Persistence

[1] Signals should be attenuated by no more than 3dB at 20MHz, and 6dB at 40MHz.

[2] A probe with a bandwidth of at least 250MHz should be used.

4.3. Measurement Results

The voltage transient measurement shown in Figure 10 was taken on the Pentium Processor Flexible Motherboard Reference Design (FMB) using the technique shown in Figure 9B. The Pentium Processor FMB is an actual motherboard designed to accommodate various Pentium Processors and Pentium OverDrive processors, regardless of specifications. The Pentium Processor FMB ensures accurate voltage regulation and proper decoupling through the Voltage Regulator Module (VRM), a small add-on module. To allow maximum flexibility, a variety of VRM models are available to accommodate all voltage specifications on the Pentium processors. For more detailed specifications of the Pentium Processor FMB or VRM, please refer to the *Pentium® Processor Flexible Motherboard Design Guidelines*, Revision 2.0 (Reference Number SC-0990).

Figure 10 shows the Pentium processor exiting the Stop Grant Mode. Measurements were taken with a Tektronix TDS-684A oscilloscope and P6245 probe, while running the "stress" program with STPCLK# toggling to potentially create worst case transients. STPCLK# was also used to trigger the measurement. The platform used a VRE Spec VRM.

The VRE specification can tolerate voltage transients from 3.4V to 3.6V. The available tolerance of 200mV allows for voltage deviations due to transients and for VRM setpoint accuracy. VRM setpoint accuracy refers to the range in which the VRM maintains the output voltage (i.e. DC offset, noise, regulation tolerance including reference resistor tolerance under line and temperature variations). In this case, the setpoint accuracy is 70mV. The maximum voltage transients measured was about 58mV. This demonstrates that the Pentium Processor Flexible Motherboard Reference Design meets the VRE voltage specification. It is important to note that the VRM and motherboard decoupling should allow for the main processor or Pentium OverDrive processor with the worst case current ramp.

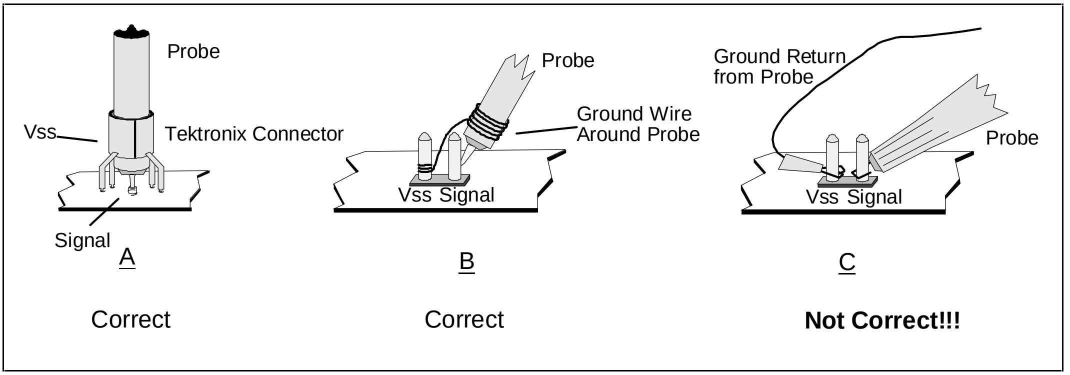

Figure 9. Correct and Incorrect Probe Connections for Measuring Transient

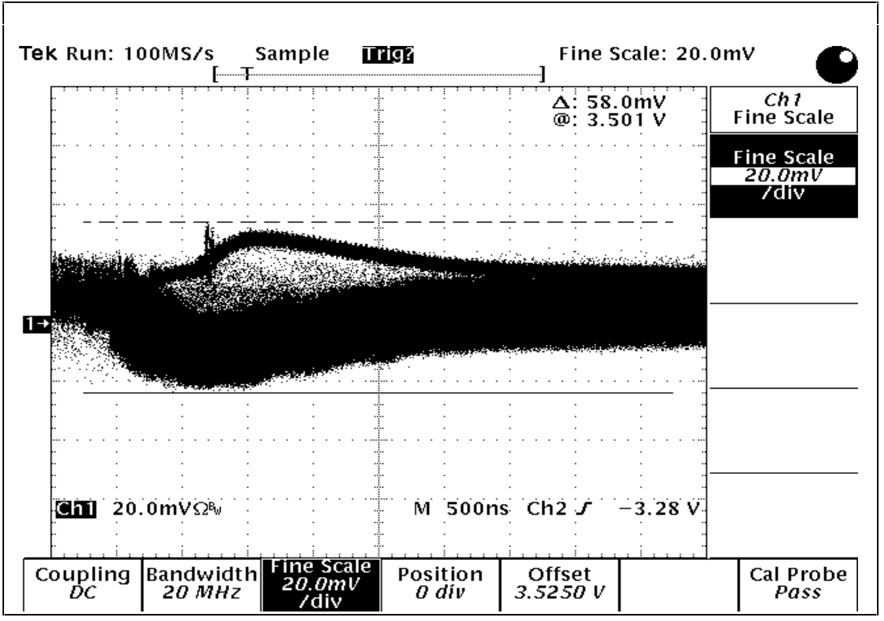

Figure 10. Transient Measurements with VRE Spec VRM

Appendix A: Test Samples and "Stress" Code

The "stress" program and may be obtained through a local Intel Field Sales representative or by calling Intel Technical Support at 1-800-628-8686. Intel Field Sales representa-tives may obtain the stress program from Sales Library Database (Technical Documents).

After the "stress" program has been obtained and installed on the C drive, a batch file should be written to run an infinite loop. The following is an example. The file is called STRESS.BAT:

```
:loop

STRY4.exe

echo on

goto loop
```

At the DOS* prompt, type STRESS and take measurements as explained in Chapter 4.0.

Appendix B: SPICE Models for Transient Simulations

OEMs with modeling capabilities may use a SPICE model to simulate voltage and current transient responses. Circuit models and SPICE Files that model the die, package, and sockets of future Pentium processors are being developed. These models may be obtained under the terms of a Non-Disclosure Agreement through a local Intel Field Sales representative.

Appendix C: Third Party Components

The following vendors offer various solutions to ensure a robust VRE-based platform. Please contact the following vendors for specifications, samples, and design support.

Table 9. Voltage Regulator Modules

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Linear Tech	Bob Scott Tel: (408) 432-1900 Fax: (408) 434-0507	Fred Killinger Tel: (49) 89-3197410 Fax: (49) 89-3194821	Dick Collins Tel: (65) 293-5322 Fax: (65) 292-0398	
Maxim/ Ambit[1]	David Timm (Maxim) Tel: (408) 737-7600 Fax: (408) 737-7194		Jacob Huang (Ambit) Tel: 886 35-784975 Fax: 886-35-775100	David Timm (Maxim) Tel: (408) 737-7600 Fax: (408) 737-7194
Power Trends[1]	Phil Lulewicz Tel: (708) 406-0900 Fax: (708) 406-0901		Joe Ywli Tel: (408) 737-7600 Fax: (408) 737-7194	Ken Katsumoto Tel: (81) 3-5367-9000 Fax: (81) 3-5467-0777
Semtech[1]	Art Fury Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-630350 Fax: (44) 592-774781	Art Fury Tel: (805) 498-2111 Fax: (805) 498-3804	
Siliconix	Howard Chen Tel: (408) 970-4151 Fax: (408) 970-3910	Eric Williams Tel: (44) 344-485757 Fax: (44) 344-427371	Howard Chen Tel: (408) 970-4151 Fax: (408) 970-3910	Tony Grizelj Tel: (81) 3-5562-3321 Fax: (81) 3-5562-3316

[1] DP VRM available

Table 10. Socket 7

Vendor	North America	Europe	APAC	Japan
Amp	Jim Crompton Tel: (910) 855-2338 Fax: (910) 855-2224	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Appros	Tony Goulart Tel: (415) 548-1636 Fax: (415) 548-1124		Appros Taiwan Inc. Tel: (886) 2-718-4774 Fax: (886) 2-718-4344	Appros Inc. Tel: (03) 3358-4857 Fax: (03) 3358-5734
Augat	David M. Barnum Tel: (508) 699-9890 Fax: (508) 695-8111	Arif Shahab Tel: (44) 952-670-281 Fax: (44) 952-670-342	Atsushi Sasaki Tel: (81) 44-853-5400 Fax: (81) 44-853-1113	
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Ronny Chiou or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Yamaichi	Ann Sheperd Tel: (408) 456-0797 Fax: (408) 456-0779	Mr. Matsuda Tel: (49) 89-451021-43 Fax: (49) 89-451021-10	Alan Liu Tel: (886) 02-546-0507 Fax: (886) 02-546-0509	Mr. Shiwaku Tel: (81) 3-3778-616 Fax: (81) 3-3778-618

Table 11. Decoupling Capacitors

Vendor	Part No.	Type	North America	APAC
AVX	1206YZ105KAT1A	1µF, X7S	Dennis Lieberman Tel: (803) 946-0616 Fax: (803) 448-2606	Singapore Steve Chan Tel: (65) 258-2833 Fax: (65) 258-8221
	TPSD107K010R0100	100µF, Tantalum		Korea K.J. Kim Tel: (82) 2-785-6504 Fax: (82) 2-784-5411
Johanson Dielectrics	160R18W105K4	1µF, X7R	Sales Department Tel: (818) 364-9800 Fax: (818) 364-6100	Taiwan Nanco Electronics Bill Yu Tel: (886) 2-758-4650 Fax: (886) 2-729-4209 Hong Kong Tel: (852) 765-3029 Fax: (852) 330-2560
KEMET Electronics	T495X107K010AS	100µF, Tantalum	Richey-Cypress Electronics Tel: (408) 956-8010 Fax: (408) 956-8245	Internation Accounts Warren Marshall Tel: (800) 421-7258 Fax: (714) 895-0060
Murata Electronics	GRM40X7R105J016	1µF, X7R	Sales Department Tel: (404) 436-1300 Fax: (404) 436-3030	Taiwan Tel: (886) 2-562-4218 Fax: (886) 2-536-6721 Hong Kong Tel: (852) 782-2618 Fax: (852) 782-1545 Korea Tel: (82) 2-730-7605 Fax: (82) 2-739-5483
TDK	CC1206HX7R105K	1 µF, X7R/X7S	Sales Department Tel: (708) 803-6100 Fax: (708) 803-6296	Korea Tel: (82) 2-554-6633 Fax: (82) 2-712-6631 Taiwan Tel: (886) 2-712-5090 Fax: (886) 2-712-3090 Hong Kong Tel: (852) 736-2238 Fax: (852) 736-2108

Table 12. Header 7

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland	Rob Rix	H. Itoh	

	Tel: (717) 780-6045 Fax: (717) 780-7027	Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	Tel: (81) 44-844-8086 Fax: (81) 44-812-3203
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Ronny Chiou or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225

Table 13. Shorting Blocks

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Ronny Chiou or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Molex	Micheal Gits Tel: (708) 527-4801 Fax: (708) 969-1352	(Molex) Tel: (49) 89-413092-0 Fax: (49) 89-401527	(Molex) Tel: (65) 268-6868 Fax: (65) 265-6044	(Molex) Tel: (81) 427-21-5539 Fax: (81) 427-21-5562

Table 14. Resistors

Vendor	Size	Type	Accuracy/ Value	Contact
Beckman	0805	thin	0.1%, 10K-100K ohms	Cathy Whittaker
Industrial		thick	1-5%, 10-1M ohms	(214) 392-7616
	0603	thick	1-5%, 10-1M ohms	
Dale Electronic	0603	thin	0.5%, 10-100K ohms	Gary Bruns
		thick	1%,2%, 10-1M ohms	(402) 371-0080
	0805	thin	0.1%, 100-100K ohms	
Koa Spear	0805	thin	0.1%, 100-100K ohms	T. Yogi
		thick	0.5-5%, 10-1M ohms	(814) 362-5536
Thin Film Technology	1206	thin	0.1%, 100-250K ohms	Thin Film TECH. (607) 625 8445 Regional Sales Managers
			0.5%, 10-250K ohms	Patrick J Lyons ext. 14 All states W. of Mississippi except Texas and S. California
	0805	thin	0.1%, 100-100K ohms	
			0.5%, 10-1M ohms	Mark Porisch ext. 12 Southern U.S. E. of Mississippi including Texas
	0603	thin	0.1%, 100-33K ohms	
			0.5%, 10-330K ohms	Tim Goertzen ext. 13 Northen U.S. E. of Mississippi & Canada
	0402	thin	0.5%, 10-100K ohms	Mike Smith (310) 768-8923 Southern California

UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119
Tel: +1 408 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26
Tel: + 81-29847-8522

FRANCE, Intel Corporation S.A.R.L.
1, Quai de Grenelle, 75015 Paris
Tel: +33 1-45717171

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: +44 1-793-641440

GERMANY, Intel GmbH
Dornacher Strasse 1
85622 Feldkirchen/ Muenchen
Tel: +49 89/99143-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: +852 2844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario M9W 6H8
Tel: +416 675-2438