

Intel® Atom™ PROCESSOR Z6XX SERIES

Datasheet

For the Intel® Atom™ Processors Z600, Z605, Z610, Z612, Z615, Z620, and Z625 on 45-nm Process Technology

May 2011

Revision 001



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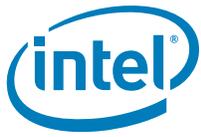
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Revision History

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325567	001	<ul style="list-style-type: none">Initial release	May 2011

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1 Read Me First

1.1 Abstract

The *Intel® Atom™ Processor Z6xx Series Datasheet* describes the architecture, features, buffers, signal descriptions, power management, pin states, operating parameters, and specifications for the Intel® Atom™ processor Z6xx series.

1.2 Audience

The *Intel® Atom™ Processor Z6xx Series Datasheet* is intended for use by hardware developers who are designing and manufacturing products using the Intel® Atom™ processor Z6xx series.

1.3 Organization

The *Intel® Atom™ Processor Z6xx Series Datasheet* is composed of seven chapters that describe the Intel® Atom™ processor Z6xx series features, signal descriptions, power architecture, controller operation, and specifications. The datasheet is organized as follows;

- Chapter 1—"Read Me First"
- Chapter 2—"Introduction"
- Chapter 3—"Signal Descriptions"
- Chapter 4—"Power Management"
- Chapter 5—"Electrical Specifications"
- Chapter 6—"Thermal Specifications"
- Chapter 7—"Mechanical Package Specifications"

Chapters 2–7 contain a list of chapter contents and may contain a list of important acronyms and a description of the acronyms used in the chapter.

Some chapters also contain an architectural or functional overview that describes the design or operation of the Intel® Atom™ processor Z6xx series.

1.4 Reference Documents

Document	Document Number	Notes
<i>Intel® Platform Controller Hub MP30 Datasheet</i>	325565-001US	1
<i>Intel® 64 and IA-32 Architectures Software Developer's Manuals</i>	http://www.intel.com/products/processor/manuals	

NOTE: ¹Contact your Intel representative for the latest revision and document number when obtaining these reference materials.



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2 Introduction

2.1 Chapter Contents

This chapter contains information about:

- "Acronyms"
- "Intel® Atom™ Processor Z6xx Series Architecture"
- "Intel® Atom™ Processor Z6xx Series Feature Set"
- "Intel® Atom™ Processor Z6xx Series Power Management"
- "External/Industry Standard Interfaces and Specifications"

2.2 Acronyms

Table 2-1 contains a list of acronyms used in this chapter.

Table 2-1. Introduction—Acronyms

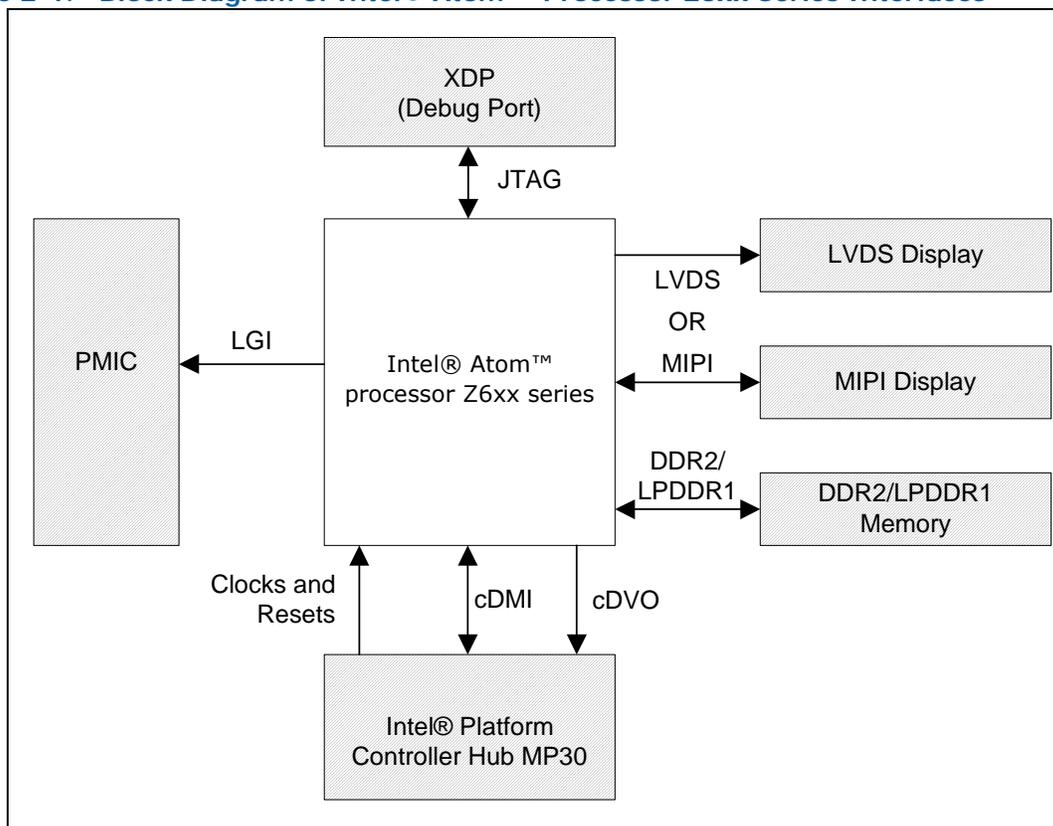
Acronym	Description
ACPI	Advanced Control Programmable Interface
CMOS	Complementary Metal-oxide Semiconductor
cDMI	CMOS Direct Media Interface
cDVO	CMOS Digital Video Output
FSB	Front Side Bus
iFSB	Internal Front Side Bus
Lincroft	Intel® Atom™ Processor Z6xx Series
Langwell	Intel® Platform Controller Hub MP30
LGI	Legacy Interface
LVDS	Low Voltage Differential Signaling, a high speed, low power data transmission standard used for display connections to LCD panels
MIPI	Mobile Industry Processor Interface
MIPI D-PHY	MIPI Physical Layer Device
MIPI-DCS	MIPI Display Command Set
MIPI-DSI	MIPI Display Serial Interface
PCH	Intel® Platform Controller Hub MP30
PMIC	Power Management Integrated Circuit
S0i1	Intel® Smart Idle Technology (Intel® SIT) State 1
S0i3	Intel® Smart Idle Technology (Intel® SIT) State 3
SIT	Intel® Smart Idle Technology (Intel® SIT)
SPT	Intel® Smart Power Technology (Intel® SPT)

2.3 Intel® Atom™ Processor Z6xx Series Architecture

The Intel® Atom™ processor Z6xx series is the next generation low power IA-32 processor that is based on the new re-partitioning architecture targeted for smart phones and tablets. The main components of the Intel® Atom™ processor Z6xx series are: an IA-compatible processor core derived from the Intel® Atom™ Z5xx Processor, a single-channel 32-bit DDR2 or LPDDR1 memory controller, a 3-D graphics engine, video decode and video encode engines, a display controller, a cDMI interface link to the Intel® Platform Controller Hub MP30, an LVDS or embedded MIPI interface to support a primary display interface link, and a cDVO interface link to the Intel® Platform Controller Hub MP30 to support an external display.

Figure 2-1. shows a block diagram of the main external interfaces for the Intel® Atom™ processor Z6xx series.

Figure 2-1. Block Diagram of Intel® Atom™ Processor Z6xx Series Interfaces



2.4 Intel® Atom™ Processor Z6xx Series Feature Set

2.4.1 Intel® Atom™ Processor Z6xx Series Processor Core

- Supports macro-operation execution
- Supports Intel® Hyper-Threading Technology (Intel® HT Technology)
- Supports Enhanced Intel SpeedStep® Technology
- Supports Intel® Burst Performance Technology (Intel® BPT)



- Supports Intel® Smart Idle Technology (Intel® SIT)
- 2-wide instruction decode and in-order execution
- 32KB, 4-way L1 instruction cache
- 24KB, 6-way L1 data cache
- 512KB, 8 way L2 cache
- 32b physical address, 48b linear address size support

2.4.2 Memory Controller

The Intel® Atom™ processor Z6xx series contains an integrated memory controller that supports DDR2 and LPDDR1 memory. The memory controller interface is fully configurable through a set of control registers. The following sections discuss the features of the integrated memory controller.

2.4.3 LPDDR1

- 32-bit data bus
- Supports 400 MT/s only
- Supports total memory size of up to 1GB
- Provides aggressive power management to reduce power consumption when idle
- Provides proactive page closing policies to close unused pages

2.4.4 DDR2

- 32-bit data bus
- Supports 800 MT/s only
- Supports total memory size of up to 2GB
- Provides aggressive power management to reduce power consumption when idle
- Provides proactive page closing policies to close unused pages

2.4.5 Intel® Graphics Media Accelerator 600 (Intel® GMA 600) Graphics

2.4.5.1 3-D Graphics/Video Decode/Video Encode

- Up to 400 MHz graphics core frequency
- Supports OpenGL* ES1.1
- Supports OpenGL* ES2.0
- Supports OpenGL* 2.1
- Supports OpenVG* 1.1
- Supports hardware-accelerated HD video decode (MPEG4 part 2, H.264, WMV, and VC1)
- Supports hardware-accelerated HD video encode (MPEG4 part 2 and H.264)



2.4.5.2 Display Controller

- Seven display planes: Display Plane A, Display Plane B, Display C/sprite, Overlay, Cursor A, Cursor B, and VGA
- Display Pipe A: Supports LVDS or MIPI display interface
- Display Pipe B: cDVO pixel data link to the Intel® Platform Controller Hub MP30 to support HDMI
- Supports 18 bpp and 24 bpp
- Supports Non-Power of 2 Tiling
- Output pixel width: 24-bit RGB
- Supports NV12 video data format
- Supports 3 x 3 panel fitter
- Dynamic Power Saving Technology (DPST) 3.0
- Support 16 x 256 byte tile size
- Supports overlay
- Supports global constant alpha blending

2.4.5.3 MIPI-DSI

- Maximum resolution (internal display) of up to 1024 x 600
- Supports 1 or 2 lane operation
- Supports lane double data rates up to 400 Mbps in high speed (HS) mode
- Supports 24 bpp, 18 bpp packed and 18 bpp loosely packed pixel formats
- Display Pixel Interface (DPI) for video-mode displays
- Supports bi-directional low power (LP) mode on Lane 0 for display-to-host communications
- Supports ECC in both directions

2.4.5.4 LVDS

- Maximum resolution (internal display) of up to 1366 x 768
- Dot clock range from 20–83 MHz
- Five differential signal pairs—Four data pairs (up to 581 Mbps on each data link) and one clock pair
- Supports 24 bpp, 18 bpp packed, and 18 bpp loosely packed pixel formats

2.4.6 cDMI

- The data interface between the Intel® Atom™ processor Z6xx series and the Intel® Platform Controller Hub MP30
- Peak raw BW of cDMI link per direction is 400 MT/s using a quad-pumped, 8-bit transmit and an 8-bit receive data bus
- Supports low power management schemes
- Supports CMOS signaling technology



2.4.7 cDVO

- The unidirectional display data link interface from the Intel® Atom™ processor Z6xx series to the Intel® Platform Controller Hub MP30
- Peak raw BW of cDVO is 400 MT/s for Intel® Atom™ Processors Z600, Z610, Z612, and Z620 and 800 MT/s for Intel® Atom™ Processors Z605, Z615, and Z625 using a quad-pumped, 6-bit transmit data bus
- Supports low power management schemes
- Supports CMOS signaling technology for Intel® Atom™ Processors Z600, Z610, Z612, and Z620 and AGTL+ signaling technology for Intel® Atom™ processors Z605, Z615, and Z625

2.4.8 LGI/LGIE/Debug

- Thermal sensing
- Legacy control signals
- JTAG debug port

2.5 Intel® Atom™ Processor Z6xx Series Power Management

The Intel® Atom™ processor Z6xx series supports fine grain power management by having several partitions of voltage islands created through on-die power switches. The Intel® Smart Power Technology (Intel® SPT) software determines the most power efficient state for the platform at any given point in time and then provides guidance to turn ON or OFF different voltage islands on the processor. For the scenario where Intel® SPT has directed the processor to go into an Intel® SIT idle mode, the processor waits for all partitions with shared voltage to reach a safe point and then turns them off.

2.5.1 Intel® Burst Performance Technology (Intel® BPT)

The Intel® Atom™ processor Z6xx series processor core supports ACPI Performance States (P-states). The P-state referred to as P0 will be a request for Intel® Burst Performance Technology (Intel® BPT). Intel® BPT opportunistically and automatically, allows the processor to run faster than the marked frequency if the part is operating within the thermal design limits of the platform. Intel® BPT can be enabled or disabled by IA-32 firmware.

2.5.2 Intel® Smart Idle Technology (Intel® SIT)

The Intel® Atom™ processor Z6xx series is targeted to deliver always on, always connected, standby power with the use of Intel® Smart Idle Technology (Intel® SIT). Intel® SIT enables the processor to enter its lowest supported idle power states, S0i1 and S0i3, which greatly increases system standby time. The OS manages entry and exit of S0i1 and S0i3 power states through the Intel® SPT.



2.6 External/Industry Standard Interfaces and Specifications

The Intel® Atom™ processor Z6xx series adheres to the following external specifications:

- JEDEC JESD79-2E (DDR2)
- JEDEC JESD209 (LPDDR1)
- TIA/EIA-644A (LVDS)
- MIPI DPHY, Revision 0.9
- MIPI DSI, Revision 1.01.00, Release 09
- MIPI DCS, Revision 1.01.00, June 2006

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3 Signal Descriptions

3.1 Chapter Contents

This chapter contains information about:

- "Acronyms"
- "Buffer Types"
- "Signal Description"

3.2 Acronyms

Table 3-1 below contains a list of acronyms used in this chapter.

Table 3-1. Signal Descriptions—Acronyms

Acronym	Description
ACPI	Advanced Control Programmable Interface
AGTL+	Assisted Gunning Transceiver Logic Plus
CKE	Clock Enable
DQ	Memory data
DQS	Memory data strobe
GPIO	General Purpose Input/Output
HPLL	Host Phase Lock Loop
IERR	Internal Error
PCH	Intel® Platform Controller Hub MP30
LP Mode	Low Power Mode
NMI	Non-Maskable Interrupt
PMIC	Power Management Integrated Circuit
SCK	System Clock
TAP	Test Access Point

3.3 Buffer Types

Table 3-2. Buffer Types

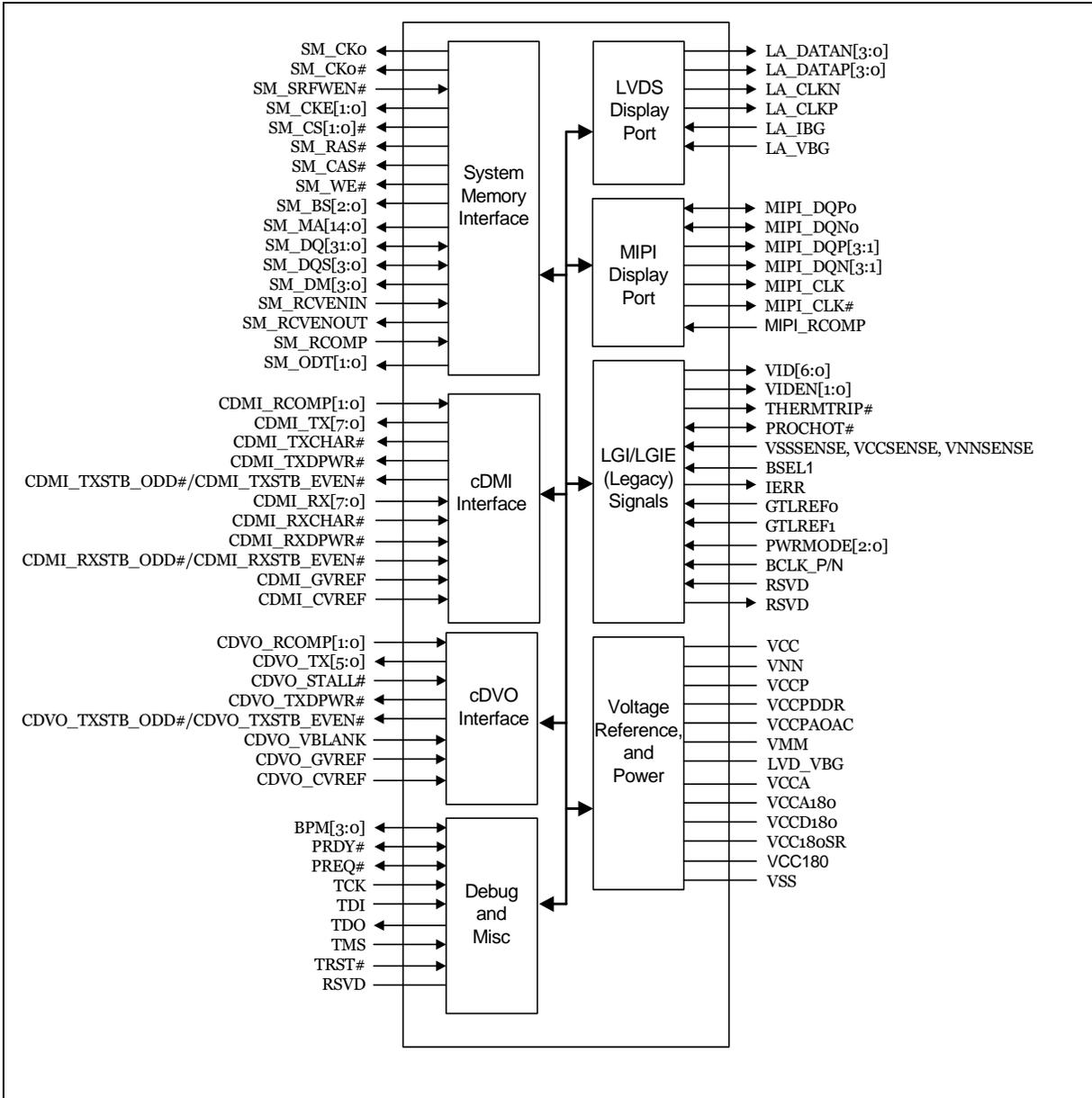
Buffer Type	Interface	Description
AGTL+	cDVO	Assisted Gunning Transceiver Logic Plus: CMOS open drain interface signals that require termination.
CMOS, CMOS_OD	cDMI, cDVO, LGI, LGIE	1.05V CMOS buffer or CMOS open drain
Analog	All	Analog reference or output: This may be used as a threshold voltage or for buffer compensation.
MIPI	MIPI	MIPI buffers: Support HSTX, LPTX, and LPRX modes.
LVDS	LVDS	Low-Voltage Differential Signal output buffers: These should drive across a 100-Ω resistor at the receiver.
CMOS1.8	DDR2/LPDDR1	1.8V CMOS buffer: These buffers can be configured as Stub Series Termination Logic.
F	Power Signals	Fixed: The voltage level is fixed to be a certain value based on the I/O family.
AON	Power Signals	Always ON: The voltage level must always be on for the component to operate safely, reliably, and deterministically.
S	Power Signals	Selectable: The voltage can be selected at the platform level.
V	Power Signals	Variable: Variable supplies are negotiable supply levels.

3.4 Signal Description

This section provides a detailed description of the Intel® Atom™ processor Z6xx series signals. The signals are arranged in functional groups according to their associated interface (see [Figure 3-1](#)).



Figure 3-1. Interface Signal Diagram





3.4.1 System Memory Interface

Table 3-3. System Memory Interface Signals (Sheet 1 of 2)

Signal	Direction Type	Power Rail	Description
SM_ODT[1:0]	O CMOS1.8	V _{CC180}	On-Die termination enable: Enables the use of on-die termination on the DDRIO and memory devices for data and strobes when asserted. When the ODT feature is enabled, ODT is dynamically enabled for the receiver of the data. The processor does this internally for read data returning from the DRAM devices. For write data to the DRAM devices, the SM_ODT[1:0] pins are asserted to enable ODT within the DRAM devices themselves. For dual rank memory configurations using x8 devices, ODT must be enabled.
SM_CK0	O CMOS1.8	V _{CC180}	Differential DDR clock: The crossing of the positive edge of SM_CK0 and the negative edge of SM_CK0# is used to sample the address and control signals on memory.
SM_CK0#	O CMOS1.8	V _{CC180}	Complementary differential DDR clock
SM_SREN#	I CMOS1.8	V _{CC180S} _R	S0i3 self-refresh enable: Signal from the Intel® Platform Controller Hub MP30 asserted after the processor places DDR in self-refresh and sends an acknowledgement of S0i3 to the Intel® Platform Controller Hub MP30.
SM_CKE[1:0]	O CMOS1.8	V _{CC180S} _R	Clock enable: SM_CKE is used for power control of the DRAM devices. There is one SM_CKE per rank.
SM_CS[1:0]#	O CMOS1.8	V _{CC180}	Chip select: These signals determine whether a command is valid in a given cycle for the devices connected to it. There is one chip select signal for each rank.
SM_RAS#	O CMOS1.8	V _{CC180}	Row address strobe: This signal is used with SM_CAS# and SM_WE# (along with SM_CS#) to define commands.
SM_CAS#	O CMOS1.8	V _{CC180}	Column address strobe: This signal is used with SM_WE#, SM_RAS#, and SM_CS# to define commands.
SM_WE#	O CMOS1.8	V _{CC180}	Write enable: This signal is used with SM_CAS#, SM_RAS#, and SM_CS# to define commands.
SM_BS[2:0]	O CMOS1.8	V _{CC180}	Bank select: These signals define which banks are being addressed within each Rank.
SM_MA[14:0]	O CMOS1.8	V _{CC180}	Multiplexed address: SM_MA signals provide multiplexed row and column address to memory.
SM_DQ[31:0]	I/O CMOS1.8	V _{CC180}	Data lines: SM_DQ signals interface to the DRAM data bus.



Table 3-3. System Memory Interface Signals (Sheet 2 of 2)

Signal	Direction Type	Power Rail	Description
SM_DQS[3:0]	I/O CMOS1.8	V _{CC180}	Data strobes: These signals are used during writes and are centered with respect to data. During read, these signals are driven by memory devices and are edge aligned with data. The following list matches the data strobe with the data bytes. SM_DQS3 -> SM_DQ[31:24] SM_DQS2 -> SM_DQ[23:16] SM_DQS1 -> SM_DQ[15:8] SM_DQS0 -> SM_DQ[7:0]
SM_DM[3:0]	O CMOS1.8	V _{CC180}	Data mask: One bit per byte indicating which bytes should be written.
SM_RCVENIN	I CMOS1.8	V _{CC180}	Receive enable in: This signal connects to SM_RCVENOUT on the motherboard. This input enables the SM_DQS input buffers during reads.
SM_RCVENOUT	O CMOS1.8	V _{CC180}	Receive enable out: This signal connects to SM_RCVENIN on the motherboard. Part of the feedback used to enable the DQS input buffers during reads.
SM_RCOMP	I Analog	V _{CC180}	RCOMP: This signal connects externally to a high-precision reference resistor on the board to dynamically calibrate the driver strengths.



3.4.2 cDMI Interface

Table 3-4. cDMI Interface Signals

Signal	Direction Type	Power Rail	Description
CDMI_RCOMP[1:0]	I Analog	V _{CCP}	CDMI_RCOMP: Connected to high-precision resistors on the motherboard. Used for compensating DMI pull-up/pull-down impedances.
CDMI_TX[7:0]	O CMOS	V _{CCP}	Data output: Quad-pumped (strobed) data bus from the processor to the Intel® Platform Controller Hub MP30.
CDMI_TXCHAR#	O CMOS	V _{CCP}	Data control character data control character output: Quad-pumped (strobed) indication that CDMI_TX[7:0] contains a control character instead of data.
CDMI_TXDPWR#	O CMOS	V _{CCP}	Line wakeup for output: When asserted, the Intel® Platform Controller Hub MP30 will power-up its receivers on CDMI_TX[7:0], CDMI_TXCHAR#, and CDMI_TXSTB[0].
CDMI_TXSTB_ODD#, CDMI_TXSTB_EVEN#	O CMOS	V _{CCP}	Data strobe output: Strobes for CDMI_TX[7:0] and CDMI_TXCHAR#.
CDMI_RX[7:0]	I CMOS	V _{CCP}	Data input: Quad-pumped (strobed) data bus from the Intel® Platform Controller Hub MP30 to the processor.
CDMI_RXCHAR#	I CMOS	V _{CCP}	Data control character input: Quad-pumped (strobed) indication that CDMI_RX[7:0] contains a control character instead of data.
CDMI_RXDPWR#	I CMOS	V _{CCP}	Line wakeup for input: Power enable from the Intel® Platform Controller Hub MP30. Used to enable Receivers on CDMI_RX[7:0], CDMI_RXCHAR#, and CDMI_RXSTB_ODD#.
CDMI_RXSTB_ODD#, CDMI_RXSTB_EVEN#	I CMOS	V _{CCP}	Data strobe input: Strobes for CDMI_RX[7:0] and CDMI_RXCHAR#.
CDMI_GVREF	I Analog	V _{CCP}	Strobe signals reference voltage for CDMI: Externally set by means of a passive voltage divider. Voltage should be 1/2 V _{CCP} when configured for CMOS.
CDMI_CVREF	I Analog	V _{CCP}	Non-strobe signals reference voltage for CDMI: Externally set by means of a passive voltage divider. Voltage should be 1/2 V _{CCP} when configured for CMOS.



3.4.3 cDVO Interface

Table 3-5. cDVO Interface Signals

Signal	Direction Type	Power Rail	Description
CDVO_RCOMP[1:0]	I Analog	V _{CCP}	CDVO_RCOMP: Connected to high-precision resistors on the motherboard. Used for compensating pull-up/pull-down impedances.
CDVO_TX[5:0]	O AGTL+ CMOS	V _{CCP}	Data output: Quad-pumped (strobed) data bus from the processor to the Intel® Platform Controller Hub MP30.
CDVO_STALL#	I AGTL+ CMOS	V _{CCP}	Stall: Allows the Intel® Platform Controller Hub MP30 to throttle the sending of display data.
CDVO_TXDPWR#	O AGTL+ CMOS	V _{CCP}	Line wakeup for output: When asserted, the Intel® Platform Controller Hub MP30 will power-up its receivers on CDVO_TX[5:0] and CDVO_TXSTB_ODD#.
CDVO_TXSTB_ODD#, CDVO_TXSTB_EVEN#	O AGTL+ CMOS	V _{CCP}	Data strobe output: Strobes for CDVO_TX[5:0].
CDVO_VBLANK#	I AGTL+ CMOS	V _{CCP}	Vertical blank: Indication from the Intel® Platform Controller Hub MP30 indicating the start of the vertical blank period.
CDVO_GVREF	I Analog	V _{CCP}	Strobe signals reference voltage for CDVO: Externally set by means of a passive voltage divider. Voltage should be 2/3 V _{CCP} when configured for AGTL+ and 1/2 V _{CCP} when configured for CMOS.
CDVO_CVREF	I Analog	V _{CCP}	Non-strobe signals reference voltage for CDVO: Externally set by means of a passive voltage divider. Voltage should be 2/3 V _{CCP} when configured for AGTL+ and 1/2 V _{CCP} when configured for CMOS.

NOTE: The cDVO interface is configured to support CMOS signaling technology for Intel® Atom™ Processors Z600, Z610, Z612, Z620, and AGTL+ signaling technology for Intel® Atom™ Processors Z605, Z615, and Z625.

3.4.4 LVDS Display Port Interface

Table 3-6. LVDS Display Port Interface Signals

Signal	Direction Type	Power Rail	Description
LA_DATAN[3:0]	O LVDS	V _{CCD180} , V _{CCA180}	Differential data output (Negative)
LA_DATAP[3:0]	O LVDS	V _{CCD180} , V _{CCA180}	Differential data output (Positive)
LA_CLKN	O LVDS	V _{CCD180} , V _{CCA180}	Differential clock output (Negative)
LA_CLKP	O LVDS	V _{CCD180} , V _{CCA180}	Differential clock output (Positive)
LA_IBG	I Analog	V _{CCD180} , V _{CCA180}	External voltage reference BG: Connected to high-precision ($\pm 1\%$) 2.43 K Ω resistor on motherboard to VSS.
LA_VBG	I Analog	V _{CCD180} , V _{CCA180} , LVD_VBG	External voltage reference BG: Requires external 1.25V $\pm 2\%$ supply.

3.4.5 MIPI Display Port Interface

Table 3-7. MIPI Display Port Interface Signals

Signal	Direction	Power Rail	Description
MIPI_DQP0	I/O MIPI	V _{MM}	Data (positive): Differential, bi-directional in LP mode
MIPI_DQN0	I/O MIPI	V _{MM}	Data (negative): Differential, bi-directional in LP mode
MIPI_DQP[3:1]	O MIPI	V _{MM}	Data (positive): Differential output only
MIPI_DQN[3:1]	O MIPI	V _{MM}	Data (negative): Differential output only
MIPI_CLK	O MIPI	V _{MM}	Clock (positive): Differential
MIPI_CLK#	O MIPI	V _{MM}	Clock (negative): Differential
MIPI_RCOMP	I Analog	V _{MM}	RCOMP: Connected to a high-precision resistor on the motherboard. Used for impedance compensation.



3.4.6 LGI/LGIE (Legacy) Interface

Table 3-8. LGI/LGIE Interface Signals (Sheet 1 of 2)

Signal	Direction Type	Power Rail	Description
VID[6:0]	O CMOS	V _{CCP}	Voltage ID: Connects to PMIC. Indicates a desired voltage for either V _{CC} or V _{NN} depending on the VIDEN[1:0] pins. Resolution of 12.5 mV.
VIDEN[1:0]	O CMOS	V _{CCPAOAC}	Voltage ID enable: Connects to PMIC. Indicates which voltage is being specified on the VID pins: 00 = VID is invalid 01 = VID = V _{CC} 10 = VID = V _{NN} 11 = RSVD
THERMTRIP#	O CMOS_OD	V _{CCPAOAC}	Catastrophic thermal trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds the trip point. This condition is signaled to the system by the THERMTRIP# (Thermal Trip) pin.
PROCHOT#	I/O O: CMOS_OD I: CMOS	V _{CCPAOAC}	Processor hot: As an output, PROCHOT# (processor hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#.
VSSSENSE, VCCSENSE, VNNSENSE	I Analog	V _{SS} , V _{CC} , V _{NN}	Voltage sense: Connects to PMIC. Voltage Regulator must connect feedback lines for V _{CC} , V _{SS} , and V _{NN} to these pins on the package.
BSEL1	O CMOS	V _{CCP}	BSEL1: Selects external reference clock for DDR, cDMI, and cDVO frequencies. 1 = Reserved 0 = 100 MHz, for cDMI/cDVO/LPDDR1 at 400 MT/s or cDVO/DDR2 at 800 MT/s.

Table 3-8. LGI/LGIE Interface Signals (Sheet 2 of 2)

Signal	Direction Type	Power Rail	Description
IERR	O CMOS	V _{CCP}	IERR: Internal error indication (debug). Positively asserted. Asserted when the processor has had an internal error and may have unexpectedly stopped executing. Assertion of IERR is usually accompanied by a SHUTDOWN transaction internal to the processor which may result in assertion of Non-Maskable Interrupt (NMI) to the processor. The processor will keep IERR asserted until the PWRMODE[2:0] pins take the processor to reset or the processor receives a reset message over cDMI. PWRMODE[2:0] M0, M1, M2, M3 M5, M7, M6, M4
GTLREF0	I Analog	V _{CCP}	Voltage reference for BPM[3:0]#: 2/3 V _{CCP} by means of an external voltage divider: 1 KΩ to V _{CCP} , 2 KΩ to V _{SS} .
GTLREF1	I Analog	V _{CCP}	Voltage reference: 2/3 V _{CCP} by means of external voltage divider: 1 KΩ to V _{CCP} , 2 KΩ to V _{SS} .
PWRMODE[2:0]	I CMOS	V _{CCPAOAC}	Power mode: The Intel® Platform Controller Hub MP30 is expected to sequence the processor through various states using the PWRMODE[2:0] pins to facilitate cold reset, warm reset, and S0i3 entry and exit.
BCLK_P/N	I CMOS	V _{CCP}	Reference clock: Differential 100 MHz.



3.4.7 Debug and Miscellaneous

Table 3-9. Debug and Miscellaneous Signals

Signal	Direction Type	Power Rail	Description
BPM[3:0]#	I/O AGTL+	V _{CCP}	Break/perf monitor: Various debug input and output functions.
PRDY#	I/O AGTL+	V _{CCP}	Probe mode ready: The processor's response to a PRDY# assertion. This signal indicates that the processor is in probe mode. Input is unused.
PREQ#	I/O AGTL+	V _{CCP}	Probe mode request: Assertion is a request for the processor to enter probe mode. Processor will respond with PRDY# assertion once it has entered. PREQ# can be enabled to cause the processor to break from C4 and C6. Internal 56 Ω pull up.
TCK	I CMOS	V _{CCP}	Processor JTAG test clock: This signal provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I CMOS	V _{CCP}	Processor JTAG test data input: This signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O OD	V _{CCP}	Processor JTAG test data output: This signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TMS	I CMOS	V _{CCP}	Processor JTAG test mode select: A JTAG specification support signal used by debug tools.
TRST#	I CMOS	V _{CCP}	Processor JTAG test reset: Asynchronously resets the Test Access Port (TAP) logic. TRST# must be driven asserted (low) during processor power on reset. The Intel® Atom™ processor Z6xx series has an internal 56 Ω pull-up to V _{CCP} , unlike the Intel® Pentium® M Processor, the Intel® Core™2 Duo Processor, and the Intel® Atom™ Z5xx Processor. The Intel® Atom™ Processor Z6xx pull-up matches the Intel® Pentium® 4 Processor and the IEEE specification.
RSVD			These pins should be treated as no connection (NC).



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4 Power Management

4.1 Chapter Contents

This chapter contains information about:

- "Acronyms"
- "Processor Voltage Rails"
- "Processor Voltage Rail States"
- "VCC/VNN VID Control"
- "Valid Power States"
- "Processor Core Low Power Features"

4.2 Acronyms

Table 4-1 contains a list of acronyms used in this chapter.

Table 4-1. Power Management—Acronyms

Acronym	Description
North Complex	The Intel® Atom™ processor Z6xx series uncore which includes the memory controller, Power Management Unit, and internal FSB Logic
PMU	Power Management Unit
RCOMP	Resistor Compensation
S0i1	Intel® Smart Idle Technology (Intel® SIT) State 1
S0i3	Intel® Smart Idle Technology (Intel® SIT) State 3
SIT	Intel® Smart Idle Technology (Intel® SIT)
SPT	Intel® Smart Power Technology (Intel® SPT)
SR	Self-Refresh

4.3 Processor Voltage Rails

Table 4-2. Voltage Rail Types

Buffer Type	Description
F	Fixed: Voltage level is fixed to be a certain value based on the I/O family.
AON	Always ON: The voltage level must always be on for the component to operate safely, reliably and deterministically.
S	Selectable: Voltage can be selected at the platform level
V	Variable: Variable supplies are negotiable supply levels

Table 4-3. Voltage Rail Descriptions

Voltage Rail Name	Rail Type	Description	Active Power States
V _{CC}	V	Core CPU	S0
V _{NN}	V	North Complex	S0-S0i1
V _{CCP} ¹	F	cDMI, cDVO, display links, legacy pads	S0
V _{CCQ}	F	MIPI PLL	S0
V _{CCPDDR} ¹	F	DDR digital core logic	S0
V _{CCPAOAC}	AON	C6 SRAM, Always-On I/Os	S0-S0i1
V _{MM}	F	MIPI I/O	S0
LVD_VBG	F	LVDS external voltage reference	S0
V _{CCA}	F	Core PLL, HPLL, thermal sensor	S0
V _{CCA180}	F	LVDS 1.8V-Analog	S0
V _{CCD180}	F	LVDS 1.8V-Digital	S0
V _{CC180SR}	AON	DDR SR Pins	AON
V _{CC180}	F	DDR I/O	S0

NOTE: ¹For Intel® Atom™ processors Z605, Z615, and Z625, V_{CCP} and V_{CCPDDR} are tied together to form a combined V_{CCP}/V_{CCPDDR} rail.

4.4 Processor Voltage Rail States

The Intel® Atom™ processor Z6xx series has four categories of voltage rails that are tied to the various platform power states.

- **Processor-Controlled (Variable)**—these are variable and controlled through the processor-PMIC interface (the processor Core voltage (V_{CC}) and the North Complex voltage (V_{NN})). This allows the processor to optimize performance and power during S0 states. During S0i3, the processor interface is invalid and should be ignored and these rails should be off.
- **Intel® Platform Controller Hub MP30 Controlled (S0i1 Off)**—these voltage rails are normally on, but allowed (not required) to be off during S0i1 as well as S0i3. The control for these rails will come from the Intel® Platform Controller Hub MP30 to the PMIC. The Intel® Platform Controller Hub MP30-PMIC interface is not covered in this document.



- **Intel® Platform Controller Hub MP30 Controlled (S0i3 Off)**—these voltage rails must be on in S0 and S0i1 but are allowed (but not required) to be off during S0i3. These include $V_{CCPAOAC}$, V_{CC} , and V_{NN} . When in S0i3, V_{CC} , and V_{NN} are allowed to be off regardless of the values on the VID[6:0] and VIDEN pins from the processor (these pins will in fact be powered-off along with all other processor pins).
- **Always On**—these voltage rails, once ramped during a cold boot, must remain on and within specification at all times. The only rail in this category is $V_{CC180SR}$, which is needed to keep the DRAM in self-refresh during S0i3 so that it preserves state.

Table 4-4. Voltage Rail States

Voltage Rail Name	S0: C0-C6	S0i1	S0i3	Notes
V_{CC}	Variable	OFF	OFF	1
V_{NN}	Variable	ON	OFF	1
V_{CCP}	ON	OFF	OFF	2
V_{CCQ}	ON	OFF	OFF	
V_{CCPDDR}	ON	OFF	OFF	2
$V_{CCPAOAC}$	ON	ON	OFF	
V_{MM}	ON	OFF	OFF	
LVD_VBG	ON	OFF	OFF	
V_{CCA}	ON	OFF	OFF	
V_{CCA180}	ON	OFF	OFF	
V_{CCD180}	ON	OFF	OFF	
$V_{CC180SR}$	ON	ON	ON	
V_{CC180}	ON	OFF	OFF	

NOTES:

1. When the processor is in S0i1 or S0i3, the VID pins are powered off. The VIDEN is driven to 0. This tells the PMIC to ignore the VID pins. All other voltages are controlled by the Intel® Platform Controller Hub MP30 communicating to the processor during S0i1 entry/exit or full power off/on.
2. For Intel® Atom™ Processors Z605, Z615, and Z625, V_{CCP} and V_{CCPDDR} are tied together to form a combined V_{CCP}/V_{CCPDDR} rail.



4.4.1 V_{NN}

V_{NN} is used by the North Complex portion of the Intel® Atom™ processor Z6xx series. The PMIC starts off with a default voltage until the processor changes it—using the VID[6:0] pins when VIDEN[1:0]=VIDEN_VNN. After debouncing, the PMIC uses this new value.

4.4.2 V_{CC}

V_{CC} is used only for the processor core portion of the Intel® Atom™ processor Z6xx series (including the L2 cache).

When the system powers on, V_{CC} is driven by the PMIC to a default value. This allows the processor reset signal to propagate through the core, solving any electrical contentions. During this time, the ring oscillator drives the clock.

Once the VID is driven out by the pads, the PMIC will gradually change the voltage to the value indicated by the VID. Once the voltage stabilizes at the new value, the processor waits a fixed amount of time to before it drives an internal signal that power is good.

4.4.3 $V_{CCPAOAC}$

This is the only 1.05V rail that stays on in S0i1. Pins on this rail are:

- PROCHOT#
- THERMTRIP#
- VIDEN[1:0]
- PWRMODE[2:0]

Any external pull-ups/downs for these pins (such as for THERMTRIP#) need to also be on $V_{CCPAOAC}$.

4.4.4 V_{CCP}

The PMIC is expected to receive a command from the Intel® Platform Controller Hub MP30 to disable power to V_{CCP} while the processor is in S0i1.

4.5 V_{CC}/V_{NN} VID Control

The V_{CC} and V_{NN} voltage inputs use two encoding pins (VIDEN[1:0]) to enable the VID pin inputs and seven voltage identification pins (VID[6:0]) to select the power supply voltage. The VID/VIDEN pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 4-6 specifies the voltage level corresponding to the state of VID[6:0]. A "1" in this refers to a high-voltage level and a "0" refers to a low-voltage level. For more details about the PMIC design to support the processor power supply requirements, refer to the vendor's specification.

4.5.1 VID Enable

Both V_{CC} and V_{NN} are variable in the Intel® Atom™ processor Z6xx series. The Intel® Atom™ processor Z6xx series implements a new VID mechanism that minimizes the number of required pins. The VID for V_{NN} and V_{CC} are multiplexed on to the same set of



pins and a separate 2-bit enable/ID is defined to specify what the driven VID corresponds to. One of the combinations is used to notify that the VID is invalid. This is used when the processor is in C6/Standby to tri-state the VID pins to save power.

Table 4-5. VIDEN Encoding

VIDEN[1:0]	Description
00b	VID is invalid
01b	VID for V_{CC}
10b	VID for V_{NN}
11b	Reserved

4.5.2 VID Table for Variable Power Supplies

The VID[6:0] is the indication produced by the processor to the voltage regulator about which voltage must be set for V_{CC} or V_{NN} (as identified by the VIDEN[] pins). For the encoding of the VID, see [Table 4-6](#).

Note: The Intel® Atom™ processor Z6xx series will not support the entire range of the voltages listed in the VID table (grayed out).

Note: VID codes below 0.3V are not supported for V_{CC} .

Table 4-6. VID Table (Sheet 1 of 2)

VID[6:0]	V_{CC}/V_{NN}	VID[6:0]	V_{CC}/V_{NN}	VID[6:0]	V_{CC}/V_{NN}	VID[6:0]	V_{CC}/V_{NN}
00h	1.5000V	20h	1.1000V	40h	0.7000V	60h	0.3000V
01h	1.4875V	21h	1.0875V	41h	0.6875V	61h	0.2875V
02h	1.4750V	22h	1.0750V	42h	0.6750V	62h	0.2750V
03h	1.4625V	23h	1.0625V	43h	0.6625V	63h	0.2625V
04h	1.4500V	24h	1.0500V	44h	0.6500V	64h	0.2500V
05h	1.4375V	25h	1.0375V	45h	0.6375V	65h	0.2375V
06h	1.4250V	26h	1.0250V	46h	0.6250V	66h	0.2250V
07h	1.4125V	27h	1.0125V	47h	0.6125V	67h	0.2125V
08h	1.4000V	28h	1.0000V	48h	0.6000V	68h	0.2000V
09h	1.3875V	29h	0.9875V	49h	0.5875V	69h	0.1875V
0Ah	1.3750V	2Ah	0.9750V	4Ah	0.5750V	6Ah	0.1750V
0Bh	1.3625V	2Bh	0.9625V	4Bh	0.5625V	6Bh	0.1625V
0Ch	1.3500V	2Ch	0.9500V	4Ch	0.5500V	6Ch	0.1500V
0Dh	1.3375V	2Dh	0.9375V	4Dh	0.5375V	6Dh	0.1375V
0Eh	1.3250V	2Eh	0.9250V	4Eh	0.5250V	6Eh	0.1250V
0Fh	1.3125V	2Fh	0.9125V	4Fh	0.5125V	6Fh	0.1125V
10h	1.3000V	30h	0.9000V	50h	0.5000V	70h	0.1000V
11h	1.2875V	31h	0.8875V	51h	0.4875V	71h	0.0875V
12h	1.2750V	32h	0.8750V	52h	0.4750V	72h	0.0750V
13h	1.2625V	33h	0.8625V	53h	0.4625V	73h	0.0625V



Table 4-6. VID Table (Sheet 2 of 2)

VID[6:0]	V _{CC} /V _{NN}						
14h	1.2500V	34h	0.8500V	54h	0.4500V	74h	0.0500V
15h	1.2375V	35h	0.8375V	55h	0.4375V	75h	0.0375V
16h	1.2250V	36h	0.8250V	56h	0.4250V	76h	0.0250V
17h	1.2125V	37h	0.8125V	57h	0.4125V	77h	0.0125V
18h	1.2000V	38h	0.8000V	58h	0.4000V	78h	0.0000V
19h	1.1875V	39h	0.7875V	59h	0.3875V	79h	0.0000V
1Ah	1.1750V	3Ah	0.7750V	5Ah	0.3750V	7Ah	0.0000V
1Bh	1.1625V	3Bh	0.7625V	5Bh	0.3625V	7Bh	0.0000V
1Ch	1.1500V	3Ch	0.7500V	5Ch	0.3500V	7Ch	0.0000V
1Dh	1.1375V	3Dh	0.7375V	5Dh	0.3375V	7Dh	0.0000V
1Eh	1.1250V	3Eh	0.7250V	5Eh	0.3250V	7Eh	0.0000V
1Fh	1.1125V	3Fh	0.7125V	5Fh	0.3125V	7Fh	0.0000V

4.6 Valid Power States

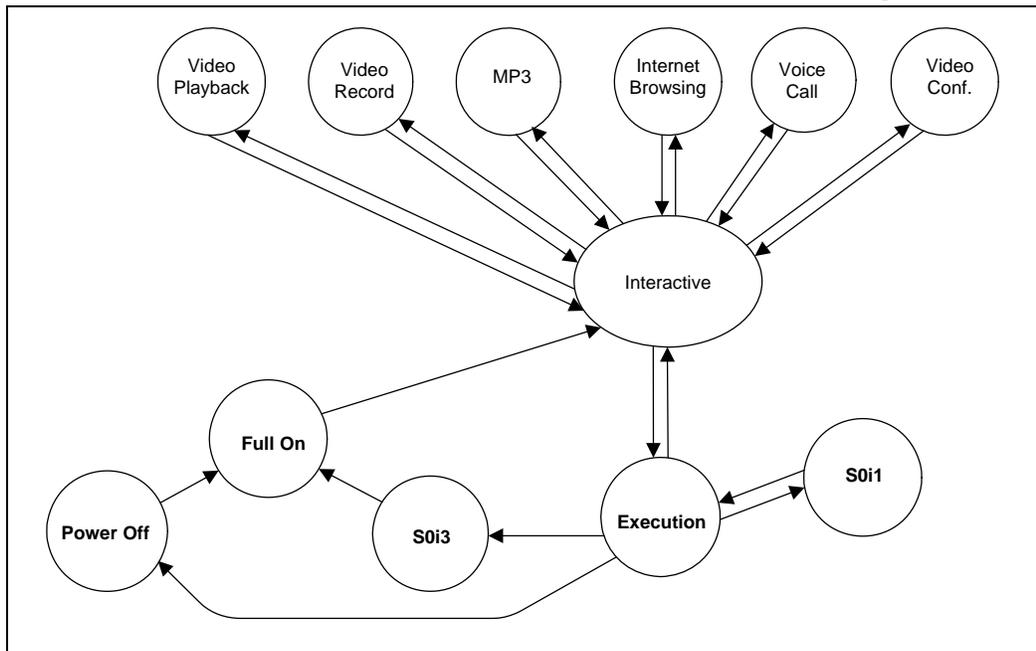
The Intel® Atom™ processor Z6xx series has various scenario power states that are used to classify its operating power in common situations. These are described in Table 4-7.

Table 4-7. Power States

Scenario Power State	Description
Power Off	System Power Off
Full ON	<ul style="list-style-type: none"> This is used only when systems are coming out of cold boot. All resources are turned on for applications to load up and for the operating system to query system status. The processor is in this mode only temporarily. It is in a transition state before entering interactive.
Interactive	<ul style="list-style-type: none"> Processor core (C0), Host Bridge on, DRAM on, Display on, Graphics on/off, Video Encode/Video Decode off. This mode is entered to allow the user to interactively select which applications to run.
Execution	<ul style="list-style-type: none"> Processor core (C0), Host Bridge on, DRAM on, Display/Graphics/Video Encode/Video Decode off. This mode used only by applications to synchronize or write to memory. No interactive resources are on.
S0i1	<ul style="list-style-type: none"> Processor core (C6), Host Bridge off, DRAM in Self-Refresh, Display/Graphics/Video Encode/Video Decode off. This mode is a low-power mode, with direct impact on standby battery life. The processor enters S0i1 after Intel® SPT queries all resources, usage, and recognizes that the platform can go into S0i1.
S0i3	<ul style="list-style-type: none"> This is the lowest power state for the processor when the platform is still running. The processor core macro-state is saved to DRAM by software. All domains in the processor are powered off from the PMIC except the self-refresh pins on DRAM. DRAM is held in self-refresh by the Intel® Platform Controller Hub MP30; CKE pins in the processor are still powered on.



Figure 4-1. Intel® Atom™ Processor Z6xx Series Power State Transition Diagram



4.7 Processor Core Low Power Features

Figure 4-2, shows the thread low power states Figure 4-3, shows the package low power states.

Note: STPCLK#, DPSLP#, and DPRSTP are internal signals only.

Figure 4-2. Thread Low Power States

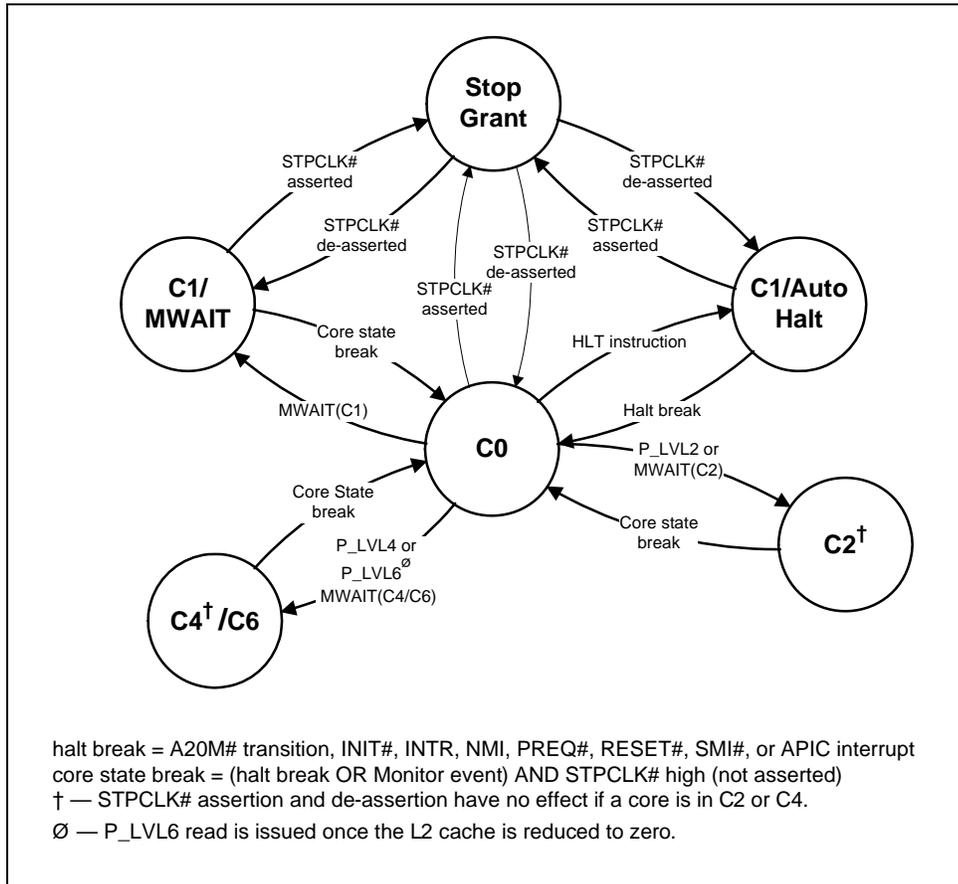
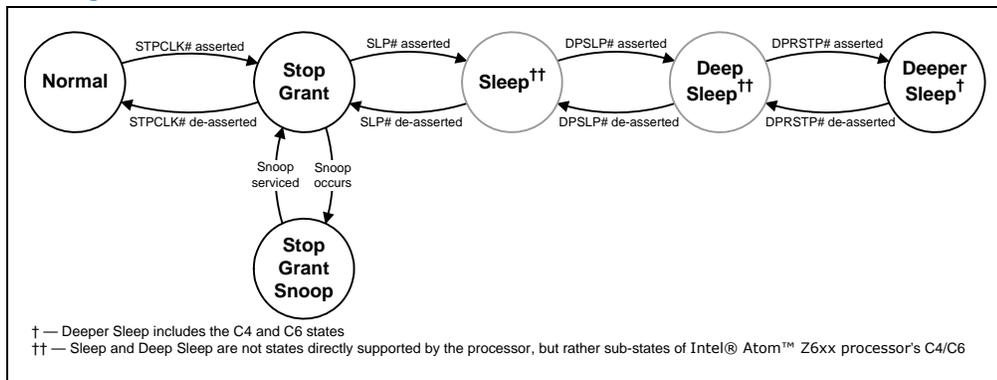


Figure 4-3. Package Low Power States



4.7.1 Cx State Definitions

4.7.1.1 C0 State—Full On

This is the only state that runs software. All clocks are running and the processor core is active. The processor can service snoops and maintain cache coherency in this state. All power management for interfaces, and clock gating, are controlled at the unit level.



4.7.1.2 C1 State—Auto-Halt

The first level of power reduction occurs when the processor core executes an Auto-Halt instruction. This stops the execution of the instruction stream and greatly reduces the processor core's power consumption. The processor core can service snoops and maintain cache coherency in this state. The processor's North Complex logic does not distinguish C1 from C0 explicitly.

4.7.1.3 C2 State—Stop Grant

The next level of power reduction occurs when the processor core is placed into the Stop Grant state. The processor core can service snoops and maintain cache coherency in this state. The North Complex only supports receiving a single Stop Grant.

Entry into the C2 state will occur after the processor core requests C2 (or deeper). C2 state will be exited, entering the C0 state, when a break event is detected. The processor must ensure that the DLLs are awake and the memory will be out of self-refresh at this point.

4.7.1.4 C1E and C2E States

C1E and C2E states are transparent to the North Complex logic. The C1E state is the same as the C1 state, in that the processor core emits a HALT cycle when entering the state. There are no other visible actions from the processor core.

The C2E state is the same as the C2 state, in that the processor core emits a Stop Grant cycle when entering the state. There are no other visible actions from the processor core.

4.7.1.5 C4 State—Deeper Sleep

In this state, the processor core shuts down its PLL and cannot handle snoop requests. The processor core voltage regulator is also told to reduce the processor voltage. During the C4 state, the North Complex will continue to handle traffic to memory so long as this traffic does not require a snoop (that is, no coherent traffic requests are serviced).

The C4 state is entered by receiving a C4 request from the processor core/OS. The exit from C4 occurs when the North Complex detects a snoopable event or a break event, which would cause it to wake up the processor core and initiate the C0 sequence.

4.7.1.6 C4E

The C4E state is essentially the same as the C4 state except that the processor core will transition to the Low Frequency Mode (LFM) frequency and voltage upon entry and exit of this state.

4.7.1.7 C6—Deep Power Down

Prior to entering the C6 state, the processor core will flush its cache and save its core context to a special on-die SRAM on a different power plane. Once the C6 entry sequence has completed, the processor core voltage can be completely shut off.

The key difference for the North Complex logic between the C4 state and the C6 state is that since the processor core cache is empty, there is no need to perform snoops on the internal FSB. This means that bus master events (which would cause a popup from the C4 state to the C2 state) can be allowed to flow unimpeded during the C6 state. However, the processor core must still be returned to the C0 state to service interrupts.



A residency counter is read by the processor core to enable an intelligent promotion/demotion based on energy awareness of transitions and history of residencies/transitions.

§



5 Electrical Specifications

5.1 Chapter Contents

This chapter contains information about:

- "Acronyms"
- "Storage Specifications"
- "Absolute Maximum Ratings"
- "DC Specifications"

5.2 Acronyms

Table 5-1 contains a list of acronyms used in this chapter.

Table 5-1. Electrical Specifications—Acronyms

Acronym	Description
LPDDR	Low Power Double Data Rate
CL	CAS Latency
WL	Write Latency
UI	Unit Interval

5.3 Storage Specifications

Table 5-2 includes a list of the specifications for device storage in terms of maximum and minimum temperatures and relative humidity. These conditions should not be exceeded in storage or transportation.

Table 5-2. Storage Conditions

Parameter	Description	Min.	Max.	Notes
$T_{\text{ABSOLUTE STORAGE}}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.	-55 °C	125 °C	1, 2, 3
$T_{\text{SUSTAINED STORAGE}}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5
$RH_{\text{SUSTAINED STORAGE}}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C		5, 6
$TIME_{\text{SUSTAINED STORAGE}}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	6 Months	6

NOTES:

1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.



2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in applicable JEDEC standard and MAS document. Non-adherence may affect processor reliability.
3. $T_{\text{ABSOLUTE STORAGE}}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel® branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C, Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{\text{SUSTAINED}}$ and customer shelf life in applicable Intel box and bags.

5.4 Absolute Maximum Ratings

Table 5-3 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, then when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 5-3. Absolute Maximum Ratings (Sheet 1 of 2)

Symbol	Parameter		Min.	Max.	Unit	Notes
T_J	Operational junction temperature	Processor Numbers: Z600, Z610, Z612, Z620	-25	90	°C	1, 2
		Processor Numbers: Z605, Z615, Z625	0	90	°C	1, 2
V_{CC}	Processor core supply voltage		-0.3	1.2	V	
V_{NN}	North Complex logic and GFX supply voltage		-0.3	1.1	V	
V_{CCP}/V_{CCQ}	1.05V MIPI PLL, cDMI, DVO, LGI, LGIE		-0.3	1.1	V	
V_{CCPDDR}	1.05V DDR DLL and logic supply voltage		-0.3	1.1	V	
$V_{CCPAOAC}$	1.05V JTAG, C6 SRAM		-0.3	1.1	V	
V_{MM}	1.2V MIPI I/O supply voltage		-0.3	1.25	V	
LVD_VBG	1.25V LVDS band gap supply voltage		-0.1	1.28	V	



Table 5-3. Absolute Maximum Ratings (Sheet 2 of 2)

Symbol	Parameter	Min.	Max.	Unit	Notes
V _{CCA}	1.5V HPLL analog PLL and thermal sensor supply voltage	-0.3	1.575	V	
V _{CCA180}	1.8V LVDS analog supply voltage	-0.3	1.9	V	
V _{CCD180}	1.8V LVDS I/O supply voltage	-0.3	1.9	V	
V _{CC180SR}	1.8V LPDDR1/DDR2 self-refresh supply voltage	-0.4	1.9	V	
V _{CC180}	1.8V LPDDR1/DDR2 I/O supply voltage	-0.4	1.9	V	

NOTES:

- As measured by the activation of the on-die Intel® Thermal Monitor. The Intel® Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to [Section 6.5, "Temperature Monitoring" on page 50](#) for more details.
- The Intel® Thermal Monitor's automatic mode must be enabled for the processor to operate within specifications.



5.5 DC Specifications

Table 5-4. Voltage and Current Specifications for the Intel® Atom™ Processors—Z600, Z610, Z612, and Z620 (Sheet 1 of 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Notes ^{1, 2}
V _{CC} HFM	V _{CC} @ Highest Frequency Mode		AVID	–	1.15	V	3
V _{CC} LFM	V _{CC} @ Lowest Frequency Mode		0.75	–	AVID	V	3
V _{CC} BFM	V _{CC} @ Burst Frequency Mode		AVID	–	1.2	V	3
V _{CC} BOOT	Default V _{CC} for initial power on		–	V _{CC} LFM	–	V	4
V _{NN} BOOT	Default V _{NN} for initial power on		–	V _{NN}	–	V	4
V _{NN}	V _{NN} supply voltage		AVID	–	0.9875	V	3
V _{CCP}	V _{CCP} supply voltage		0.9975	1.05	1.1025	V	
V _{CCQ}	V _{CCQ} supply voltage		0.9975	1.05	1.1025	V	
V _{CCPDDR}	V _{CCPDDR} supply voltage		1.029	1.05	1.071	V	5
V _{CCPAOAC}	V _{CCPAOAC} supply voltage		0.9975	1.05	1.1025	V	
V _{MM}	V _{MM} supply voltage		1.14	1.20	1.26	V	
LVD_VBG	LVDS band gap reference voltage		1.225	1.25	1.275	V	
V _{CCA}	V _{CCA} supply voltage		1.47	1.5	1.53	V	
V _{CCA180}	V _{CCA180} supply voltage		1.746	1.8	1.854	V	
V _{CCD180}	V _{CCD180} supply voltage		1.71	1.8	1.89	V	
V _{CC180SR}	V _{CC180SR} supply voltage		1.71	1.8	1.89	V	
V _{CC180}	V _{CC180} supply voltage		1.71	1.8	1.89	V	
I _{VCC}	Processor Number	Core Frequency	–	–	–	–	
	Z600	BFM: 1.2 GHz HFM: 0.8 GHz LFM: 0.6 GHz	–	–	2.00 1.06 0.62	A	6, 7
	Z610	BFM: 1.2 GHz HFM: 0.8 GHz LFM: 0.6 GHz	–	–	2.00 1.06 0.62	A	6, 7
	Z612	BFM: 1.5 GHz HFM: 0.9 GHz LFM: 0.6 GHz	–	–	2.21 1.37 0.62	A	6, 7
	Z620	BFM: 1.5 GHz HFM: 0.9 GHz LFM: 0.6 GHz	–	–	2.21 1.37 0.62	A	6, 7
I _{VNN}	V _{NN} supply current		–	–	1.20	A	7
I _{VCCP}	V _{CCP} supply current		–	–	0.12	A	7
I _{VCCQ}	V _{CCQ} supply current		–	–	0.01	A	7
I _{VCCPDDR}	V _{CCPDDR} supply current		–	–	0.250	A	7
I _{VCCPAOAC}	V _{CCPAOAC} supply current		–	–	0.045	A	7


Table 5-4. Voltage and Current Specifications for the Intel® Atom™ Processors—Z600, Z610, Z612, and Z620 (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes ^{1, 2}
I _{VMM}	V _{MM} supply current	–	–	0.02	A	7, 8
I _{VCCA}	V _{CCA} supply current	–	–	0.102	A	7
I _{VCCA180}	V _{CCA180} supply current	–	–	0.0491	A	7, 9, 10
I _{VCCD180}	V _{CCD180} supply current					
I _{VCC180SR}	V _{CC180SR} supply current	–	–	0.01	A	7
I _{VCC180}	V _{CC180} supply current	–	–	0.15	A	7

NOTES:

- Maximum specifications are based on measurements done with currently existing workloads and test conditions. These numbers are subject to change.
- Specified at T_J = 90° C.
- Each processor is programmed with a maximum valid Voltage Identification Value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® Technology, or Enhanced Halt State). Typical AVID (Automatic Voltage Identification) range is 0.75–1.2V for V_{CC} and 0.75–0.9875V for V_{NN}.
- This specification corresponds to what value gets driven by the processor. It is possible for firmware to override these values.
- Voltage specification of ± 2% includes AC and DC variations. The sum of AC noise and DC variations should not exceed 1.05V ± 2%.
- Specified at the nominal V_{CC}.
- Peak Sustained Current is defined as the maximum sustainable current measured as an RMS value over 1 μs.
- Specification based on MIPI panel configuration of 800 x 480 resolution, 30 Hz refresh rate, and 24bpp color depth.
- This is the sum of current on both rails.
- Specification based on LVDS panel configuration of 1024 x 600 resolution, 60 Hz refresh rate, and 18 bpp color depth.

Table 5-5. Voltage and Current Specifications for the Intel® Atom™ Processors—Z605, Z615, and Z625 (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes ^{1, 2}
V _{CC} HFM	V _{CC} @ Highest Frequency Mode	AVID	–	1.15	V	3
V _{CC} LFM	V _{CC} @ Lowest Frequency Mode	0.75	–	AVID	V	3
V _{CC} BFM	V _{CC} @ Burst Frequency Mode	AVID	–	1.2	V	3
V _{CC} BOOT	Default V _{CC} for initial power on	–	V _{CC} LFM	–	V	4
V _{NN} BOOT	Default V _{NN} for initial power on	–	V _{NN}	–	V	4
V _{NN}	V _{NN} supply voltage	AVID	–	0.9875	V	3
V _{CCP} / V _{CCPDDR}	V _{CCP} /V _{CCPDDR} supply voltage	1.018	1.05	1.081	V	5
V _{CCQ}	V _{CCQ} supply voltage	0.9975	1.05	1.1025	V	
V _{CCPAOAC}	V _{CCPAOAC} supply voltage	0.9975	1.05	1.1025	V	
V _{MM}	V _{MM} supply voltage	1.14	1.20	1.26	V	



Table 5-5. Voltage and Current Specifications for the Intel® Atom™ Processors—Z605, Z615, and Z625 (Sheet 2 of 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Notes ^{1, 2}
LVD_VBG	LVDS band gap reference voltage		1.225	1.25	1.275	V	
V _{CCA}	V _{CCA} supply voltage		1.47	1.5	1.53	V	
V _{CCA180}	V _{CCA180} supply voltage		1.746	1.8	1.854	V	
V _{CCD180}	V _{CCD180} supply voltage		1.71	1.8	1.89	V	
V _{CC180SR}	V _{CC180SR} supply voltage		1.71	1.8	1.89	V	
V _{CC180}	V _{CC180} supply voltage		1.71	1.8	1.89	V	
I _{VCC}	Processor Number	Core Frequency	–	–	–	–	
	Z605	HFM: 1.0 GHz LFM: 0.6 GHz	–	–	1.46 0.61	A	6, 7
	Z615	BFM: 1.6 GHz HFM: 1.2 GHz LFM: 0.6 GHz	–	–	2.32 1.70 0.61	A	6, 7
	Z625	BFM: 1.9 GHz HFM: 1.5 GHz LFM: 0.6 GHz	–	–	2.49 1.89 0.61	A	6, 7
I _{VNN}	V _{NN} supply current		–	–	1.58	A	7
I _{VCCP/VCCPDDR}	V _{CCP/VCCPDDR} supply current		–	–	0.355	A	7
I _{VCCQ}	V _{CCQ} supply current		–	–	0.015	A	7
I _{VCCPAOAC}	V _{CCPAOAC} supply current		–	–	0.03	A	7
I _{VMM}	V _{MM} supply current		–	–	0.01	A	7, 8
I _{VCCA}	V _{CCA} supply current		–	–	0.150	A	7
I _{VCCA180}	V _{CCA180} supply current		–	–	0.05	A	7, 9, 10
I _{VCCD180}	V _{CCD180} supply current						
I _{VCC180SR}	V _{CC180SR} supply current		–	–	0.01	A	7
I _{VCC180}	V _{CC180} supply current		–	–	0.40	A	7

NOTES:

1. Maximum specifications are based on measurements done with currently existing workloads and test conditions. These numbers are subject to change.
2. Specified at T_J = 90° C.
3. Each processor is programmed with a maximum valid Voltage Identification Value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® Technology, or Enhanced Halt State). Typical AVID (Automatic Voltage Identification) range is 0.75–1.2V for V_{CC} and 0.75–0.9875V for V_{NN}.
4. This specification corresponds to what value gets driven by the processor. It is possible for firmware to override these values.
5. Voltage specification of ± 3% includes AC and DC variations. The sum of AC noise and DC variations should not exceed 1.05V ± 3%.
6. Specified at the nominal V_{CC}.



7. Peak Sustained Current is defined as the maximum sustainable current measured as an RMS value over 1 μ s.
8. Specification based on MIPI panel configuration of 800 x 480 resolution, 30 Hz refresh rate, and 24bpp color depth.
9. This is the sum of current on both rails.
10. Specification based on LVDS panel configuration of 1024 x 600 resolution, 60 Hz refresh rate, and 18bpp color depth.

Table 5-6. Differential Clock DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Differential Clock (BCLK)						
V _{IH}	Input high voltage	–	–	1.15	V	
V _{IL}	Input low voltage	–	–	-0.3	V	
V _{CROSS}	Crossing voltage	0.3	–	0.55	V	
Δ V _{CROSS}	Range of crossing points	–	–	140	mV	
V _{SWING}	Differential output swing	300	–	–	mV	
I _{LI}	Input leakage current	-5	–	+5	μ A	
C _{PAD}	Pad capacitance	1.2	1.45	2.0	pF	

Table 5-7. AGTL+, CMOS, and CMOS Open Drain Signal Group DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes ¹
GTLREF	AGTL+ reference voltage	–	$2/3 V_{CCP}$	–	V	
CMREF	CMOS reference voltage	–	$1/2 V_{CCP}$	–	V	
R _{COMP}	Compensation resistor	27.73	27.5	27.78	Ω	10
R _{ODT}	Termination resistor	–	55	–	Ω	11
V _{IH} (GTL)	Input high voltage AGTL+ signal	GTLREF + 0.10	V _{CCP}	V _{CCP} + 0.10	V	3, 6
V _{IL} (GTL)	Input low voltage AGTL+ signal	-0.10	0	GTLREF - 0.10	V	2, 4
V _{IH} (CMOS)	Input high voltage CMOS signal	CMREF + 0.10	V _{CCP}	V _{CCP} + 0.10	V	3, 6
V _{IL} (CMOS)	Input low voltage CMOS signal	-0.10	0	CMREF - 0.10	V	2, 4
V _{OH}	Output high voltage	V _{CCP} - 0.10	V _{CCP}	V _{CCP}	V	6
R _{TT} (GTL)	Termination resistance	46	55	61	Ω	7
R _{TT} (CMOS)	Termination resistance	46	55	61	Ω	11
R _{ON} (GTL)	AGTL+ buffer on resistance	21	25	29	Ω	5
R _{ON} (CMOS)	CMOS buffer on resistance	42	50	55	Ω	12
R _{ON} (CMOS_C)	CMOS common clock buffer on resistance	42	50	58	Ω	12
I _{LI}	Input leakage current	–	–	± 100	μ A	8
C _{PAD}	Pad capacitance	1.6	2.1	2.55	pF	9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP} . However, input signal drivers must comply with the signal quality specifications.
5. R_{ON} is the pull-down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at $0.33 \cdot V_{CCP}$.
6. GTLREF and CMREF should be generated from V_{CCP} with a 1% tolerance resistor divider. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP} .
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at $0.33 \cdot V_{CCP}$. R_{TT} is connected to V_{CCP} on die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on die R_{TT} and R_{ON} are turned off. V_{IN} between 0 and V_{CCP} .
9. C_{PAD} includes die capacitance only. No package parasitics are included.
10. This is the external resistor on the component pins.
11. On die termination resistance for CMOS is measured at $0.5 \cdot V_{CCP}$.
12. R_{ON} for CMOS pull-down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at $0.5 \cdot V_{CCP}$.

Table 5-8. CMOS1.8 Signal Group DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes ¹
V_{IH}	Input high voltage	$(V_{CC180/2}) + 0.125$	-	1.9	V	3
V_{IL}	Input low voltage	-0.4	-	$(V_{CC180/2}) - 0.125$	V	2
V_{OH}	Output high voltage	$(V_{CC180/2}) + 0.25$	-	-	V	4
V_{OL}	Output low voltage	-	-	$(V_{CC180/2}) - 0.25$	V	4

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP} . However, input signal drivers must comply with the signal quality specifications.

Table 5-9. LVDS Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes ¹
V_{OS}	Offset voltage	1.125	1.25	1.375	V	
ΔV_{OS}	Change in offset voltage	-	-	50	mV	
V_{OD}	Differential output voltage	250	350	450	mV	
ΔV_{OD}	Change in differential output voltage	-	-	50	mV	
I_{SC}	Short-circuit current	-	-	12	mA	
I_{SCC}	Short-circuit comment current	-	-	24	mA	
I_L	Leakage current	-380	150	380	μ A	



Table 5-9. LVDS Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes ¹
	Dynamic offset	–	–	150	mV	
	Overshoot	–	–	90	mV	
	Ringback	–	–	90	mV	

NOTE: ¹Unless otherwise noted, all specifications in this table apply to all processor frequencies.

Table 5-10. MIPI Signal Group DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes ¹
V _{PIN}	Pin signal voltage range	-50	–	1350	mV	
I _{LEAK}	Pin leakage current	-280	150	280	μA	
V _{GND} SH	Ground shift	-50	–	50	mV	
V _{PIN} (absmax)	Transient pin voltage level	-50	–	1.45	V	
T _{VPIN} (absmax)	Maximum transient time above V _{PIN} (max) or below V _{PIN} (min)	–	–	20	ns	
MIPI HS-TX						
V _{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	
V _{CMTX(1,0)}	V _{CMTX} mismatch when output is Differential-1 or Differential-0	–	–	5	mV	
V _{OD}	HS transmit differential voltage	140	200	270	mV	
ΔV _{OD}	V _{OD} mismatch when output is Differential-1 or Differential-0	–	–	10	mV	
V _{OHHS}	HS output high voltage	–	–	360	mV	
Z _{OS}	Single-ended output impedance	40	50	62.5	Ω	
ΔZ _{OS}	Single-ended output impedance mismatch	–	–	10	%	
MIPI LP-TX						
V _{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V _{OL}	Thevenin output low level	-50	–	50	mV	
Z _{OLP}	Output impedance of LP transmitter	110	–	–	Ω	
C _{LOAD}	RX load	–	–	40	pF	
MIPI LP-RX						
V _{IH}	Logic 1 input voltage	880	–	–	mV	3
V _{IL}	Logic 0 input voltage, not in ULP state	–	–	550	mV	2
V _{IL-ULPS}	Logic 0 input voltage, ULP state	–	–	300	mV	
V _{HYST}	Input hysteresis	25	–	–	mV	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.



3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.

§



6 Thermal Specifications

6.1 Chapter Contents

This chapter contains thermal specification information about:

- "Acronyms"
- "Package and Die Thermal Characteristics"
- "Thermal Design"
- "Temperature Monitoring"

6.2 Acronyms

Table 6-1 contains a list of acronyms used in this chapter.

Table 6-1. Thermal Specifications—Acronyms

Acronym	Description
Θ_{JA}	Thermal Resistance – Junction-to-Ambient
Θ_{JB}	Thermal Resistance – Junction-to-Board
Ψ_{JMT}	Characterization for thermal resistance – Junction-to-Mold-Top
DTS	Digital Thermal Sensor
LFM	Low Frequency Mode
MSR	Model-Specific Register
T_J	Junction (die) Operating Temperature
TCC	Thermal Control Circuit
TDP	Thermal Design Power
TM1	Thermal Monitor 1
TM2	Thermal Monitor 2
VR	Voltage Regulator

6.3 Package and Die Thermal Characteristics

Table 6-2. Package and Die Thermal Characteristics

Symbol	Parameter		Min.	Nom.	Max.	Unit	Notes
T_J	Operational junction temperature	Processor Numbers: Z600, Z610, Z612, Z620	-25	—	90	°C	1, 2
		Processor Numbers: Z605, Z615, Z625	0	—	90	°C	1, 2
Θ_{JA}	Thermal resistance from junction to ambient (JA)		—	27	—	°C/W	3
Θ_{JB}	Thermal resistance from junction to board (JB)		—	15	—	°C/W	3
Ψ_{JMT}	Thermal resistance from junction to mold top		—	0.26	—	°C/W	3

NOTES:

- As measured by the activation of the on-die Intel® Thermal Monitor. The Intel® Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to section 6.5 for more details.
- The Intel® Thermal Monitor's automatic mode must be enabled for the processor to operate within specifications.
- Values are based on measurements taken on the package mounted on a 4-layer board (2s2p) in a JEDEC environment. These values are intended to characterize the thermal resistance from the die to its environment. They are not meant to reflect in-device measurements for the package or die.

6.4 Thermal Design

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in section 6.3. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. Maintaining the proper thermal environment is the key to reliable, long-term system operation. A complete thermal solution includes both component and system level thermal management features.

Note: Trading thermal solutions also involves trading performance.

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding Thermal Design Power (TDP) value listed in Table 6-3 and Table 6-4. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The maximum junction temperature is defined by an activation of the processor Intel® Thermal Monitor. Refer to section 6.5.1 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 6-3 and Table 6-4. The Intel® Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to section 6.5.1. In all cases, the Intel® Thermal Monitor feature must be enabled for the processor to remain within specification.



Table 6-3. Power Specifications for Intel® Atom™ Processors—Z600, Z610, Z612, and Z620

Symbol	Processor Number	Core Frequency and Voltage	Thermal Design Power			Unit	Notes
TDP	Z600	0.8 GHz and HFM V _{CC} 0.6 GHz and LFM V _{CC}	1.3			W	@ 90°C 1, 2, 3
	Z610	0.8 GHz and HFM V _{CC} 0.6 GHz and LFM V _{CC}	1.3			W	@ 90°C 1, 2, 3
	Z612	0.9 GHz and HFM V _{CC} 0.6 GHz and LFM V _{CC}	1.3			W	@ 90°C 1, 2, 3
	Z620	0.9 GHz and HFM V _{CC} 0.6 GHz and LFM V _{CC}	1.3			W	@ 90°C 1, 2, 3
Symbol	Parameter		Min.	Typical	Max.	Unit	Notes
P _{S0i1}	Intel® SIT S0i1 Power		—	10	—	mW	@ 30°C 4
P _{S0i3}	Intel® SIT S0i3 Power		—	200	—	μW	@ 30°C 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. The Intel® Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
3. Intel® Hyper-Threading Technology (Intel® HT Technology) requires a computer system with an Intel processor supporting Hyper-Threading Technology and an HT Technology enabled chipset, firmware, and operating system. HT Technology can add 300 mW of power above TDP when multi-threaded applications are run.
4. Average power as measured in a forced steady-state environment.

Table 6-4. Power Specifications for Intel® Atom™ Processors—Z605, Z615, and Z625

Symbol	Processor Number	Core Frequency and Voltage	Thermal Design Power			Unit	Notes
TDP	Z605	1.0 GHz and HFM V _{CC} 0.6 GHz and LFM V _{CC}	2.2			W	@ 90°C 1, 2, 3, 4
	Z615	1.2 GHz and HFM V _{CC} 0.6 GHz and LFM V _{CC}	2.2			W	@ 90°C 1, 2, 3, 4
	Z625	1.5 GHz and HFM V _{CC} 0.6 GHz and LFM V _{CC}	2.2			W	@ 90°C 1, 2, 3, 4
Symbol	Parameter		Min.	Typical	Max.	Unit	Notes
P _{S0i1}	Intel® SIT S0i1 Power		—	10	—	mW	@ 30°C 5
P _{S0i3}	Intel® SIT S0i3 Power		—	200	—	μW	@ 30°C 5

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.



2. The Intel® Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
3. Intel® Hyper-Threading Technology (Intel® HT Technology) requires a computer system with an Intel processor supporting Hyper-Threading Technology and an HT Technology enabled chipset, firmware, and operating system. HT Technology can add 350 mW of power above TDP when multi-threaded applications are run.
4. Enabling ODT can add 450 mW of power above TDP.
5. Average power as measured in a forced steady-state environment.

6.5 Temperature Monitoring

The processor incorporates two methods of monitoring die temperature:

- By Digital Thermal Sensor (DTS)
- By Intel® Thermal Monitor

The Intel® Thermal Monitor (detailed in section 6.5.1) must be used to determine when the maximum specified processor junction temperature has been reached.

6.5.1 Intel® Thermal Monitor

The Intel® Thermal Monitor helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel® Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable.

An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel® Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep® Technology transition when the processor silicon reaches its maximum operating temperature. The Intel® Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called the Intel® Thermal Monitor 1 (TM1) and the Intel Thermal Monitor 2 (TM2). These modes are selected by writing values to the MSRs of the processor. After the automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

When the TM1 mode is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50 percent duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be



modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

When the TM2 mode is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep® Technology transition to the LFM. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep® Technology transition to the last requested operating point.

The Intel® Thermal Monitor automatic mode and Enhanced Intel SpeedStep® Technology must be enabled through IA-32 Firmware for the processor to be operating within specifications. Intel recommends that TM1 and TM2 be enabled on the processors.

TM1 and TM2 can co-exist within the processor. If both TM1 and TM2 bits are enabled, TM2 will take precedence over TM1. However, if Force TM1 over TM2 is enabled and TM2 is not sufficient to cool the processor below the maximum operating temperature, then TM1 will also activate to help cool down the processor.

If a processor load-based Enhanced Intel SpeedStep® Technology transition (through MSR write) is initiated when a TM2 period is active, there are two possible results:

- If the processor load-based Enhanced Intel SpeedStep® Technology transition target frequency is higher than the TM2 transition based target frequency, the processor load-based transition will be deferred until the TM2 event has been completed.
- If the processor load-based Enhanced Intel SpeedStep® Technology transition target frequency is lower than the TM2 transition based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep® Technology target frequency point.

The TCC may also be activated using on-demand mode. If bit 4 of the ACPI Intel® Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable using bits 3:1 of the same ACPI Intel® Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off. However in on-demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments.

On-demand mode may be used at the same time automatic mode is enabled; however, if the system tries to enable the TCC using on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel® Thermal Monitor also includes one ACPI register, one performance counter register, three MSRs, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel® Thermal Monitor feature. The Intel® Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Sleep, Deep Sleep, and Deeper Sleep low power states (see [Table 6-5](#)). If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage.



If the Intel® Thermal Monitor automatic mode is disabled, the processor will operate out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached its critical trip point. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must shut down within a specified time.

Table 6-5. Support for PROCHOT#/THERMTRIP# in Active and Idle States

System State	Core State	PROCHOT# (Bi-Directional)			THERMTRIP# (Output)
		Input		Output	
		Core	North Complex		
S0	C0	Supported	Optional	Active	Active
	C1/C1E	Supported	Optional	Active	Active
	C2/C2E	Supported	Optional	Active	Active
	C4/C4E	Ignored	Optional	Invalid	Active
	C6	Ignored	Optional	Invalid	Active
S0i1	C6	Ignored	Ignored	Invalid	Inactive
S0i3	OFF	Ignored	Ignored	OFF	OFF

6.5.2 Digital Thermal Sensor

The processor core has a unique Digital Thermal Sensor (DTS) this device temperature is accessible using the processor MSRs. The DTS is able to accurately track the die temperature and potentially activate the processor core clock modulation using the Intel® Thermal Monitor. The DTS is only valid while the processor is in an active state.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{j\max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS is always at or below $T_{j\max}$.

The DTS-relative temperature readout corresponds to the Intel® Thermal Monitor (TM1/TM2) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 or TM2 hardware thermal control mechanism will activate. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Catastrophic temperature conditions are detectable using an Out of Specification status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Specification Status bit is set.

Changes to the temperature can be detected using two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts using the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.



6.5.3 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 or TM2 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC using PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When the processor's thermal sensor trips, the PROCHOT# signal is driven by the processor package. If only TM1 is enabled and the processor is above the TCC temperature trip point, PROCHOT# will be asserted and the core clocks modulated. If TM2 is enabled and the processor is above the TCC temperature trip point, it will enter the lowest programmed TM2 performance state. It is important to note that Intel recommends that both TM1 and TM2 be enabled.

When PROCHOT# is driven by an external agent, if only TM1 is enabled on the processor, then the processor will have the clocks modulated. If TM2 is enabled, then the processor will enter the lowest programmed TM2 performance state. It should be noted that Force TM1 on TM2, enabled using IA-32 Firmware, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when TM1, TM2, and Force TM1 on TM2 are all enabled, then the processor will still apply only TM2.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption.

Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power-intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

6.5.4 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 or TM2 are triggered and the temperature remains high, an "Out Of Specification" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

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7 Mechanical Package Specifications

7.1 Chapter Contents

This chapter contains the following information:

- "Pin Out Information"
- "Package Specifications"

7.2 Pin Out Information

Figure 7-1 describes the package pin out as viewed from the top of the package. Table 7-1, and Table 7-2 describe the Processor Pin out top view. Table 7-3 describes the pin out arranged alphabetically by signal name.

Table 7-1. Processor Pin Out (Top View—Columns 21-31)

	31	30	29	28	27	26	25	24	23	22	21	
AL	V _{SS_NCTF}	V _{SS_NCTF}	CDVO_T X3	CDVO_T X2	CDVO_T XSTB_O DD#		CDVO_C VREF	CDMI_R XCHAR#		CDMI_R XSTB_EV EN#	CDMI_R X6	AL
AK		CDVO_T XDPWR#		CDVO_T X4	CDVO_T X0	CDVO_T XSTB_EV EN#		CDVO_R COMPO	CDVO_V BLANK#	CDMI_R XSTB_O DD#		AK
AJ	LA_DATA P0	LA_DATA N0	V _{SS}	LA_DATA P1	V _{SS}		V _{SS}	V _{SS}		V _{SS}	V _{SS}	AJ
AH	LA_CLKP		V _{SS}		CDVO_S TALL#	CDVO_T X5		CDVO_T X1	CDVO_R COMP1	V _{CCP}		AH
AG		LA_CLKN		LA_DATA N1		V _{SS}				V _{SS}		AG
AF	LA_DATA N2	LA_DATA P2	V _{SS}	LA_DATA N3		V _{CCD180}		V _{CCA180}		V _{CCP}		AF
AE	LA_IBG		V _{SS}				V _{SS}		V _{SS}		V _{SS}	AE
AD	RSVD	LA_VBG	V _{SS}	LA_DATA P3		V _{CCD180}		V _{CCA180}		V _{CCP}		AD
AC		RSVD		V _{CCP}			V _{SS}			V _{SS}	V _{SS}	AC
AB	MIPI_DQ P0		V _{SS}									AB
AA	MIPI_DQ P1	MIPI_DQ N0	V _{SS}	V _{CCPAOAC}		V _{NN}		V _{MM}		V _{CC}		AA
Y		MIPI_DQ N1		MIPI_RC OMP			V _{NN}		V _{SS}		V _{SS}	Y
W	MIPI_CLK#	MIPI_CLK	V _{SS}	RSVD		V _{NN}		V _{CC}		V _{CC}		W
V	MIPI_DQ P2		V _{SS}				V _{NN}		V _{SS}		V _{SS}	V
U		MIPI_DQ N2		RSVD		V _{NN}		V _{CC}		V _{CC}		U



Table 7-1. Processor Pin Out (Top View—Columns 21-31)

	31	30	29	28	27	26	25	24	23	22	21	
T	MIPI_DQ P3	MIPI_DQ N3	VNNSENSE	VSS			VNN		VSS		VSS	T
R	VNN		VNN			VNN		VNN		VNN		R
P	VSS	VNN	VSS	VNN			VNN		VSS		VSS	P
N		VNN		VNN		VNN		VNN		VNN		N
M	VNN	VCC180	VNN	VCC180			VNN		VSS		VSS	M
L	VCC180		VCC180			VNN						L
K		VCC180		VCC180			VSS	VSS				K
J	SM_DQ1	SM_DQ0	VSS	SM_BS2								J
H	SM_DQ3		VSS			VCC180		VCC180		VCCPDDR		H
G	SM_DQS 1	SM_DQ2	VSS	SM_BS1			VSS		VSS		VSS	G
F		SM_DM0		SM_MA2		VCC180		VCC180		VCCPDDR		F
E	SM_DQ5		VSS			VSS		VSS				E
D	SSM_DQ 4		SM_MA4	SM_MA1 2		SM_BS0	SM_MA3	SM_MA7		SM_MA8	SM_MA0	D
C	SM_DQ6	VSS	VSS		VSS	VSS		VSS	VSS		VSS	C
B	SM_DQ7		SM_DQ8	SM_DQ1 0		SM_DQS 0	SM_DQ1 2	SM_DQ1 4		SM_RCV ENOUT	SM_RCV ENIN	B
A	VSS_NCTF	SM_DQ9	SM_DQ1 1		SM_DM1	SM_MA1 0		SM_DQ1 3	SM_DQ1 5		SM_MA1	A
	31	30	29	28	27	26	25	24	23	22	21	

Table 7-1. Processor Pin Out (Top View—Columns 11-20) (Sheet 1 of 2)

	20	19	18	17	16	15	14	13	12	11	
AL		CDMI_RX 4	CDMI_RX 1	CDMI_CV REF		CDMI_TX DPWR#	CDMI_TX 6		CDMI_TX 3	CDMI_TX 1	AL
AK	CDMI_RX 7	CDMI_RX 3		CDMI_RX 0	CDMI_GV REF		CDMI_TX 7	CDMI_TX 4	CDMI_TX 2		AK
AJ		VSS	VSS	VSS		VSS	VSS		VSS	VSS	AJ
AH	CDMI_RX DPWR#	CDMI_RX 5		CDMI_RX 2	CDMI_TX CHAR#		CDMI_TX 5	CDMI_TX 0	VCCP		AH
AG	VSS				VSS		VSS				AG
AF	CDVO_GV REF		VNN		VCCP		VCCP		VNN		AF
AE		VSS		VSS		VSS		VSS		VSS	AE
AD	VCCP		VNN		VCCP		VCCP		VNN		AD
AC		VSS		VSS		VSS		VSS		VSS	AC
AB											AB
AA	VCC		VCC		VCC		VCC		VCC		AA
Y		VSS		VSS		VSS		VSS		VSS	Y



Table 7-1. Processor Pin Out (Top View—Columns 11-20) (Sheet 2 of 2)

	20	19	18	17	16	15	14	13	12	11	
W	V _{CC}		V _{CC}		V _{CC}		V _{CC}		V _{CC}		W
V		V _{SS}		V _{SS}		V _{SS}		V _{SS}		V _{SS}	V
U	V _{CC}		V _{CC}		V _{CC}		V _{CC}		V _{CC}		U
T		V _{SS}		V _{SS}		V _{SS}		V _{SS}		V _{SS}	T
R	V _{NN}		V _{NN}		V _{NN}		V _{NN}		V _{NN}		R
P		V _{SS}		V _{SS}		V _{SS}		V _{SS}		V _{SS}	P
N	V _{NN}		V _{NN}		V _{NN}		V _{NN}		V _{NN}		N
M		V _{SS}		V _{SS}		V _{SS}		V _{SS}		V _{SS}	M
L											L
K	V _{SS}	V _{SS}	V _{SS}				V _{SS}	V _{SS}	V _{SS}		K
J											J
H	V _{CC180}		V _{CC180}		V _{CCPDDR}		V _{CC180}		V _{CC180}		H
G		V _{SS}		V _{SS}		V _{SS}		V _{SS}		V _{SS}	G
F	V _{CC180}		V _{CC180}		V _{CCPDDR}		V _{CC180}		V _{CC180}		F
E	V _{SS}		V _{SS}				V _{SS}		V _{SS}		E
D		SM_CK0	SM_CK0#		V _{CC180SR}	RSVD	SM_MA14		SM_RAS#	SM_WE#	D
C	V _{SS}	V _{SS}		V _{SS}	V _{SS}		V _{SS}	V _{SS}	V _{SS}		C
B		SM_RCO MP	SM_MA6		SM_SREN #	SM_MA11	SM_DQ25		SM_DQ27	SM_DQS3	B
A	SM_MA9	SM_CKE0		SM_CKE1	SM_MA5		SM_MA13	SM_DQ24	SM_DQ26		A
	20	19	18	17	16	15	14	13	12	11	

Table 7-2. Processor Pin Out (Top View—Columns 1-10) (Sheet 1 of 2)

	10	9	8	7	6	5	4	3	2	1	
AL		CDMI_TX STB_ODD #	CDMI_RC OMP1	PRDY#		BPM2#	BPM1#		VID6	V _{SS_NCTF}	AL
AK	CDMI_TX STB_EVEN#	CDMI_RC OMP0		GTLREF0	PREQ#		BPM3#	RSVD	VID4		AK
AJ		V _{SS}	V _{SS}	V _{SS}		V _{SS}	V _{SS}		V _{SS}	VID1	AJ
AH	IERR	BPM0#		RSVD	VID5		VID2	VID3	VID0		AH
AG	V _{SS}		V _{SS}			V _{SS}	RSVD	V _{SS}	RSVD	RSVD	AG
AF	V _{CCP}		V _{CCP}		V _{NN}			V _{SS}		PROCHOT #	AF
AE		V _{SS}		V _{SS}		V _{SS}	THERMTR IP#		PWRMOD E1		AE
AD	V _{CCP}		V _{CCP}		V _{NN}		VIDEN0	V _{SS}	PWRMOD E2	VIDEN1	AD
AC		V _{SS}				V _{CCP}		V _{SS}		PWRMOD E0	AC



Table 7-2. Processor Pin Out (Top View—Columns 1-10) (Sheet 2 of 2)

	10	9	8	7	6	5	4	3	2	1	
AB							V _{CCPAOAC}	V _{CC}	V _{SS}	V _{CC}	AB
AA	V _{CC}		V _{CC}	V _{CC}			V _{CC}		V _{CC}		AA
Y		V _{SS}	V _{SS}		V _{SS}			V _{SS}		V _{SS}	Y
W	V _{CC}		V _{CC}	V _{CC}			V _{CC}	V _{CC}	V _{CC}	V _{CC}	W
V		V _{SS}	V _{SS}		VSSSENS E		V _{SS}		V _{SS}		V
U	V _{CC}		V _{CC}	V _{CC}			V _{CC}	V _{CC}	V _{CC}	V _{CC}	U
T		V _{SS}	V _{SS}		V _{CCA}			VCCSENS E		V _{CCA}	T
R	V _{NN}		V _{NN}	V _{NN}			V _{SS}		V _{SS}		R
P		V _{SS}	V _{SS}		V _{CCA}		RSVD	V _{SS}	RSVD	V _{CCPAOAC}	P
N	V _{NN}		V _{NN}	V _{SS}				V _{SS}		BCLK_N	N
M		V _{SS}	V _{SS}		V _{CCP}		RSVD	V _{SS}	BCLK_P	RSVD	M
L							RSVD		RSVD		L
K		V _{SS}		V _{CCP}		V _{CCPAOAC}		V _{SS}		RSVD	K
J							V _{SS}	V _{SS}	TMS	TRST#	J
H	V _{CCPDDR}		V _{CC180}		V _{CCP}		TDO		TCK		H
G		V _{SS}		V _{SS}		V _{SS}	BSEL1	V _{SS}	RSVD	V _{SS}	G
F	V _{CCPDDR}		V _{CC180}		V _{CCP}			V _{SS}		TDI	F
E			V _{SS}		V _{SS}		SM_CAS#		RSVD		E
D		SM_ODT0	SM_ODT1	SM_CS1#		SM_CS0#	GTLREF1	V _{SS}	SM_DQ23	SM_DQ22	D
C	V _{SS}	V _{SS}		V _{SS}	V _{SS}			V _{SS}		SM_DQ20	C
B		SM_DQ29	SM_DQ31	SM_DQ17		SM_DQ19	SM_DM2	SM_DQS2	SM_DQ21	V _{SS_NCTF}	B
A	SM_DM3	SM_DQ28		SM_DQ30	SM_DQ16		SM_DQ18		V _{SS_NCTF}		A
	10	9	8	7	6	5	4	3	2	1	



Table 7-3. Pin Out—Ordered by Signal Name (Sheet 1 of 6)

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
BCLK_P	M2	BCLK_N	N1	BPM0#	AH9
BPM1	AL4	BPM2#	AL5	BPM3#	AK4
BSEL1	G4	CDMI_CVREF	AL17	CDMI_RXDPWR#	AH20
CDMI_TXDPWR#	AL15	CDMI_GVREF	AK16	CDMI_RCOMP0	AK9
CDMI_RCOMP1	AL8	CDMI_RX0	AK17	CDMI_RX1	AL18
CDMI_RX2	AH17	CDMI_RX3	AK19	CDMI_RX4	AL19
CDMI_RX5	AH19	CDMI_RX6	AL21	CDMI_RX7	AK20
CDMI_RXCHAR#	AL24	CDMI_RXSTB_ODD#	AK22	CDMI_RXSTB_EVEN#	AL22
CDMI_TX0	AH13	CDMI_TX1	AL11	CDMI_TX2	AK12
CDMI_TX3	AL12	CDMI_TX4	AK13	CDMI_TX5	AH14
CDMI_TX6	AL14	CDMI_TX7	AK14	CDMI_TXCHAR#	AH16
CDMI_TXSTB_ODD#	AL9	CDMI_TXSTB_EVEN#	AK10	CDVO_CVREF	AL25
CDVO_GVREF	AF20	CDVO_RCOMP0	AK24	CDVO_RCOMP1	AH23
CDVO_STALL#	AH27	CDVO_TX0	AK27	CDVO_TX1	AH24
CDVO_TX2	AL28	CDVO_TX3	AL29	CDVO_TX4	AK28
CDVO_TX5	AH26	CDVO_TXDPWR#	AK30	CDVO_TXSTB_EVEN#	AK26
CDVO_TXSTB_ODD#	AL27	CDVO_VBLANK#	AK23	GTLREF0	AK7
GTLREF1	D4	IERR	AH10	LA_CLKN	AG30
LA_CLKP	AH31	LA_DATAN0	AJ30	LA_DATAN1	AG28
LA_DATAN2	AF31	LA_DATAN3	AF28	LA_DATAP0	AJ31
LA_DATAP1	AJ28	LA_DATAP2	AF30	LA_DATAP3	AD28
LA_IBG	AE31	LA_VBG	AD30	MIPI_CLK	W30
MIPI_CLK#	W31	MIPI_DQN0	AA30	MIPI_DQN1	Y30
MIPI_DQN2	U30	MIPI_DQN3	T30	MIPI_DQP0	AB31
MIPI_DQP1	AA31	MIPI_DQP2	V31	MIPI_DQP3	T31
MIPI_RCOMP	Y28	PRDY#	AL7	PREQ#	AK6
PROCHOT#	AF1	PWRMODE0	AC1	PWRMODE1	AE2
PWRMODE2	AD2	RSVD	AG4	RSVD	L4
RSVD	AG1	RSVD	AG2	RSVD	P2
RSVD	P4	RSVD	G2	RSVD	E2
SM_BS0	D26	SM_BS1	G28	SM_BS2	J28
SM_CAS#	E4	SM_CK0	D19	SM_CK0#	D18
SM_CKE0	A19	SM_CKE1	A17	SM_CS0#	D5



Table 7-3. Pin Out—Ordered by Signal Name (Sheet 2 of 6)

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
SM_CS1#	D7	SM_DM0	F30	SM_DM1	A27
SM_DM2	B4	SM_DM3	A10	SM_DQ0	J30
SM_DQ1	J31	SM_DQ10	B28	SM_DQ11	A29
SM_DQ12	B25	SM_DQ13	A24	SM_DQ14	B24
SM_DQ15	A23	SM_DQ16	A6	SM_DQ17	B7
SM_DQ18	A4	SM_DQ19	B5	SM_DQ2	G30
SM_DQ20	C1	SM_DQ21	B2	SM_DQ22	D1
SM_DQ23	D2	SM_DQ24	A13	SM_DQ25	B14
SM_DQ26	A12	SM_DQ27	B12	SM_DQ28	A9
SM_DQ29	B9	SM_DQ3	H31	SM_DQ30	A7
SM_DQ31	B8	SM_DQ4	D31	SM_DQ5	E31
SM_DQ6	C31	SM_DQ7	B31	SM_DQ8	B29
SM_DQ9	A30	SM_DQS0	B26	SM_DQS1	G31
SM_DQS2	B3	SM_DQS3	B11	SM_MA0	D21
SM_MA1	A21	SM_MA2	F28	SM_MA3	D25
SM_MA4	D29	SM_MA5	A16	SM_MA6	B18
SM_MA7	D24	SM_MA8	D22	SM_MA9	A20
SM_MA10	A26	SM_MA11	B15	SM_MA12	D28
SM_MA13	A14	SM_MA14	D14	SM_ODT0	D9
SM_ODT1	D8	SM_RAS#	D12	SM_RCOMP	B19
SM_RCVENIN	B21	SM_RCVENOUT	B22	SM_SREN#	B16
SM_WE#	D11	TCK	H2	TDI	F1
TDO	H4	RSVD	L2	RSVD	K1
RSVD	M4	RSVD	M1	RSVD	AK3
RSVD	AH7	RSVD	D15	RSVD	AC30
RSVD	AD31	THERMTRIP#	AE4	RSVD	W28
RSVD	U28	TMS	J2	TRST#	J1
VCC	AA10	VCC	AA12	VCC	AA14
VCC	AA16	VCC	AA18	VCC	AA2
VCC	AA20	VCC	AA22	VCC	AA4
VCC	AA7	VCC	AA8	VCC	AB1
VCC	AB3	VCC	U1	VCC	U10
VCC	U12	VCC	U14	VCC	U16
VCC	U18	VCC	U2	VCC	U20



Table 7-3. Pin Out—Ordered by Signal Name (Sheet 3 of 6)

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
VCC	U22	VCC	U24	VCC	U3
VCC	U4	VCC	U7	VCC	U8
VCC	W1	VCC	W10	VCC	W12
VCC	W14	VCC	W16	VCC	W18
VCC	W2	VCC	W20	VCC	W22
VCC	W24	VCC	W3	VCC	W4
VCC	W7	VCC	W8	VCC180	F12
VCC180	F14	VCC180	F18	VCC180	F20
VCC180	F24	VCC180	F26	VCC180	F8
VCC180	H12	VCC180	H14	VCC180	H18
VCC180	H20	VCC180	H24	VCC180	H26
VCC180	H8	VCC180	K28	VCC180	K30
VCC180	L29	VCC180	L31	VCC180	M28
VCC180	M30	VCC180SR	D16	VCCA	P6
VCCA	T1	VCCA	T6	VCCA180	AD24
VCCA180	AF24	VCCD180	AD26	VCCD180	AF26
VCCP	K7	VCCP	AC28	VCCP	AC5
VCCP	AD10	VCCP	AD14	VCCP	AD16
VCCP	AD20	VCCP	AD22	VCCP	AD8
VCCP	AF10	VCCP	AF14	VCCP	AF16
VCCP	AF22	VCCP	AF8	VCCP	F6
VCCP	H6	VCCP	M6	VCCP	AH12
VCCP	AH22	VCCPAOAC	AB4	VCCPAOAC	AA28
VCCPAOAC	K5	VCCPAOAC	P1	VCCPDDR	F10
VCCPDDR	F16	VCCPDDR	F22	VCCPDDR	H10
VCCPDDR	H16	VCCPDDR	H22	VCCSENSE	T3
VID0	AH2	VID1	AJ1	VID2	AH4
VID3	AH3	VID4	AK2	VID5	AH6
VID6	AL2	VIDEN0	AD4	VIDEN1	AD1
VMM	AA24	VNN	AA26	VNN	AD12
VNN	AD18	VNN	AD6	VNN	AF12
VNN	AF18	VNN	AF6	VNN	L26
VNN	M25	VNN	M29	VNN	M31
VNN	N10	VNN	N12	VNN	N14



Table 7-3. Pin Out—Ordered by Signal Name (Sheet 4 of 6)

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
VNN	N16	VNN	N18	VNN	N20
VNN	N22	VNN	N24	VNN	N26
VNN	N28	VNN	N30	VNN	N8
VNN	P25	VNN	P28	VNN	P30
VNN	R10	VNN	R12	VNN	R14
VNN	R16	VNN	R18	VNN	R20
VNN	R22	VNN	R24	VNN	R26
VNN	R29	VNN	R31	VNN	R7
VNN	R8	VNN	T25	VNN	U26
VNN	V25	VNN	W26	VNN	Y25
VNNSENSE	T29	VSS_NCTF	A2	VSS_NCTF	A31
VSS	AA29	VSS	AB2	VSS	AB29
VSS	AC11	VSS	AC13	VSS	AC15
VSS	AC17	VSS	AC19	VSS	AC21
VSS	AC22	VSS	AC25	VSS	AC3
VSS	AC9	VSS	AD29	VSS	AD3
VSS	AE11	VSS	AE13	VSS	AE15
VSS	AE17	VSS	AE19	VSS	AE21
VSS	AE23	VSS	AE25	VSS	AE29
VSS	AE5	VSS	AE7	VSS	AE9
VSS	AF29	VSS	AF3	VSS	AG10
VSS	AG14	VSS	AG16	VSS	AG20
VSS	AG22	VSS	AG26	VSS	AG3
VSS	AG5	VSS	AG8	VSS	AH29
VSS	AJ11	VSS	AJ12	VSS	AJ14
VSS	AJ15	VSS	AJ17	VSS	AJ18
VSS	AJ19	VSS	AJ2	VSS	AJ21
VSS	AJ22	VSS	AJ24	VSS	AJ25
VSS	AJ27	VSS	AJ29	VSS	AJ4
VSS	AJ5	VSS	AJ7	VSS	AJ8
VSS	AJ9	VSS_NCTF	AL1	VSS_NCTF	AL30
VSS_NCTF	AL31	VSS_NCTF	B1	VSS	C10
VSS	C12	VSS	C13	VSS	C14
VSS	C16	VSS	C17	VSS	C19



Table 7-3. Pin Out—Ordered by Signal Name (Sheet 5 of 6)

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
VSS	C20	VSS	C21	VSS	C23
VSS	C24	VSS	C26	VSS	C27
VSS	C29	VSS	C3	VSS	C30
VSS	C6	VSS	C7	VSS	C9
VSS	D3	VSS	E12	VSS	E14
VSS	E18	VSS	E20	VSS	E24
VSS	E26	VSS	E29	VSS	E6
VSS	E8	VSS	F3	VSS	G11
VSS	G13	VSS	G15	VSS	G17
VSS	G19	VSS	G21	VSS	G23
VSS	G25	VSS	G29	VSS	G3
VSS	G5	VSS	G7	VSS	G9
VSS	H29	VSS	J29	VSS	J3
VSS	J4	VSS	K12	VSS	K13
VSS	K14	VSS	K18	VSS	K19
VSS	K20	VSS	K24	VSS	K25
VSS	K3	VSS	K9	VSS	M11
VSS	M13	VSS	M15	VSS	M17
VSS	M19	VSS	M21	VSS	M23
VSS	M3	VSS	M8	VSS	M9
VSS	N3	VSS	N7	VSS	P11
VSS	P13	VSS	P15	VSS	P17
VSS	P19	VSS	P21	VSS	P23
VSS	P29	VSS	P3	VSS	P31
VSS	P8	VSS	P9	VSS	R2
VSS	R4	VSS	T11	VSS	T13
VSS	T15	VSS	T17	VSS	T19
VSS	T21	VSS	T23	VSS	T28
VSS	T8	VSS	T9	VSS	V11
VSS	V13	VSS	V15	VSS	V17
VSS	V19	VSS	V2	VSS	V21
VSS	V23	VSS	V29	VSS	V4
VSS	V8	VSS	V9	VSS	W29
VSS	Y1	VSS	Y11	VSS	Y13



Table 7-3. Pin Out—Ordered by Signal Name (Sheet 6 of 6)

Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #
VSS	Y15		VSS	Y17		VSS	Y19
VSS	Y21		VSS	Y23		VSS	Y3
VSS	Y6		VSS	Y8		VSS	Y9
VSS	G1		VSSSENSE	V6			



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