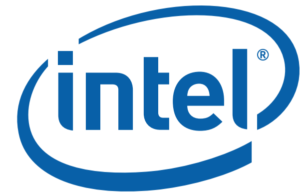

Intel® Atom™ Processor D400/D500 Storage Platform

Addendum

March 2010

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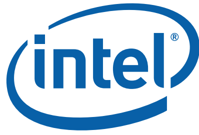

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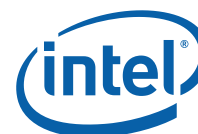

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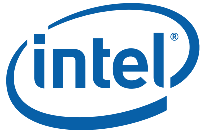

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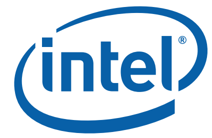

Revision History

Date	Revision	Description
March 2009	001	Initial Release.

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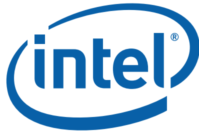


1.0 DMI Interfaces

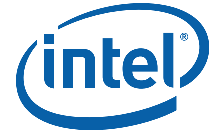
This section documents the routing guidelines for DMI interfaces on Intel® Atom™ Processor D400/D500 Series (D400/D500). The general routing guidelines discussed in Section 1.1, "DMI Layout Design Guidelines" apply to both interfaces. Section 1.2, "DMI Topology Guidelines" list routing specifics per interface.

Note: Only DMI is supported on this platform. The DMI link between the Intel® Atom™ Processor and the ICH9R have similar functionality with different electrical considerations as called out below:

- DMI is used when the link is DC coupled.
- See Section 1.4 for additional details.

Table 1. PCI Express Signal Groups

Section	Signal Group	Signal Name	Description
Section 1.2	ICH Input DMI/ESI	DMIRXN[3:0] DMIRXP[3:0]	DMI/ESI Receive Differential Pair
Section 1.2	ICH Output DMI/ESI	DMITXN[3:0] DMITXP[3:0]	DMI/ESI Transmit Differential Pair
Section 1.3	Processor DMI/ESI COMP	DMI_COMP	Intel® Atom™ Processor D400/D500 Series Compensation
Section 1.3	ICH DMI/ESI COMP	DMI_ZCOMP DMI_IRCOMP	ICH9R DMI/ESI Current Compensation



1.1 DMI Layout Design Guidelines

This section contains information and details for layout and routing guidelines.

One of the key points for DMI board design is to follow a set of rules that minimize losses, jitter, crosstalk, and mode conversion for differential traces.

Loss is attenuation of the differential voltage signal swing on the trace from transmitter to receiver. The trace is subject to resistive, dielectric and skin effect losses. Loss increases as trace length or frequency increases. In addition, conductor loss increases as trace width decreases. Vias and connectors that are a part of the interconnect also introduce losses. Other factors such as data patterns, edge rates, impedance discontinuities, crosstalk, and so forth will also contribute to system loss. Total loss allowed on the interconnect is defined in the PCI Express Base Specification. PCB traces introduces as much as 0.25 to 0.35dB of loss per inch per differential pair, based on inherent physical properties of the PCB differential pairs. It is best to keep trace routing as short as possible without breaking minimum specifications.

Jitter (including jitter from crosstalk) consists of random and deterministic contributions to signal edge timing that reduce the signal valid time. PCB traces introduce upwards of 1-5ps of jitter per inch per differential pair, based on inherent physical properties of the PCB differential pairs. Other factors, such as data patterns, edge rates, impedance discontinuities, crosstalk, and so forth will also contribute to system jitter. Therefore, it is best to keep trace length within specifications.

Crosstalk is the coupling of energy from one signal trace to the other which results in the signal voltage and phase change. There are two kinds of crosstalk, Far-End (FEXT) and Near-End (NEXT). Whether the transmitter and receiver pairs are interleaved, the Far-End appears at the transmitter or receiver. Crosstalk within the differential pair is not a concern. Crosstalk between differential pairs are minimized by keeping a large pair-to-pair spacing compared to spacing within a pair.

Mode conversions are due to imperfections and other trace mismatches on the interconnect which transform differential mode voltage to common mode voltage and vice versa. For example, length mismatch within pairs or an asymmetric via layout cause mode conversion.

Differential signaling encodes information in the difference between the voltages on two nets. The differential receiver is designed to be very sensitive to this difference, while being insensitive to portions of the signal that are similar (the common-mode signal). It is important to equalize the total length of the traces in the pair throughout the trace; use equal segments of trace length along the entire length of the pair. Tight coupling within the differential pair and increased spacing to other differential pairs helps to minimize EMI and crosstalk.

Trace segment length matching within pairs is required to ensure trace lengths are equal on a segment-by-segment basis. The compensation is done using a bend in opposite direction, or adding serpentine bumps (wiggles) to the shorter one of the pair. Once the guideline is met, further reduction in the length mismatch of signals within a differential pair is done at any location along the routing of the signals. Examples of segments include breakout areas, routes between two vias, routes between an AC coupling capacitor and a connector pin, etc. The points of discontinuity are the via, the capacitor pad, or the connector pin. In addition, correct length mismatches, closely following the mismatch site to minimize common mode conversion effects.

See Section 1.1.6, “Via Requirements and Usage” on page 11 for via requirements.

1.1.1 Impedance Requirements

For the reference stack-up, reference *Intel® Atom™ Processor D400/D500 Series Specification Update*, for trace widths and impedance targets.

Stripline traces are routed on internal layers. Signals travel slower on stripline traces than on microstrip traces. They have a very low FEXT and very low dispersion.

Microstrip traces are routed on the outer layers. Signals travel a bit faster on the microstrip traces compared to stripline traces. They have significant FEXT and notable frequency and mode dependence of velocity.

1.1.2 Reference Planes

The concept of reference planes is important for DMI/ESI traces even when routed as tightly coupled differential pairs. Since a large amount of coupling to the reference plane still occurs with differential pairs, adhere to the following guidelines:

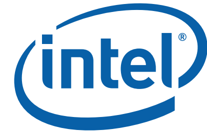
- It is preferred that DMI/ESI traces on the system board reference the ground (GND) plane.
- Avoid traces discontinuities in the reference plane, such as splits and other voids.
  - Good reference planes help to minimize any AC Common mode voltage found on the differential pair as well as benefiting signal quality and EMI impacts.
- When routing near the edge of their reference plane, maintain traces for at least a 20 mil air gap to the edge of the plane.
- Traces of a differential pair need to remain over the same reference plane for the entire length of the differential pair. When for some reason a differential pair changes routing layers, the reference plane remains constant and use GND stitching vias to tie the two reference planes together.
  - One to three GND stitching vias per differential pair is recommended.
  - Locate GND stitching vias as close as possible to, and in symmetry with, each signal via in order to minimize return path discontinuities.
  - For example, place a single stitching via directly between two signal vias of a differential pair, while an additional stitching via on either side of the two signal vias ps preferred. Generally, the more stitching vias that are accommodated, the better.

As with most other high-speed signals, DMI/ESI traces do not cross any splits or voids as previously mentioned. However, it is acknowledged for the possibility of a trace to be partially routed over a via anti-pad void in the LGA/BGA escape area. minimize the amount of the trace that is over the void in terms of the length and percentage of the width of the trace; at worst, to no more than half of the trace width over the via anti-pad at any given time.

1.1.3 Breakout Routing Guidelines

Use the following guidelines for breakout areas of a DMI/ESI interconnect.

- DMI/ESI signal pinouts are to be broken out, or grouped, as differential pairs.
- Tightly coupled pairs in breakout region need to follow breakout width and space guidelines. Section 1.2 has detailed breakout routing allowances for each interface.
- Breakout sections also require special care in terms of crosstalk management, since differential pairs are likely to be tightly grouped. Minimize congested routing lengths since crosstalk impacts are proportional to length of spacing encroachment.



1.1.4 Length Matching

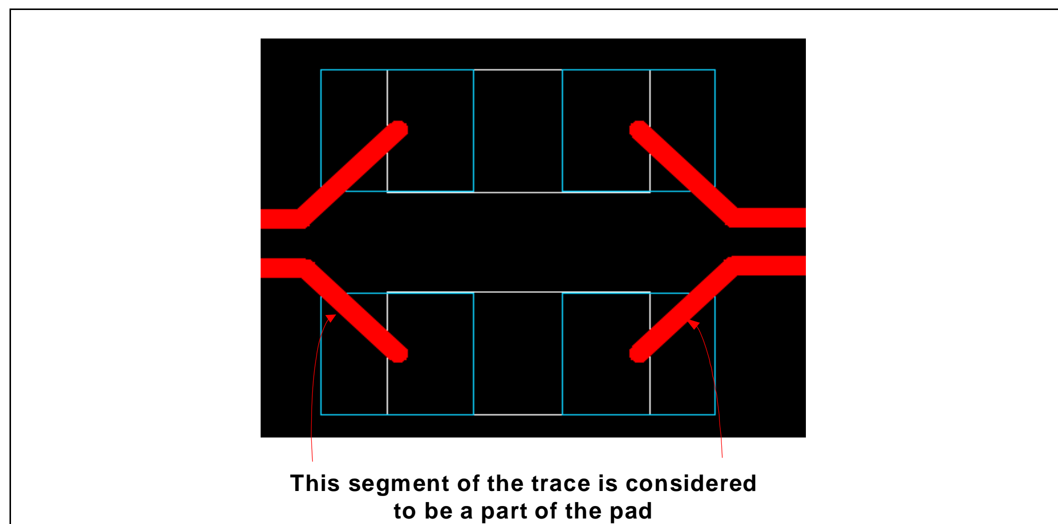
The following are length matching guidelines for DMI/ESI differential pairs:

- Length matching between pairs of a link is not generally required due to the large amount of skew allowed between pairs by the specification. However, it is desirable to keep the differences within a range of 0″ to 7″ to help minimize latency.
- Match the length of both nets within a differential pair, allowing no more than a 5 mil delta between the lengths of the two signals.
- Length match each net within a differential pair whenever possible on a segment-by-segment basis at the point of discontinuity. Examples of segments include breakout areas, routes running between two vias, routes between an AC coupling capacitor and a connector pin, and so forth. The points of discontinuity are the via, the capacitor pad, or the connector pin.
    - It is recommended to keep the running skew less than 20mil (10mil is preferred). For skew larger than 20mils, the mis-match needs to be compensated within 600mils of the mis-match.

When length matching compensation occurs, make it as close as possible to the point where the variation occurs.

- In determining the overall length of a given net in a differential pair, use pad or pin edge-to-edge distances rather than the total etch present, unless the amount of etch routing into each and every pad and pin is identical. This is due to the amount of etch within a given pad is electrically part of the pad itself.
- Only the etch outside of the pad edge itself is relevant to the overall length of a differential pair. For example, when the DP signal of the differential pair has an extra 5 mils of etch length compared to the DN signal, and the extra 5 mils occurs due to extra etch extending into an edge finger, consider the two nets to be of identical length. Similarly, trying to length match nets by adding etch inside a pad boundary (such as extra bends inside the pad itself) does not produce the intended length matching effect on the interconnect. See Figure 1 below for an example.

Figure 1. Etch Within a Pad



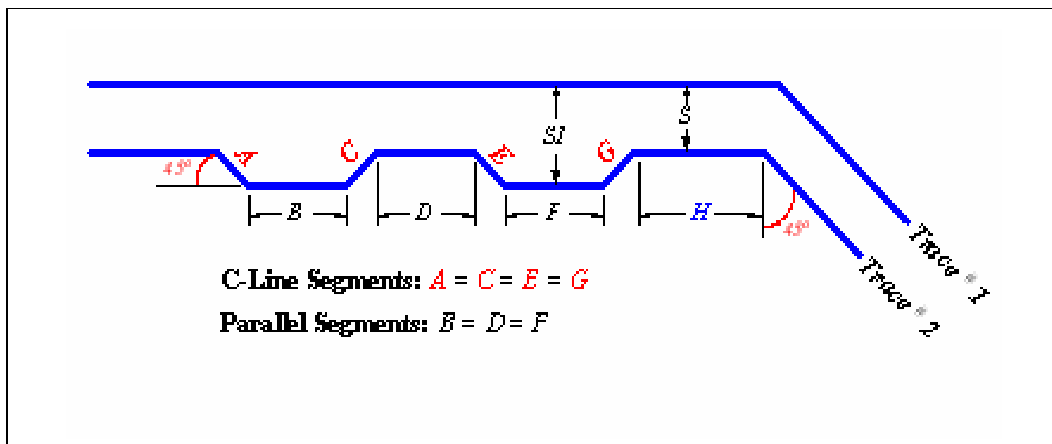
1.1.5 Bends

While serpentine routing is not required to match lengths from one differential pair to another, bends are likely encountered while routing an interconnect. Follow these guidelines and considerations concerning bends:

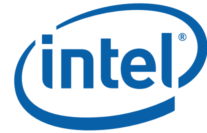
- Keep bends to a minimum. Bends can introduce common mode noise into the system, which can affect the signal integrity of the differential pair.
- If bends are used, they must be at a 45° angle or smaller, do not use 90° bends or turns.
- For coupled differential pairs, every attempt should be made to match the number of left and right bends as closely as possible to minimize skew due to length differences between each signal to the differential pair.
- Alternate left and right turns to minimize skew due to length difference between each signal of the differential pair.

  Matching the number of right and left turns and alternating such bends helps to minimize the amount of skew between rising or falling edges of a propagating differential signal pair at any point along the length of the pairs. For example, a series of the left turns adds length to the outside trace that increases the delay of that trace. Although this length could potentially be made up at the end of the trace route, thereby ensuring that the signal pair is in sync at both the beginning and the end of the trace route, the signal pair is actually out of synchronization in the area around the series of left turns.
- Whenever it is not possible to match the number of bends, determine the length required to match the two traces as a result of the difference in the number of bends, and then add half of this length to each end of the shorter trace of the pair. For example, if the D+ of a highly coupled differential pair signal was 10 mils shorter than the D- signal due to bends, add 5 mils to the D+ signal line before the bends occur, and add 5 mils after the bends complete to achieve an overall length match between the D+ and D- signals within the pair. This solves skew mismatch, but not the common mode noise effects that were introduces

Figure 2. Intra-Pair Length Matching



Note: Rule: S1 < 2 x S, B=D=F=H=3 x w, 45° bend, where w is the trace width.

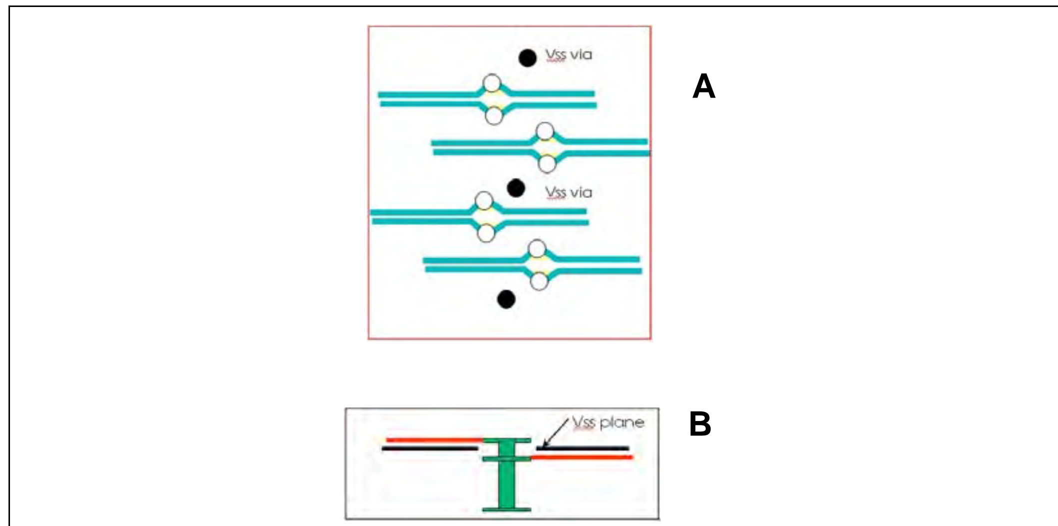


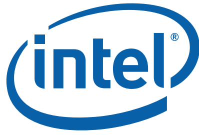
1.1.6 Via Requirements and Usage

Vias are allowed on DMI/ESI interconnects, but limit their use. Via guidelines are as follows:

- Vias impact the overall loss and jitter budget and therefore be carefully used since they impact the overall length of route achievable.
- Chip-to-chip on motherboard: Intel recommends no more than four vias per TX trace and four vias per RX trace.
  - One via located at each chip breakout section to transition layers when routing chip to chip.
- The number of vias for each signal line within a differential pair – whether or not that pair is tightly coupled – must be matched because each signal within the differential pair must stay on the same layer.
  - When for some reason, a design requires four vias and the differential pairs change routing layers, the reference plane remains constant, and use stitching vias to tie the two ground reference planes together.
    - Add 1 Vss via per 2 differential via pairs (4 signal vias) with ≤50mils for the nearest and ≤200mils for the farthest. See picture (A) in Figure 3.
  - When layer transition keeps the same Vss plane (e.g., layer transition from layer 1 to 3) then there is no need for GND vias. See picture (B) in Figure 3.
- Have pads on unused via internal layers removed to minimize excess via capacitance.

Figure 3. Ground vias for Layer Transition





- Routing clearance from anti-pad for minimum signaling impact. See Table 2 for recommendations.

Table 2. Via Anti-Pad Routing Clearance

Type	Guideline	Notes
Fast-switching power signals (>1A/ns)	5xh	1, 2
Other high-speed signals	3xh	1, 3
Static, low-current signals or same type of signal (Rx or Tx)	2xh	1, 4
Mounting hole anti-pads	>0xh	1

Notes:
1. When a signal has violations in several or all cases above, then maximum count not applicable and review situation by signal integrity expert.
2. Violations - 2(maximum) allowed at >3xh when and only when signal not routed at worst case conditions (i.e., maximum length, longest via stub, etc.).
3. Violations - 2(maximum) allowed at >0xh.
4. Violations - 4(maximum) allowed at >0xh.

Vias on the differential pair not only match in number but in relative location. This is especially important for tightly coupled pairs where trace lengths before and after the via transition matched to within a 5mil delta. At the same time, the overall trace route also needs to conform to a total of a 5mil delta between the DP and DN signals within the differential pair.

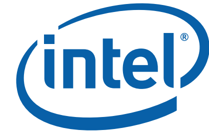
For example, when a via is needed to escape one half of a differential pair from a BGA/LGA, then both traces in the differential pair must transition through a via at the BGA/LGA. When there is a via transition in the middle of the trace, then both traces in the pair must have the vias located at the exact same location on the trace for tightly coupled pairs.

Table 3. Mother Board via Requirements

	Via 1	Via 2
Fill Hole Size	10mils	8mils
Pad Size	20mils	18mils
Anti-pad size	30mils	28mils
Pair center-to-center spacing	40mils	40mils

Note: Implementation of the RX and TX topologies have the traces entering the connector from the bottom layer and not the top layer in order to avoid signal degradation. Example for TX and RX topology is as shown in Figure 4, “Routing into AC Caps” on page 14.

Note: Place components such as LAI pad and cap on the bottom side of the board.



1.1.7 Passive Components and Connectors

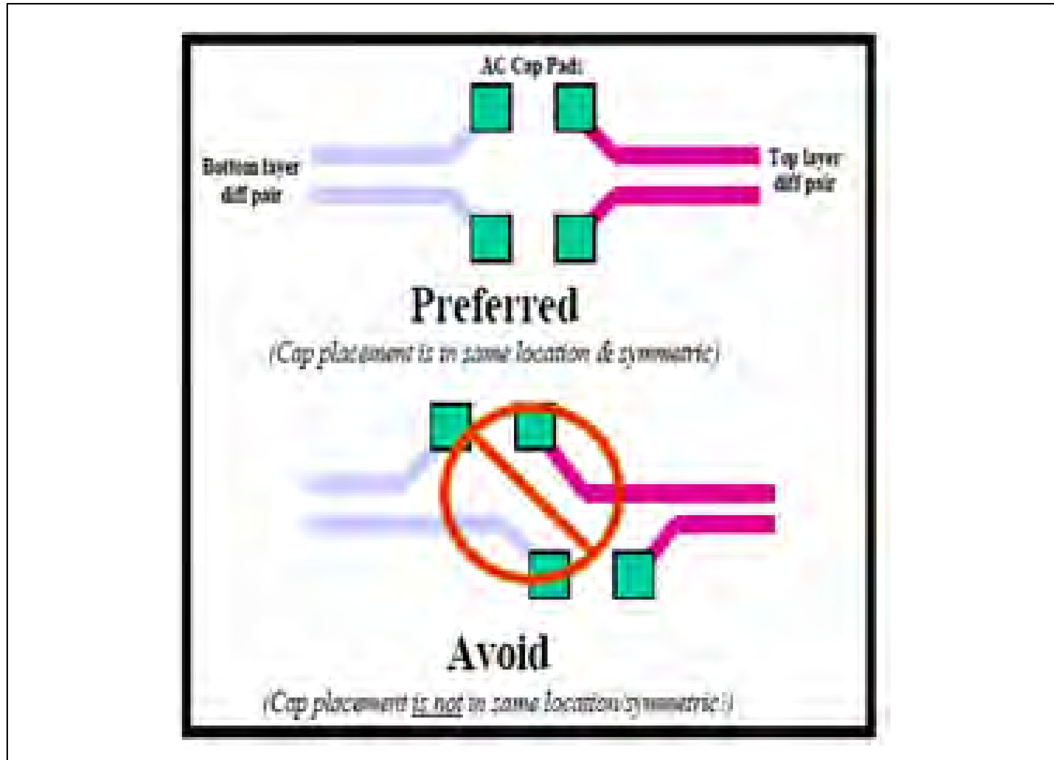
1.1.7.1 AC Coupling Capacitors

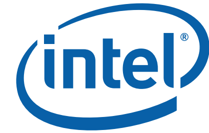
Each DMI lane is AC coupled between the transmitter and receiver. The AC coupling capacitor is located on the motherboard for down devices. Use the following guidelines for AC coupling capacitors:

- Add-in cards:
  - — AC coupling capacitors are located on the card itself for each of the TX pairs originating from the add-in card device and going to a RX pair on the motherboard.
  - — AC coupling capacitors are required on the motherboard itself for the TX pairs originating from the motherboard device and going to the add-in card RX pairs.
- Locate capacitors for differential pair traces at the same location along the differential traces (not staggered from one trace to the other), and place them as close to each other as possible as allowed by DFM rules.
- While size 0603 capacitors will be acceptable, size 0402 capacitors are strongly encouraged. The smaller the package size, the less the inductance introduced.
- Use the same package size of capacitor for each signal in a differential pair.
- C-packs are not allowed for DMI AC coupling capacitor purposes.
- Pad sizes for each of the capacitors are to be the minimum allowed per DFM to minimize parasitic impacts.
- The spec requires that a value anywhere between a minimum of 75nF and a maximum of 200nF be used for each of the capacitors.
- Tolerance values of the capacitors are irrelevant as long as the overall range of tolerances falls within the specification minimum/maximum values of 75nF to 200nF.
- Dielectric properties are not a major consideration for AC coupling capacitors. It is anticipated that any type from COG capacitors to X7R is acceptable as long as the capacitors meet all other requirements.
- Some capacitors perform at less than 50% of their nominal value when exposed to heat. This causes the value of the capacitor to fall out side the range defined by the minimum and maximum specification values. This characteristic has lead to device training issues on the PCI Express bus. When selecting components, consider a capacitor tolerance to temperature. Board designers, be cautious when placing capacitors next to devices that generate heat such as power FETs.

Have symmetrical “breakout” into and out of the capacitors for both signal lines in a differential pair. Minimize such an area in order to maximize the amount of coupling between the signal pairs. See Figure 4 for a routing example.

Figure 4. Routing into AC Caps





It is also important that the amount of trace length before and after the capacitor is matched exactly between the two signal lines. For example, when the capacitor on signal DP is placed 150mils from the pin of the connector and 2000mils from the pin of the RX input on the motherboard device, the capacitor on the DN signal must also be placed 150mils from the pin of the connector and 2000mils from the pin of the RX input on the motherboard device. Have no more than a 5mil delta between signal pair line segment lengths for either of these trace sections; also, no more than a 5mil delta for the entire route of the trace.

Table 4. AC Coupling Capacitor Guidelines

Parameter (For AC Coupling Capacitors)	Requirement
Cap size	• 0402 • C-packs **not** allowed
Cap Value	• 75nF minimum • 200nF maximum • Cap values must be the same for each signal in a differential pair
Cap Value Tolerance	• Not applicable as long as specified minimum/maximum range is met when the tolerance is considered.
Cap Placement—Coupled Pair	• Must be placed at same exact location within the two signal lines • Symmetric routing into the caps and matched line lengths on either side of the caps for each line of the diff pair.
Cap Location—Chip to Connector Routing	• Place capacitors generally within 500mils of the connector (x1, x4), 400mils from the connector(x16). See the routing rules for allowable minimum/maximum lengths.

Though the capacitors theoretically are placed anywhere along the interconnect, and tend to reside near the connector, it is recommended that they are close to the connector pins. Use the pin closest to the edge of the connector as the reference point when the DP and DN pin locations are staggered, as is the case with a thru-hole style of connector.

1.1.8 Test Points and Probing

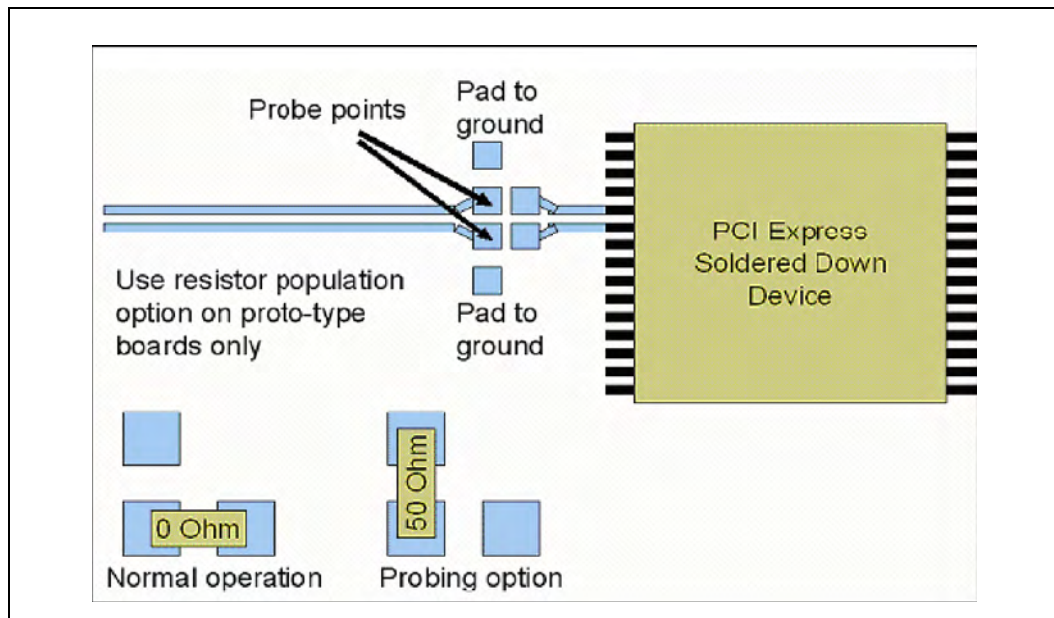
The inclusion of test points and probing structures has the ability to impact the loss and jitter budgets of a DMI/ESI interconnect. This is not to say they cannot be tolerated, however. In general, do not introduce test points and probe structures to stubs on the differential pairs or cause them to wildly deviate from the recommendations given throughout this chapter. Use existing vias, pads or pins wherever possible to accommodate such structures. Careful consideration must be taken whenever additional probing structures are used.

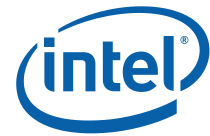
1.1.8.1 Probe Points for Testing Soldered Down DMI/ESI Devices

In order to actively characterize the transmit path signal quality for a soldered down DMI device, there must be a terminated probing point on the motherboard very near the soldered down device. This probing point affects the overall signal quality of the system during normal operation due to the effects of stubs and impedance mismatches of the traces themselves.

The probing point requires populating a resistor stuffing option that is used to break the path to the device very near the device pins and ideally terminate each line (TX_DP/TX_DN) to ground through a 50Ω 1% resistor. Also, an AC coupling capacitor is required near the device pins. The resistor package/footprint must be as small as possible, preferably size 0402. The population of a 50Ω resistor, as shown in Figure 5, will force the transmitting silicon (host or add-in card) to enter the compliance mode and begin transmitting the compliance packet. The population of two 0Ω resistors will allow normal operation of the device. One replaces the AC coupling cap, the other connects the channel.

Figure 5. Board Preparation Example





1.2 DMI Topology Guidelines

This section details design requirements for the following topologies:

- Intel® Atom™ Processor D400/D500 Series and ICH9R DMI LAI topologies

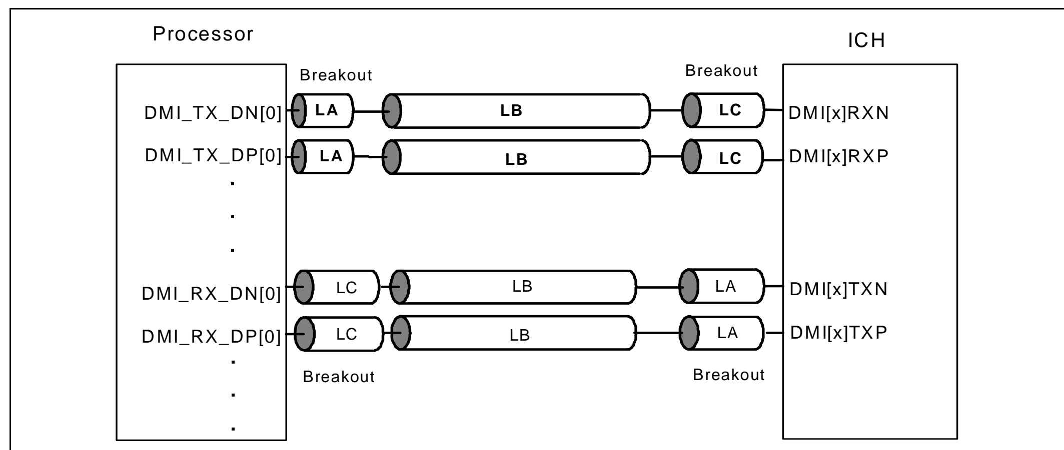
The transmit and receive directions of the link have different guidelines due to capacitive decoupling, and there are different guidelines based on whether the signals are routed on a microstrip or a stripline layer. These guidelines are provided for each link topology.

Guidelines for Logic Analyzer Interface (LAI) pads are also provided for device-to-device links. LAI use interposers to probe the processor-to-connector topologies. Use of an LAI interposer in a PCI Express connector will likely result in a reduced solution space. Customers are encouraged to work with their LAI vendor and simulate their processor-to-connector solution when planning to use an LAI interposer.

1.2.1 Intel® Atom™ Processor and ICH9R DMI Guidelines

Figure 6 shows routing between the processor and the ICH9R component.

Figure 6. DMI Topology



Notes:
1. LA and LC is the pin field region.

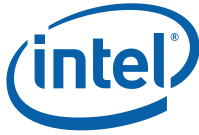
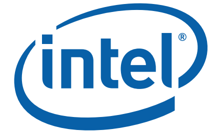


Table 5. DMI Routing Guidelines

Signal	Segment	Width (W)/ Spacing (S)	Microstrip /Stripline	Length	Differential Impedance	Reference Plane	Notes
TXp/n	LA	W = 4mils S = 4mils S1 = Breakout S2 = Breakout	Microstrip	Minimum = 0.25” Maximum = 0.5”	Breakout	Ground	Breakout on the same layer as main route.
	LB	W = 5.0mils S = 7.0mils S1 = 12mils S2 = 12mils	Microstrip	Minimum = 1.0” Maximum = 6.0” -(LA+LC)	85Ω ±12%		
	LC	W = 4mils S = 4mil S1 = Breakout S2 = Breakout	Microstrip	Minimum = 0.25” Maximum = 0.5”	Breakout		Breakout on the same layer as main route.

Notes:
1. Based on Reference Stackup.
2. Signal routing Non-interleaved (= TxTxTx or RxRxRx) for all segments.
3. S = Spacing between signals within the differential pair (p/n).
4. S1 = Spacing between pairs; (stripline = 3xh; microstrip = 7xh). Where h is the dielectric height between signal and ground plane.
5. S2 = Spacing to other signals; (stripline = 5xh; microstrip = 7xh). Where h is the dielectric height between signal and ground plane.
6. References to a specific layer (e.g., Layer 3) are intended only to provide context into the stackup characteristics required to meet the guideline. Routing on that specific layer is not required unless otherwise indicated.
7. Maximum of four vias.
8. Length Match to ±5mils.



1.3 Compensation Signal Guidelines

1.3.1 Processor DMI/ESI Compensation

Tie Intel® Atom™ Processor signals PE_ICOMPO, and PE_COMPI together, then connected to the GND via a single 49.9Ω ±1% resistor. Pull PE_RBIAS to the ground through a 750Ω ±1% resistor.

Figure 7. Intel® Atom™ Processor PCI Express and DMI/ESI Compensation Topology

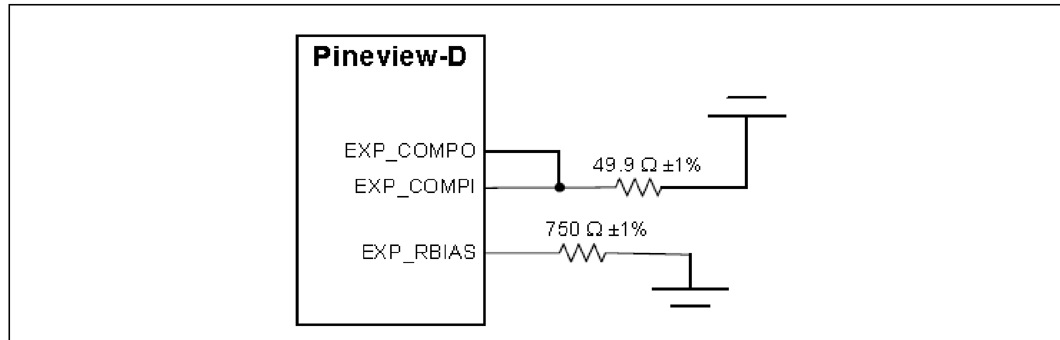


Table 6. Intel® Atom™ Processor PCI Express and DMI/ESI Compensation Routing Guidelines

Signal Name	Width (W) / Spacing (S)	Length	Resistor	Notes
EXP_ICOMPO EXP_ICOMPI	W = 10mils S = 6mils spacing for 300mils at breakout, 15 mils spacing after that	Maximum 1.0”	49.9Ω ±1%	1
PE_RBIAS	W= 10mils S = 6mils spacing for 300mils at breakout, 15mils spacing after that	Maximum 1.0”	750Ω ±1%	1

1. W represents width of signal; S represents spacing to any other signal

1.3.2 ICH9R DMI/ESI Compensation

Tie DMI/ESI compensation pins together and connected to ICH9R 1.5V rail (Vcc1_5_Filter) via a 49.9Ω, ±1% resistor, as shown in Figure 8. These signals follow the standard DMI/ESI routing guidelines of 4mil width with 8mil spacing. Place the resistor within 500mils of ICH9R and avoid routing next to clock pins.

Figure 8. PCH Compensation Connection

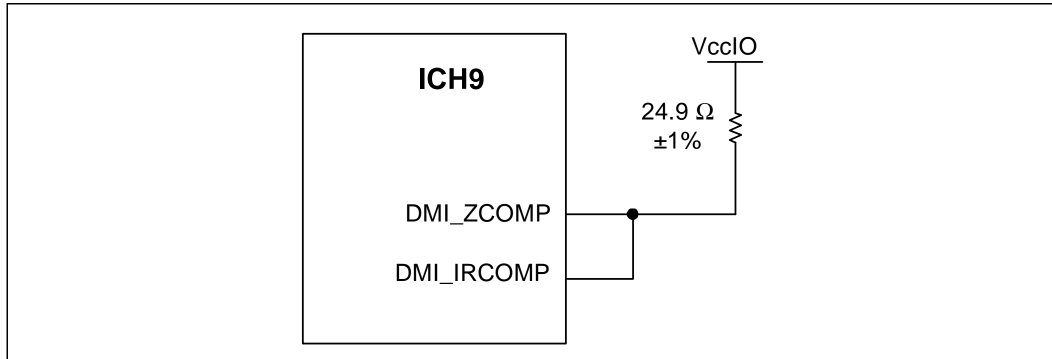
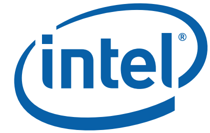


Table 7. ICH9R DMI/ESI Compensation Signals Routing Guidelines

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Resistor	Notes
DMI_ZCOMP DMI_IRCOMP	50Ω ±15%	W = 4mils S = 8mils	Microstrip	0.5" Maximum	24.9Ω ±1%	1

1. W represents width of signal; S represents spacing to any other signal.



1.4 DMI Initialization Configuration

The ICH9R must be properly configured for the same mode as Intel® Atom™ Processor D400/D500 Series for the DMI interface to function properly.

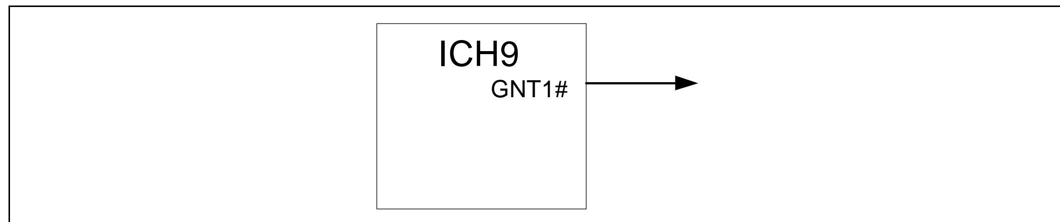
- DMI mode is used when the interface is not AC Coupled.

ICH9R uses the GNT1#/GPIO51 pin for ESI/DMI initialization. The GNT1# is sampled at the rising edge of PWROK. After PWROK, use this pin for its primary purpose. See the ICH9R EDS Pin Straps section for details.

Note: ICH9R has a weak internal pull-up which configures ICH9R to DC coupled mode by default.

The following figure shows how to properly configure for DMI mode.

Figure 9. DMI Initialization Strapping for ICH9R



The figure shows how to properly configure for DMI mode.

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