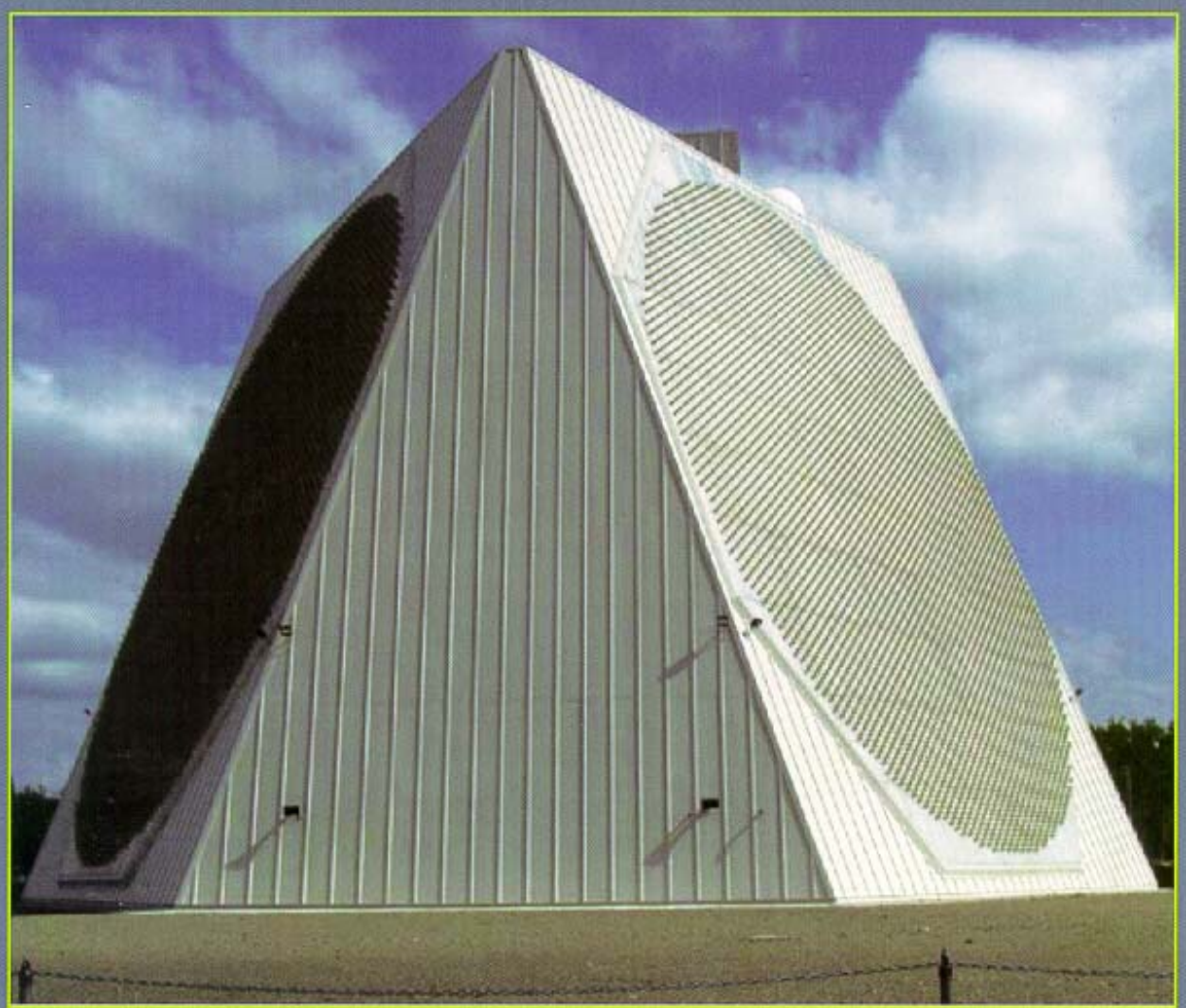
Electromagnetics for Engineers

WITH APPLICATIONS



Clayton R. Paul

6.2 TIME-DOMAIN EXCITATION OF TRANSMISSION LINES

We will now examine a transmission line connecting a source to a load as illustrated in Fig. 6.7. The source consists of an open-circuit voltage source, $V_S(t)$, and source resistance, R_S, and the load is represented by a resistance R_L. The line will have a total length $\mathscr{L}$. The source voltage can have an arbitrary waveform.

6.2.1 The General Solution

The second-order, uncoupled transmission-line equations are given in (6.2). It is a simple matter to show that their solutions are

$$V(z,t) = \underbrace{V^+\left(t - \frac{z}{v}\right)}_{\substack{\text{forward } (+z) \\ \text{traveling wave}}} + \underbrace{V^-\left(t + \frac{z}{v}\right)}_{\substack{\text{backward } (-z) \\ \text{traveling wave}}} \tag{6.13a}$$

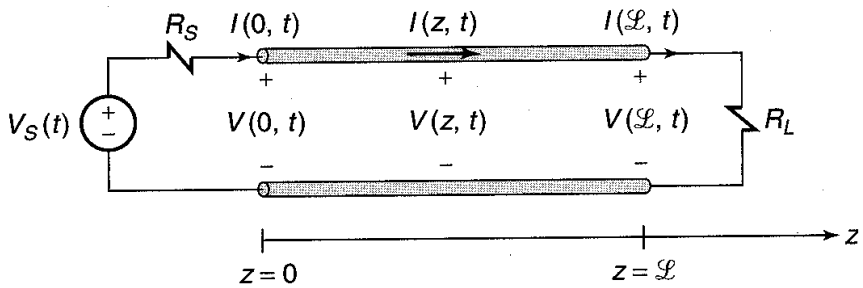


Figure 6.7 Terminations of a two-conductor line.

and

$$I(z,t) = \underbrace{\frac{V^+\left(t - \frac{z}{v}\right)}{Z_C}}_{\substack{\text{forward } (+z) \\ \text{traveling wave}}} - \underbrace{\frac{V^-\left(t + \frac{z}{v}\right)}{Z_C}}_{\substack{\text{backward } (-z) \\ \text{traveling wave}}} \tag{6.13b}$$

where the *characteristic impedance* is

$$Z_C = \sqrt{\frac{l}{c}} \quad \Omega \tag{6.14}$$

and the velocity of propagation is

$$v = \frac{1}{\sqrt{lc}} \quad \text{m/s} \tag{6.15}$$

The voltage and current solutions in (6.13) consist of the sum and difference of forward-traveling (in the $+z$ direction) and backward-traveling (in the $-z$ direction) waves. The forward-traveling wave is given by the function $V^+(t - z/v)$. It is easy to see that this is traveling in the $+z$ direction because the argument of the function, $t - z/v$, must be constant in order to track movement of a point on the waveform. Hence as t increases, z must also increase, and the wave travels in the $+z$ direction to accomplish this. Similarly, the function $V^-(t + z/v)$ represents a wave traveling in the $-z$ direction because, in order to keep the argument constant, when t increases, z must decrease in order to keep the argument constant. The precise form of the functions V^+ and V^- depend on the waveform of the source voltage, $V_S(t)$. However, t, z, and v can only appear in these as $t - z/v$ or $t + z/v$.

The characteristic impedance, Z_C, is a real (not complex) number. Hence it would be more properly called the characteristic *resistance*. The word "impedance" is a frequency-domain (phasor) term but here the source voltage waveform is not necessarily a single-frequency sinusoid but may have an arbitrary waveform. However, it has become an industry standard to refer to Z_C as the characteristic *impedance*, as we will continue to do here.

It is important to observe that because of the important minus sign between the two waves in the current expression in (6.13b) that $I(z,t) \neq V(z,t)/Z_C$. In other words, the input resistance seen looking into one end of the line is not equal to the characteristic impedance. The characteristic impedance Z_C only relates the voltage and current in the forward-traveling wave and the voltage and current in the backward-traveling wave.

QUICK REVIEW EXERCISE 6.7

Determine the characteristic impedances and velocities of propagation of the wire-type lines in Quick Review Exercise Problems 6.1, 6.2, and 6.3.

ANSWERS 225.1 Ω, 3×10^8 m/s; 151 Ω, 3×10^8 m/s, 51 Ω; 1.98×10^8 m/s.

QUICK REVIEW EXERCISE 6.8

Determine the characteristic impedances and velocities of propagation of the rectangular cross section lines in Quick Review Exercise Problems 6.4, 6.5, and 6.6.

ANSWERS 63.8 Ω, 1.38×10^8 m/s; 151 Ω, 1.72×10^8 m/s; 144.45 Ω, 1.8×10^8 m/s. ◀

6.2.2 Wave Tracing and the Reflection Coefficients

Now consider the termination at the load, $z = \mathscr{L}$. The total voltage and current at the load are

$$V(\mathscr{L},t) = V^+(t - T) + V^-(t + T) \tag{6.16a}$$

and

$$I(\mathscr{L},t) = \frac{V^+(t - T)}{Z_C} - \frac{V^-(t + T)}{Z_C} \tag{6.16b}$$

where the one-way time delay is

$$\boxed{T = \frac{\mathscr{L}}{v} \quad \text{s}} \tag{6.17}$$

At the load, Ohm's law dictates that

$$\frac{V(\mathscr{L},t)}{I(\mathscr{L},t)} = R_L \tag{6.18}$$

But this cannot be satisfied with only a forward-traveling wave because

$$\frac{V^+(t - T)}{I^+(t - T)} = Z_C \tag{6.19}$$

Hence there must exist both forward- and backward-traveling waves in order to satisfy (6.18).

If $R_L = Z_C$ we say that the line is *matched* at the load. In this case there will only be forward-traveling waves on the line as evidenced by (6.19). In the case of a mismatched line, $R_L \neq Z_C$, we define a (voltage) reflection coefficient at the load as the ratio of the backward-traveling (reflected) voltage wave to the forward-traveling (incident) voltage wave as

$$\Gamma_L = \frac{V^-(t + T)}{V^+(t - T)} \tag{6.20}$$

so that the voltage and current expressions at the load become

$$V(\mathscr{L},t) = V^+(t - T)[1 + \Gamma_L] \tag{6.21a}$$

and

$$I(\mathscr{L},t) = \frac{V^+(t - T)}{Z_C}[1 - \Gamma_L] \tag{6.21b}$$

Taking the ratio of (6.21a) and (6.21b) must yield

$$\begin{aligned} \frac{V(\mathscr{L},t)}{I(\mathscr{L},t)} &= R_L \\ &= Z_C \frac{[1 + \Gamma_L]}{[1 - \Gamma_L]} \end{aligned} \tag{6.22}$$

Solving (6.22) for the reflection coefficient we obtain the load (voltage) reflection coefficient as

$$\boxed{\Gamma_L = \frac{R_L - Z_C}{R_L + Z_C}} \tag{6.23}$$

Because of the minus sign in the current expression in (6.13b), the reflection coefficient for current is the negative of the voltage reflection coefficient.

It is interesting to compare this to the case of a uniform plane wave incident normal to a boundary discussed in Section 5.5 of Chapter 5. (See Fig. 5.8.) The portion of the incident electric field wave that is reflected is

$$\Gamma = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1}$$

where $\eta_1 = \sqrt{\mu_1/\varepsilon_1}$ is the intrinsic impedance of the left medium (containing the incident electric field) and $\eta_2 = \sqrt{\mu_2/\varepsilon_2}$ is the intrinsic impedance of the right medium containing the transmitted electric field. This allows us to make a correspondence between the two similar problems if we make the following correspondence:

$$V \Leftrightarrow E$$
$$I \Leftrightarrow H$$
$$Z_C \Leftrightarrow \eta_1$$
$$R_L \Leftrightarrow \eta_2$$

as indicated in Fig. 6.8. Hence what we learned about uniform plane waves can, in many cases, be carried over to transmission lines in an analogous fashion.

The preceding has shown that at a mismatched load, the incoming (forward-traveling) voltage wave is partially reflected and sent back to the source. This is illustrated in Fig. 6.9.

The wave initially sent out from the source is a forward-traveling wave and has not reached the mismatched load to produce a reflection. Hence until the wave reaches the

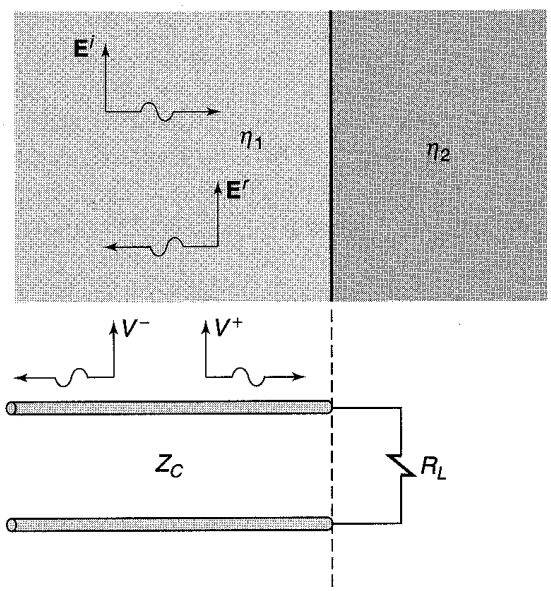


Figure 6.8 The analogy of a transmission-line termination and normal incidence of uniform plane waves on a plane, material boundary.

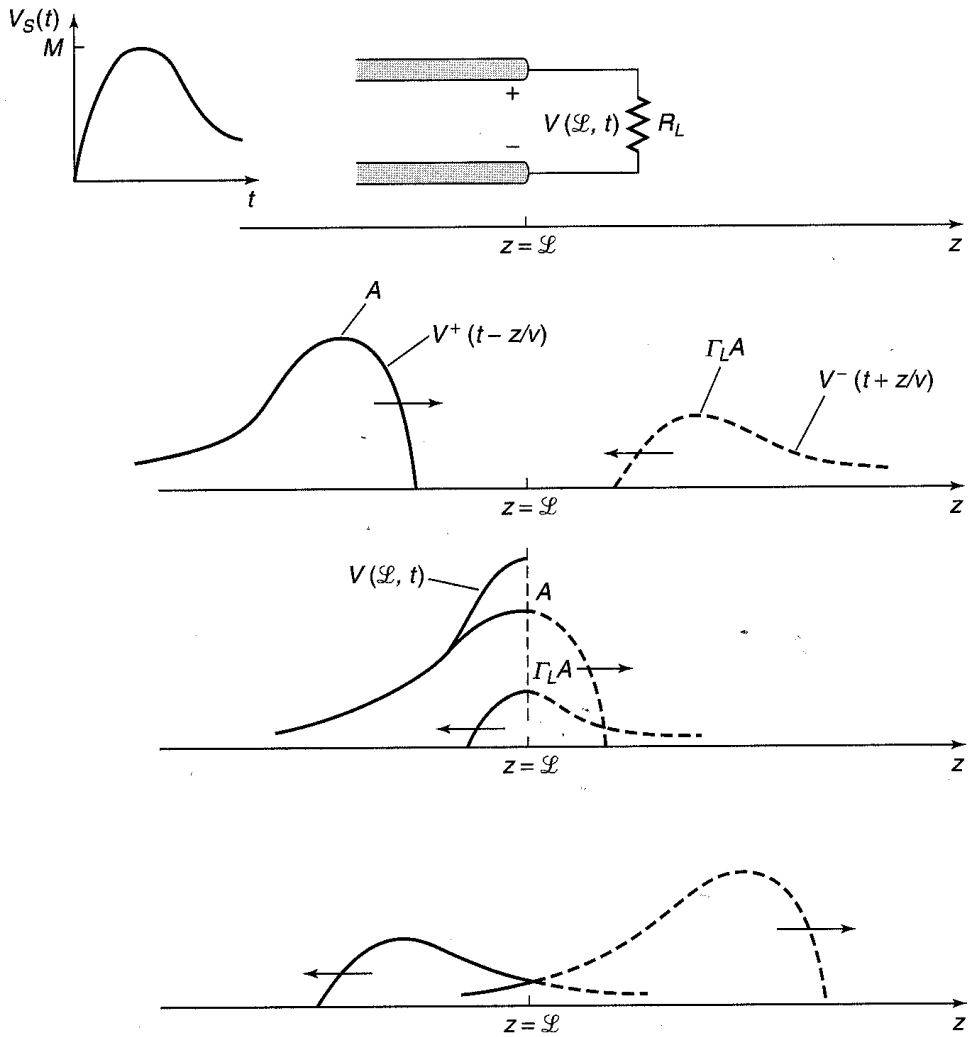


Figure 6.9 Illustration of the reflection of voltage waves at the load of a transmission line.

load and causes a reflected wave, there is only a forward-traveling wave on the line. But this reflected wave does not appear at the line input until after a round-trip delay of $2T$. Thus, according to (6.13), the source initially sees an input impedance looking into the line of Z_C as shown in Fig. 6.10. After the wave arrives at the load and produces a reflected wave, this is no longer true because there will be both forward- and backward-traveling waves on the line and the ratio is not Z_C because of the minus sign in the current expression in (6.13). Hence the initially sent out wave can be determined by voltage division as shown in Fig. 6.10 as

$$V(0,t) = \frac{Z_C}{R_S + Z_C} V_S(t) \qquad t < 2T \tag{6.24a}$$

Similarly, the initial current wave sent out by the source is

$$I(0,t) = \frac{V_S(t)}{R_S + Z_C} \qquad t < 2T \tag{6.24b}$$

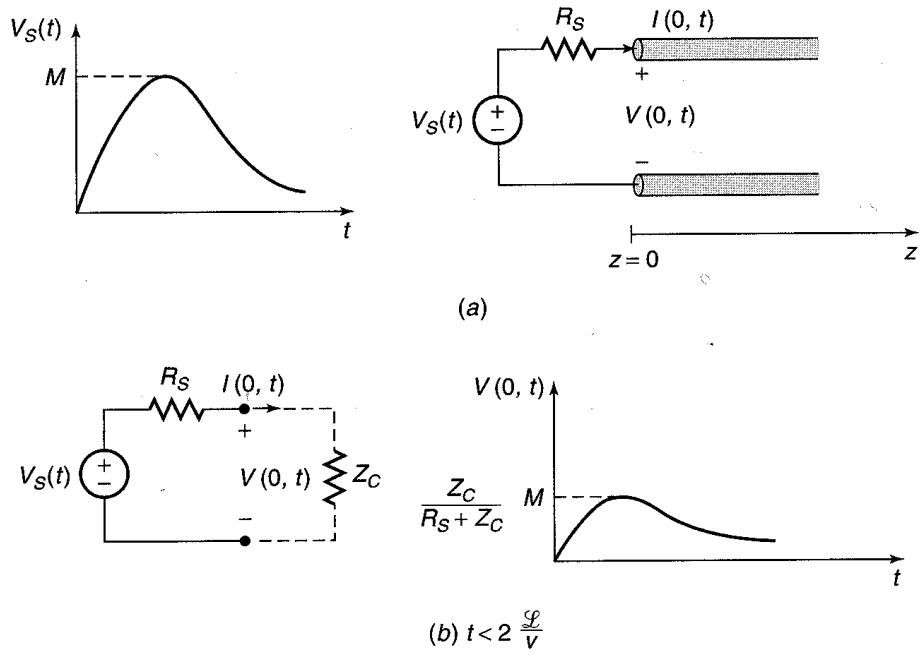


Figure 6.10 Illustration of determining the initially sent out pulse at the source.

The wave reflected at the load will, after a travel delay of $T = \mathscr{L}/v$, be incident on the source. We define in a similar manner the source (voltage) reflection coefficient as

$$\boxed{\Gamma_S = \frac{R_S - Z_C}{R_S + Z_C}} \tag{6.25}$$

Thus a portion of the incoming voltage wave (which was reflected by the load) will be reflected back toward the load. The reflection coefficient for the current wave is, because of the minus sign in the current expression in (6.13b), the negative of the voltage reflection coefficient. This process continues indefinitely.

This is conveniently shown by the "bounce" or lattice diagram in Fig. 6.11. From this we can write an expression for the voltage at $z = 0$ and at the load, $z = \mathscr{L}$, as

$$\begin{aligned} V(0,t) = \frac{Z_C}{R_S + Z_C}[&V_S(t) + (1 + \Gamma_S)\Gamma_L V_S(t - 2T) \\ &+ (1 + \Gamma_S)(\Gamma_S\Gamma_L)\Gamma_L V_S(t - 4T) \\ &+ (1 + \Gamma_S)(\Gamma_S\Gamma_L)^2\Gamma_L V_S(t - 6T) + \cdots] \end{aligned} \tag{6.26a}$$

and

$$\begin{aligned} V(\mathscr{L},t) = \frac{Z_C}{R_S + Z_C}[&(1 + \Gamma_L)V_S(t - T) + (1 + \Gamma_L)\Gamma_S\Gamma_L V_S(t - 3T) \\ &+ (1 + \Gamma_L)(\Gamma_S\Gamma_L)^2 V_S(t - 5T) \\ &+ (1 + \Gamma_L)(\Gamma_S\Gamma_L)^3 V_S(t - 7T) + \cdots] \end{aligned} \tag{6.26b}$$

So the total voltages are the sum of the source voltage waveforms scaled and delayed by multiples of the one-way time delay, T. Although the source and load voltage waveforms could be sketched from (6.26), it is much simpler to "trace the individual incident

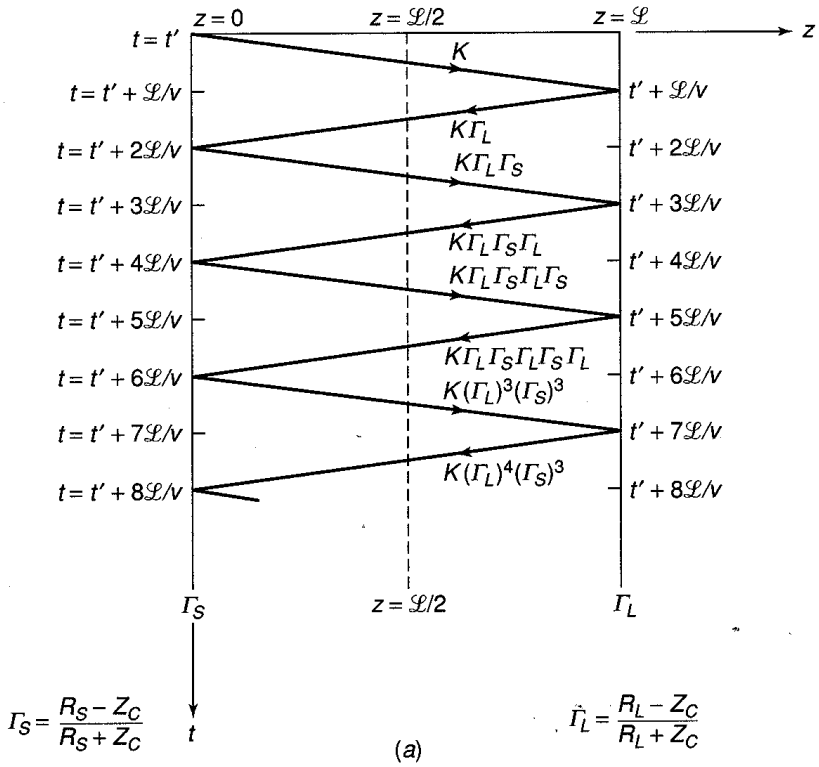


Figure 6.11 The "bounce diagram" for determining the voltages on the line at different instants of time.

and reflected waves" and at any time add all those present at that time. The following example illustrates this simple technique.

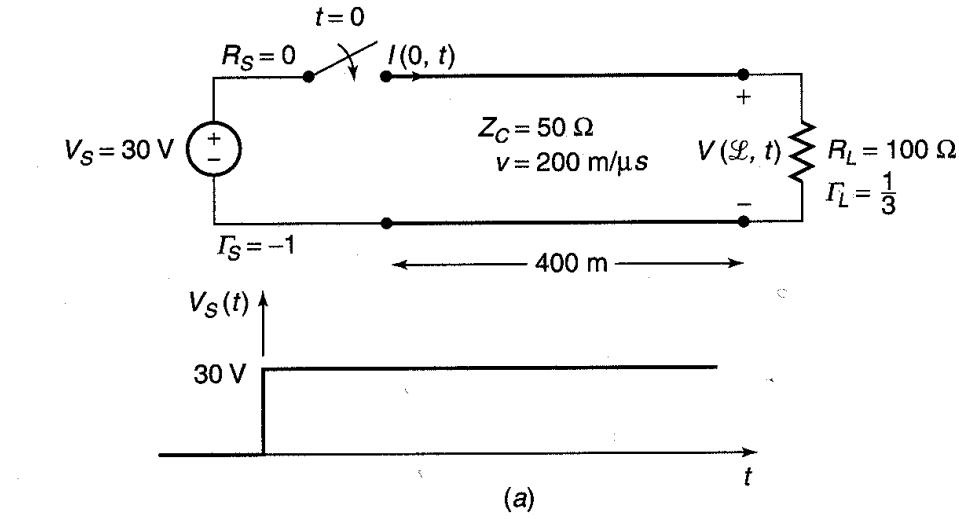
▶ EXAMPLE 6.1

Figure 6.12 shows a line wherein a 30-V battery is switched onto a line of length 400 m. The line has a characteristic impedance of 50 Ω and a velocity of propagation of 2×10^8 m/s or 200 m/μs. The source resistance is zero ($R_S = 0$) and the load resistance is 100 Ω($R_L = 100\ \Omega$). Sketch the current at the input to the line and the voltage at the load.

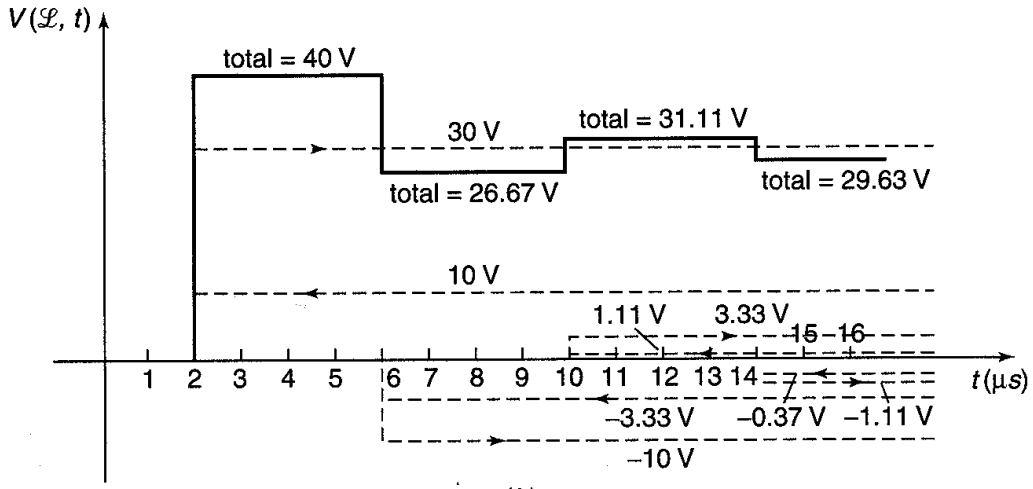
SOLUTION The source reflection coefficient is

$$\Gamma_S = \frac{0 - 50}{0 + 50}$$

$$= -1$$



(a)



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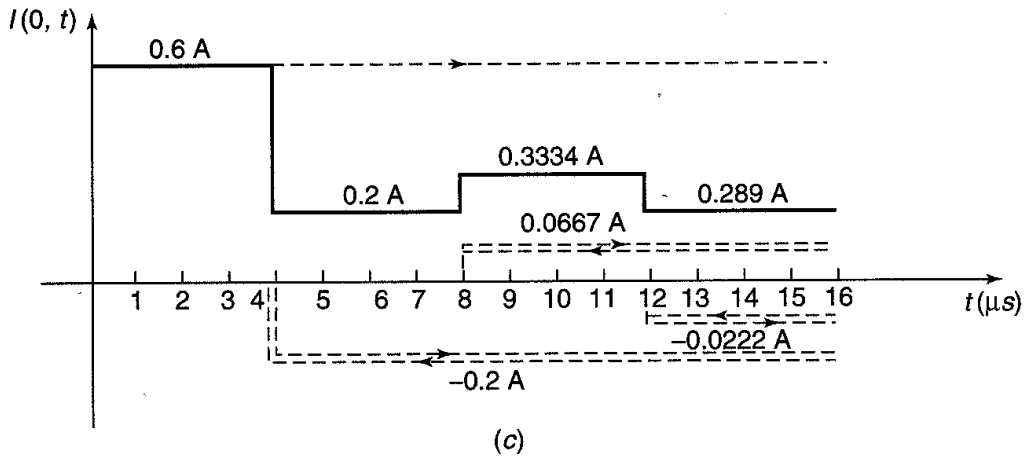


(c)

Figure 6.12 Example 6.1; determining the current at the input to the line and the load voltage. (a) The problem specification. (b) The load voltage. (c) The input current to the line.

and the load reflection coefficient is

$$\Gamma_L = \frac{100 - 50}{100 + 50}$$
$$= \frac{1}{3}$$

The one-way time delay is

$$T = \frac{\mathscr{L}}{v}$$
$$= 2\ \mu s$$

First we sketch the load voltage, $V(\mathscr{L},t)$. The initially sent out voltage is, since the source resistance is zero, 30 V. The incident and reflected voltages are sketched as dashed lines with an arrow added to indicate whether it is associated with a forward-traveling or a backward-traveling wave. After a time delay of 2 μs the initially sent out voltage of 30 V arrives at the load and a reflected voltage of $\frac{1}{3} \times 30 = 10$ V is sent back toward the source. This reflected voltage arrives at the source at 4 μs and a reflected voltage of $-1 \times 10 = -10$ V is sent back toward the load. When this, now incident, voltage arrives at the load a portion, $\frac{1}{3} \times -10 = -3.33$ V is sent back toward the source. These incident and reflected voltages are sketched in Fig. 6.12b. Adding the voltages present at any one time gives the total as shown by a solid line.

The current can be similarly sketched. The initially sent out current is $30\ V/Z_C = 0.6$ A. The current reflection coefficient at the load is the negative of the voltage reflection coefficient or $-\frac{1}{3}$. Similarly, the current reflection coefficient at the source is the negative of the voltage reflection coefficient or $+1$. Tracing these incident and reflected currents in the same manner as for the voltage produces the result shown in Fig. 6.12c.

And finally we should "sanity check" these results. After a sufficiently long time, the reflections will decay to zero and we would expect the line to have no effect. Consequently the results should converge after several round-trip delays to 30 V and $30\ V/100\ \Omega = 0.3$ A. The sketches indicate that this is indeed the case. ◀

▶ EXAMPLE 6.2

This example shows the effect of pulse width on the total voltages. Consider a line of length 0.2 m (7.9 in.) shown in Fig. 6.13a. The source voltage is a pulse of 20 V amplitude and 1 ns duration. The line has a characteristic impedance of 100 Ω and a velocity of propagation of 2×10^8 m/s. The source resistance is 300 Ω ($R_S = 300\ \Omega$) and the load is open circuited ($R_L = \infty$). Sketch the voltage at the input to the line and at the load.

SOLUTION The source reflection coefficient is

$$\Gamma_S = \frac{300 - 100}{300 + 100}$$
$$= \frac{1}{2}$$

and the load reflection coefficient is

$$\Gamma_L = \frac{\infty - 100}{\infty + 100}$$
$$= 1$$

The one-way time delay is

$$T = \frac{\mathscr{L}}{v}$$
$$= 1\ \text{ns}$$

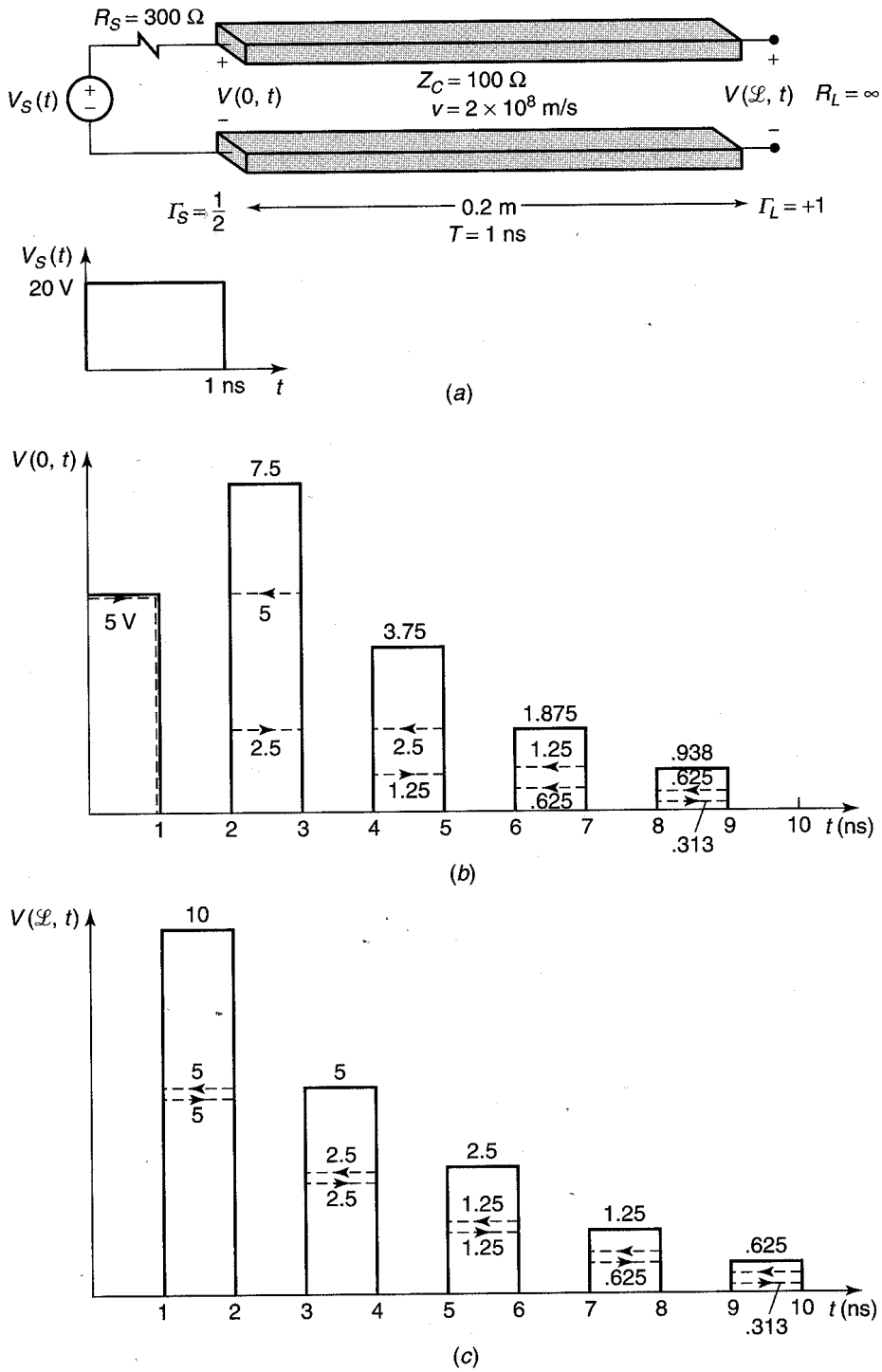


Figure 6.13 Example 6.2. Illustration of the effect of pulse width on the terminal voltages. (a) The problem specification. (b) The voltage at the input to the line. (c) The load voltage.

First we sketch the source voltage, $V(0,t)$. The initially sent out voltage is

$$\frac{100}{300 + 100} \times 20 = 5\ \text{V}$$

The incident and reflected voltages are again sketched in Fig. 6.13b with dashed lines with an arrow added to indicate whether they are associated with a forward-traveling or a backward-traveling

wave. The incident pulse is sent to the load, arriving there after one time delay of 1 ns, where it is reflected as a pulse of 5 V because the load reflection coefficient is $\Gamma_L = 1$. This pulse reflected at the load arrives at the source after an additional 1-ns time delay. This incoming pulse is reflected as $\Gamma_S \times 5V = 2.5$ V, which arrives at the load after 1 ns, where it is reflected as 2.5 V, arriving at the source after a 1-ns delay. The process continues as shown. Adding all the incident and reflected pulses at the source, we obtain the total voltage drawn with a solid line. Clearly this total decays to zero, as it should in steady state.

Now we sketch the voltage at the load. After a time delay of 1 ns, the initially sent out voltage of 5 V arrives at the load and a reflected voltage of 5 V is sent back toward the source. This reflected voltage arrives at the source after 2 ns, and a reflected voltage of 2.5 V is sent back toward the load and arrives there at 3 ns. When this pulse reflected at the source arrives at the load, a reflected voltage of 2.5 V is sent back toward the source, which is reflected at the source as 1.25 V, arriving at the load at 5 ns. These incident and reflected voltages are sketched in Fig. 6.13c. Adding the voltages present at any one time gives the total as shown by a solid line. Clearly this load voltage is decaying to zero, as it should in steady state. ◀

▶ EXAMPLE 6.3

This example illustrates the effect of a pulse width that is greater than the round-trip delay. Consider the coaxial cable shown in Fig. 6.14a. The source voltage is a pulse of 100 V amplitude and 6 μs duration. The line is specified by its per-unit-length capacitance and inductance: $c = 100$ pF/m and $l = 0.25$ μH/m. This corresponds to the RG-58U coaxial cable whose per-unit-length parameters were computed in Quick Review Exercise Problem 6.3. The line has a characteristic impedance of

$$Z_C = \sqrt{\frac{l}{c}}$$
$$= 50\ \Omega$$

The velocity of propagation is

$$v = \frac{1}{\sqrt{lc}}$$
$$= 200\ \text{m}/\mu\text{s}$$

The source resistance is 150 Ω ($R_S = 150\ \Omega$) and the load resistance is a short circuit ($R_L = 0\ \Omega$). Sketch the voltage at the input to the line.

SOLUTION The source reflection coefficient is

$$\Gamma_S = \frac{150 - 50}{150 + 50}$$
$$= \frac{1}{2}$$

and the load reflection coefficient is

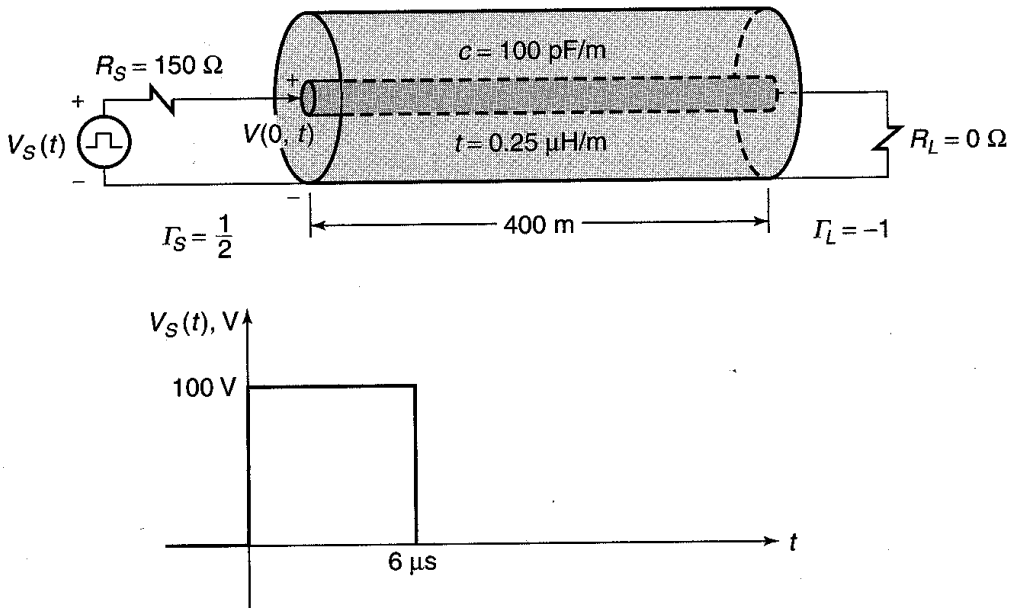
$$\Gamma_L = \frac{0 - 50}{0 + 50}$$
$$= -1$$

The one-way time delay is

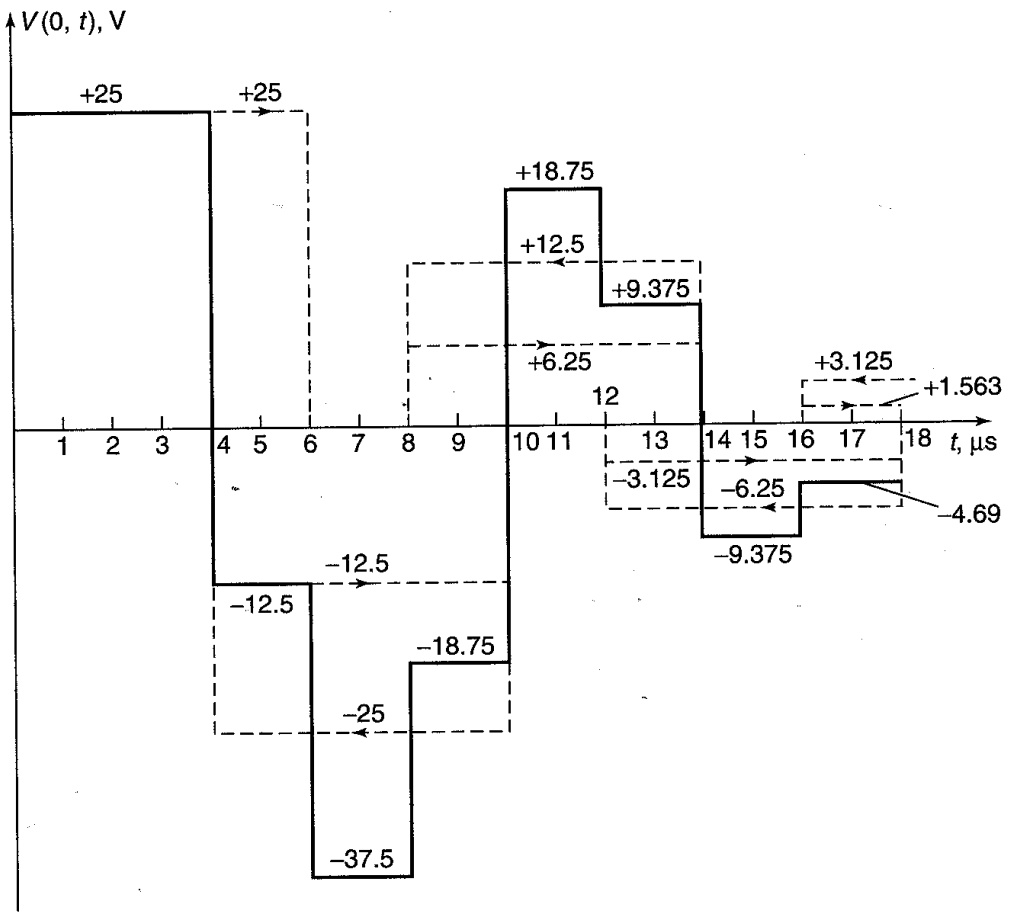
$$T = \frac{\mathscr{L}}{v}$$
$$= 2\ \mu\text{s}$$

The initially sent out voltage is

$$\frac{50}{150 + 50} \times 100 = 25\ \text{V}$$



(a)



(b)

Figure 6.14 Example 6.3. Illustration of the effect of pulse width on the terminal voltages. (a) The problem specification. (b) The voltage at the input to the line.

The incident and reflected voltages are again sketched with dashed lines in Fig. 6.14b with an arrow added to indicate whether they are associated with a forward-traveling or a backward-traveling wave. The incident pulse is sent to the load, arriving there after one time delay of 2 μs, where it is reflected as a pulse of −25 V. This pulse reflected at the load arrives at the source after an additional 2-μs time delay. This incoming pulse is reflected as −12.5 V, which arrives at the load after 2 μs, where it is reflected as 12.5 V, arriving at the source after a 2-μs delay. The process continues as shown. Adding all the incident and reflected pulses at the source, we obtain the total voltage drawn with a solid line. Clearly this total decays to zero, as it should in steady state.

Observe that in this example the pulse width of 6 μs is three time delays. Hence the initially sent out pulse and the arriving pulse (which was the sent out pulse reflected at the load) overlap. This overlap creates a rather interesting and complicated waveform. ◀

6.2.3 The SPICE Model

The solution to the transmission-line equations in (6.13) is repeated here:

$$V(z,t) = V^+\left(t - \frac{z}{v}\right) + V^-\left(t + \frac{z}{v}\right) \tag{6.27a}$$

$$Z_C I(z,t) = V^+\left(t - \frac{z}{v}\right) - V^-\left(t + \frac{z}{v}\right) \tag{6.27b}$$

In the equation for the current we have multiplied both sides by the characteristic impedance. Add and subtract these to give

$$V(z,t) + Z_C I(z,t) = 2V^+\left(t - \frac{z}{v}\right) \tag{6.28a}$$

$$V(z,t) - Z_C I(z,t) = 2V^-\left(t + \frac{z}{v}\right) \tag{6.28b}$$

Evaluating (6.28a) at the source and at the load gives

$$V(\mathscr{L},t) + Z_C I(\mathscr{L},t) = 2V^+(t - T) \tag{6.29a}$$

$$V(0,t - T) + Z_C I(0,t - T) = 2V^+\left(t - \frac{0}{v} - T\right) = 2V^+(t - T) \tag{6.29b}$$

Observe that we have delayed (6.29b) by one time delay, T, for reasons to become apparent. Eliminating V^+ by subtracting these, we obtain

$$\boxed{V(\mathscr{L},t) + Z_C I(\mathscr{L},t) = V(0,t - T) + Z_C I(0,t - T)} \tag{6.30a}$$

Performing a similar evaluation on (6.28b) yields

$$\boxed{V(0,t) - Z_C I(0,t) = V(\mathscr{L},t - T) - Z_C I(\mathscr{L},t - T)} \tag{6.30b}$$

Equations (6.30) allow us to model the line as a two port as shown in Fig. 6.15a. Each controlled voltage source is a function of the voltage and current at the other end of the line delayed by one time delay.

The SPICE circuit analysis program includes an exact model of a two-conductor, lossless transmission line which implements the model in Fig. 6.15a. For details on the use of SPICE see C.R. Paul, *Fundamentals of Electric Circuit Analysis*, John Wiley, 2001. The form of the SPICE coding is shown in Fig. 6.15b:

```
TXXX N1 N2 N3 N4 Z0=   TD=
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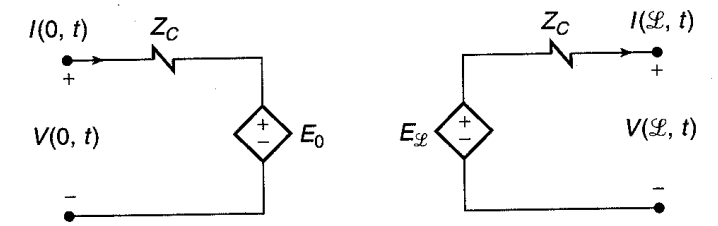
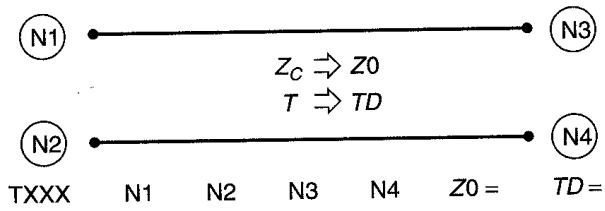


$E_0 = V(\mathscr{L}, t-T) - Z_C I(\mathscr{L}, t-T)$ $\quad E_{\mathscr{L}} = V(0, t-T) + Z_C I(0, t-T)$

(a)



(b)

Figure 6.15 The SPICE (PSPICE) model of a transmission line. (a) An exact model of the line. (b) The SPICE coding.

The XXX is an arbitrary name for this line chosen by the user. SPICE refers to the characteristic impedance as Z0 and the time delay as TD.

EXAMPLE 6.4

Use the SPICE (or the personal computer version, PSPICE) to solve the problem shown in Fig. 6.12 that was obtained in Example 6.1.

SOLUTION The SPICE (PSPICE) coding is shown in Fig. 6.16a:

```
EXAMPLE 6.4
VS 1 0 PWL(0 0 .01U 30)
T 1 0 2 0 Z0=50 TD=2U
RL 2 0 100
.TRAN .01U 20U 0 .01U
.PRINT TRAN V(2) I(VS)
*THE LOAD VOLTAGE IS V(2) AND
*THE INPUT CURRENT IS -I(VS)
.PROBE
.END
```

We have used the SPICE piecewise linear function (PWL) to specify the source voltage. This function specifies a piecewise linear graph of it as a sequence of straight lines between time points T1, T2, T3, . . . whose values are V1, V2, V3, . . . as

```
VXXX N1 N2 PWL(T1 V1 T2 V2 T3 V3 . . .)
```

Also, we have specified the battery voltage with a very small (.01 μs) rise time in order to specify it with the PWL function. We have used the .PROBE feature of PSPICE to provide plots of

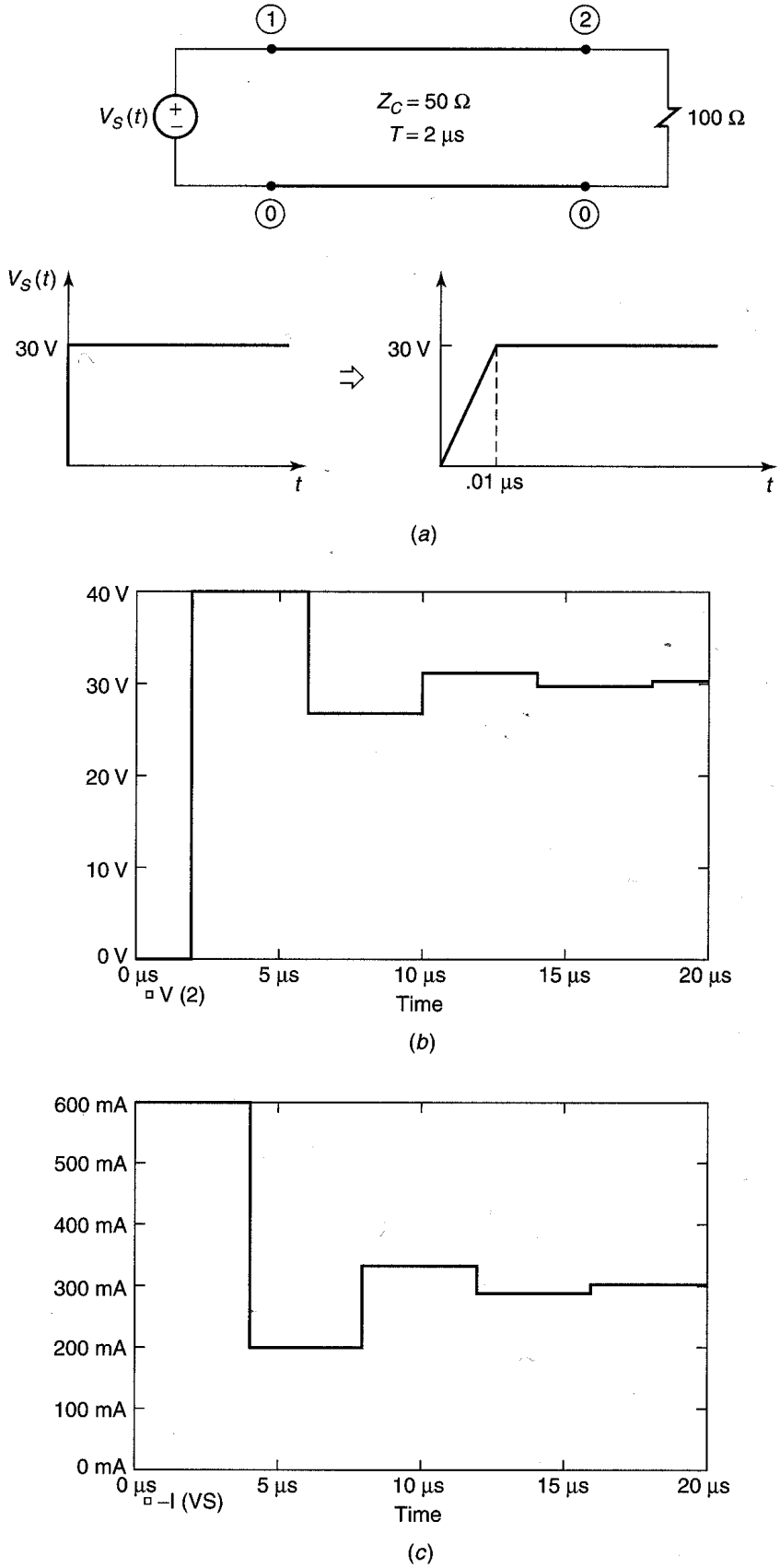


Figure 6.16 Example 6.4; the SPICE solution of the problem of Example 6.1. (a) The SPICE node labeling. (b) The SPICE solution for the line load voltage. (c) The SPICE solution for the input current to the line.

the load voltage and input current which are shown in Fig. 6.16b and Fig. 6.16c, respectively. Compare these to the corresponding plots obtained manually and shown in Fig. 6.12.

The format of the .TRAN line is

```
.TRAN [print step] [final solution time] [print start]
[maximum solution time step]
```

The *print step* is the time interval that solutions are printed to a file if so requested in a .PRINT statement, and the *final solution time* is the final time for which a solution is desired. These first two parameters are required, and the remaining two are optional. All solutions start at $t = 0$ but the *print start* parameter delays the printing of the results to an output file until this time. Usually the *print start* parameter is set to zero. Specification of the remaining term, *maximum solution time step*, is often required in order to control the accuracy and resolution of the solution. SPICE (PSPICE) solves the equations of the transmission line and associated termination circuits by discretizing the time interval into increments Δt. These are solved in a "bootstrapping" fashion by updating the results at the next time step with those from the previous intervals. The *maximum solution time step* parameter in the .TRAN line sets that maximum discretization time step. When the circuit contains a transmission line, the line voltages and currents will be changing in intervals of time on the order of the one-way time delay, T, as we have seen. In order to not miss any such important variations, the *maximum solution time step* must be considerably less than this one-way delay. The SPICE program developed in the 1960s automatically set the maximum discretization time step to be one-half of the smallest line delay when the circuit contained transmission lines. In many problems the voltages and currents will be varying in time intervals much smaller than this. For example, the source voltage waveform may be specified as having a rise/fall time in order to specify it with the PWL function. This rise/fall time may be (and usually is) much smaller than the line one-way delay. Hence the *maximum solution time step* should be set on the order of the smallest time variation.

EXAMPLE 6.5

Use the SPICE (or the personal computer version, PSPICE) to solve the problem shown in Fig. 6.13 that was obtained in Example 6.2.

SOLUTION The SPICE (PSPICE) coding is shown in Fig. 6.17a:

```
EXAMPLE 6.5
VS 1 0 PWL(0 0 0.01N 20 1N 20 1.01N 0)
RS 1 2 300
T 2 0 3 0 Z0=100 TD=1N
RL 3 0 1E8
.TRAN 0.01N 10N 0 0.01N
.PRINT TRAN V(2) V(3)
*THE LOAD VOLTAGE IS V(3) AND
*THE INPUT VOLTAGE IS V(2)
.PROBE
.END
```

We have again used the SPICE piecewise linear function to specify the source voltage. Also, we have specified the pulse with very small (.01 ns) rise and fall times in order to specify it with

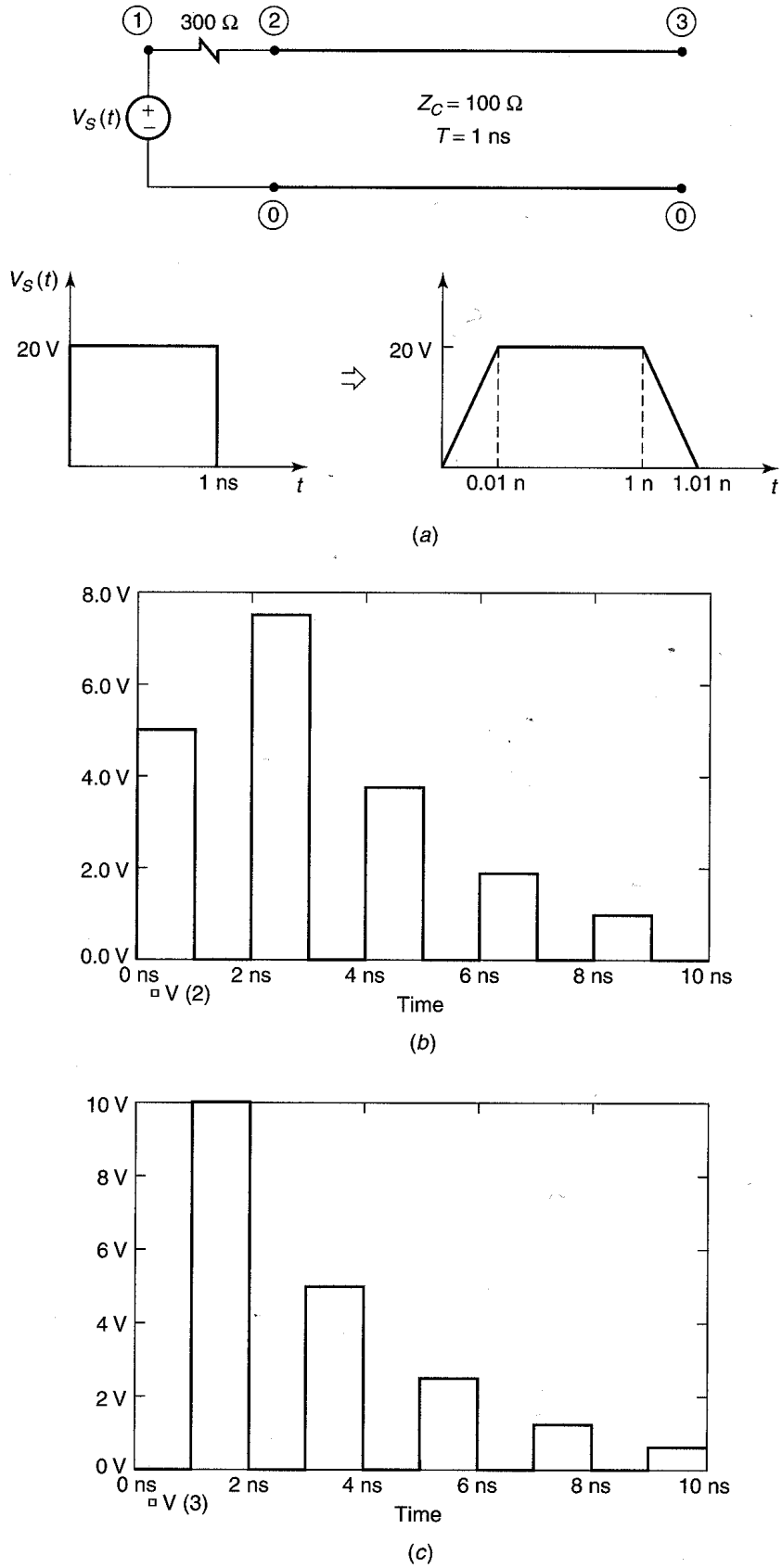


Figure 6.17 Example 6.5; the SPICE solution of the problem of Example 6.2. (a) The SPICE node labeling. (b) The SPICE solution for the input voltage to the line. (c) The SPICE solution for the line load voltage.

the PWL function. The open-circuit load is specified as a large (10^8-Ω) resistance. The input voltage and output voltage are shown in Fig. 6.17b and Fig. 6.17c, respectively. Compare these to the corresponding plots obtained manually and shown in Fig. 6.13.

EXAMPLE 6.6

Use the SPICE (or the personal computer version, PSPICE) to solve the problem shown in Fig. 6.14 that was obtained in Example 6.3.

SOLUTION The SPICE (PSPICE) coding is shown in Fig. 6.18a:

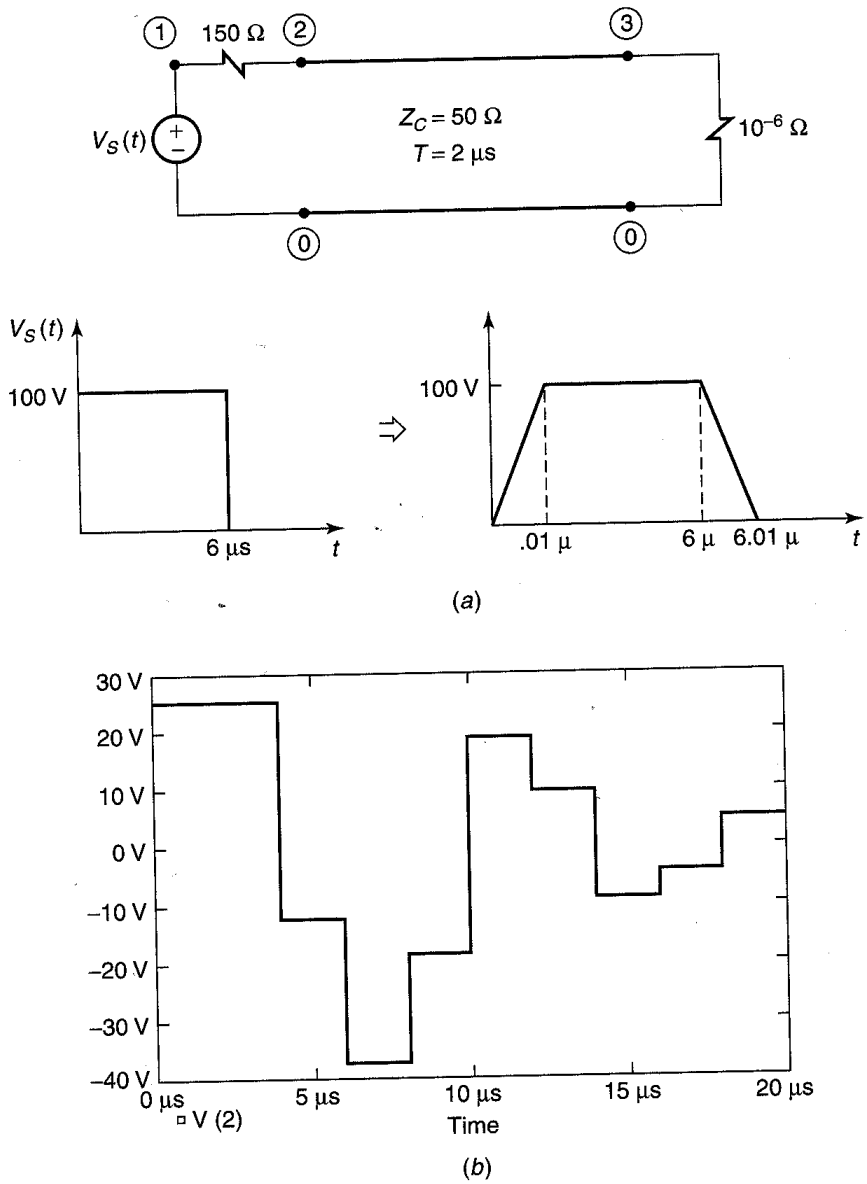


Figure 6.18 Example 6.6; the SPICE solution of the problem of Example 6.3. (a) The SPICE node labeling. (b) The SPICE solution for the input voltage to the line.

```
EXAMPLE 6.6
VS 1 0 PWL(0 0 .01U 100 6U 100 6.01U 0)
RS 1 2 150
T 2 0 3 0 Z0=50 TD=2U
RL 3 0 1E-6
.TRAN .01U 20U 0 .01U
.PRINT TRAN V(2) V(3)
*THE INPUT VOLTAGE IS V(2)
.PROBE
.END
```

Again we used the PWL function to specify the pulse. The short-circuit load is represented with a 1-μΩ resistor since SPICE does not allow for zero-ohm resistors. The input voltage to the line is shown in Fig. 6.18b. Compare this to the corresponding plot obtained manually and shown in Fig. 6.14b. ◀

6.2.9. Sketch the load voltage, $V(\mathcal{L},t)$, and the input current to the line, $I(0,t)$, for the problem depicted in Fig. P6.2.9 for $0 < t < 10$ ns. What should these plots converge to in the steady state? [$V(\mathcal{L},t)$,$0 < t < 1$ ns, 0 V,1 ns $< t <$ 3 ns, 9.375 V, 3 ns $< t <$ 5 ns, 8.203 V, 5 ns $< t <$ 7 ns, 8.35 V,7 ns $< t <$ 9 ns, 8.331 V, 9 ns $< t <$ 11 ns, 8.334 V, steady state 8.333 V, and $I(0,t)$,$0 < t <$ 2 ns, 0.125 A, 2 ns $< t <$ 4 ns, 0.047 A, 4 ns $< t <$ 6 ns, 0.057 A, 6 ns $< t <$ 8 ns, 0.055 A, 8 ns $< t <$ 10 ns, 0.056 A, steady state 0.056 A]

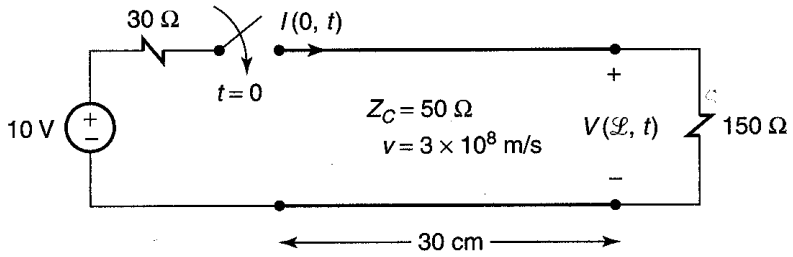


Figure P6.2.9 Problem 6.2.9.

6.2.10. Sketch the load voltage, $V(\mathcal{L},t)$, and the input voltage to the line, $V(0,t)$, for the problem depicted in Fig. P6.2.10 for $0 < t < 20$ ns. What should these plots converge to in the steady state?

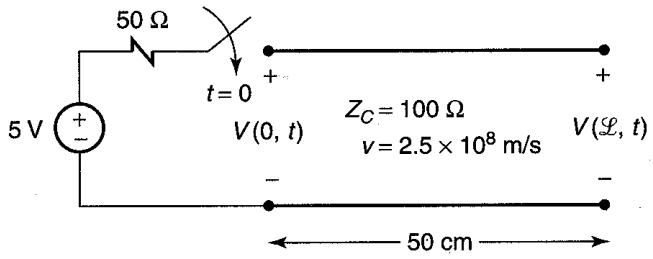


Figure P6.2.10 Problem 6.2.10.

6.2.11. Sketch the input voltage to the line, $V(0,t)$, and the load current, $I(\mathcal{L},t)$, for the problem depicted in Fig. P6.2.11 for $0 < t < 10$ μs. What should these plots converge to in the steady state? [$V(0,t)$,$0 < t <$ 2 μs, 66.67 V, 2 μs $< t <$ 4 μs, 22.22 V, 4 μs $< t <$ 6 μs, 7.407 V, 6 μs $< t <$ 8 μs, 2.469 V, 8 μs $< t <$ 10 μs, 0.823, steady state 0 V and $I(\mathcal{L},t)$, $0 < t <$ 1 μs, 0 V, 1 μs $< t <$ 3 μs, 1.33 A, 3 μs $< t <$ 5 μs, 1.778 A, 5 μs $< t <$ 7 μs, 1.926 A, 7 μs $< t <$ 9 μs, 1.975 A, 9 μs $< t <$ 11 μs, 1.992 A, steady state 2 A]

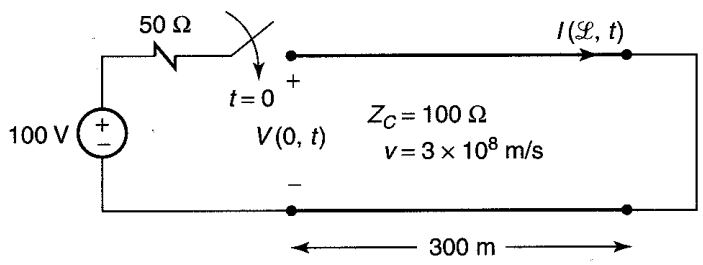


Figure P6.2.11 Problem 6.2.11.

6.2.12. Sketch the input voltage to the line, $V(0,t)$, and the load voltage, $V(\mathcal{L},t)$, for the problem depicted in Fig. P6.2.12 for $0 < t < 32$ ns. What should these plots converge to in the steady state?

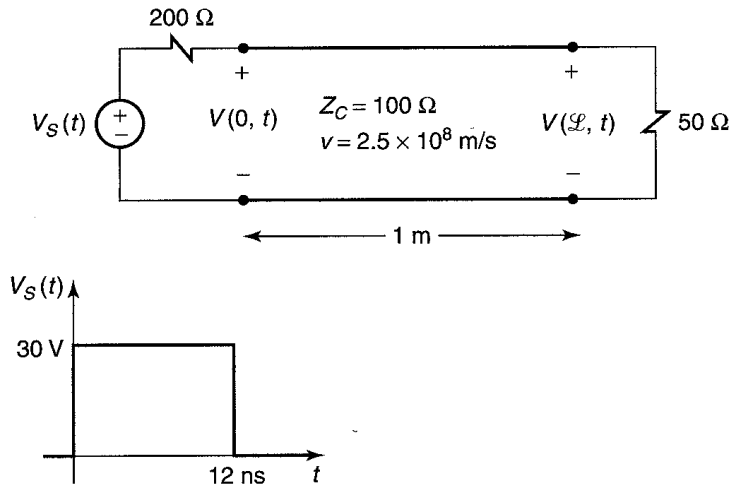


Figure P6.2.12 Problem 6.2.12.

6.2.13. A time-domain reflectometer (TDR) is an instrument used to determine properties of transmission lines. In particular, it can be used to detect the locations of imperfections such as breaks in the line. The instrument launches a pulse down the line and records the transit time for that pulse to be reflected at some discontinuity and to return to the line input. Suppose a TDR having a source impedance of 50 Ω is attached to a 50-Ω coaxial cable having some unknown length and load resistance. The dielectric of the cable is Teflon ($\varepsilon_r = 2.1$). The open-circuit voltage of the TDR is a pulse of duration 10 μs. If the recorded voltage at the input to the line is as shown in Fig. P6.2.13, determine (a) the length of the line and (b) the unknown load resistance.

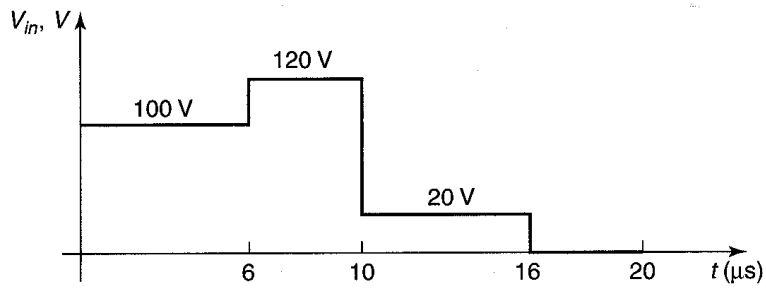


Figure P6.2.13 Problem 6.2.13.

6.2.14. A 12-V battery ($R_S = 0$) is attached to an unknown length of transmission line that is terminated in a resistance. If the input current to the line for 6 μs is as shown in Fig. P6.2.14, determine (a) the line characteristic impedance and (b) the unknown load resistance. [$Z_C = 80\ \Omega, R_L = 262.9\ \Omega$]

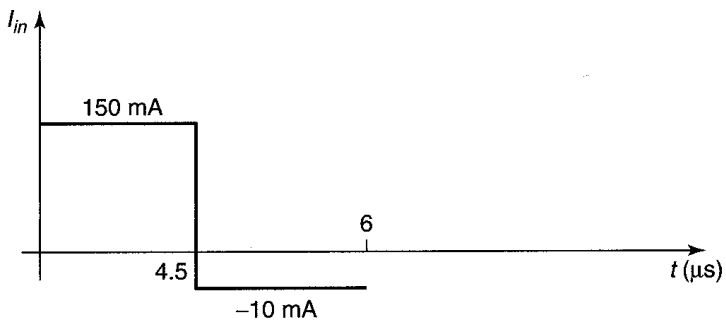


Figure P6.2.14 Problem 6.2.14.

6.2.15. Digital clock and data pulses should ideally consist of rectangular pulses. Actual clock and data pulses, however, resemble pulses having a trapezoidal shape with certain rise and fall times. Depending on the ratio of the rise/fall time to the one-way transit time of the transmission line, the received voltage may oscillate about the desired value, possibly causing a digital gate at that end to switch falsely to an undesired state and cause errors. Matching the line eliminates this problem because there are no reflections, but matching cannot always be accomplished. In order to investigate this problem, consider a line connecting two CMOS gates. The driver gate is assumed to have zero source resistance ($R_S = 0$), and the open-circuit voltage is a ramp waveform (simulating the leading edge of the clock/data pulse) given by $V_S(t) = 0$ for $t < 0$, $V_S(t) = 5(t/\tau)_r$ V for $0 \leq t \leq \tau_r$, and $V_S(t) = 5$ V for $t \geq \tau_r$ where τ_r is the pulse rise time. The input to a CMOS gate (the load on the line here) can be modeled as a capacitance of some 5 pF–15 pF. However, in order to simplify the problem, we will assume that the input to the load CMOS gate is an open circuit $R_L = \infty$. Sketch the load voltage of the line (the input voltage to the load CMOS gate) for line lengths having one-way transit times T such that (a) $\tau_r = T/10$, (b) $\tau_r = 2T$, (c) $\tau_r = 3T$, (d) $\tau_r = 4T$. This example shows that in order to avoid problems resulting from mismatch, one should choose line lengths short enough such that $T \ll \tau_r$, that is, the line one-way delay is much less than the rise time of the clock/data pulses being carried by the line.

6.2.16. Highly mismatched lines in digital products can cause what appears to be "ringing" on the signal output from the line. This is often referred to as "overshoot" or "undershoot" and can cause digital logic errors. To simulate this we will investigate the problem shown in Fig. P6.2.16. Two CMOS gates are connected by a transmission line as shown. A 5-V step function voltage of the first gate is applied. Sketch the output voltage of the line (the input voltage to the load CMOS gate) for $0 < t < 9T$.
[$0 < t < T$, 0 V, $T < t < 3T$, 6.944 V, $3T < t < 5T$, 3.858 V, $5T < t < 7T$, 5.23 V, $7T < t < 9T$, 4.62 V. Steady state is 5 V]

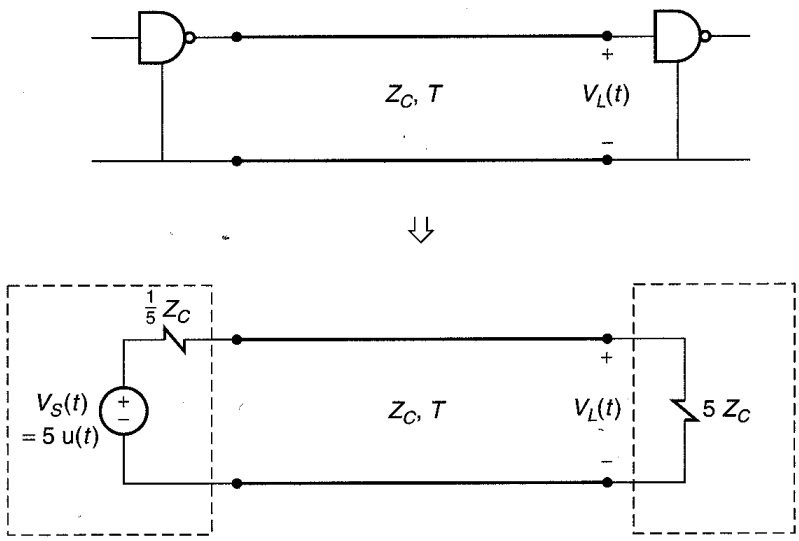


Figure P6.2.16 Problem 6.2.16.

6.2.17. A transmission line of total length 200 m and velocity of propagation of $v = 2 \times 10^8$ m/s has $Z_C = 50\ \Omega$, $R_L = 20\ \Omega$. It is driven by a source having $R_S = 100\ \Omega$ and an open-circuit voltage that is a rectangular pulse of 6-V magnitude and 3-μs duration. Sketch the input current to the line for a total time of 5 μs.

6.2.18. Confirm the results of Problem 6.2.9 using SPICE (PSPICE).

6.2.19. Confirm the results of Problem 6.2.10 using SPICE (PSPICE).

6.2.20. Confirm the results of Problem 6.2.11 using SPICE (PSPICE).

6.2.21. Confirm the results of Problem 6.2.12 using SPICE (PSPICE).

6.2.22. Confirm the results of Problem 6.2.13 using SPICE (PSPICE).

6.2.23. Confirm the results of Problem 6.2.14 using SPICE (PSPICE).

6.2.24. Confirm the results of Problem 6.2.15 using SPICE (PSPICE).

6.2.25. Confirm the results of Problem 6.2.16 using SPICE (PSPICE).

6.2.26. Confirm the results of Problem 6.2.17 using SPICE (PSPICE).

6.2.27. One of the important advantages in using SPICE to solve transmission-line problems is that it will readily give the solution for problems that would be difficult to solve by hand. For example, consider the case of two CMOS inverter gates connected by a 5-cm length of 100-Ω transmission line as shown in Fig. P6.2.27. The output of the driver gate is represented by a ramp waveform voltage rising from 0 V to 5 V in 1 ns and a 30-Ω internal source resistance. The receiving gate is represented at its input by 10 pF. Because of the capacitive load, this would be a difficult problem to do by hand. Use SPICE (PSPICE) to plot the output voltage of the line, $V_L(t)$, for $0 < t < 10$ ns. Observe in the solution that this output voltage varies rather drastically about the desired 5 V level going from 4.2 V to 7 V before it stabilizes to 5 V well after 10 ns.

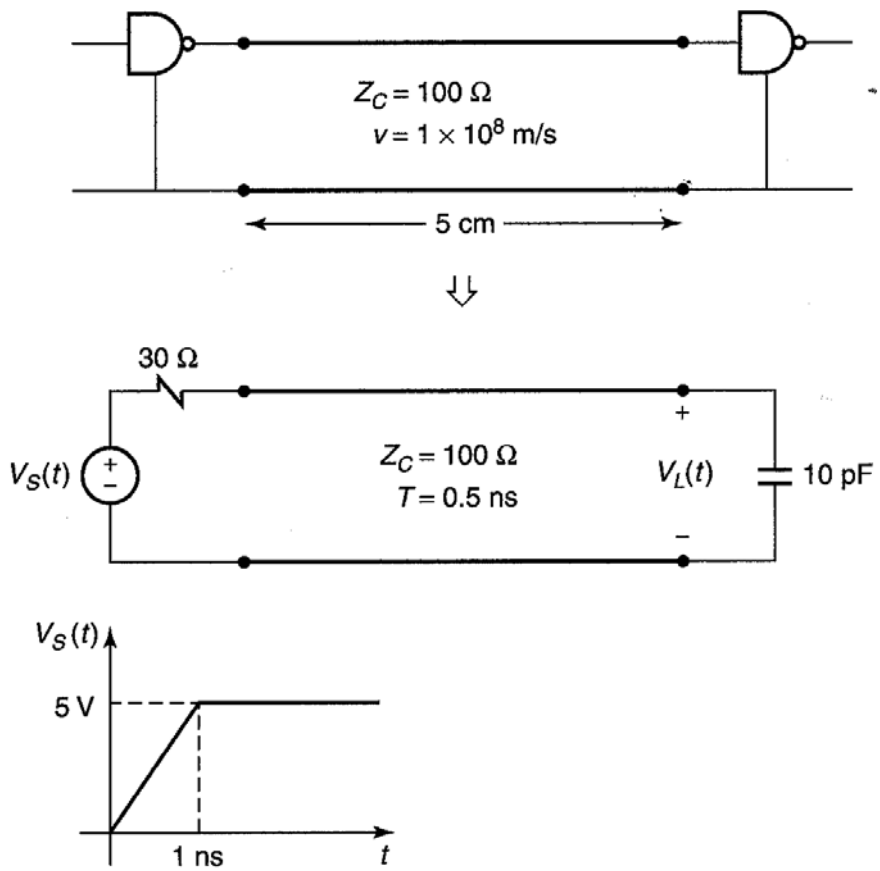


Figure P6.2.27 Problem 6.2.27.