

# CMOS - Transistors and Inverters

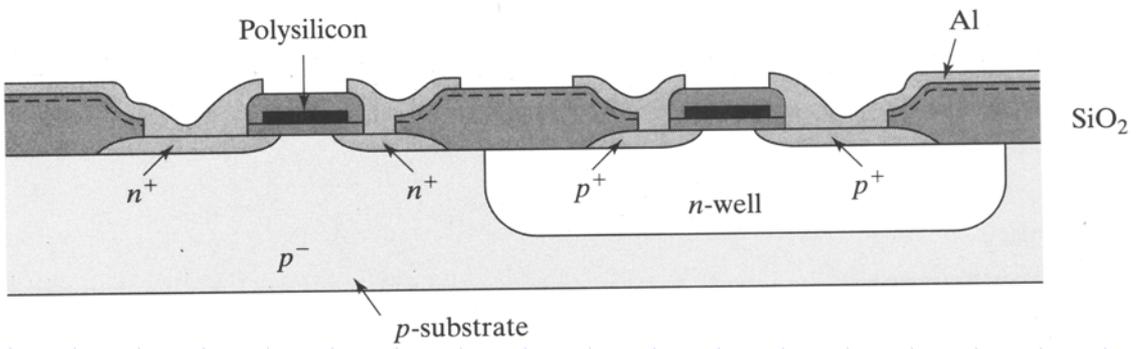
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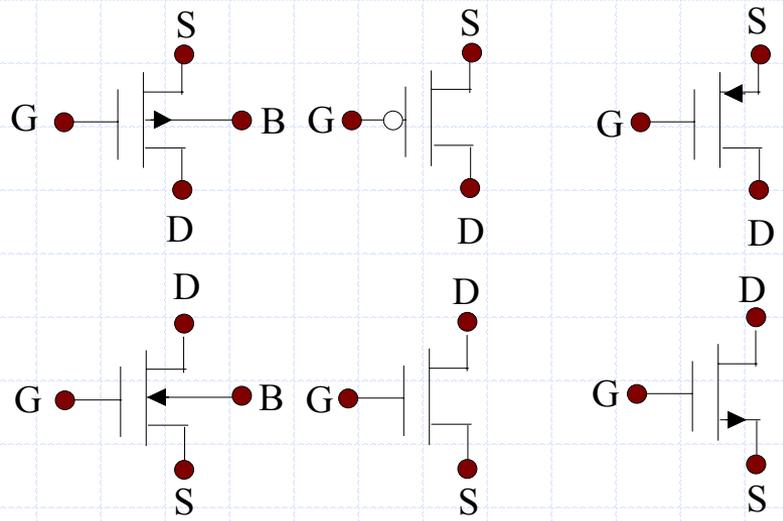
University of South Carolina



# Complimentary-MOS Logic (CMOS)



PMOS (P-channel enhancement-mode Metal Oxide Semiconductor transistor)



NMOS (N-channel enhancement-mode Metal Oxide Semiconductor transistor)



# Definition of Symbols

Symbol	Description	Typical Values and Units
$I_D$	Drain Current	1 $\mu\text{A}$ to 100 mA
$V_{DS}$	Drain-Source Voltage	-3 to 3 V
$V_{GS}$	Gate-Source Voltage	-3 to 3 V
$V_T$	MOS Threshold Voltage	-0.8 to 0.8 V
$\mu_n$	Surface Electron Mobility	400 $\text{cm}^2/\text{Vs}$
$\mu_p$	Surface Hole Mobility	150 $\text{cm}^2/\text{Vs}$
$C_{ox}$	Oxide Capacitance per Unit Area	3 to 10 $\text{fF}/\mu\text{m}^2$
$W$	Effective Channel Width	0.2 to 3 $\mu\text{m}$
$L$	Effective Channel Length	0.1 to 0.5 $\mu\text{m}$
$E_{sat}$	Saturation Electric Field Value	1 to 5 $\text{V}/\mu\text{m}$

# Definitions of Some Derived Symbols

Process Transconductance Parameters (A/V<sup>2</sup>)

$$k'_n = \mu_n C_{ox} = \mu_n \epsilon_{ox} / t_{ox}$$

$$k'_p = \mu_p C_{ox} = \mu_p \epsilon_{ox} / t_{ox}$$

Gain Factors (A/V<sup>2</sup>)

$$k_n = k'_n (W_n / L_n)$$

$$k_p = k'_p (W_p / L_p)$$

# Metal Oxide Semiconductor Field-Effect Transistor Behavior

In the resistive region of operation for NMOS:

$$I_D = \frac{\mu_n C_{ox}}{1 + \frac{V_{DS}}{E_{sat} L}} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] = \mu_n C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \kappa(V_{DS})$$

$$\kappa(V_{DS}) = \frac{1}{1 + \frac{V_{DS}}{E_{sat} L}}$$

For long channels or small drain-source voltages,  $\kappa$  approaches 1 and the expression for the drain current reduces to the traditionally used equation describing a MOSFET in its resistive region of operation.  $V_{DS}/L$  is approximately the average electric field in the channel.

# Metal Oxide Semiconductor Field-Effect Transistor Behavior

In the saturation region of operation for NMOS:

$$I_{Dsat} = \mu_n C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DSsat} - \frac{V_{DSsat}^2}{2} \right] \kappa(V_{DSsat}) = v_{sat} C_{ox} W (V_{GS} - V_T - V_{DSsat})$$

$$V_{DSsat} = \frac{V_{GS} - V_T}{1 + \frac{V_{GS} - V_T}{E_{sat} L}}$$

When the electric field in the channel reaches the saturation value, then all carriers at the drain reach the saturation drift velocity ( $v_{sat} = 10^5$  cm/s) and the drain current remains constant (to first order at  $I_{Dsat}$ ) with respect to increases in drain-source voltage.

# PMOS Equations

In the resistive region of operation for PMOS:

$$I_D = \frac{-\mu_p C_{ox}}{1 + \frac{V_{DS}}{E_{sat} L}} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] = -\mu_p C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \kappa(V_{DS})$$

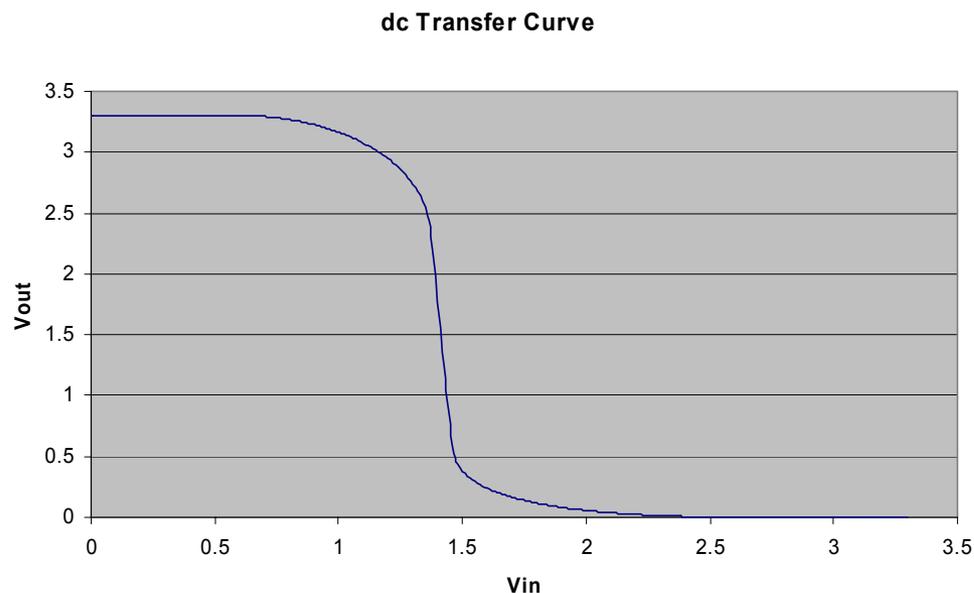
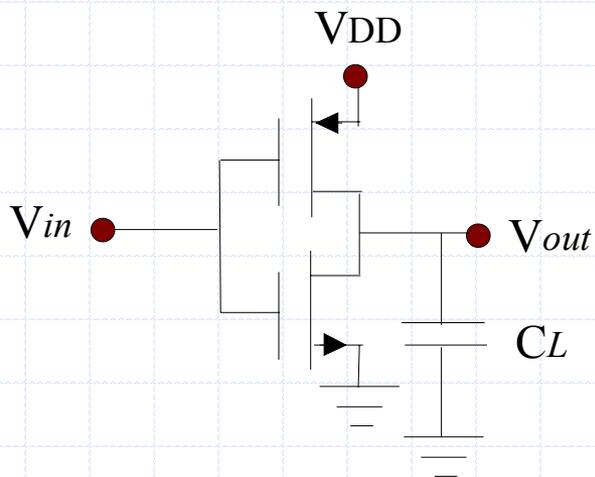
$$\kappa(V_{DS}) = \frac{1}{1 + \frac{V_{DS}}{E_{sat} L}}$$

In the saturation region of operation for PMOS:

$$I_{Dsat} = -\mu_p C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DSsat} - \frac{V_{DSsat}^2}{2} \right] \kappa(V_{DSsat}) = -v_{sat} C_{ox} W (V_{GS} - V_T - V_{DSsat})$$

$$V_{DSsat} = \frac{V_{GS} - V_T}{1 + \frac{V_{GS} - V_T}{E_{sat} L}}$$

# CMOS Buffer/Inverter - Static Operation



$V_{in} = 0 \text{ V} \rightarrow V_{GSp} < 0 \text{ V}, V_{GSn} = 0 \text{ V} \rightarrow$  PMOS "On", NMOS "Off"  $\rightarrow V_{out} \approx V_{DD}$

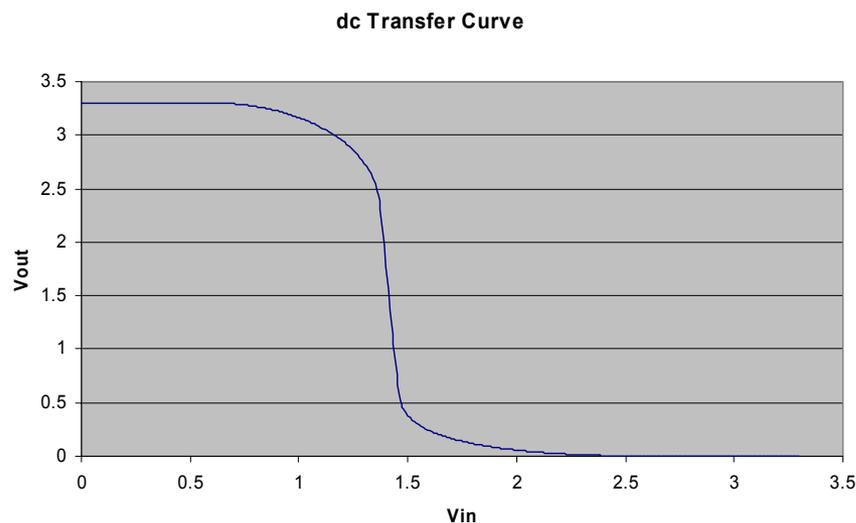
$V_{in} = V_{DD} \rightarrow V_{GSp} = 0 \text{ V}, V_{GSn} > 0 \text{ V} \rightarrow$  PMOS "Off", NMOS "On"  $\rightarrow V_{out} \approx 0 \text{ V}$

No dc current path from source to ground so ideally no power dissipation!

# Transfer Curve Information

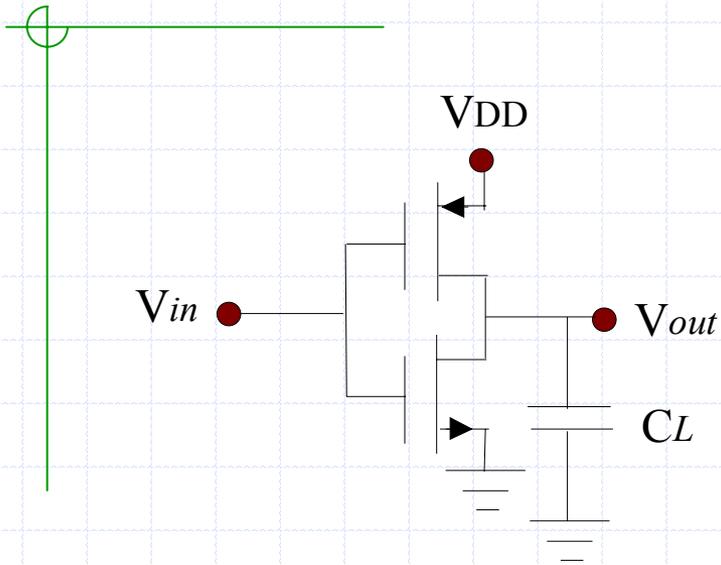
- Gate threshold voltage,  $V_{TH}$

- Noise Margins

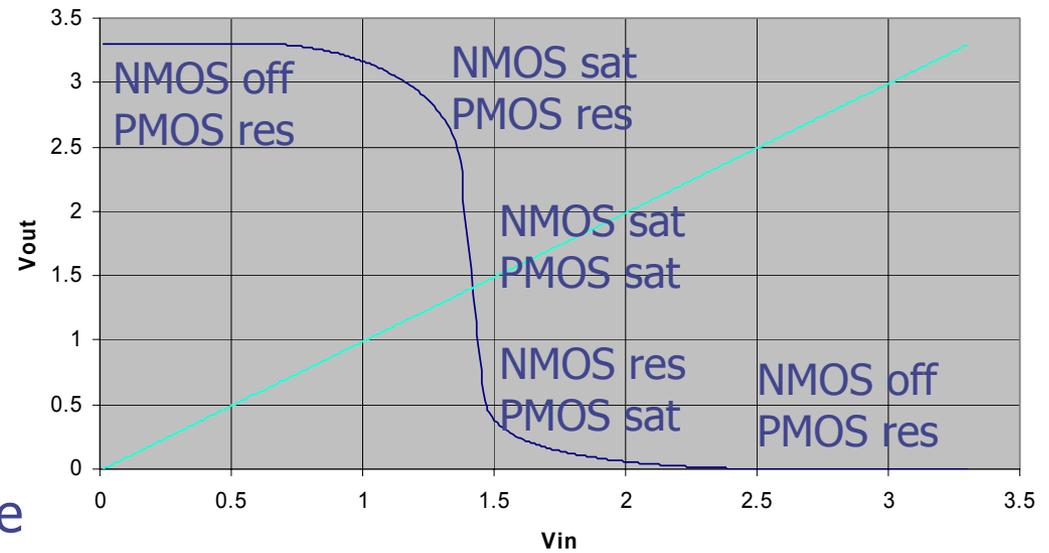


- Small-signal gain of gate at its threshold voltage

# Threshold Voltage



dc Transfer Curve with Gate Threshold



$V_{TH} = 1.43$  V for this example

Gate Threshold Voltage is defined as  
 $V_{TH} \equiv V_{in}$  that gives the same value of  $V_{out}$   
 It is the boundary between logic states.

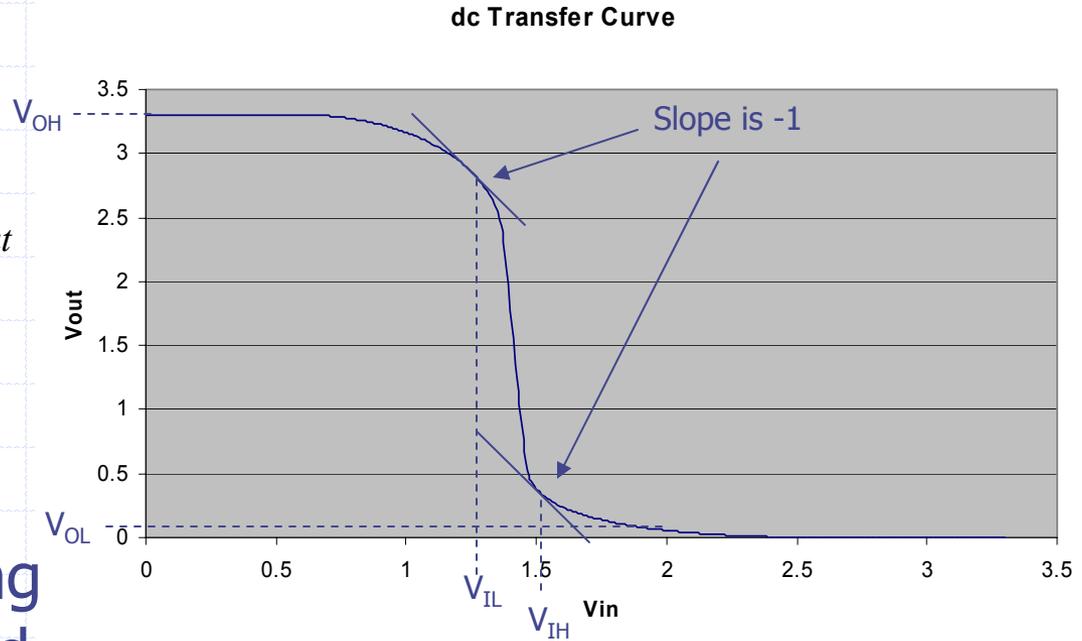
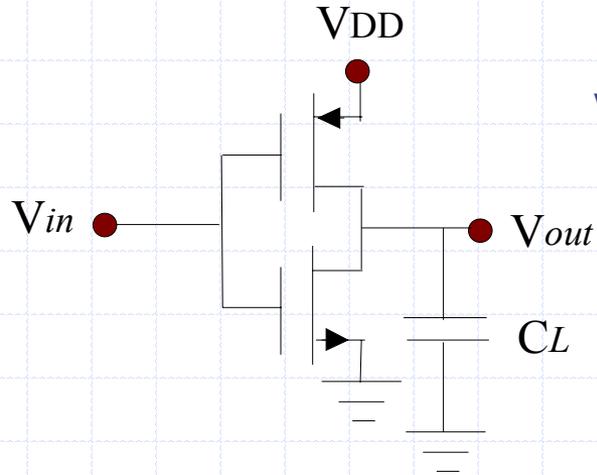
# Threshold Voltage

$$V_{TH} = \frac{\left( V_{Tn} + \frac{V_{DSsatn}}{2} \right) + r \left( V_{DD} + V_{Tp} + \frac{V_{DSsatp}}{2} \right)}{1 + r}$$

$$r = \frac{k_p V_{DSsatp}}{k_n V_{DSsatn}} = \frac{\mu_p \left( \frac{W_p}{L_p} \right) V_{DSsatp}}{\mu_n \left( \frac{W_n}{L_n} \right) V_{DSsatn}} = \frac{v_{satp} W_p}{v_{satn} W_n}$$

Assumes identical oxide thicknesses for NMOS and PMOS, and ignores channel length modulation effects.

# Noise Margins



The points corresponding to  $V_{IL}$  and  $V_{IH}$  are defined where the gain is  $-1$ .  
*i.e.*  $dV_{out}/dV_{in} = -1$

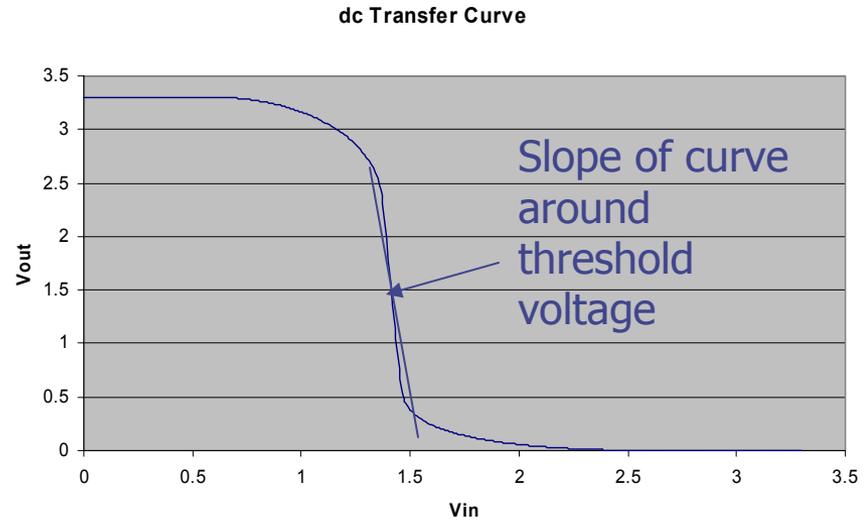
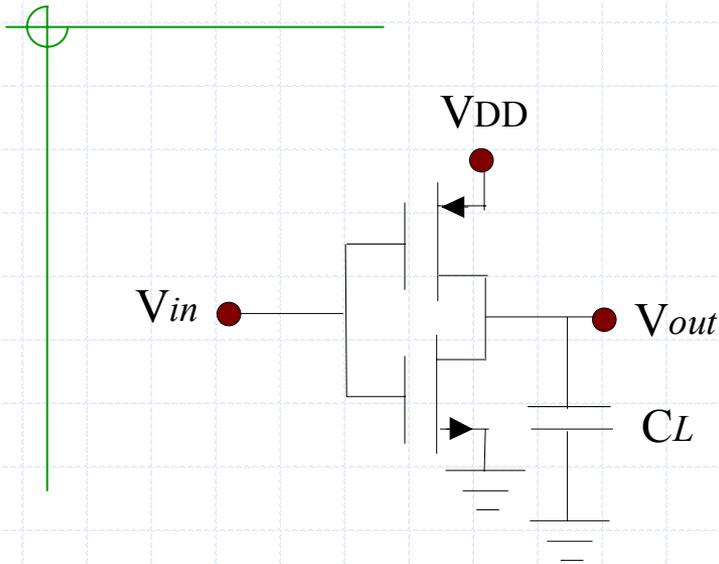
Noise margins are the difference in what the nominal output voltage is at a given logic level and what the input of a similar gate must see to interpret the level correctly.

Noise Margins are defined as:

$$NM_L \equiv V_{IL} - V_{OL} = \text{Max. input for logic 0} - \text{Nominal value of logic 0}$$

$$NM_H \equiv V_{OH} - V_{IH} = \text{Nominal value of logic 1} - \text{Min. value for logic 1}$$

# Small-signal Gain

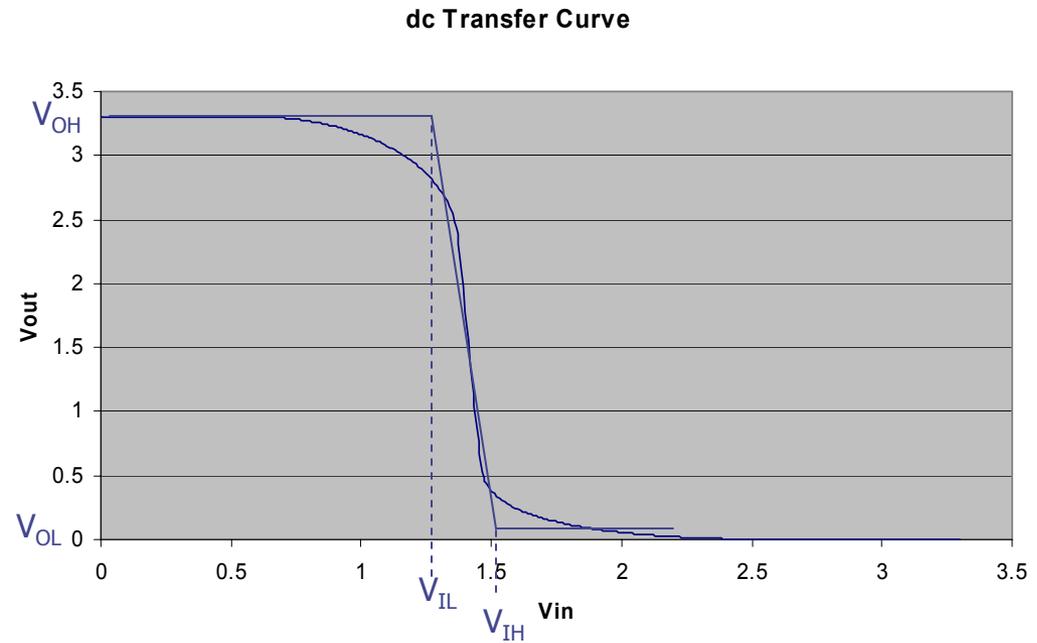
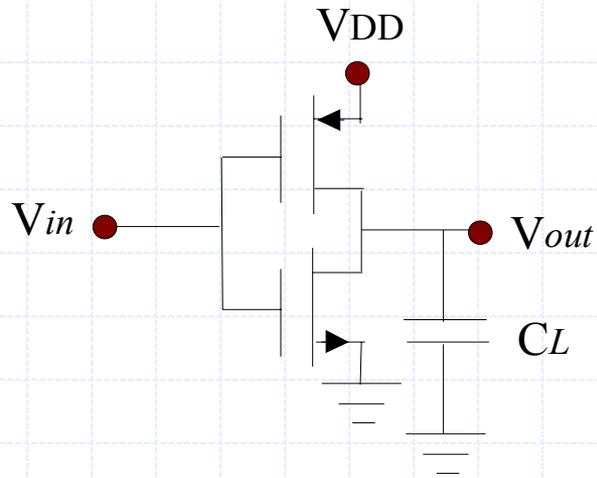


For this example:

$$g = |A_v| = \left. \frac{dV_{out}}{dV_{in}} \right|_{V_{TH}} = \frac{1}{1/26} = 26$$

Must have voltage gain  $> 1$  otherwise signals will fall below  $V_{TH}$  after passing through several gates. Minimum allowable value for absolute value of voltage gain of a digital gate is about  $\sqrt{2}$ . Typical gains are from 2 to 50.

# Calculation of Noise Margins



Linearize the transfer curve as shown with the slope between the transitions equal to the gain,  $g$ , at  $V_{TH}$ .

# Calculation of Noise Margins

From the definition of gain and the nominal values of the gate:

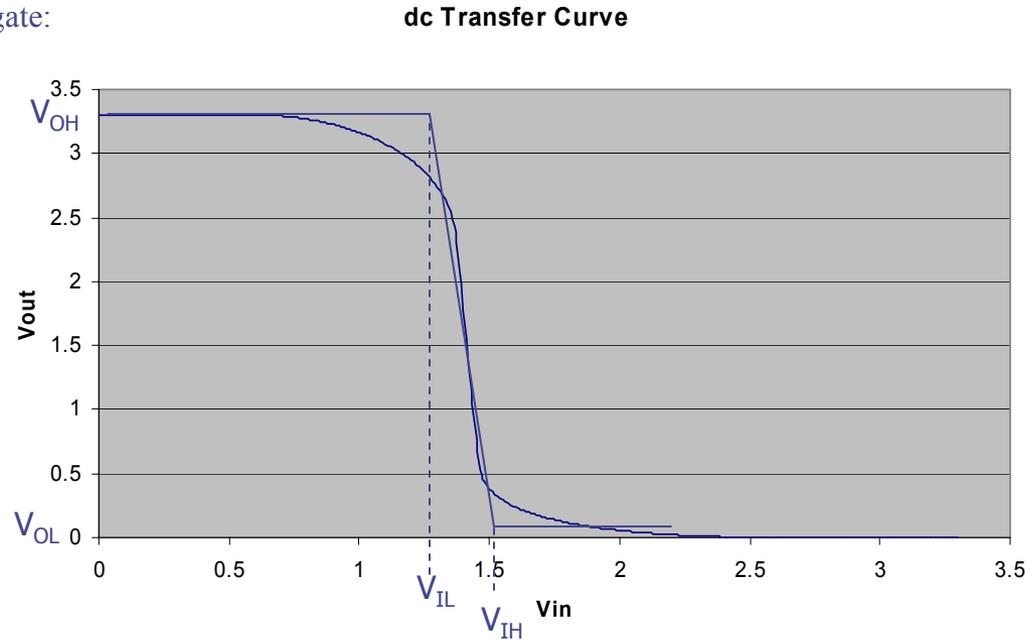
$$g = \frac{V_{OH} - V_{OL}}{V_{IL} - V_{IH}} = -\frac{V_{DD} - 0}{V_{IH} - V_{IL}}$$

From the equation of the slanted line:

$$V_{IH} = V_{TH} - \frac{V_{TH}}{g}$$

Therefore combining the top two equations:

$$V_{IL} = V_{TH} + \frac{V_{DD} - V_{TH}}{g}$$



$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{TH} + \frac{V_{TH}}{g} \approx V_{OH} - V_{TH} \approx V_{DD} - V_{TH}$$

for large gain

$$NM_L = V_{IL} - V_{OL} = V_{IL} = V_{TH} + \frac{V_{DD} - V_{TH}}{g} \approx V_{TH} - V_{OL} \approx V_{TH}$$

for large gain

# Calculation of Gain at $V_{TH}$

Write a nodal equation with the drain currents of each transistor equal to each other and  $V_{GSn} = V_{in}$ ,  $V_{DSn} = V_{out}$ ,  $V_{GSp} = V_{in} - V_{DD}$ , and  $V_{DSp} = V_{out} - V_{DD}$ .

Next, differentiate  $V_{out}$  with respect to  $V_{in}$  and solve for  $dV_{out}/dV_{in}$

$$g = \frac{k_n V_{DSsatn} (1 + \lambda_n V_{TH}) + k_p V_{DSsatp} (1 + \lambda_p V_{TH} - \lambda_p V_{DD})}{\lambda_n k_n V_{DSsatn} \left( V_{TH} - V_{Tn} - \frac{V_{DSsatn}}{2} \right) + \lambda_p k_p V_{DSsatp} \left( V_{TH} - V_{DD} - V_{Tp} - \frac{V_{DSsatp}}{2} \right)} \approx \frac{1 + r}{\left( V_{TH} - V_{Tn} - \frac{V_{DSsatn}}{2} \right) (\lambda_n - \lambda_p)}$$

Channel-length modulation factors,  $\lambda$ , CANNOT be ignored for this analysis (depletion region at drain-end encroaches on channel and reduces its effective length thus causing drain current to increase).

# Channel-Length Modulation Factor

$$I_D = I_{Dsat} (1 + \lambda V_{DS})$$

$$l_a = (0.22 \text{ cm}^{1/6}) d_j^{1/2} t_{ox}^{1/3}$$

$d_j$  is the drain junction depth

$$\lambda = \frac{l_a \ln \left[ 1 + \frac{V_{DS} - V_{DSsat}}{V_E} \right]}{V_{DS} \left\{ L - l_a \ln \left[ 1 + \frac{V_{DS} - V_{DSsat}}{V_E} \right] \right\}}$$

$V_E$  is determined empirically and is  $< 1 \text{ V}$

Y.A. El-Mansy and A.R. Boothroyd, "A simple two-dimensional model for IGFET operation in the saturation region," *IEEE Trans. ED*, vol. 24, pp. 254-262, 1977.

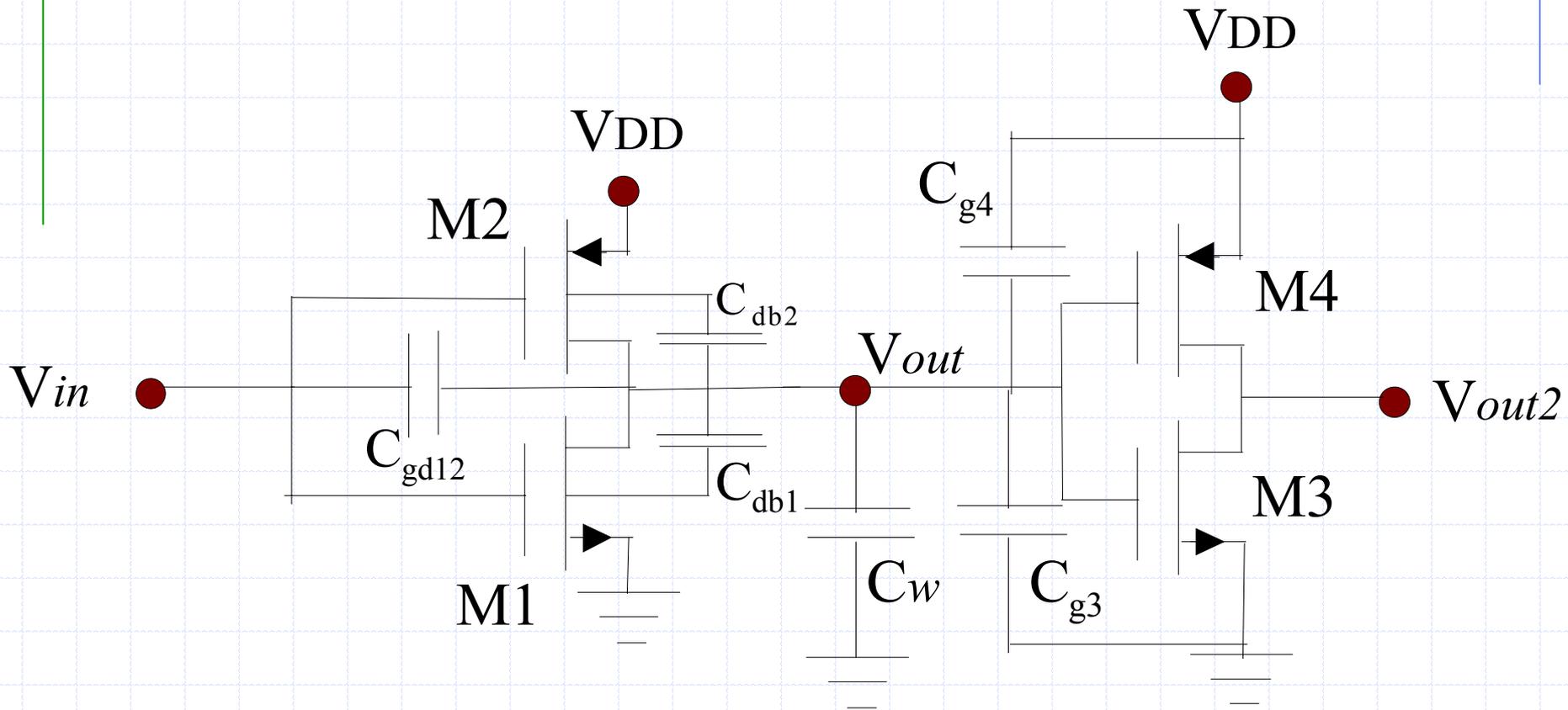
P.K. Po, "Approaches to scaling," pp. 1-37, *Advanced MOS Device Physics*, N.G. Einspruch and G. Goldenblat, eds., **VLSI Electronics**, vol. 18, Academic Press, New York, 1989.

N.D. Arora, *MOSFET Models for VLSI Circuit Simulation-Theory and Practice*, **Computational Microelectronics Series**, S. Selberherr, ed., Springer-Verlag, New York, 1993.

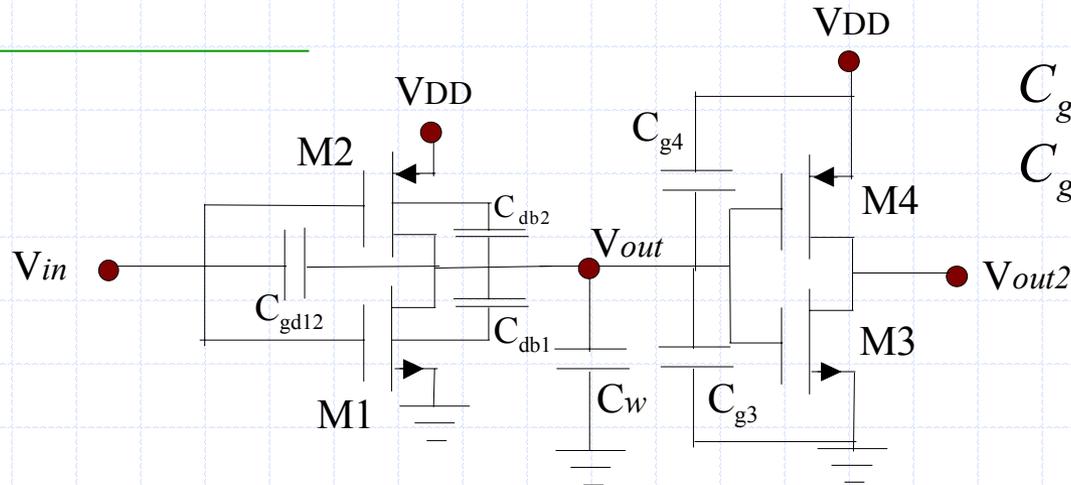
H.C. de Graaff and F.M. Klaassen, *Compact Transistor Modeling for Circuit Design*, Springer-Verlag, New York, 1990.



# Parasitic Capacitances Influencing CMOS Inverter Pair



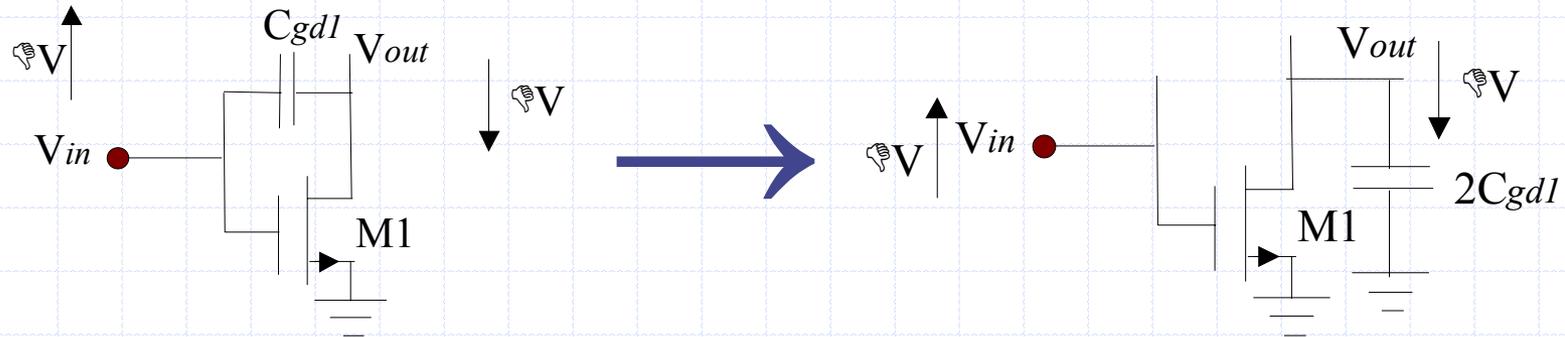
# Miller Capacitances



$$C_{gd2} = 2C_{GDOp}W_p = 2C_{oxp}x_{dp}W_p$$

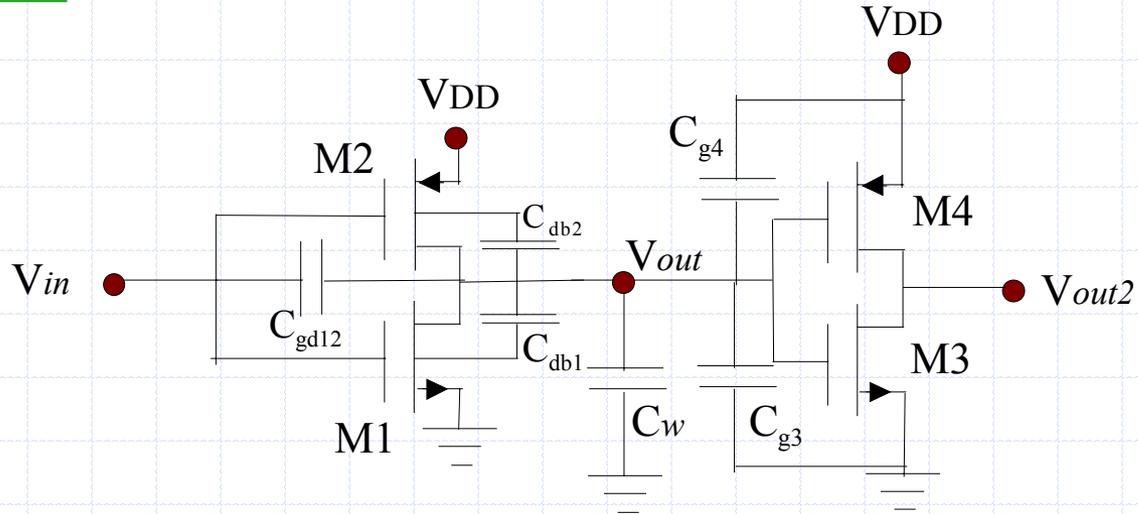
$$C_{gd1} = 2C_{GDO n}W_n = 2C_{oxn}x_{dn}W_n$$

$C_{GDO}$  is the overlap capacitance per unit width,  $x_d$  is the extension of the drain implantation under the gate oxide.



Can replace gate-drain capacitances (Miller caps) with equivalent at output wrt ground because of  $\Delta V$  change at each capacitance terminal.

# Fan-out Gate Capacitances

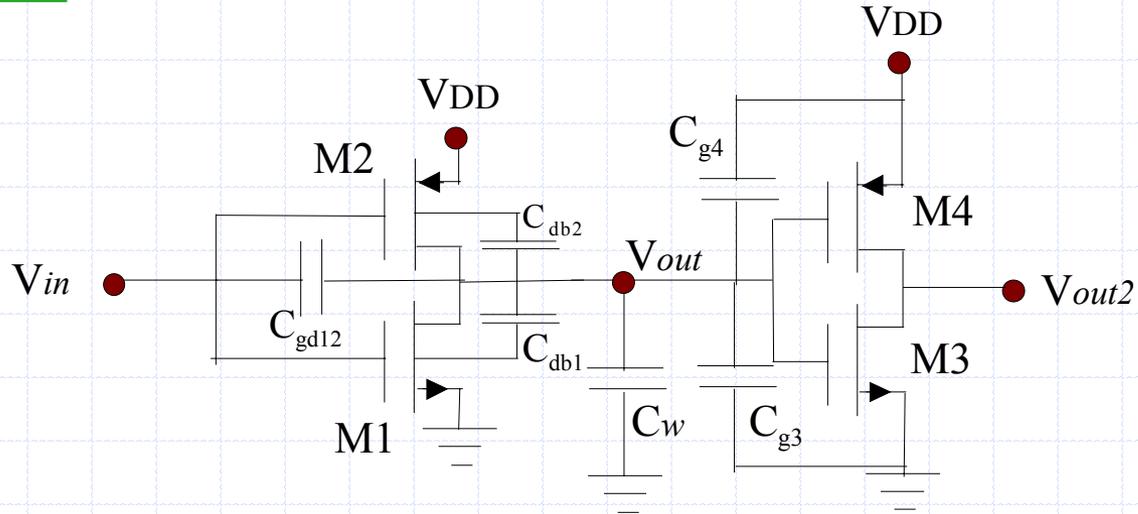


Each gate capacitance is made of the oxide capacitance along the channel plus the overlap capacitance between gate oxide and source, plus the overlap capacitance between the drain and gate oxide.

$$C_{fan-out} = C_{g3} + C_{g4} = (C_{GSO_n}W_n + C_{GDO_n}W_n + C_{oxn}W_nL_n) + (C_{GSO_p}W_p + C_{GDO_p}W_p + C_{oxp}W_pL_p)$$

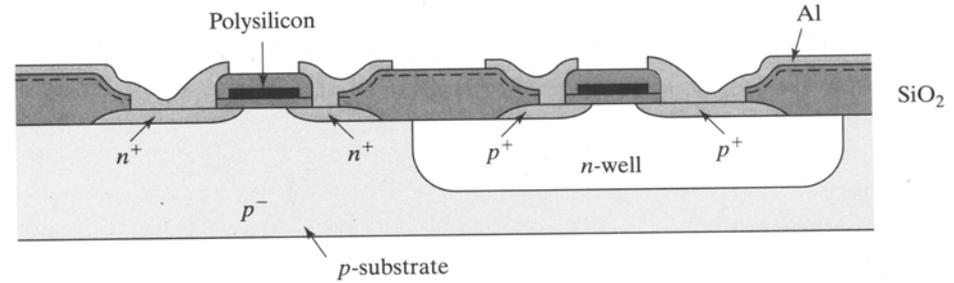
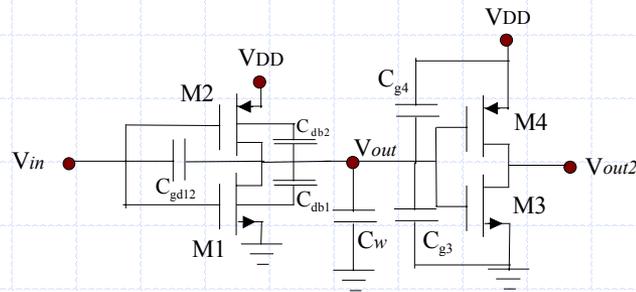
$$= C_{oxn}W_n(2x_n + L_n) + C_{oxp}W_p(2x_p + L_p)$$

# Wiring Capacitance



The wiring capacitance,  $C_w$ , depends upon the length and width of the connecting traces and is a function of the distance between load gates and driving gates, as well as the number of load gates.

# Diffusion Capacitances between Drain and Body



$C_{db}$  is due to the reverse biased  $pn$ -junction between the drain and body AND is the capacitance that is non-linear and voltage dependent.

$$C_{db} = C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{V_{bi}}\right)^m}$$

$$C_{j0} = \sqrt{\frac{q\epsilon_{si}}{2V_{bi}} \left( \frac{N_A N_D}{N_A + N_D} \right)}$$

$C_{j0}$  is the zero-biased junction capacitance per unit area.  
 $V_D$  is the applied body voltage with respect to the drain.  
 $V_{bi}$  is the built-in potential of the junction (typically about 0.64 V).

$m$  is the grading factor (1/2 for abrupt junctions and 1/3 for linear junctions).

$N_A$  and  $N_D$  are the acceptor and donor impurity concentrations, respectively.

# Approximate Diffusion Capacitance between Drain and Body

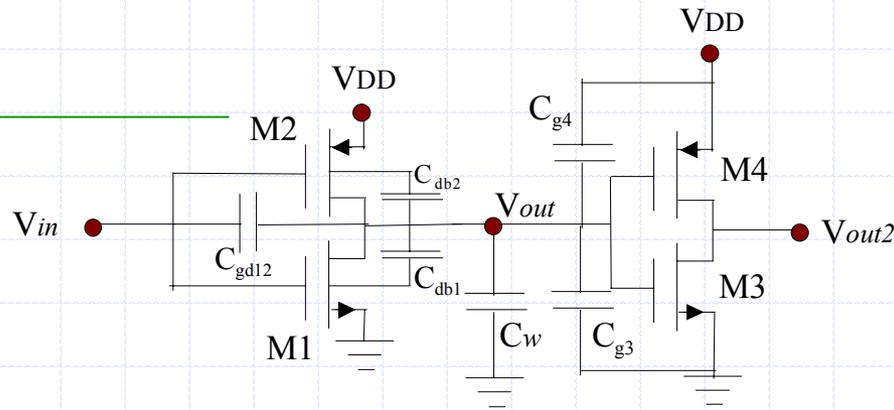
Using an approximation for the large-signal swing in capacitance and in terms of the grading factor gives:

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-V_{bi}^m}{(V_{high} - V_{low})(1-m)} [(V_{bi} - V_{high})^{1-m} - (V_{bi} - V_{low})^{1-m}]$$

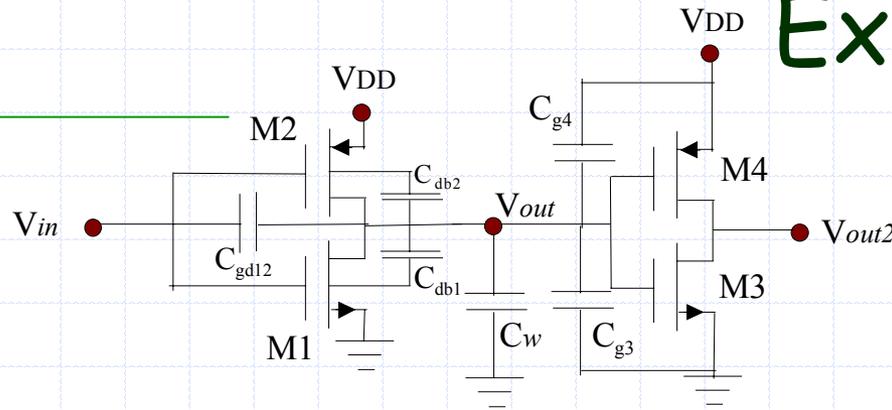
$$C_{j0} = \sqrt{\frac{q\epsilon_{si}}{2V_{bi}} \left( \frac{N_A N_D}{N_A + N_D} \right)}$$

# Example



The propagation delay is defined by the time between the 50% transitions of the input and output. For a CMOS inverter this is the time instance where  $V_{out}$  reaches 1.25 V as the output voltage swing from rail-to-rail is 2.5 V ( $V_{DD} = 2.5$  V). The drain-body capacitance is linearized over the voltage intervals of 2.5 V to 1.25 V for high-to-low and 0 V to 1.25 V for low-to-high transitions of the NMOS (M1). A similar computation is performed for the PMOS.

# Example (page 2)



During the high-to-low transition of the output:

For the NMOS:

$$V_{high} = -2.5 \text{ V}$$

$$V_{low} = -1.25 \text{ V}$$

For the PMOS:

$$V_{high} = -1.25 \text{ V}$$

$$V_{low} = 0 \text{ V}$$

During the low-to-high transition of the output:

For the NMOS:

$$V_{high} = -1.25 \text{ V}$$

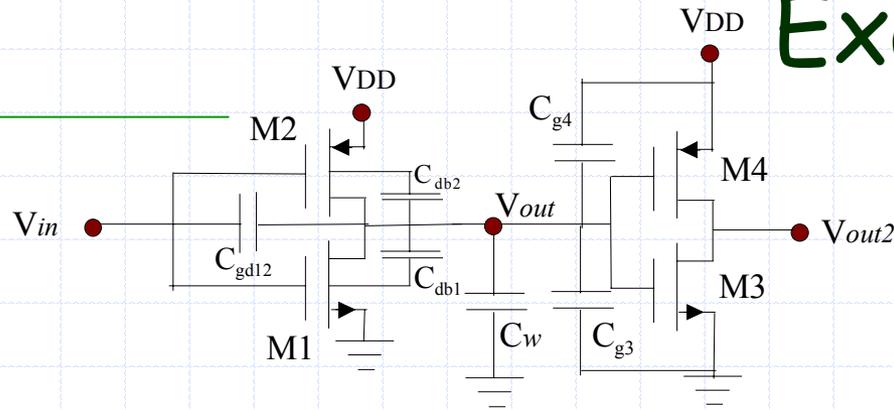
$$V_{low} = 0 \text{ V}$$

For the PMOS:

$$V_{high} = -2.5 \text{ V}$$

$$V_{low} = -1.25 \text{ V}$$

# Example (page 3)



During both transitions of the output:

For the NMOS:

*Bottom plate:*  $m=0.5$ ,  $V_{bi}=0.9$  V

*Side Wall:*  $m=0.44$ ,  $V_{bi}=0.9$  V

For the PMOS:

*Bottom plate:*  $m=0.48$ ,  $V_{bi}=0.9$  V

*Side Wall:*  $m=0.32$ ,  $V_{bi}=0.9$  V

# Example (page 4)

	$K_{eq}$
NMOS Bottom Plate (L-H)	0.79
NMOS Sidewall (L-H)	0.81
PMOS Bottom Plate (L-H)	0.59
PMOS Sidewall (L-H)	0.7
NMOS Bottom Plate (H-L)	0.57
NMOS Sidewall (H-L)	0.61
PMOS Bottom Plate (H-L)	0.79
PMOS Sidewall (H-L)	0.86

	W/L	$A_D (\mu\text{m}^2)$	$P_D (\mu\text{m})$	$A_S (\mu\text{m}^2)$	$P_S (\mu\text{m})$
<b>NMOS</b>	0.375/0.25	0.3	1.875	0.3	1.875
<b>PMOS</b>	1.125/0.25	0.7	2.375	0.7	2.375

Capacitor	Value (fF) High to Low	Value (fF) Low to High
$C_{gd1}$	0.23	0.23
$C_{gd2}$	0.61	0.61
$C_{db1}$	0.66	0.90
$C_{db2}$	1.5	1.15
$C_{g3}$	0.76	0.76
$C_{g4}$	2.28	2.28
$*C_w$	0.12	0.12
<b><math>C_L</math> (total)</b>	<b>6.16</b>	<b>6.05</b>

# Propagation Delay

During the high-to-low transition, the PMOS is turning off and the NMOS is on. Represent the NMOS by its average equivalent resistance during the load capacitance discharge. Use similar expressions for the low-to-high transition.

$$R_{eq} = \frac{1}{V_{DD}/2} \int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{Dsat}(1+\lambda V)} dV \approx \frac{3V_{DD}}{4I_{Dsat}} \left( 1 - \frac{7\lambda V_{DD}}{9} \right)$$

$$t_{pHL} = 0.69 R_{eqn} C_{L-HL} \quad I_{Dsat} = k' \frac{W}{L} \left[ (V_{DD} - V_t) V_{DSsat} - \frac{V_{DSsat}^2}{2} \right]$$

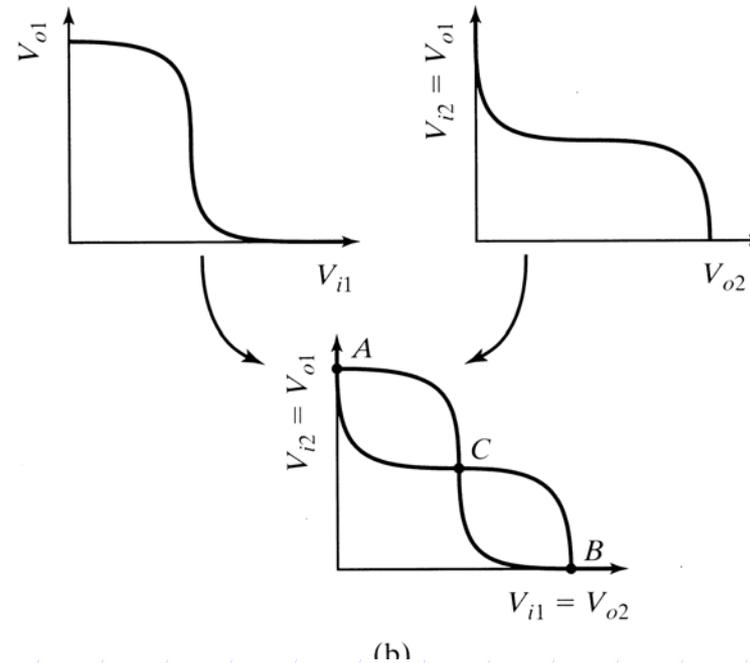
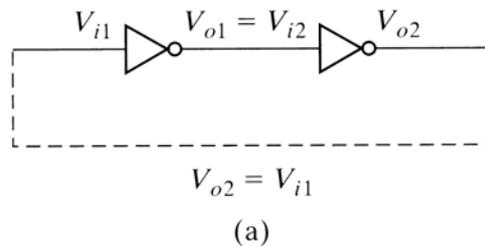
$$t_{pLH} = 0.69 R_{eqp} C_{L-LH}$$

Propagation Delay of Inverter is average of the two values:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.345 (R_{eqp} C_{L-LH} + R_{eqn} C_{L-HL}) \approx 0.345 C_{Lavg} (R_{eqp} + R_{eqn})$$



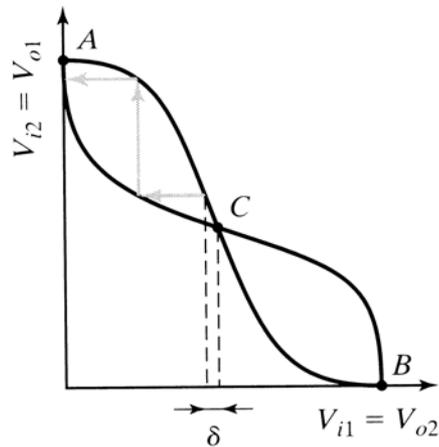
# Metastability



Two inverters cascaded, with a gain in the transition region  $>1$ , has two stable operating points, A and B, and one metastable operating point, C.

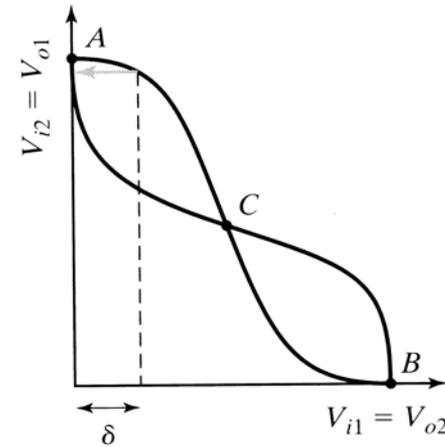
NOTE: Gain near A and B is  $\ll 1$ .

# Metastability



(a)

In figure (a) if initial operating point is C, any noise will cause transition to a stable operating point such as A.



(b)

In figure (b) if initial operating point is away from C, any noise will cause transition back to a stable operating point such as A.

# SPICE Models

## ■ Level 1:

- Shichman-Hodges model based on square-law, long-channel expressions between current and voltage.
- DOES NOT HANDLE SHORT CHANNEL EFFECTS!

## ■ Level 2

- Geometry based model that incorporates velocity saturation, mobility dependencies, and drain-induced barrier lowering.

# SPICE Models (cont.)

## ■ Level 3:

- Semiempirical model combining analytical and empirical expressions. Uses measured data for model parameters.
- Works well for channel lengths down to about 1  $\mu\text{m}$ .

## ■ Berkeley Short-channel IGFET Model (BSIM)

- Analytically simple with a 'small' number of parameters derived from empirical data.
- BSIM3v3 model (Level 49) has over 200 parameters, most related to modeling 2<sup>nd</sup> order effects.
- Manufacturer provides a set of models valid over a limited parameter space of L and W (delineated by LMIN, LMAX, WMIN, and WMAX, called a bin).

<http://bwrc.eecs.berkeley.edu/IcBook/>  
for BSIM and Matlab models



# SPICE Models-Example File

A CMOS Inverter using Level 3 Model for 0.8 um Process

```

*
.MODEL nch NMOS
+ LEVEL=3 PHI=0.70 TOX=1.0E-08 XJ=0.20U TPG=1
+ VTO=0.8 DELTA=2.5E-01 LD=4.0E-08 KP=1.88E-04
+ UO=545 THETA=2.5E-01 RSH=2.1E+01 GAMMA=0.62
+ NSUB=1.4E+17 NFS=7.1E+11 VMAX=1.9E+05 ETA=2.2E-02
+ KAPPA=9.7E-02 CGDO=3.7E-10 CGSO=3.7E-10 CGBO=4.0E-10
+ CJ=5.4E-04 MJ=0.6 CJSW=1.5E-10 MJSW=0.3 PB=0.99
*
.MODEL pch PMOS
+ LEVEL=3 PHI=0.70 TOX=1.0E-08 XJ=0.20U TPG=-1
+ VTO=-0.9 DELTA=2.5E-01 LD=6.7E-08 KP=4.45E-05
+ UO=130 THETA=1.8E-01 RSH=3.4E+00 GAMMA=0.52
+ NSUB=9.8E+16 NFS=6.5E+11 VMAX=3.1E+05 ETA=1.8E-02
+ KAPPA=6.3E+00 CGDO=3.7E-10 CGSO=3.7E-10 CGBO=4.3E-10
+ CJ=9.3E-04 MJ=0.5 CJSW=1.5E-10 MJSW=0.3 PB=0.95
*
M1 3 2 0 0 nch W=5u L=0.8u AS=7.2p PS=7.6u AD=7.2p PD=7.6u
M2 3 2 1 1 pch W=5u L=0.8u AS=9.9p PS=9.1u AD=9.9p PD=9.1u
CL 3 0 0.05pF
*
VDD 1 0 3.3V
VIN 2 0 PULSE(0 3.3 0 100p 100p 5n 10n)
*
.TRAN 0.05n 10n
*
.DC VIN 0V 3.3V 0.01V
*
.PROBE
*
.END

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# References for CMOS Transistors

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