Matthew J. Adiletta
Intel Fellow, Intel Architecture Group
Director, Communication Processor Architecture
INTEL CORPORATION

Patents

- 6,823,438, Method for memory allocation and management using push/pop apparatus, 11/23/2004
- 6,792,488, Communication between processors, 9/14/2004
- 6,760,478, Method and apparatus for performing two pass quality video compression through pipelining and buffer management, 7/6/2004
- 6,728,845, SRAM controller for parallel processor architecture and method for controlling access to a RAM using read and read/write queues, 4/27/2004
- 6,721,925, Employing intelligent logical models to enable concise logic representations for clarity of design description and for rapid design capture, 4/13/2004
- 6,694,380, Mapping requests from a processing unit that uses memory-mapped input-output space, 2/17/2004
- 6,687,246, Scalable switching fabric, 2/3/2004
- 6,681,300, Read lock miss control and queue management, 1/20/2004
- 6,671,827, Journaling for parallel hardware threads in multithreaded processor, 12/30/2003
- 6,668,317, Microengine for parallel processor architecture, 12/23/2003
- 6,668,311, Method for memory allocation and management using push/pop apparatus, 12/23/2003
- 6,667,920, Scratchpad memory, 12/23/2003
- 6,661,794, Method and apparatus for gigabit packet assignment for multithreaded packet processing, 12/9/2003
- 6,643,836, Displaying information relating to a logic design, 11/4/2003
- 6,640,329, Real-time connection error checking method and process, 10/28/2003
- 6,631,462, Memory shared between processing threads, 10/7/2003
- 6,631,430, Optimizations to receive packet status from fifo bus, 10/7/2003
- 6,629,237, Solving parallel problems employing hardware multi-threading in a parallel processing environment, 9/30/2003
- 6,625,654, Thread signaling in multi-threaded network processor, 9/23/2003
- 6,606,704, Parallel multithreaded processor with plural microengines executing multiple threads each microengine having loadable microcode, 8/12/2003
- 6,587,906, Parallel multi-threaded processing, 7/1/2003
- 6,584,522, Communication between processors, 6/24/2003
- 6,577,542, Scratchpad memory, 6/10/2003

- 6,560,667, Handling contiguous memory references in a multi-queue system, 5/6/2003
- 6,532,509, Arbitrating command requests in a parallel multi-threaded processing system, 3/11/2003
- 6,463,072, Method and apparatus for sharing access to a bus, 10/8/2002
- 6,427,196, SRAM controller for parallel processor architecture including address and command queue and arbiter, 7/30/2003
- 6,411,651, Method and system for distributed video compression in personal computer architecture, 6/25/2002
- 6,324,624, Read lock miss control and queue management, 11/27/2001
- 6,307,789, Scratchpad memory, 10/23/2001
- 6,304,604, Method and apparatus for configuring compressed data coefficients to minimize transpose operations, 10/16/2001
- 6,295,546, Method and apparatus for eliminating the transpose buffer during a decomposed forward or inverse 2-dimensional discrete cosine transform through operand decomposition, storage and retrieval, 9/25/2001
- 6,279,062, System for reducing data transmission between coprocessors in a video compression/decompression environment by determining logical data elements of non-zero value and retrieving subset of the logical data elements, 8/21/2001
- 6,160,809, Distributed packet data with centralized snooping and header processing router, 12/12/2000
- 6,101,276, Method and apparatus for performing two pass quality video compression through pipelining and buffer management, 8/8/2000
- 6,052,706, Apparatus for performing fast multiplication, 4/18/2000
- 6,026,217, Method and apparatus for eliminating the transpose buffer during a decomposed forward or inverse 2-dimensional discrete cosine transform through operand decomposition storage and retrieval, 2/15/2000
- 5,995,080, Method and apparatus for interleaving and de-interleaving YUV pixel data, 11/30/1999
- 5,968,153, Mechanism for high bandwidth DMA transfers in a PCI environment, 10/19/1999
- 5,884,050, Mechanism for high bandwidth DMA transfers in a PCI environment, 3/16/1999
- 5,825,680, Method and apparatus for performing fast division, 10/20/1998
- 5,793,658, Method and apparatus for video compression and decompression using high speed discrete cosine transform, 8/11/1998
- 5,159,568, High speed parallel multiplier circuit, 10/27/1992
- 5,146,421, High speed parallel multiplier circuit, 9/8/1992
- 4,992,968, Division method and apparatus including use of a Z--Z plot to select acceptable quotient bits, 2/12/1991
- 4,805,131, BCD adder circuit, 2/14/1989

Publications

- Adiletta, Matthew; Berstein, Debra; Rosebluth, Mark; Wilkinson, Hugh; and Wolrich, Gilbert, "The Next Generation of Intel IXP Network Processors," Intel Technology Journal, Volume 6, Issue 3, August 15, 2002.
- Adiletta, Matthew; Hooper, Donald; and Wilde, Myles, "Packet over SONET: Achieving 10 Gigabit/sec Packet Processing with an IXP2800," Intel Technology Journal, Volume 6, Issue 3, August 15, 2002.
- Adiletta, Matthew; Beck, John; Carrigan, Doug; Rosenbluth, Mark; Tiso, Bill; and Hady, Frank, "Enterprise Edge Convergence: Packet Processing and Computing Silicon in the Data Center," Volume 7, Issue 4, November 14, 2003.
- Adiletta, Matthew; Bernstein, Debra; Ho, Samuel; Emer, Joel; and Wheeler, William, "Architecture of a flexible real-time Video encoder/decoder: The DECchip 21230," IEEE/SPIE, Proceedings Multimedia Hardware Architectures 1997.
- Adiletta, Matthew, and Litwinetz, Dennis, "Semiconductor Technology in a High Performance VAX System." Digital Technical Journal — Oct. 1990.
- Adiletta, Matthew; Gutfreund, Keith; and Cooper, Elizabeth, "Automatic Test generation for Generic Scan Designs," Proceedings IEEE Test Symposium Nov. 1985.