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Patents

- 6,704,861, Mechanism for executing computer instructions in parallel, 3/9/2004
- 6,675,192, Temporary halting of thread execution until monitoring of armed events to memory location identified in working registers, 1/6/2004.
- 6,493,741, Method and apparatus to quiesce a portion of a simultaneous multithreaded central processing unit, 12/10/2002
- 6,470,443, Pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information, 10/22/2002
- 6,449,713, Implementation of a conditional move instruction in an out-of-order processor, 9/10/2002
- 6,154,828, Method and apparatus for employing a cycle bit parallel executing instructions, 11/28/2000
- 6,108,770, Method and apparatus for predicting memory dependence using store sets, 8/22/2000
- 6,081,887, System for passing an index value with each prediction in forward direction to enable truth predictor to associate truth value with particular branch instruction, 6/27/2000
- 6,073,159, Thread properties attribute vector based thread selection in multithreading processor, 6/6/2000
- 5,933,860, Multiprobe instruction cache with instruction-based probe hint generation and training whereby the cache bank or way to be accessed next is predicted, 8/3/1999
- 5,758,142, Trainable apparatus for predicting instruction outcomes in pipelined processors, 5/26/1998
- 5,428,807, Method and apparatus for propagating exception conditions of a computer system, 6/27/1995
- 5,421,022, Apparatus and method for speculatively executing instructions in a computer system, 5/30/1995
- 5,420,990, Mechanism for enforcing the correct order of instruction execution, 5/30/1995
- 5,285,323, Integrated circuit chip having primary and secondary random access memories for a hierarchical cache, 2/8/1994