Ian Alexander Young
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Patents

- 6,760,801, Ground referenced voltage source input/output scheme for multi-drop bus, 7/6/2004
- 6,754,407, Flip-chip package integrating optical and electrical devices and coupling to a waveguide on a board, 6/22/2004
- 6,670,833, Multiple VCO Phase Locked-Loop Architecture, 12/30/2003
- 6,650,161, Clock Distribution Network having Regulated Power Supply, 11/18/2003
- 6,636,976, Mechanism to Control di/dt for a Microprocessor, 10/21/2003
- 6,556,471, VDD modulated SRAM for highly scaled, high performance cache, 4/29/2003
- 6,538,497, On-chip power supply boost for voltage droop reduction, 3/25/2003
- 6,512,861, Packaging and assembly method for optical coupling, 1/28/2003
- 6,407,600, Method and apparatus for providing a start-up control voltage, 6/18/2002
- 6,303,464, Method and structure for reducing interconnect system capacitance through enclosed voids in a dielectric layer, 10/16/2001
- 6,229,861, Clock distribution network utilizing local deskewing clock generator circuitry, 5/8/2001
- 6,172,937, Multiple synthesizer based timing signal generation scheme, 1/9/2001
- 6,125,217, Clock distribution network, 9/26/2000
- 6,081,141, Hierarchical clock frequency domains for a semiconductor device, 6/27/2000
- 6,075,908, Method and Apparatus for optically Modulating Light through the back-side of an Integrated Circuit Die, 6/13/2000
- 6,064,223, Low leakage circuit configuration for MOSFET circuits, 5/16/2000
- 6,081,141, Hierarchical Clock Frequency Domains for a Semiconductor Device, 6/27/2000
- 5,446,867, Microprocessor PLL clock circuit with selectable delayed feedback, 8/29/1995
- 5,412,349, PLL clock generator integrated with microprocessor, 5/2/1995
- 5,300,829, BiCMOS Circuit with Negative Vbe Protection, 4/15/1994
- 5,280,605, Clock speed limiter for microprocessor, 1/18/1994
- 5,274,337, Clock Speed Limiter for a Microprocessor by Comparing Clock Signal with a Predetermined Frequency, 12/28/1993

- 5,247,479, Current sensing amplifier for SRAM, 9/21/1993
- 5,235,549, Semiconductor device with apparatus for performing electrical tests on single memory cells, 8/10/1993
- 5,113,096, BiCMOS circuit, 5/12/1992
- 5,111,077, BiCMOS Non-inverting Buffer and Logic Gates, 5/5/1992
- 5,049,765, BiCMOS Non-inverting Buffer and Logic Gates, 9/17/1991
- 4,888,503, Constant current biased common gate differential sense amplifier, 12/19/1989
- 4,796,230, Folded-cascode configured differential current steering column decoder circuit, 1/13/1989
- 4,710,647, Substrate bias generator including multivibrator having frequency independent of supply voltage, 12/1/1987
- 4,658,160, Common gate MOS differential sense amplifier, 4/14/1987
- 4,379,267, Low power differential amplifier, 4/5/1983
- 4,338,571, Low sensitivity switched-capacitor ladder filter using monolithic MOS chip, 7/6/1982
- 4,316,106, Dynamic Ratioless Circuitry for Random Logic Applications, 2/16/1982

Publications/Speakerships

- Member of a Panel at the Symposium on VLSI Circuits — "BiCMOS versus CMOS" — June 1991.
- Moderator for Panel at the Symposium on VLSI Circuits on "High Performance Microprocessor Challenges" — June 1994.
- Moderator International Solid-State Circuits Conference (ISSCC) Panel on "Microprocessors in the Year 2000" — Feb. 1992.
- Member of a Panel on "Process Technology driver, Logic or Memory" — Feb. 1994
- Presenter at the Solid-State Circuits Technology Workshop on "Merged DRAM and Logic Technology" — Feb. 1995.
- Moderator for Panel at the ISSCC 2002 on Optical Interconnect for VLSI
- Short Course; "Design of Clock Distribution in Microprocessors," International Interconnect Technology Conference, June 2003
- MIT Distinguished Lecturer Series; "Clocking in High performance Microprocessors" — May 2002
- Presenter at the MARCO Interconnect Focus Center Optical Workshop, Stanford University, Dec 2003
- "A Comparison of State-of-the-Art NMOS and SiGe HBT Devices for Analog/Mixed-signal/RF Circuit Applications," K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoorn, I. Young, Symp. VLSI Circuits, pp. 224-225, June 2004.
- Optical I/O technology for digital VLSI, E. M. Mohammed, T. P. Thomas, D. Lu, H. Braunisch, S. Towle, B. Barnett, I. Young, G. Vandentop, Proceedings of the SPIE, vol #5358, January 2004.
- A CMOS 10Gb/s SONET Transceiver, Muthali, H; Thomas,T; Young, I European Solid State Circuits Conference, Estoril, Portugal, September 2003
- On Chip Optical Clock Distribution, Zheng, J; Robertson, F; Mohammed, E; Young, I; Ahn, D; Wada, J; Michel, J; Kimerling, L Optics in Computing Conference, June 2003
- 130nm CMOS Replica-Biased PLL with 1xVCO, Kurd, N, Griffin, J, Barkatullah, J, Young, I; International Solid-State Circuits Conference, Feb 2003, Digest of Technical Papers
- 50 Years of Digital Logic and Microprocessors at ISSCC, Young, I. A Solid-State Circuits Conference, Feb. 2003. Digest of Technical Papers, 50th Anniversary Supplement
- A 90 nm communication technology featuring SiGe HBT transistors, RF CMOS, precision R-L-C RF elements and 1 /spl mu/m/sup 2/ 6-T SRAM cell, Kuhn, K.; Agostinelli, M.; Ahmed, S.; Chambers, S.; Cea, S.; Christensen, S.; Fischer, P.; Gong, J.; Kardas, C.; Letson, T.; Henning, L.; Murthy, A.; Muthali, H.; Obradovic, B.; Packan, P.; Pae, S.W.; Post, I.; Putna, S.; Raol, K.; Roskowski, A.; Soman, R, Young, I Electron Devices Meeting, 2002. IEDM '02. Digest. International, 8-11 Dec. 2002, Page(s):73-76

- Four-way processor 800 MT/s front side bus with ground referenced voltage source I/O, Thomas, T.P.; Young, I.A.; VLSI Circuits Digest of Technical Papers, 2002. Symposium on, 13-15 June 2002, Page(s):70-71
- A comprehensive metric for evaluating interconnect performance Young, I.; Raol, K.; Interconnect Technology Conference, 2001. Proceedings of the IEEE 2001 International, 4-6 June 2001, Page(s): 119 -121
- Clock generation and distribution for the first IA-64 microprocessor Tam, S.; Rusu, S.; Nagarji Desai, U.; Kim, R.; Ji Zhang; Young, I.; Solid-State Circuits, IEEE Journal of, Volume: 35 Issue: 11, Nov. 2000, Page(s): 1545 -1552
- Dual Threshold Voltages And Substrate Bias: Keys To High Performance, Low Power, 0.1um Logic Designs Thompson, S.; Young, I.; Greason, J.; Bohr, M.; VLSI Technology, 1997. Digest of Technical Papers., 1997 Symposium on, June 10-12, 1997, Page(s): 69 -70
- Digital Circuit Interconnect: Issues, Models, Analysis And Design Young, I.; Pillage, L.; Cohn, J.;
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- Young, "A Phase Regenerative Parametric Amplifier for PSK Microwave Signals." Eng. Sc. Dissertation, University of Melbourne, Australia, 1975.

Professional Affiliations

- Fellow of IEEE for contributions to the development of Phase Locked Loops for Microprocessors
- Chairman, Technical Program Committee, 2005, International Solid-State Circuits Conference.
- Vice-Chairman, Technical Program Committee, 2004 International Solid-State Circuits Conference.
- Digital Sub-Committee Chairman, Technical Program Committee, International Solid-State Circuits Conference, 1997-2003.
- Member of the International Solid-State Circuits Conference Technical Program Committee, 1992-Present.
- Member of the Executive Committee for the Symposia on VLSI Technology and Circuits, 1999-Present
- Symposium Chairman/Co-Chairman, Symposium on VLSI Circuits, 1997-8
- Technical Program Chairman/Co-Chairman, Symposium on VLSI Circuits, 1995-6.
- Member of the Symposium on VLSI Circuits Technical Program Committee, 1991-1996.
- Guest Editor, April 1997, IEEE Journal of Solid-State Circuits.
- Guest Editor, April 1996, IEEE Journal of Solid-State Circuits.
- Guest Editor, December 1994, IEEE Journal of Solid-State Circuits.