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Patents

- 5,694,362 Method & Apparatus for High-Speed Comparison
- 5,815,432 Single-ended Read, Dual-ended Write SRAM Cell
- 5,949,256 Asymmetric Sense Amplifier for Single-ended Memory Arryas
- 5,986,923 Method & Apparaturs for Improving Read/Write Stability of a Single-port SRAM Cell
- 6,026,011 CMOS Latch Design with Soft Error Immunity
- 6,038,693 Error Correction Scheme for an Integrated L2 Cache
- 6,087,849 Soft Error Immunity in CMOS Circuits with Large Shared Diffusion Areas
- 6,181,608 Dual Vt SRAM Cell with Bitline Leakage Control
- 6,198,656 Asymmetric Memory Cell for Single-ended Sensing
- 6,198,684 Wordline Decoder for Dual-port Cache Memory
- 6,204,698 Robust Low Voltage Swing Sense Amplifier (missed eariler)
- 6,255,861 Hybrid Low Voltage Swing Sense Amplifier
- 6,282,143 Multi-port Static Random Access Memory Design for Column Interleaved Arrays
- 6,292,401 Method and Apparatus for Global Bitline Multiplexing for a High-speed Memory
- 6,330,182 Method for Evaluating Soft Error Immunity of CMOS Circuits
- 6,407,589 Device for Current Sensing in An Amplifer with PMOS Voltage Conversion
- 6,442,089 Multi-level, Low Voltage Swing Sesning Scheme for High Speed Memory Design
- 6,456,121 Sense Amplifer for Integrated Circuits Using PMOS Transistors
- 6,483,375 Low Power Operation Mechanism and Method
- 6,507,531 Cache Column Multiplexing Using Redundant Form Addresses
- 6,518,826 Method & Apparatus for Dynamic Leakage Control
- 6,621,726 Biasing Technique for a High Density SRAM
- 6,622,267 Method & Apparatus for Detecting Multi-Hit Errors in Cache
- 6,650,171 Low Power Operation Mechanism and Method
- 6,662,333 Shared Error Correction for Memory Design
- 6,707,752 TAG Design for Cache Access with Redundant-Form Address
- 6,778,444 Buffer for Split Cache Line Access
- 6,775,181 Biasing Technique for a High Density SRAM
- 6,816,554 Communication Bus for Low Voltage Swing Data Signal
- 6,862,207 Static RAM Access Memory (new issued)

- 6,862,225 Buffer for Split Cache Line Access (new issued)
- 6,948,079 Method and Apparatus for Providing Supply Voltages for a Processor

Publications

- K. Zhang, et al., "A 70Mb SRAM with Dynamic Power Supply for Stability and Power Reduction," IEEE J. Solid-State Circuits, Jan, 2006.
- K. Zhang, "Challenges and Opportunities in Nano-Scale VLSI Design," VLSI-TSA International Symposium, pp 6-7, April 2005.
- K. Zhang, et al., "A 70Mb SRAM with Column Based Dynamic Power Supply in 65nm CMOS Technology," ISSCC Technical Digest, pp. Feb. 2005.
- K. Zhang, et al., "SRAM Design with Dynamic Leakage Reduction on 65nm CMOS Technology," IEEE J. Solid State Circuits, Vol. 40, No. 4, pp. 895-901, Apr 2005.
- K. Zhang, et al., "A SRAM Design on 65nm CMOS Technology with Integrated Leakage Reduction Scheme," VLSI Circuit Symposium, Digest of Tech. Papers, pp. 294-295, June 2004.
- K. Zhang, et al., "A Fully Synchronized, Pipelined, and Re-configurable 50Mb SRAM on 90nm CMOS Technology for Logic Applications," VLSI Circuit Symposium, Digest of Tech Papers, pp. 253-254, June 2003.
- K. Zhang, et al., "The Scaling of Data Sensing Schemes for High Speed Cache Design in sub-0.18um Technologies," VLSI Circuit Symposium, Digest of Tech Papers, pp. 226-227, June 2000.
- K. Zhang, "The Challenges and Opportunities in GHz Microprocessor Design on 0.13um and Beyond Technologies," Proceedings. 6th International Conference on Solid-State and Integrated Circuit Technology, Vol. 2, pp. 1102-1106, Oct. 2001.
- K. Zhang, et al., "Methods for Reducing Soft Errors in Deep Submicron Integrated Circuits," Proceedings of 5th International Conference on Solid-State and Integrated Circuit Technology, pp. 516-519, Oct 1998.
- K. Zhang, et al., "The Impact of In-Situ Rapid Thermal Dielectric Processes on Deep Submicron MOSFETs," Solid-State Electronics, Vol. 41, p691, 1997.
- K. Zhang, et al., "A 0.25um MOSFET Technology Using In-situ Rapid Thermal Gate Dielectrics," Journal of Electrochemical Society, 143(2), 744, 1996.
- K. Zhang, et al., "Reliability of In-situ Rapid Thermal Gate Dielectrics in Deep Submicron MOSFET's", IEEE Tran Electron Device, Vol. 42, No. 12, p2191, 1995.