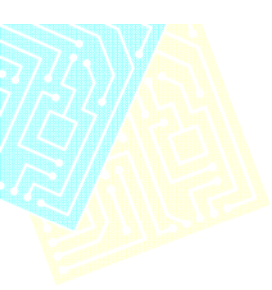


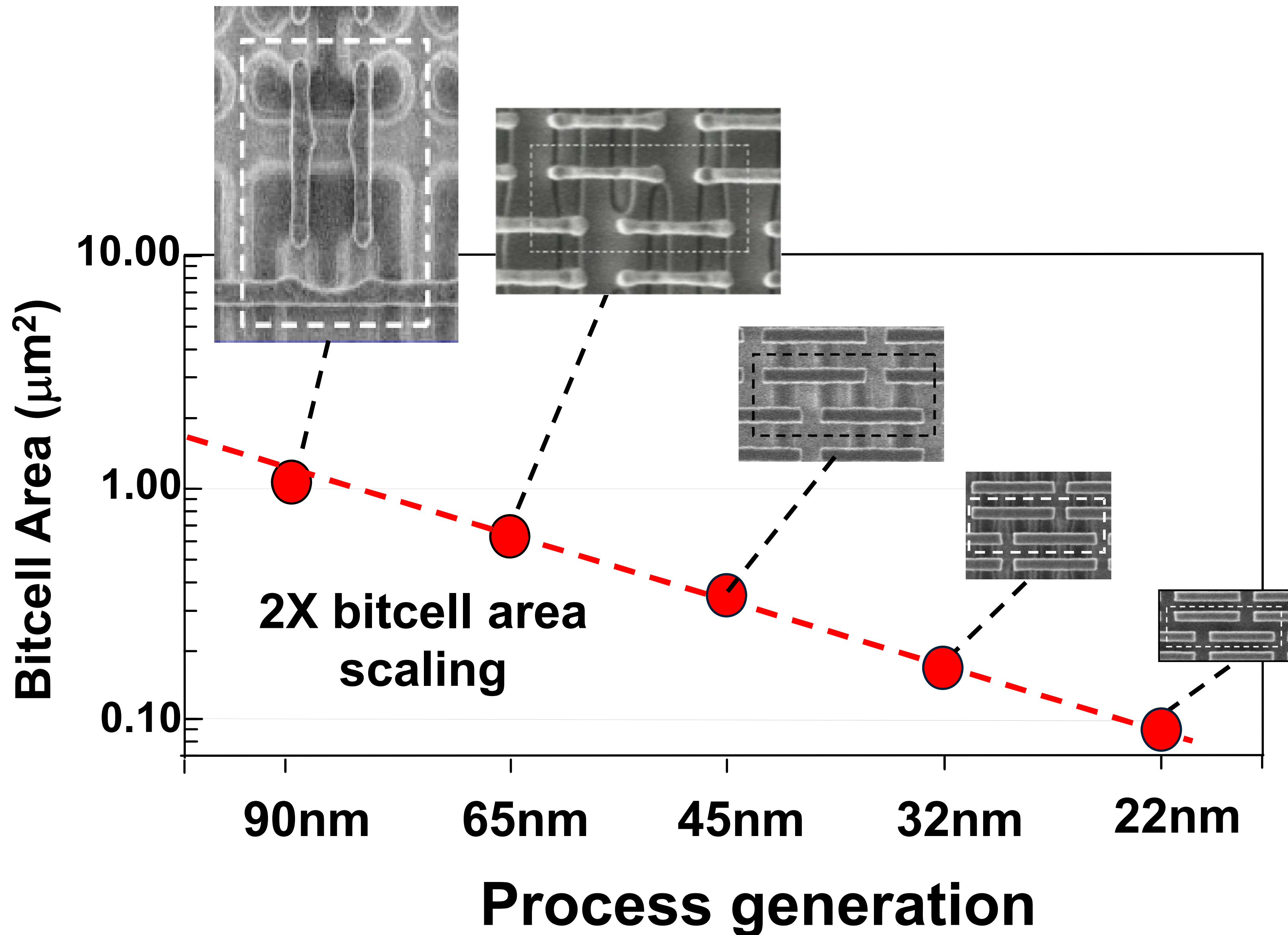
CMOS scaling for the 22nm node and beyond: Device Physics and Technology

Kelin J. Kuhn

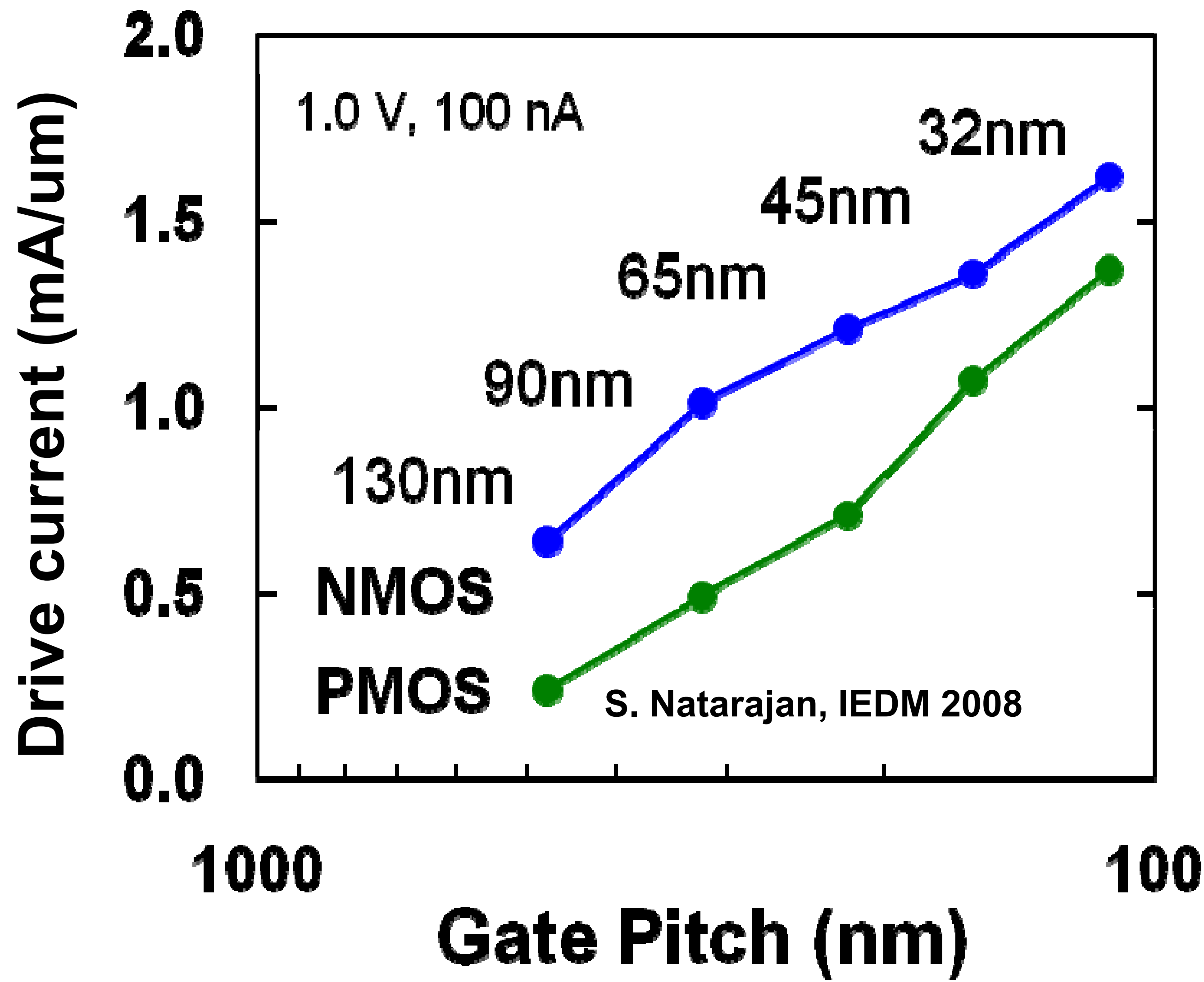
Intel Fellow

Director of Advanced Device Technology

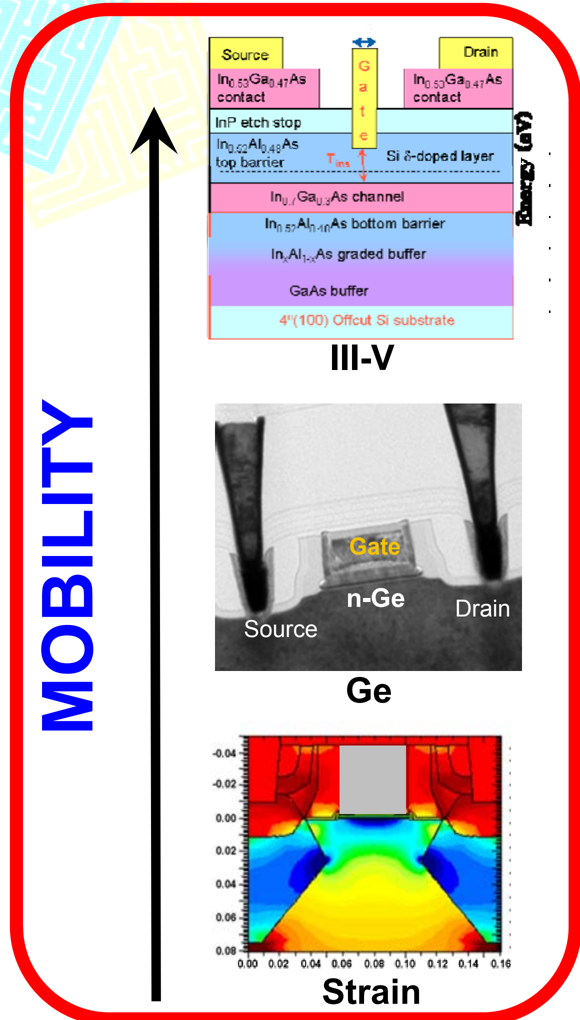
Moore's Law Scaling of the SRAM

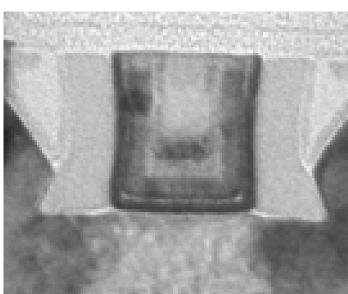


Impact of Process Enhancers

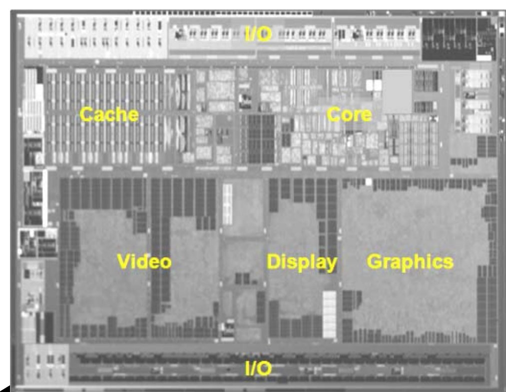


S. Natarajan, IEDM 2008

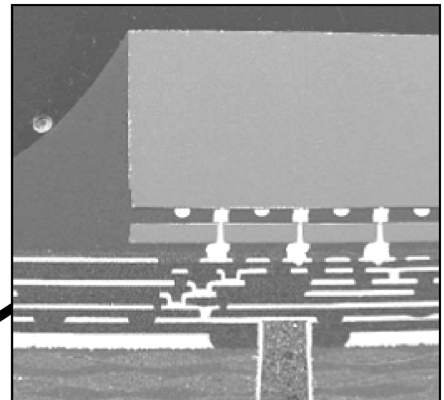




32nm

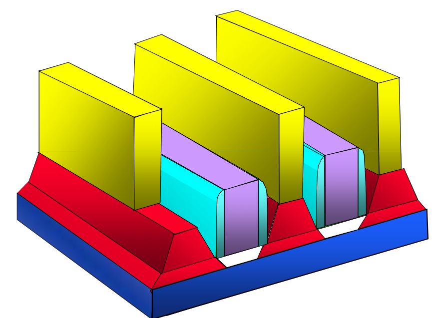


System-on-chip

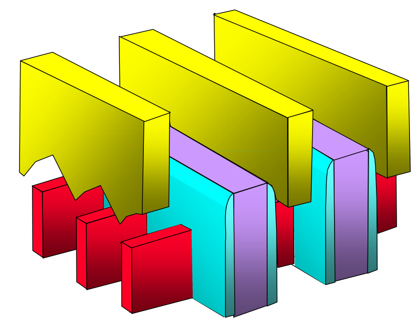


System-in-package

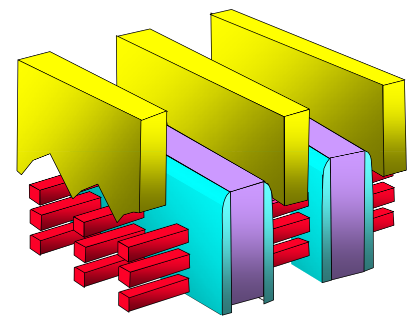
STRUCTURE



UTB SOI



Fins

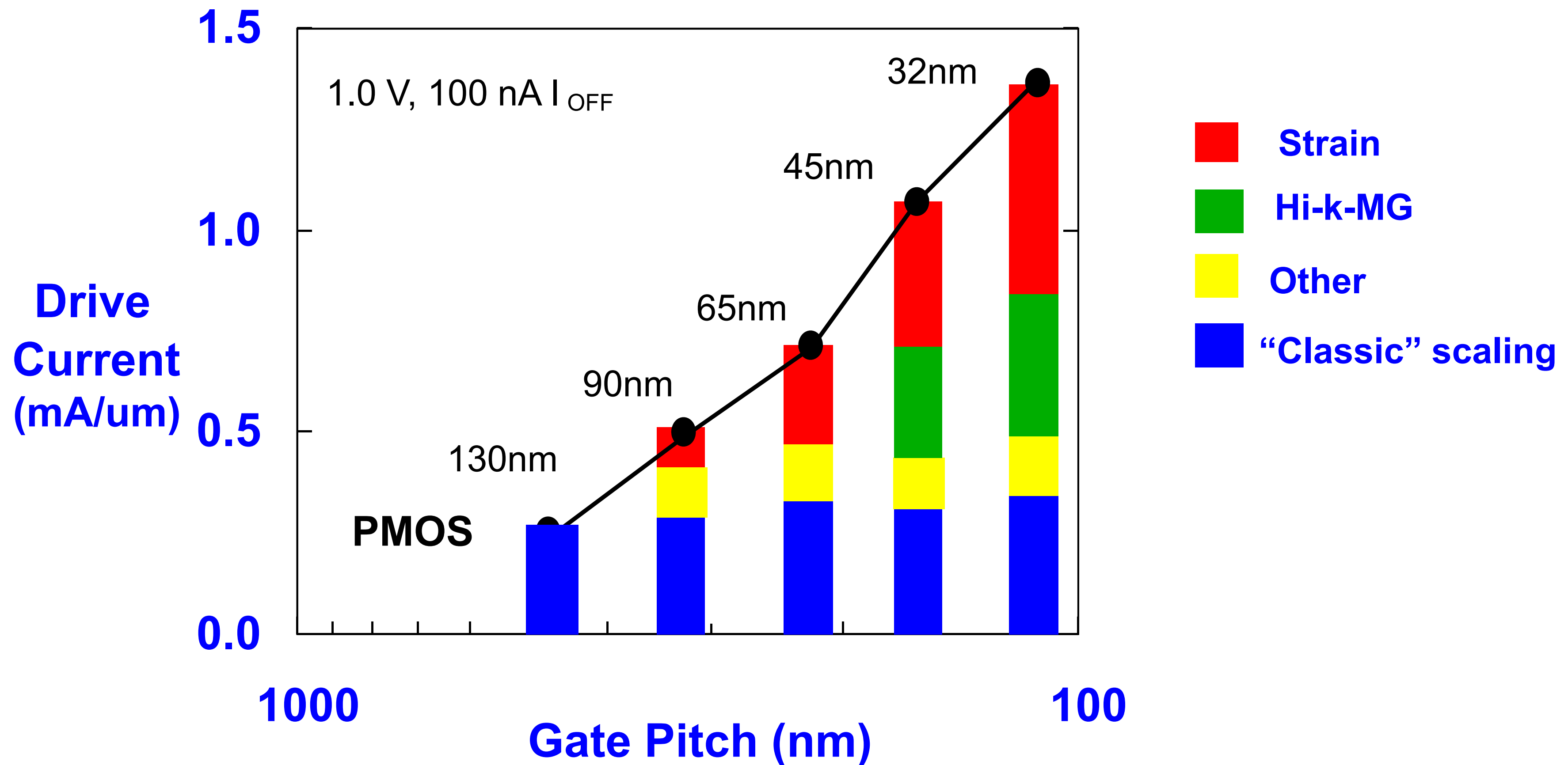


Wires/Ribbons

ELECTROSTATIC CONFINEMENT

VLSI SINCE 1983

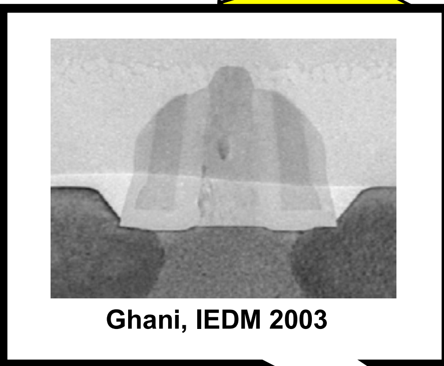
Transistor Performance Trend

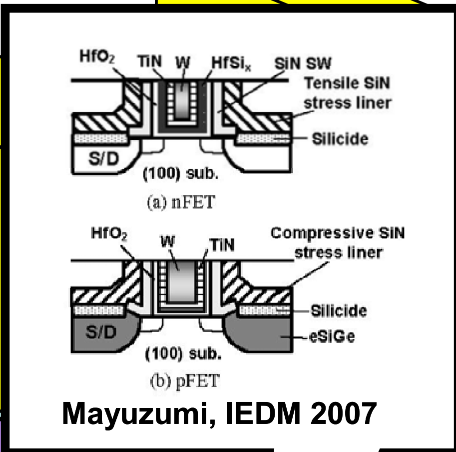


Strain is a critical ingredient in modern transistor scaling

Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation

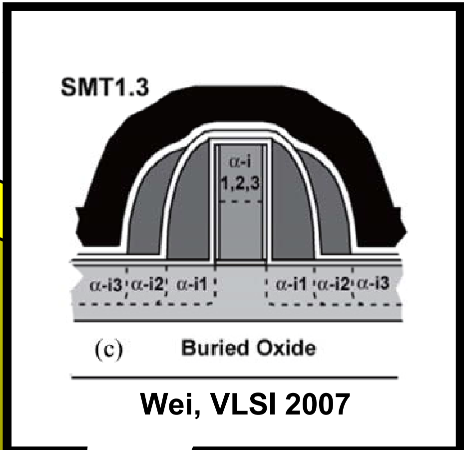
Strain in modern devices


Ghani, IEDM 2003

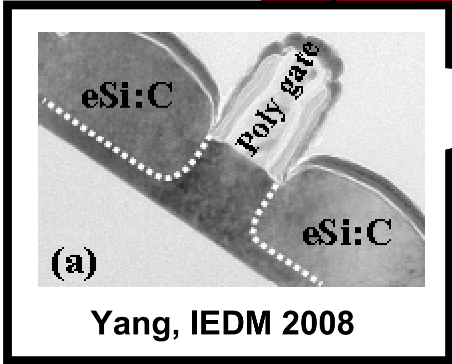


Mayuzumi, IEDM 2007

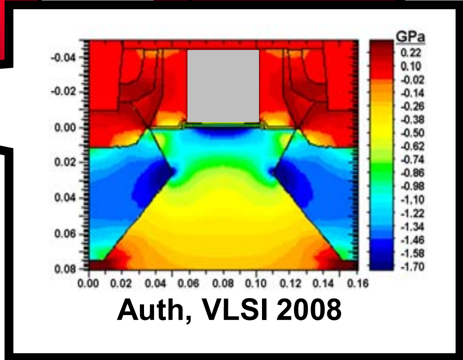
Stress memorization



Wei, VLSI 2007



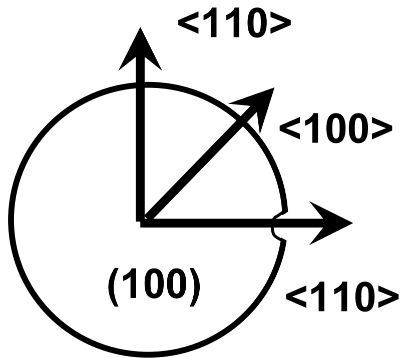
Yang, IEDM 2008



Auth, VLSI 2008

ORIENTATION

(100) surface – top down

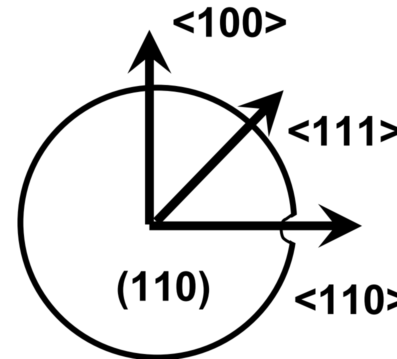


Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a "45 degree" wafer)

Both <110> directions are the same.

(110) surface – top down

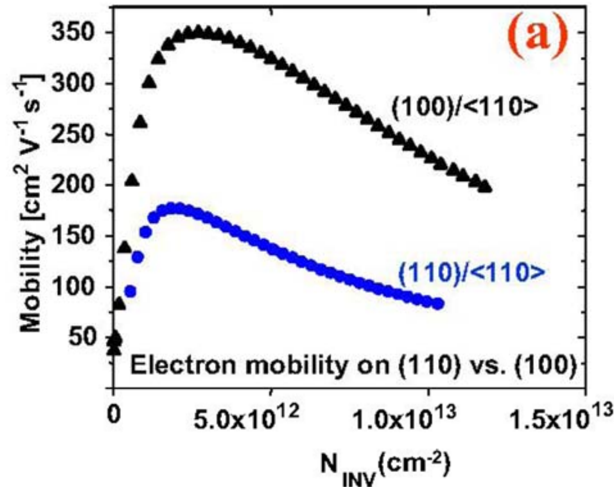


Non-standard

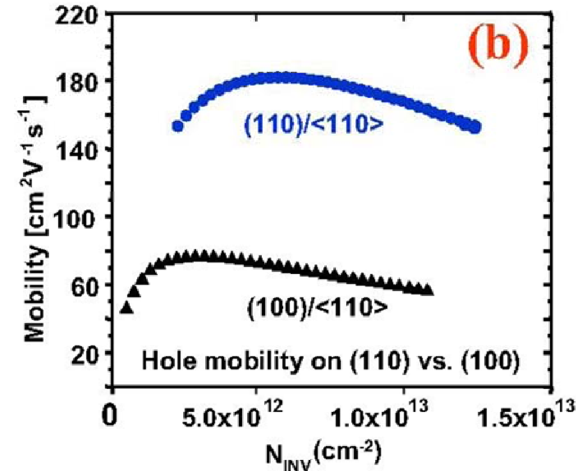
(110) Surface

Three possible channel directions
<110> <111> and <100>

(100) BEST NMOS

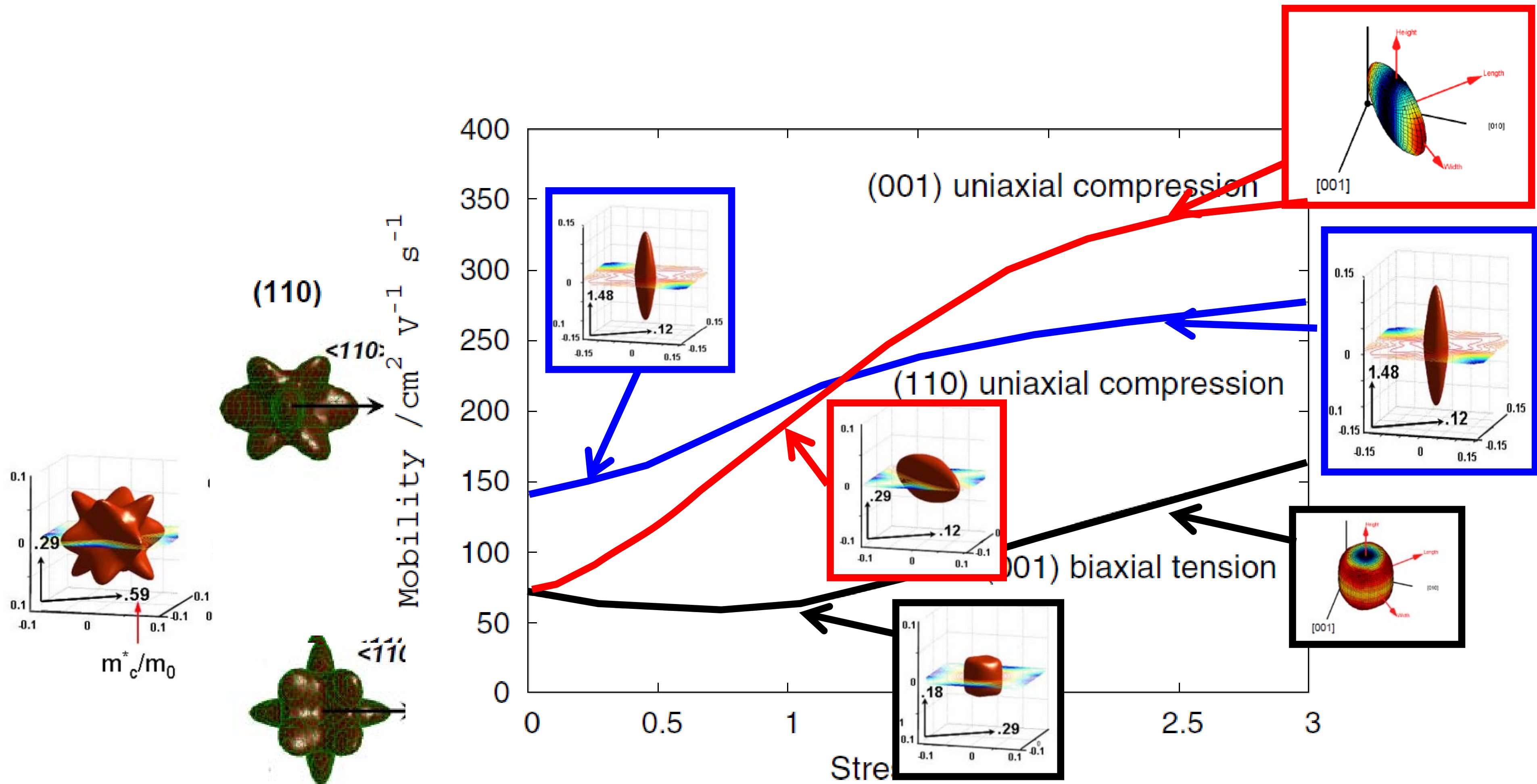


(110) <110> BEST PMOS



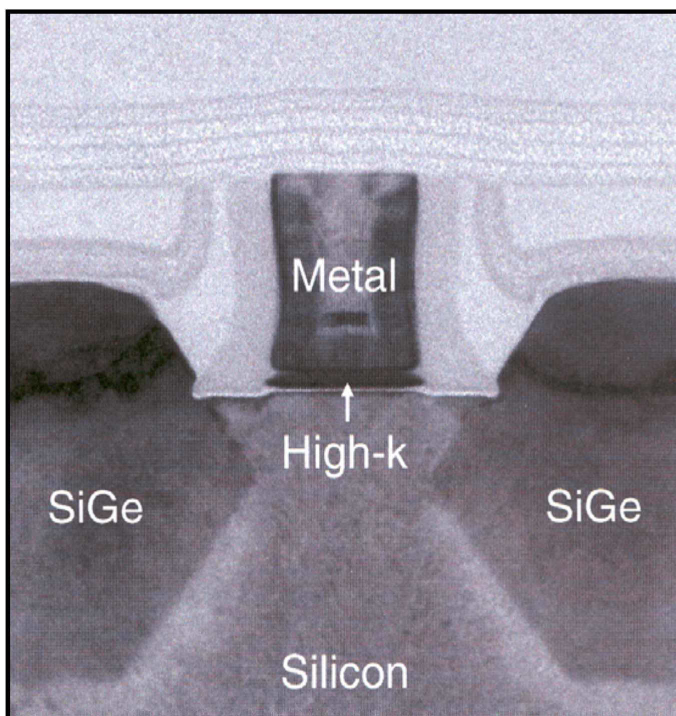
Yang
EDST
2007

Orientation and Strain: More complex for non-(100) orientations

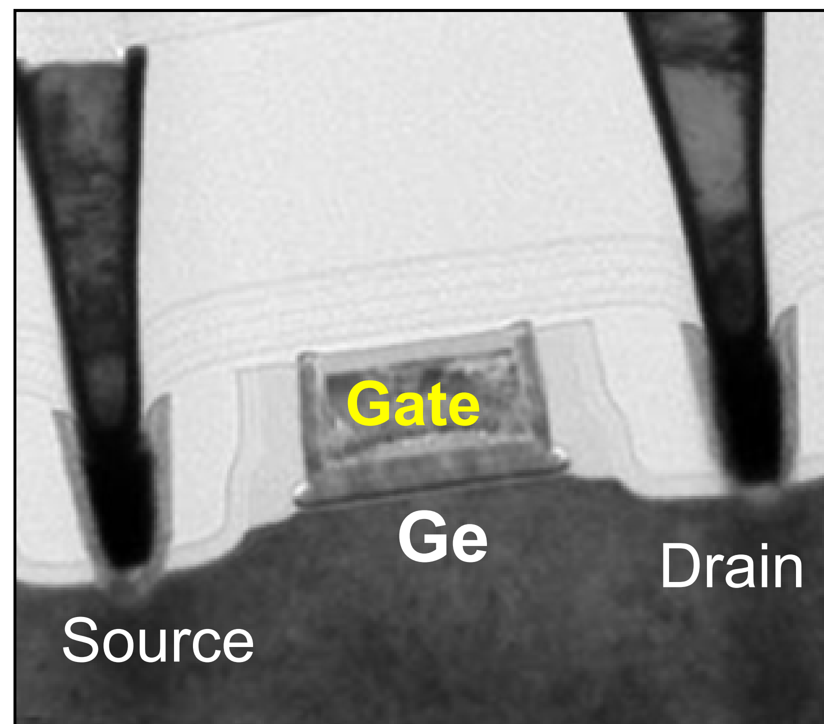


Modified from Thompson – IEDM 2006

Si vs Ge MOSFETs



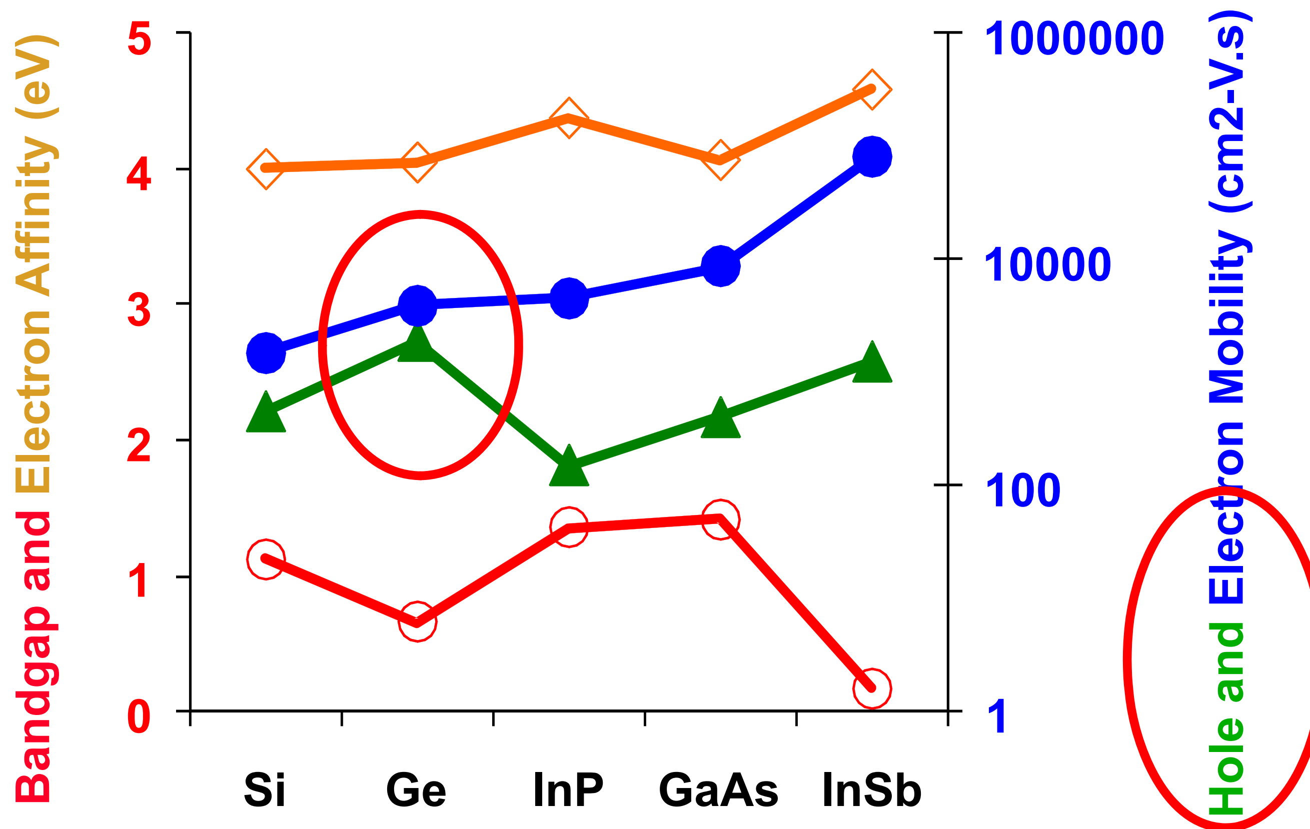
Intel 45nm HiK-MG Si device



Intel HiK-MG Ge device

The introduction of manufacturable HiK-MG transistors has led to the reconsideration of Ge channels

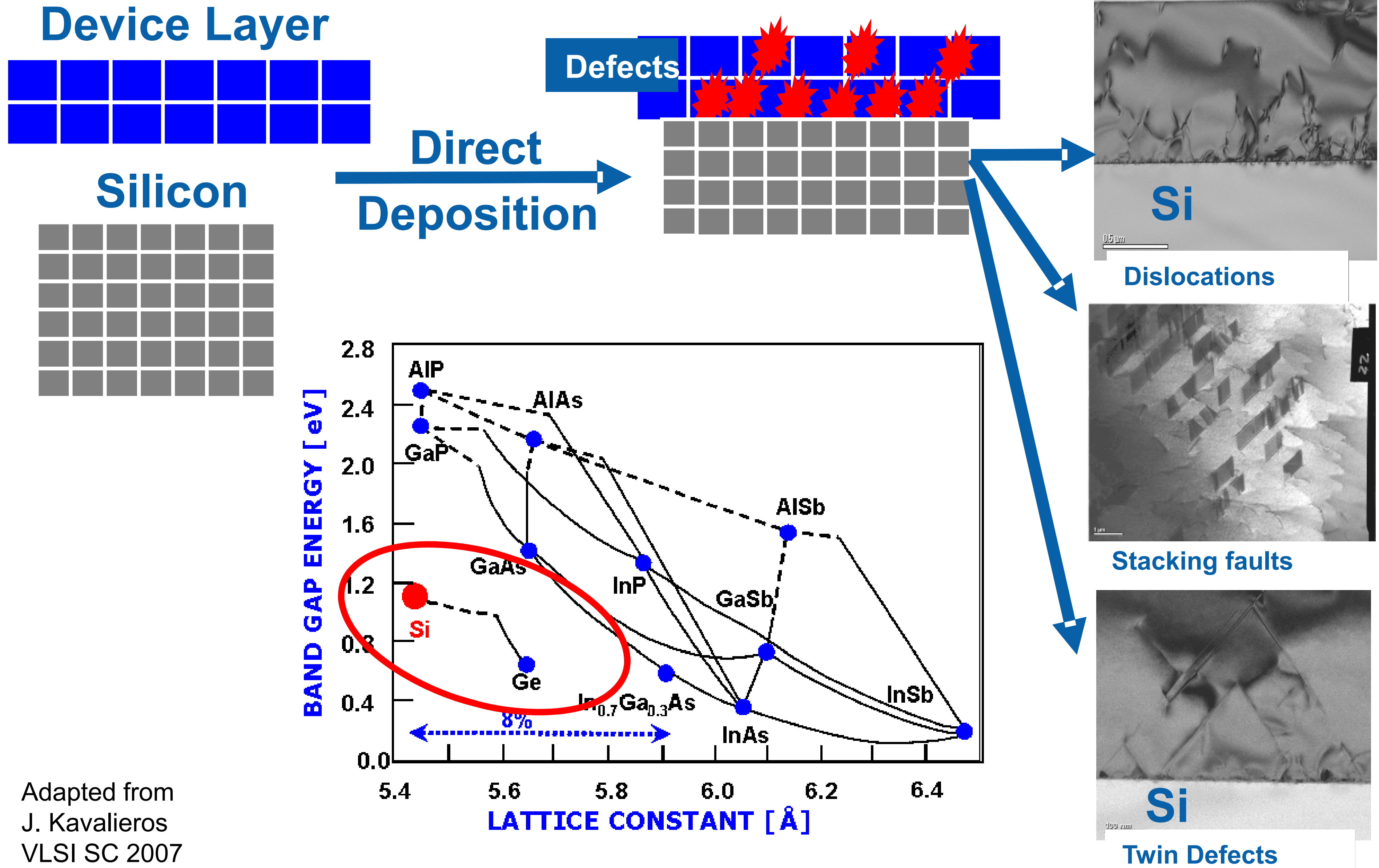
Ge and PMOS



Ge mobility makes it uniquely interesting for PMOS

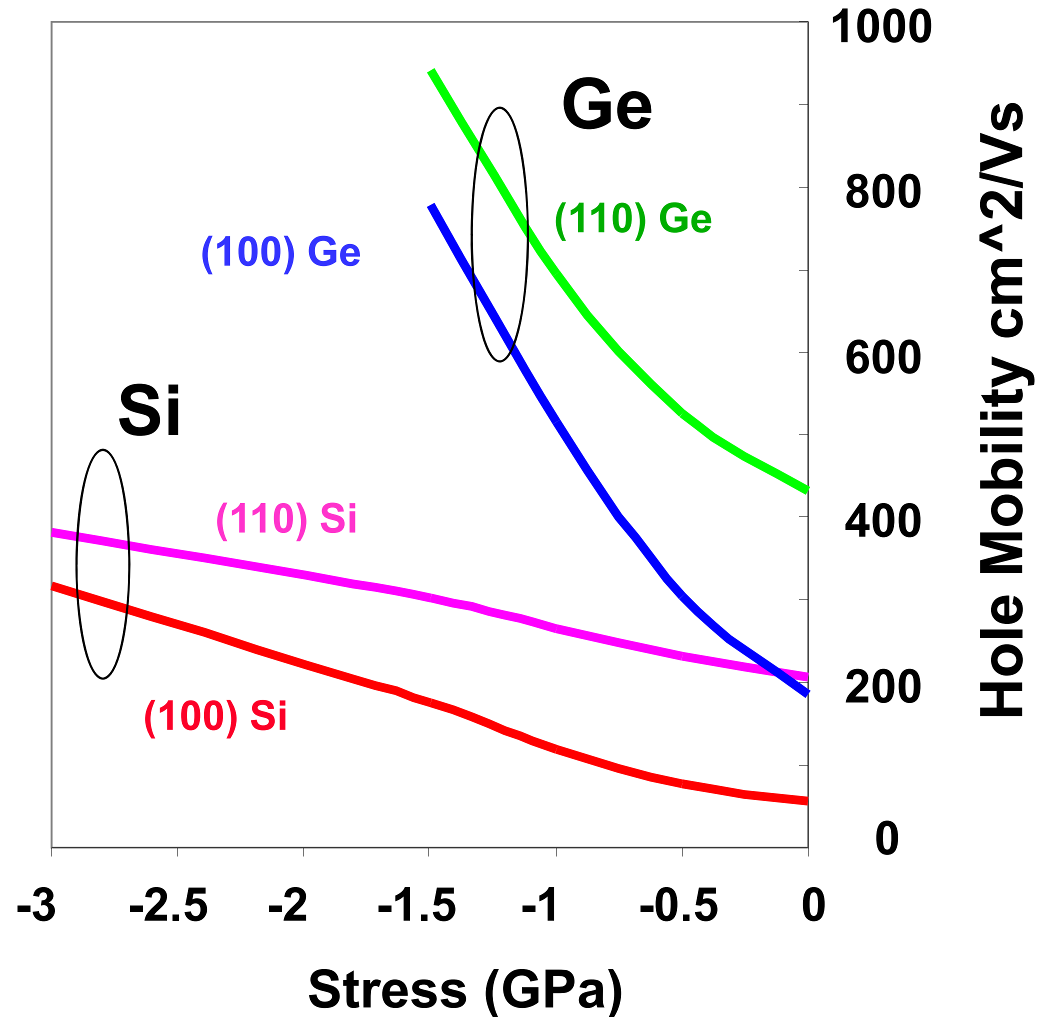
K. Kuhn ECS 2010

Challenge of Lattice Mismatch



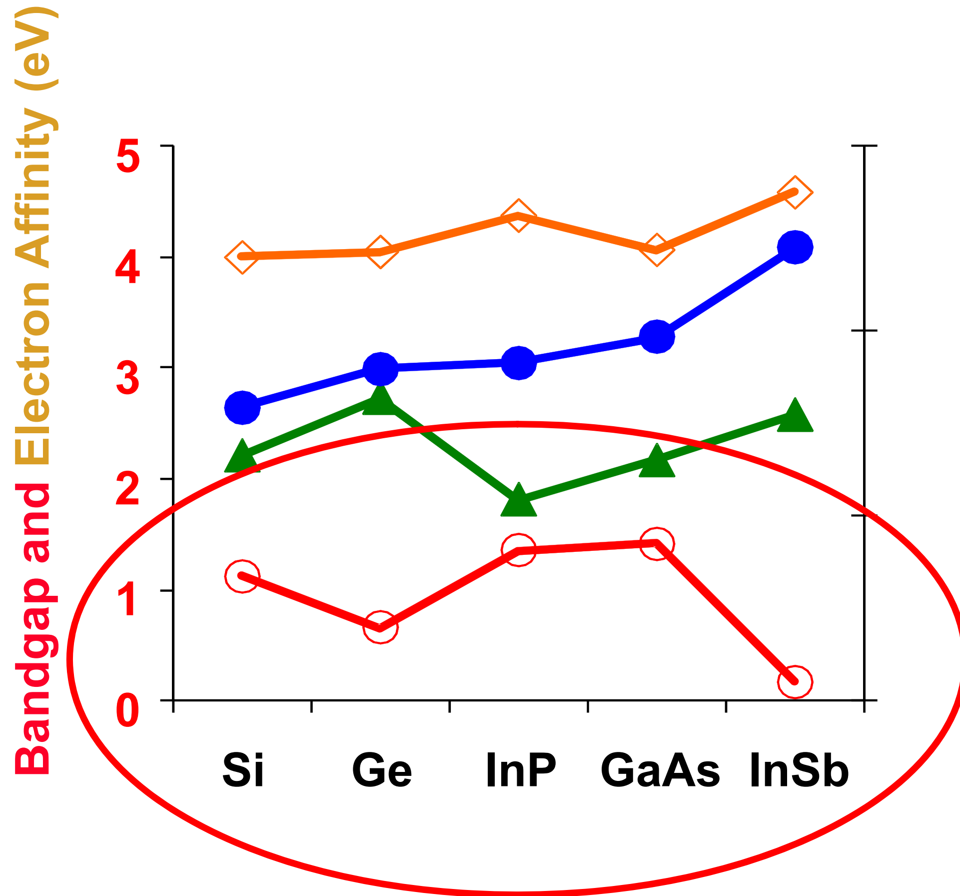
Adapted from
J. Kavalieros
VLSI SC 2007

Low Field Long Channel Mobility
(as a function of stress)

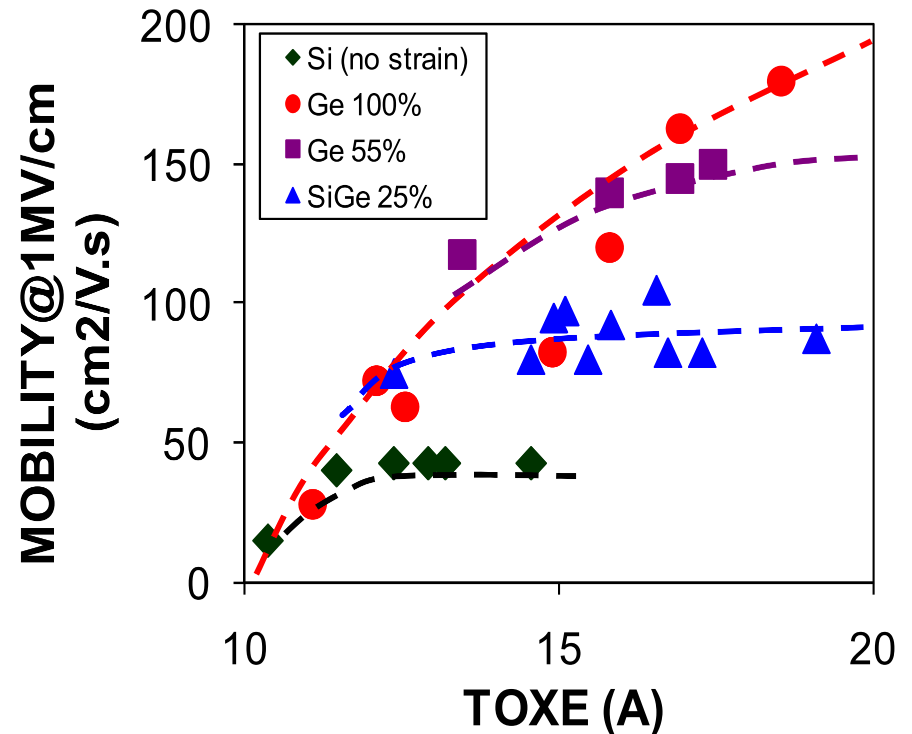


K. Kuhn ECS 2010

Ge Historical Issues:
Still critical today



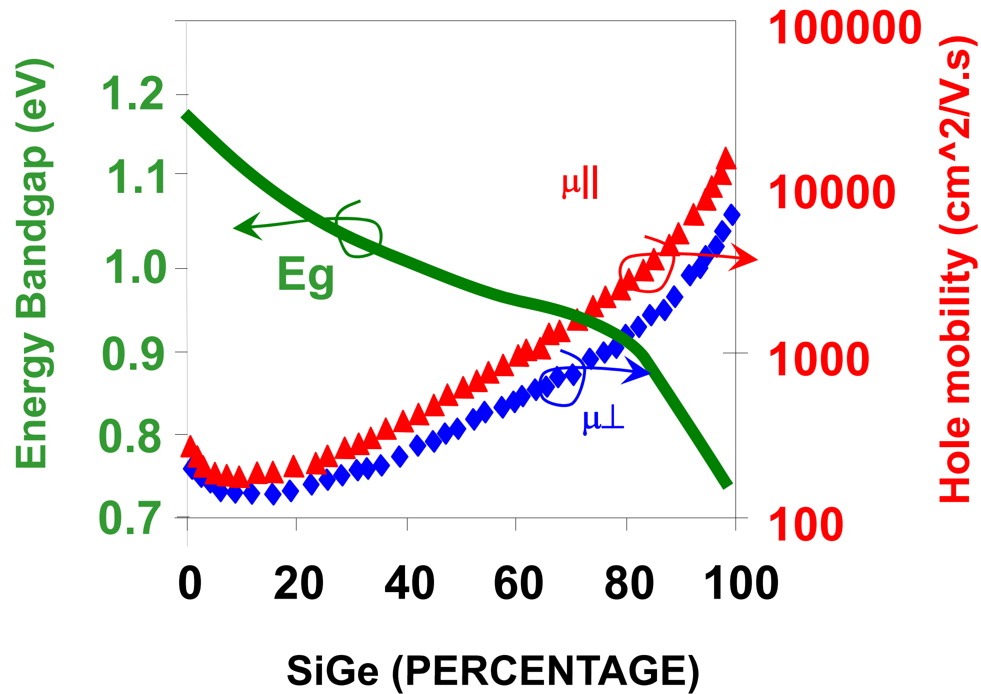
Narrow Bandgap



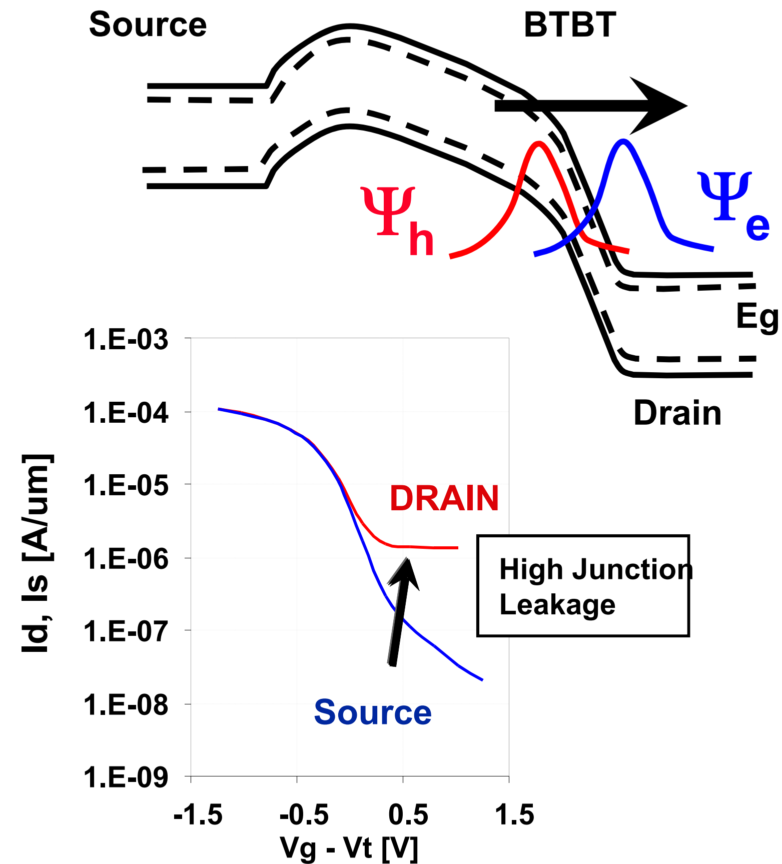
Poor Quality Dielectric

K. Kuhn ECS 2010

Narrow Bandgap



Adapted from Saraswat [59], Krishnamohan [60]

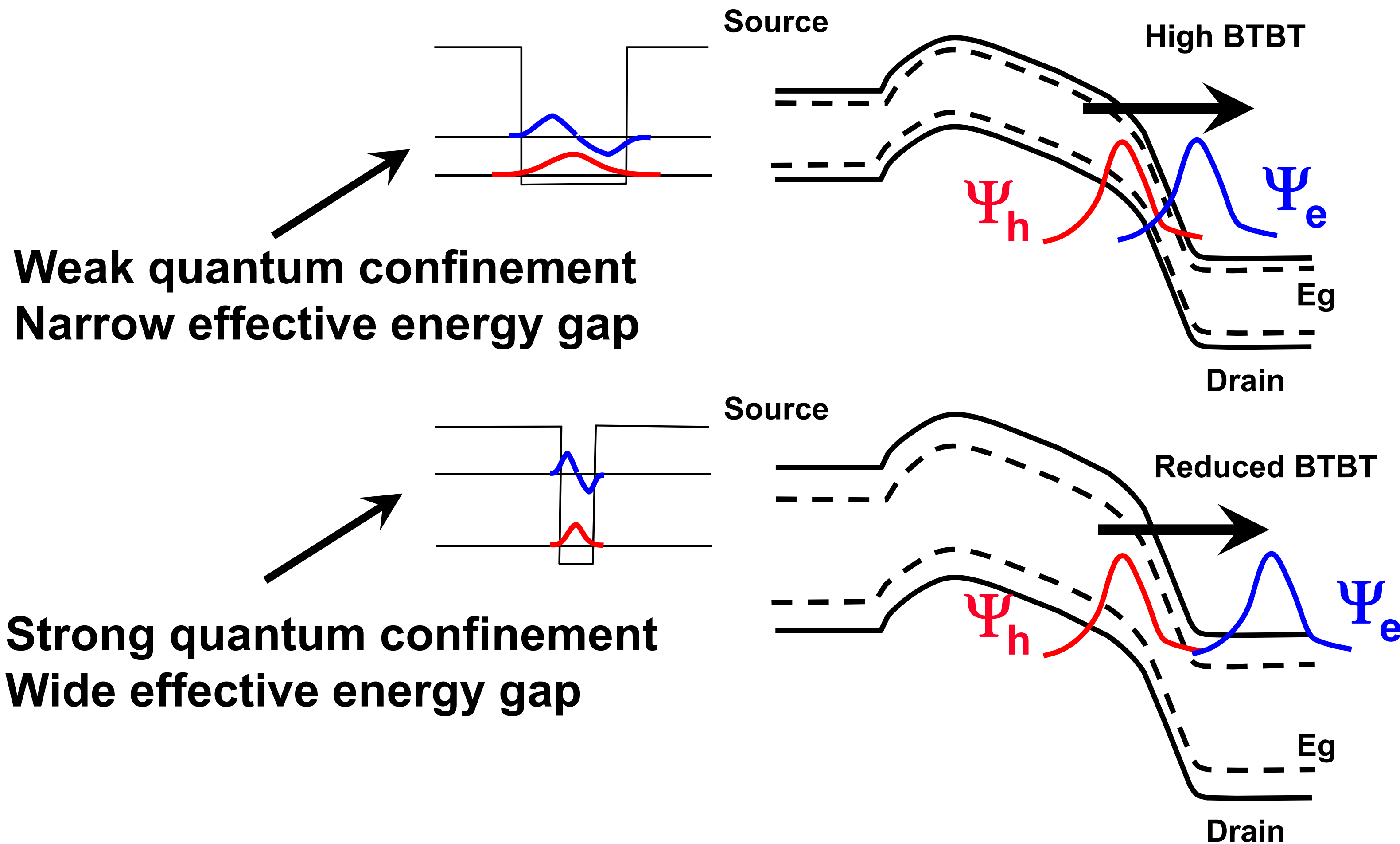


Band-to-band tunneling: challenge for low Eg materials

K. Kuhn ECS 2010

Narrow Bandgap

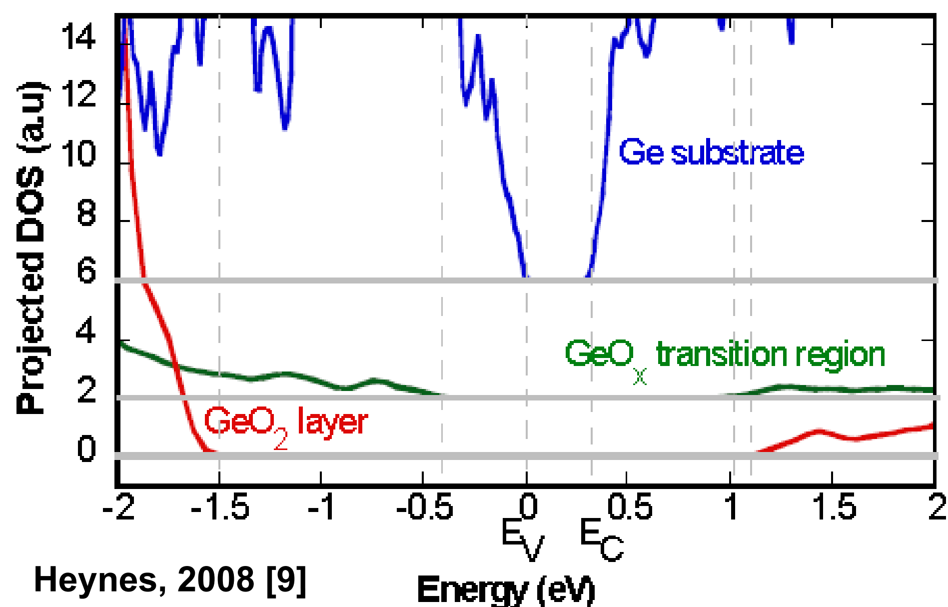
Adapted from Saraswat [59], Krishnamohan [60]

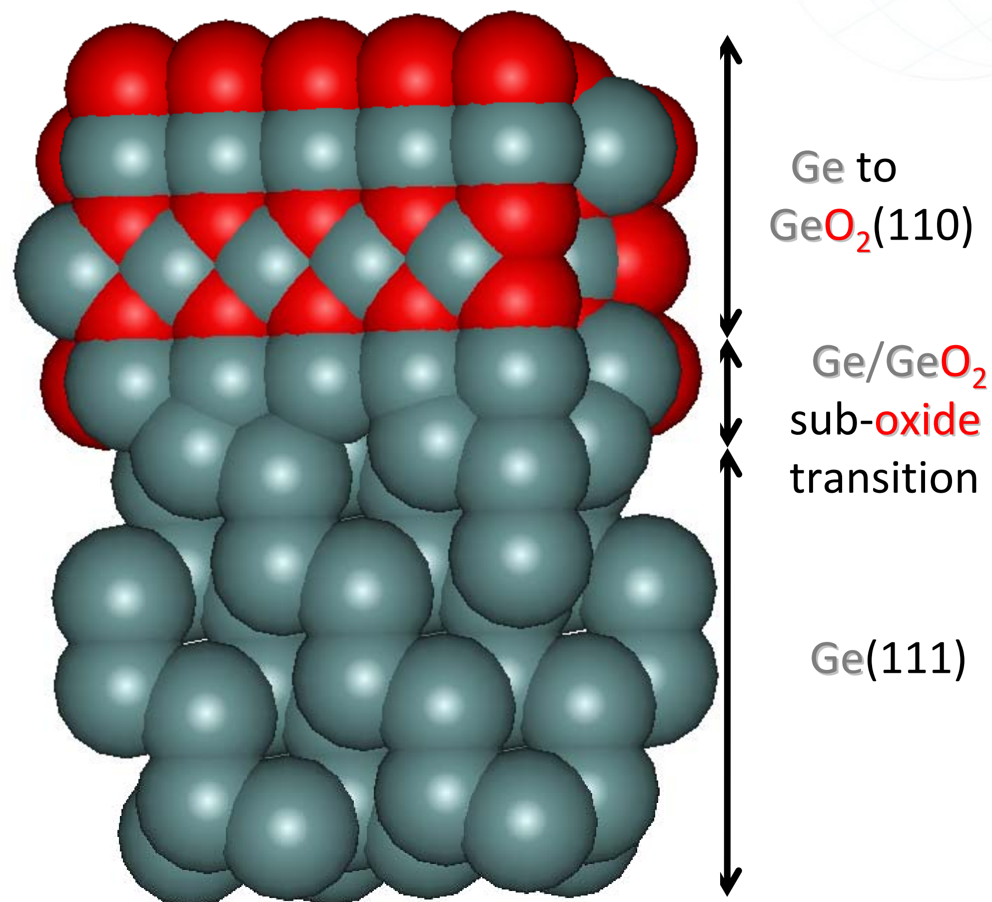


Two solutions: Use lower voltages and/or use quantum confined systems

K. Kuhn ECS 2010

Dielectric Quality



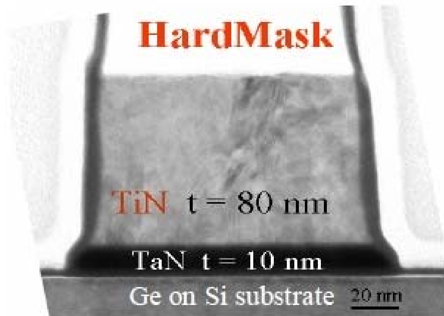


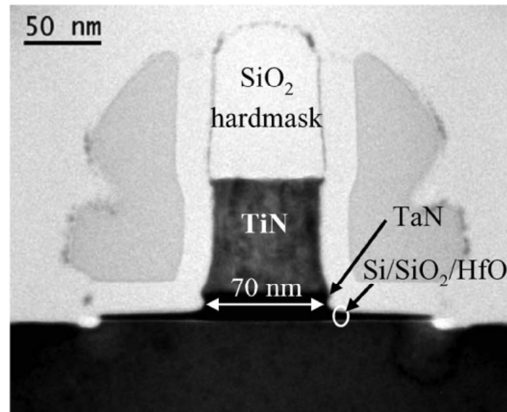
Since HiK-MG dielectrics typically form with a bilayer (the HiK + an interface layer) the challenge of germanium oxide still exists.

Germanium oxide exists in several morphologies, unfortunately, most are hydroscopic and/or volatile.

K. Kuhn ECS 2010

Ge Dielectric:
One strategy: Use an Si passivation layer





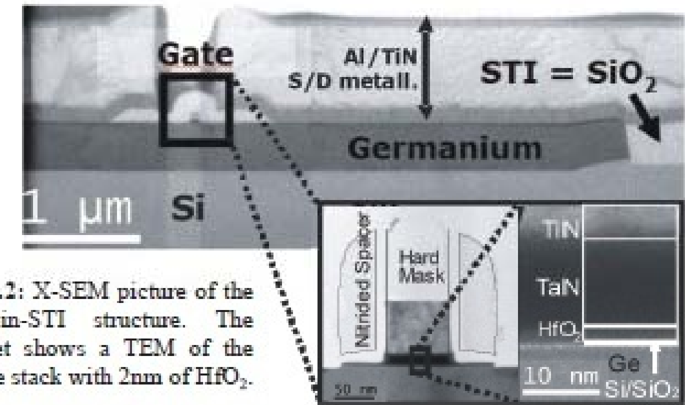
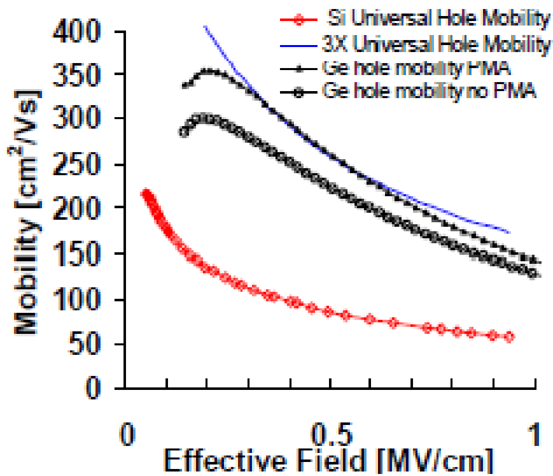
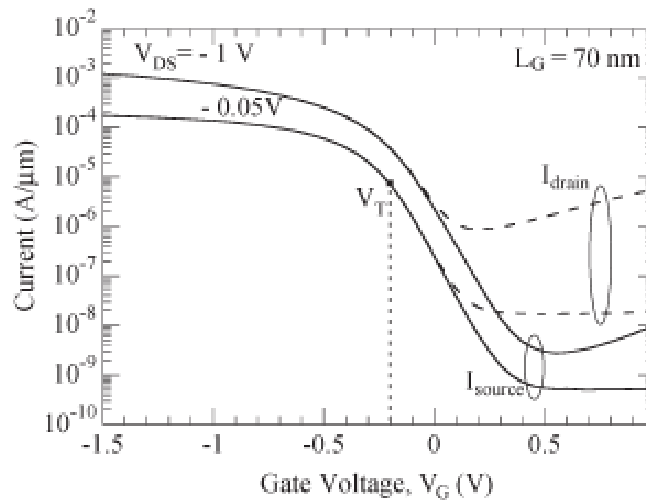
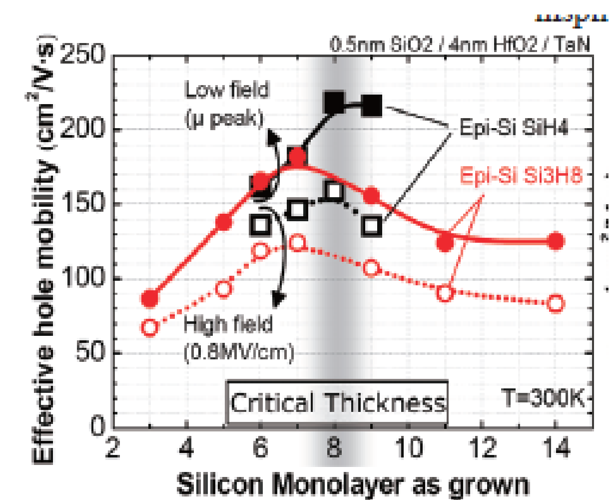


Fig.2: X-SEM picture of the Ge-in-STI structure. The inset shows a TEM of the gate stack with 2nm of HfO$_2$.







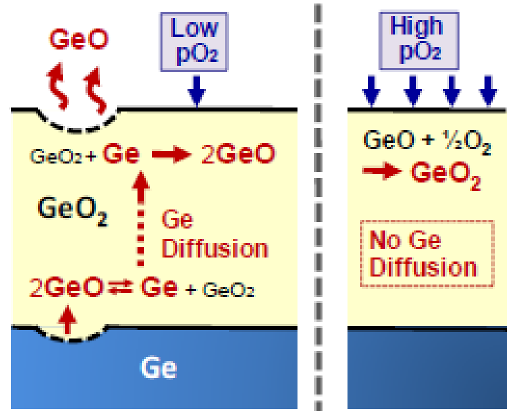
Zimmerman
IEDM 2006
Si passivation

Hellings
EDL 2009
Si passivation

Mitard
VLSI 2009
Si passivation

Ge Dielectric:

Another strategy: Advanced GeO_2 processing



Ge diffusion

High-pressure O2 (HPO) suppresses surface reaction

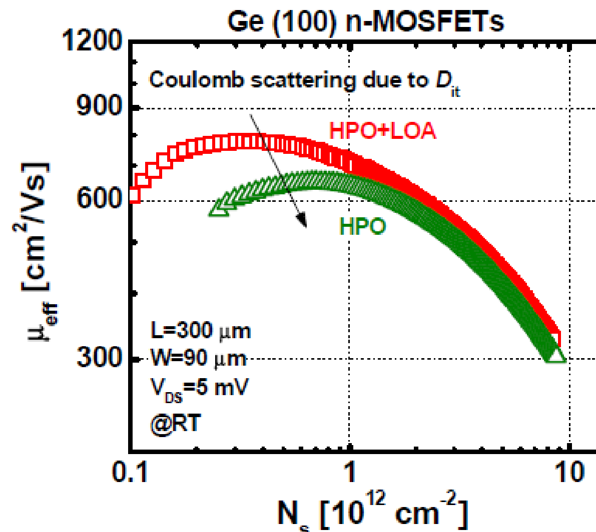
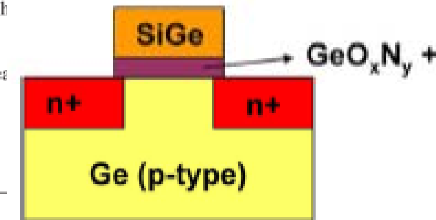
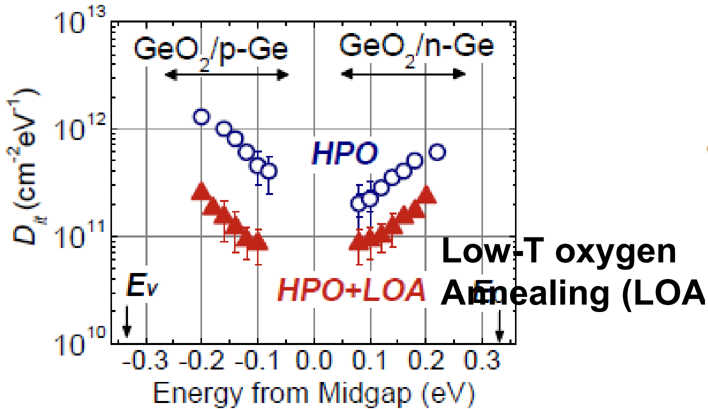


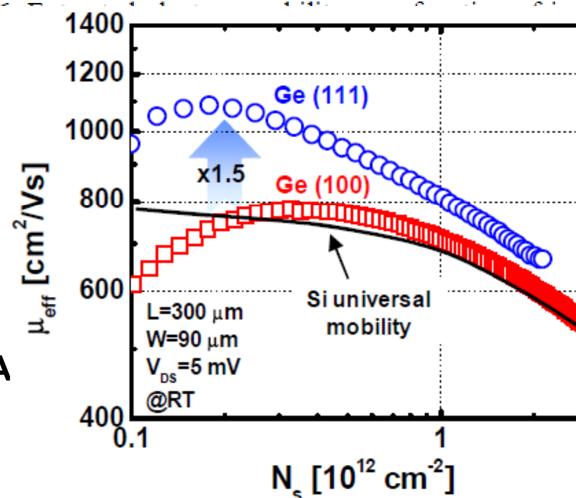
TABLE I
Si-CMOS-LIKE PROCESS FLOW

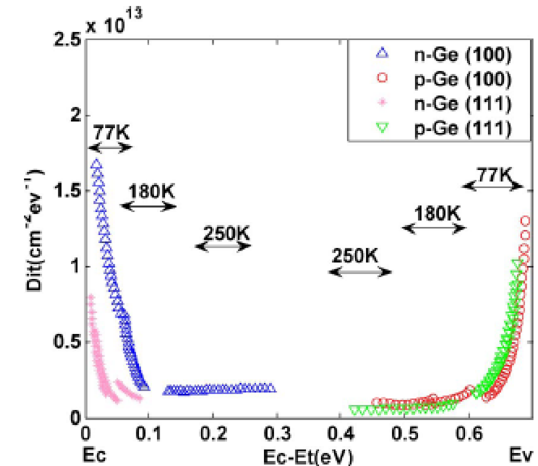
1.	Pre-diffusion clean for Ge
2.	GeON growth & LPCVD SiO_2 for isolation
3.	Active area lithography & oxide etch
4.	GeON growth & LPCVD SiO_2 for gate stack
5.	Poly SiGe deposition
6.	Gate lithography & etch
7.	Source/Drain Implant
8.	Dopant activation annea
9.	Backend dielectric
10.	Ti/Al contact pads
11.	FGA anneal





Low-T oxygen Annealing (LOA



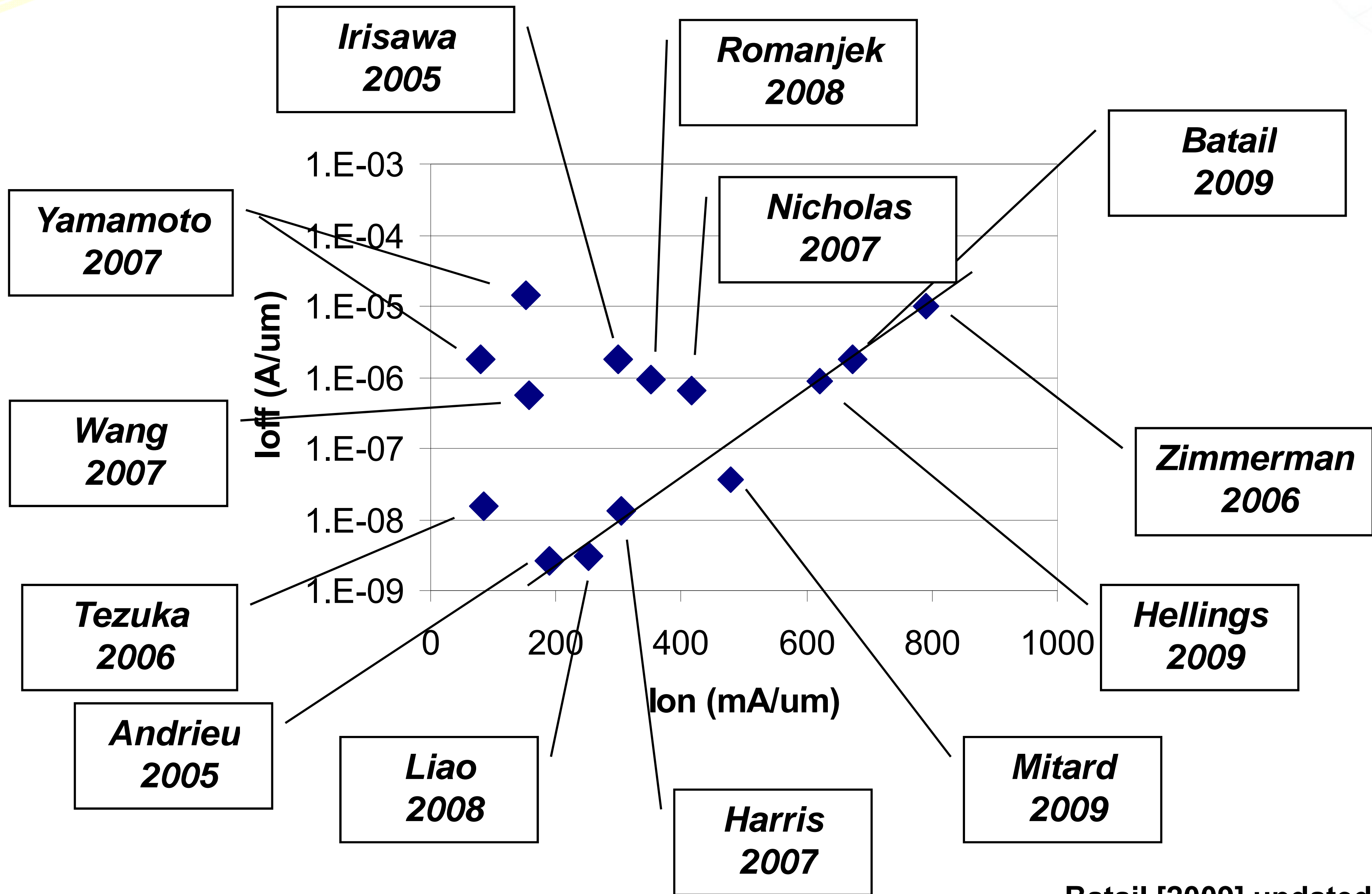


Kita
IEDM 2009
HPO + LOA

Lee
IEDM 2009
HPO + LOA

Kuzum
TED 2009
GeOxNy + LOA

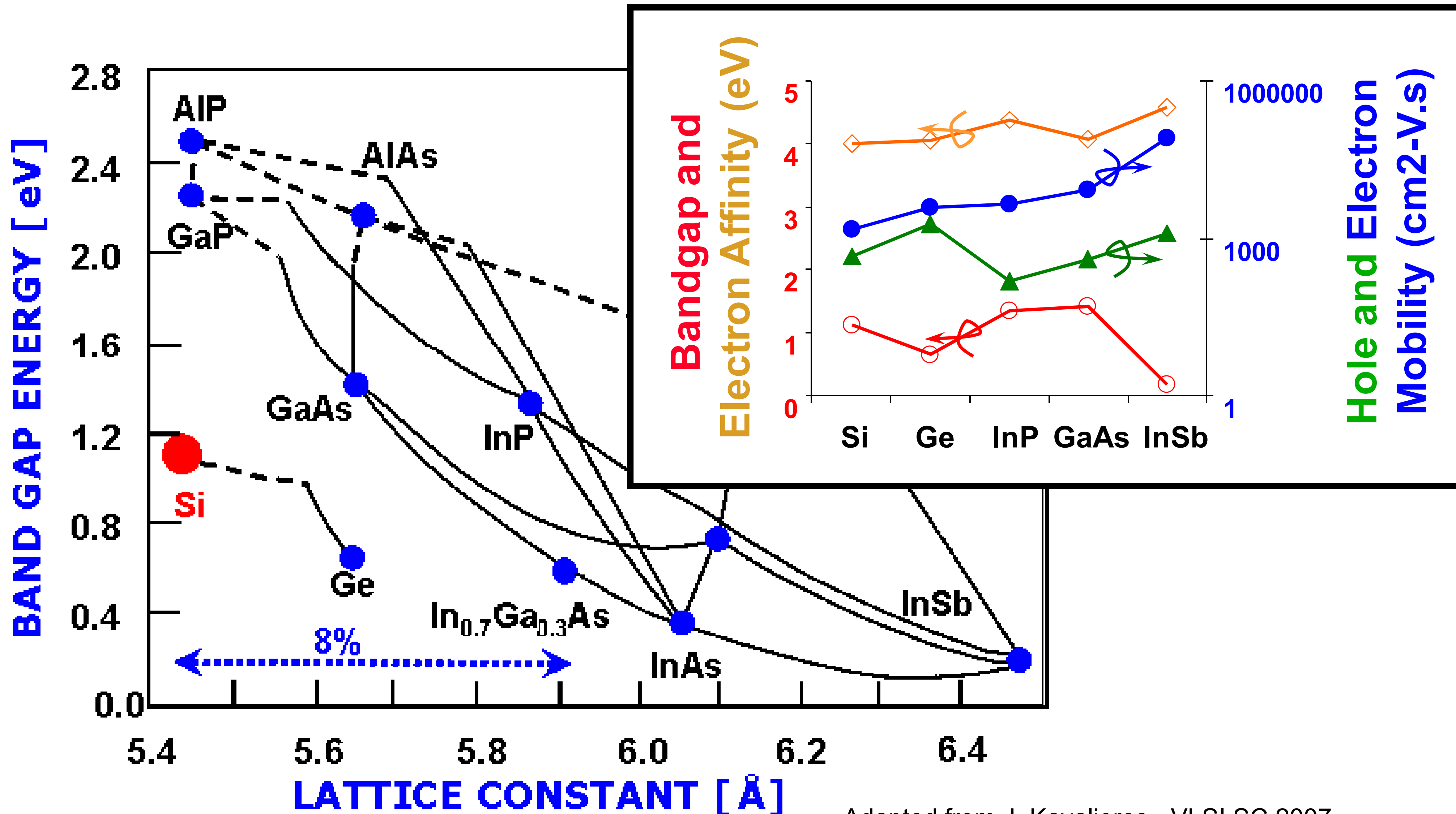
Ge Benchmarking



Batail [2009] updated

III-V vs Ge: NMOS

The Lure of High Mobility



Adapted from J. Kavalieros - VLSI SC 2007
K. Kuhn – ECS 2010

Low m* MOSFETs: "Density-of-states bottleneck"

- **On-current of a MOSFET**

$$I = Q\upsilon$$

- **Velocity υ**
  - Diffusive : mobility μ, $\upsilon = \mu \mathscr{E}$
  - Ballistic: injection velocity υ_{inj}
  - Light $m^* \rightarrow$ high μ, high υ_{inj}
- **Charge Q**
  - MOS limit ($C_Q \gg C_{ox}$), $C \approx C_{ox}$
  - Light $m^* \rightarrow$ less D (C_Q), less C, less Q
  - More important for thin oxide (large C_{ox}),

"DOS bottleneck"

$$Q = C\left(V_G - V_{th}\right)$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_Q}$$

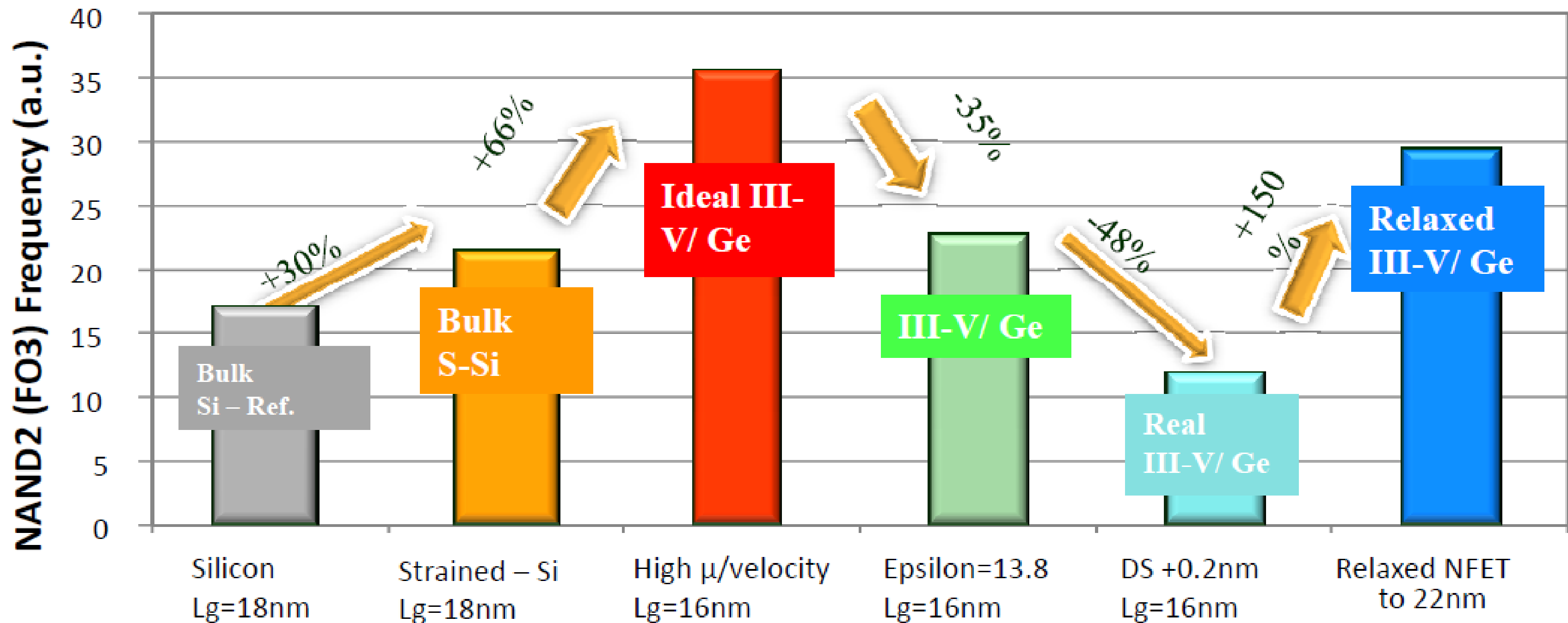
$$C_Q = q^2 D$$

From R. Kim

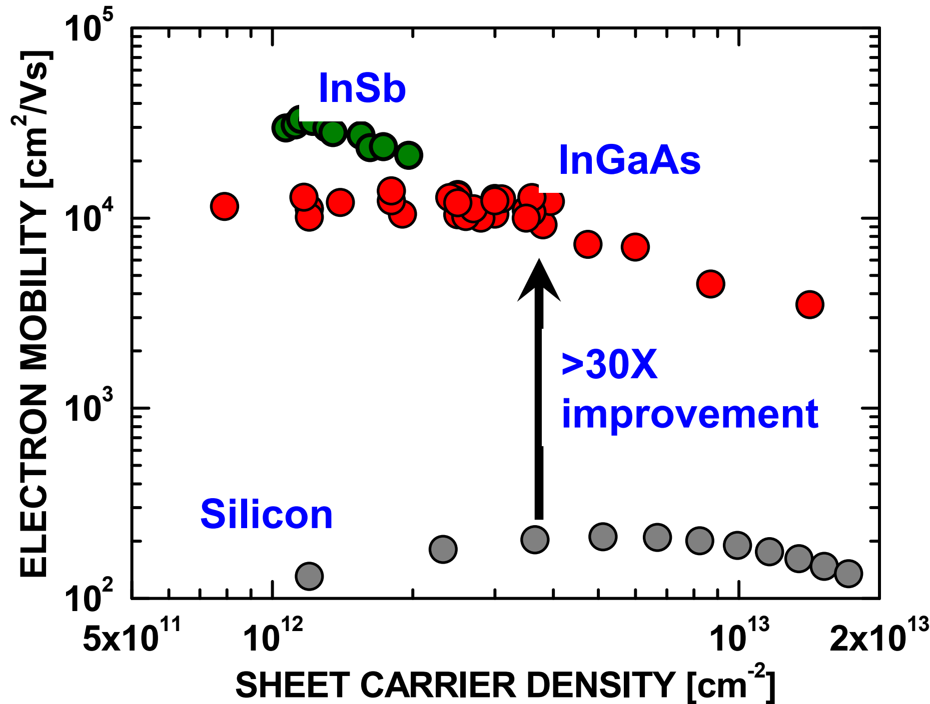
T. Skotnicki,
IEDM 2010 SC

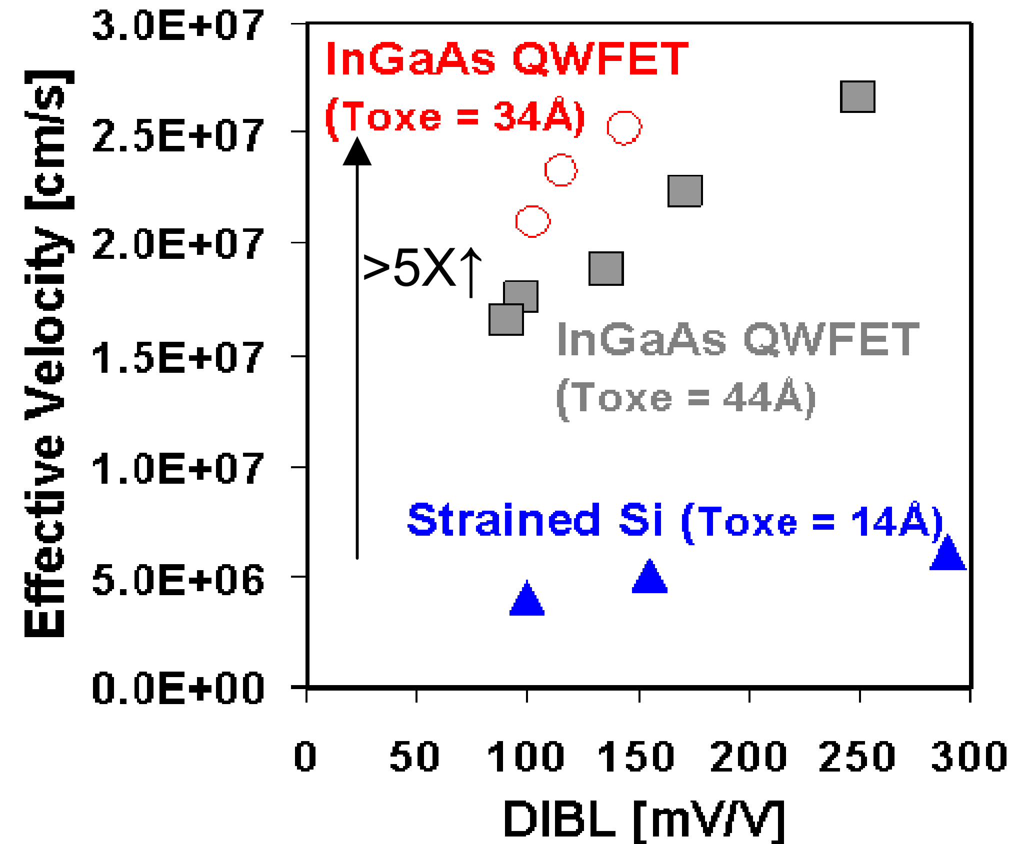
Step-by-Step High-μ Material Analysis for 16nm node at Ioff = 0.5nA/μm

Material	Epsilon	Kvs	Kμ	DS (nm)	remark
S-Si (n)	12	1.7	1.8	+0.3	Full Strain-Si
S-Si (p)	12	1.5	7	+0.5	Full Strain-Si
UTB	12	1.1	1.2	+0.3	Slightly Strained
Virtual III-V	13.8	>3	10	+0.5	High μ for electron
Ge	16	1.5	3	+0.5	High μ for holes



Success of III-V Materials as Transistor Channel (Vcc = 0.5V)

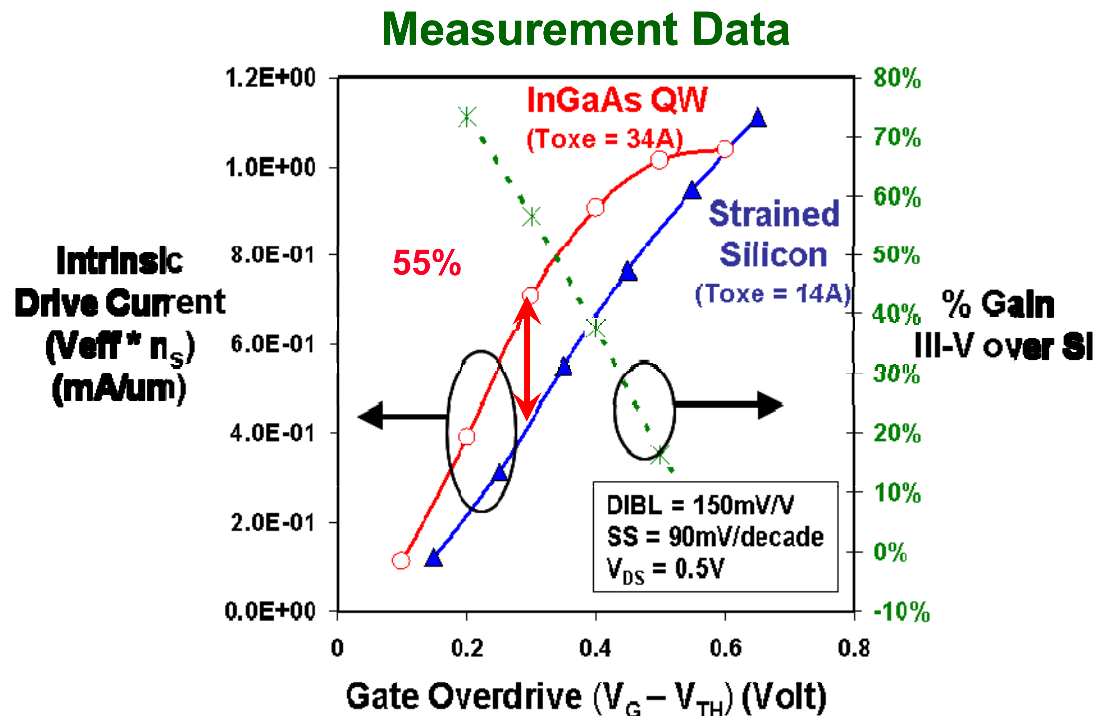


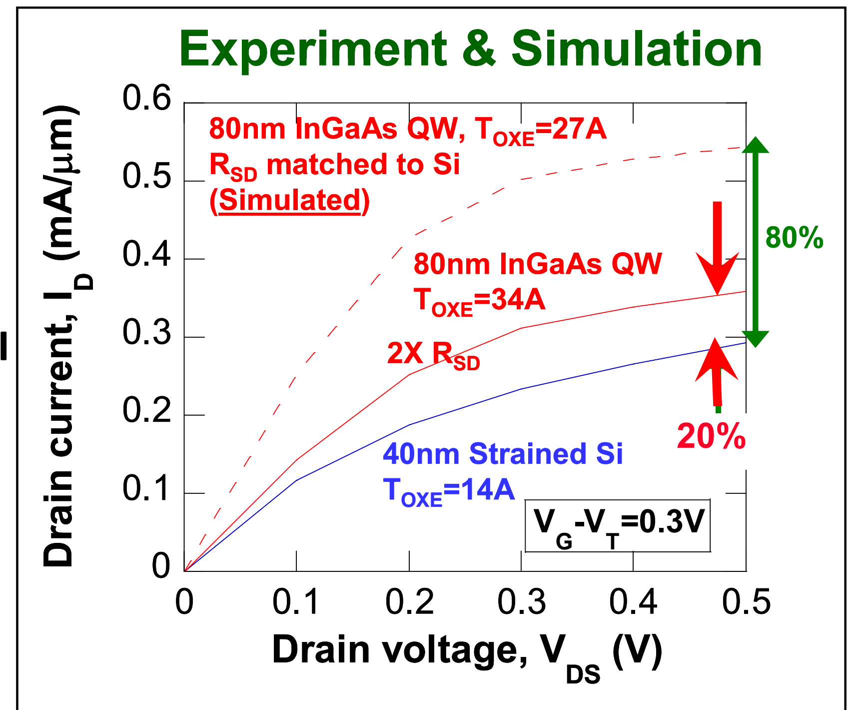


R. Chau, Intel, ESSDERC 2008

At Vcc ~ 0.5V III-V n-channel devices show significantly higher mobility (30X) and higher effective velocity (5X) than strained silicon MOSFETs

Significant Gain in Intrinsic Drive Over Si at Low Vcc (e.g. 0.5V)





R. Chau, ESSDERC 2008

At a gate overdrive = 0.3V, III-V QWFET shows 55% intrinsic drive current gain over strained Si

At a drain voltage of 0.5V, III-V QWFET shows >20% I_{DSAT} gain over strained Si (despite thicker Toxe and higher R_{SD})

5 High-Current L & Γ-L channels: 5 Approaches

Rodwell et al, 2010 Device Research Conference 6/21/2010

Standard [100] channel Γ transport

[111] channel: transport in Γ, 1st two L[111] eigenstates

[111] stacked wells: transport in two L[111] wells

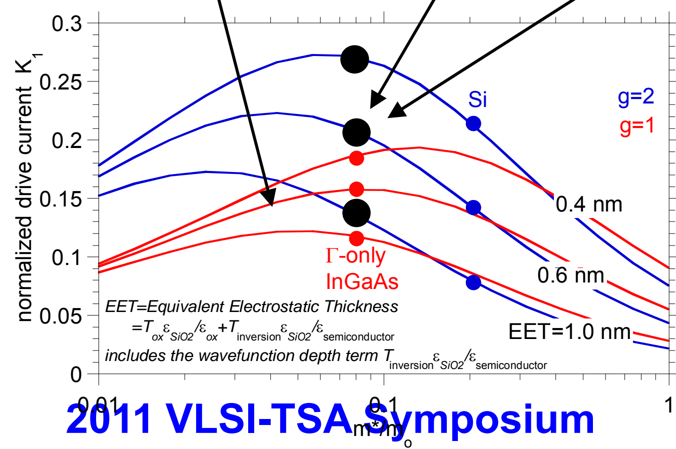
[110] wafer: transport in two anisotropic L bands

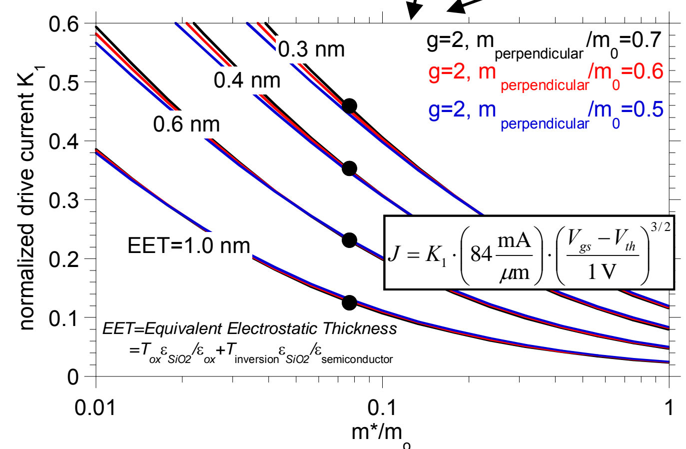
[110] fin on [100] wafer: transport in two anisotropic L bands

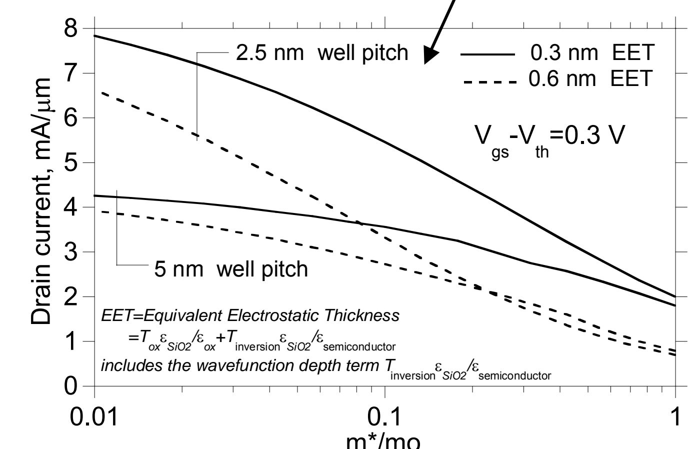
[011] MQW fin on [111] wafer: L[111] transport in array of 1D channels

Rodwell, DRC, 2010

blue=occupied
red=vacant

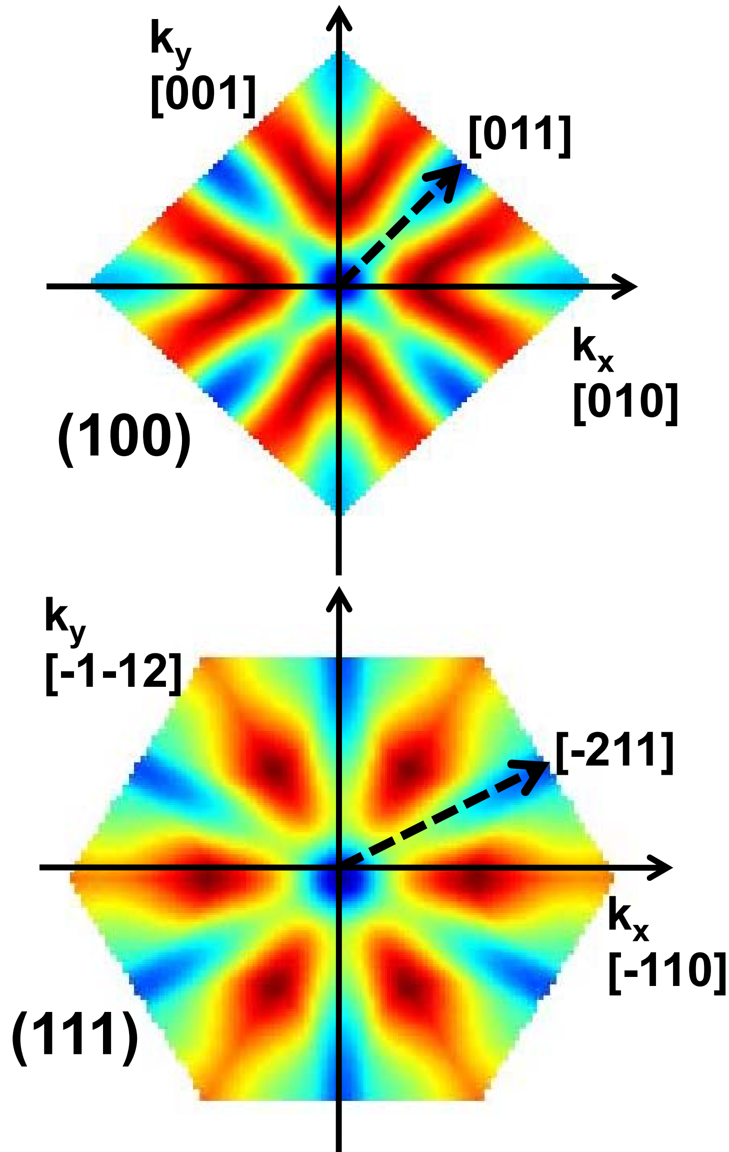


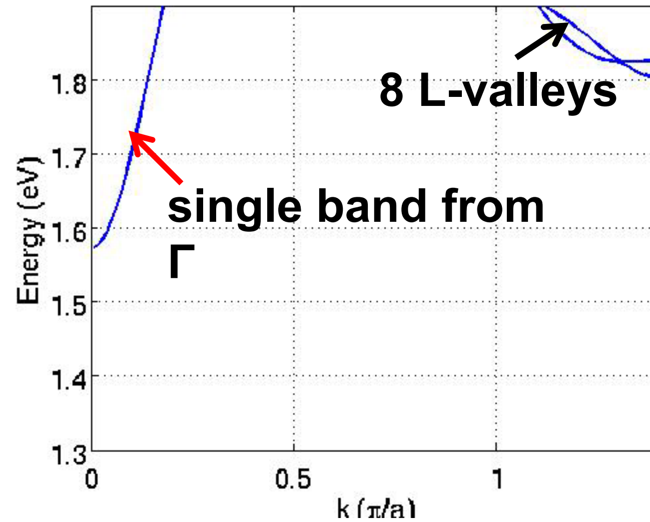




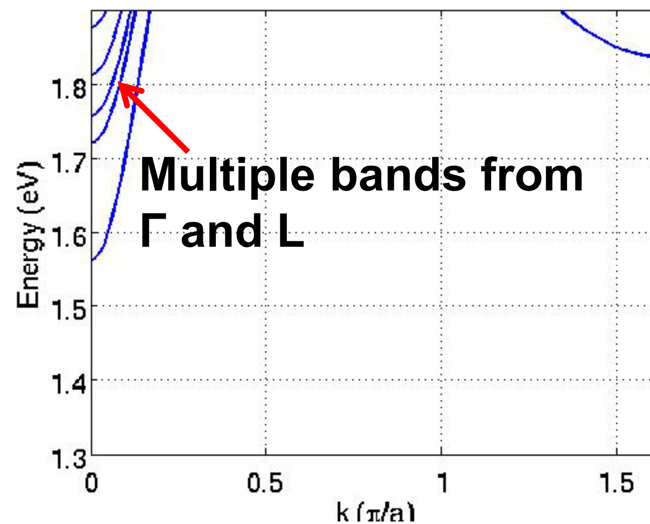
Use of L-valleys: GaAs

- GaAs 4 nm





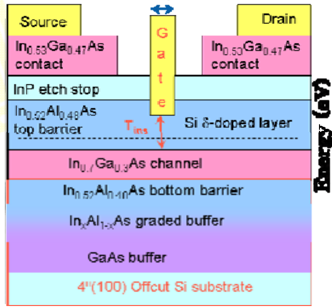
Small DOS with high v_{inj}
High DOS with low v_{inj}



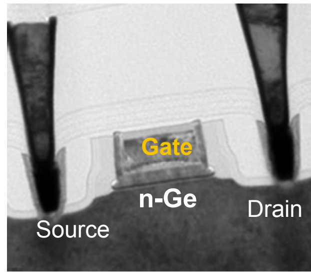
More DOS with high v_{inj}

From R. Kim

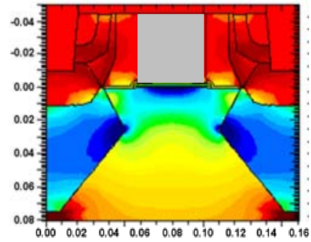
MOBILITY



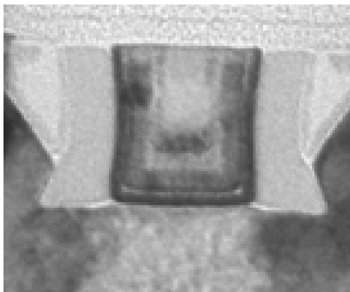
III-V



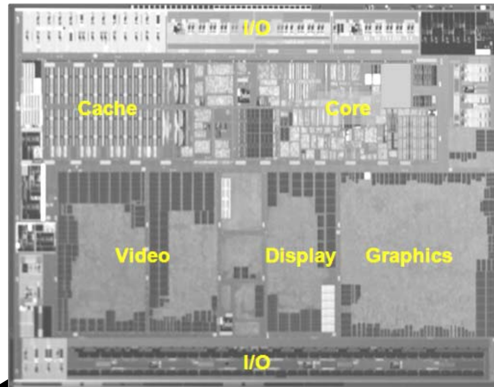
Ge



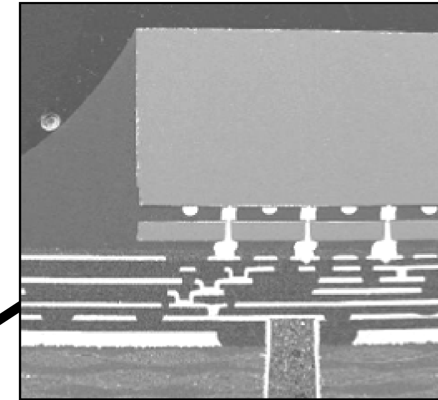
Strain



32nm

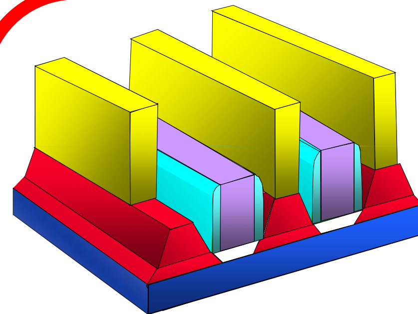


System-on-chip

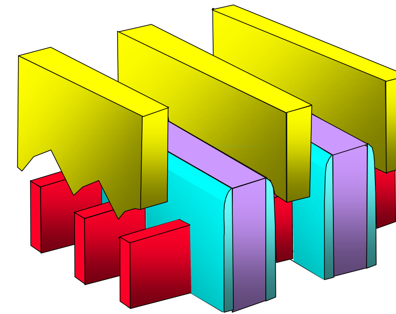


System-in-package

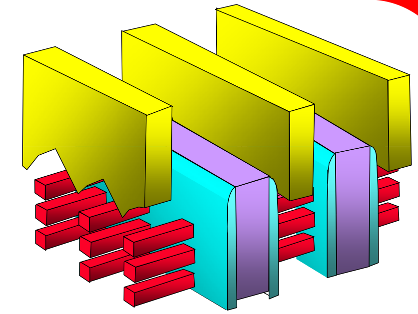
STRUCTURE



UTB SOI



Fins



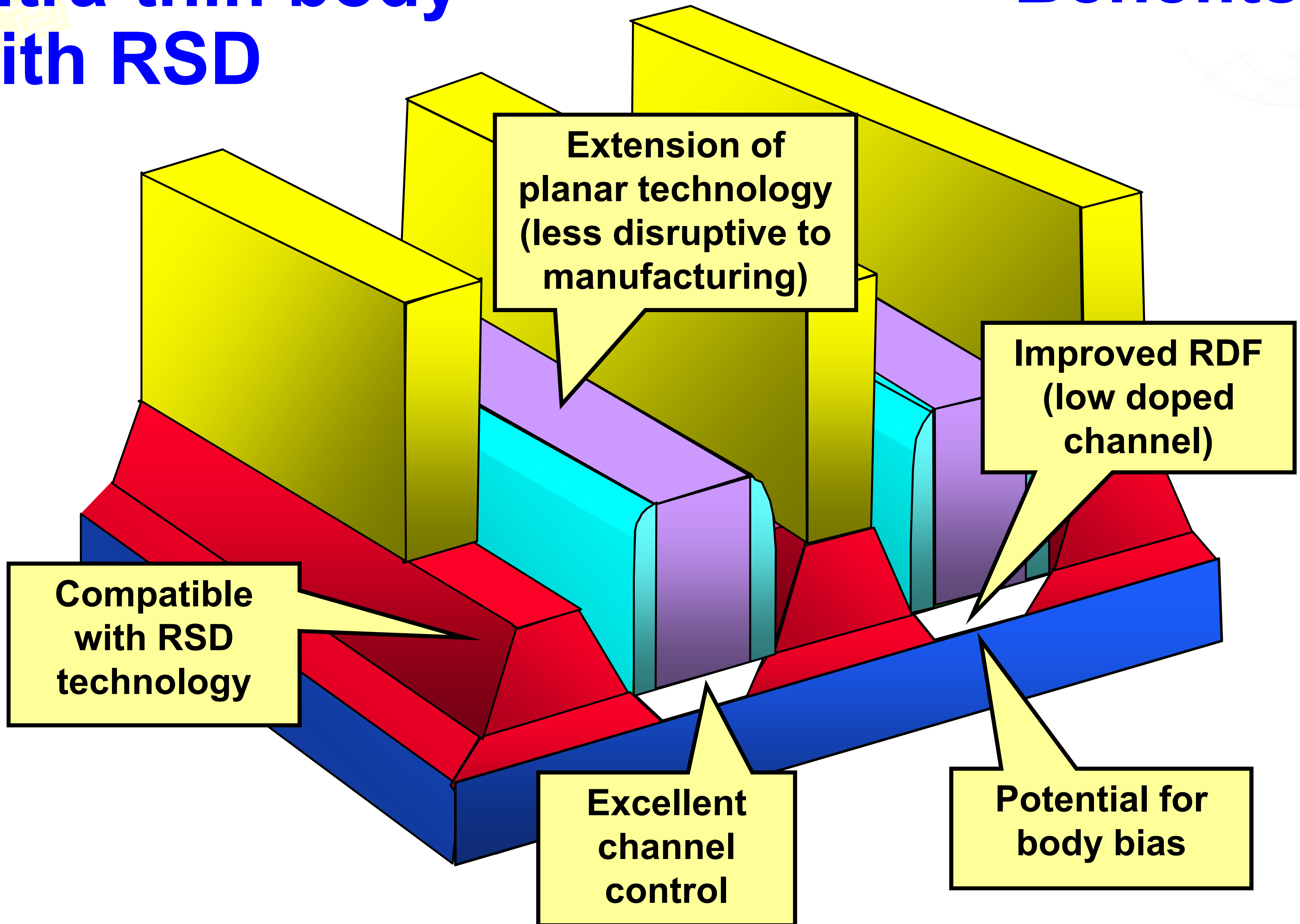
Wires/Ribbons

ELECTROSTATIC CONFINEMENT

VLSI SINCE 1983

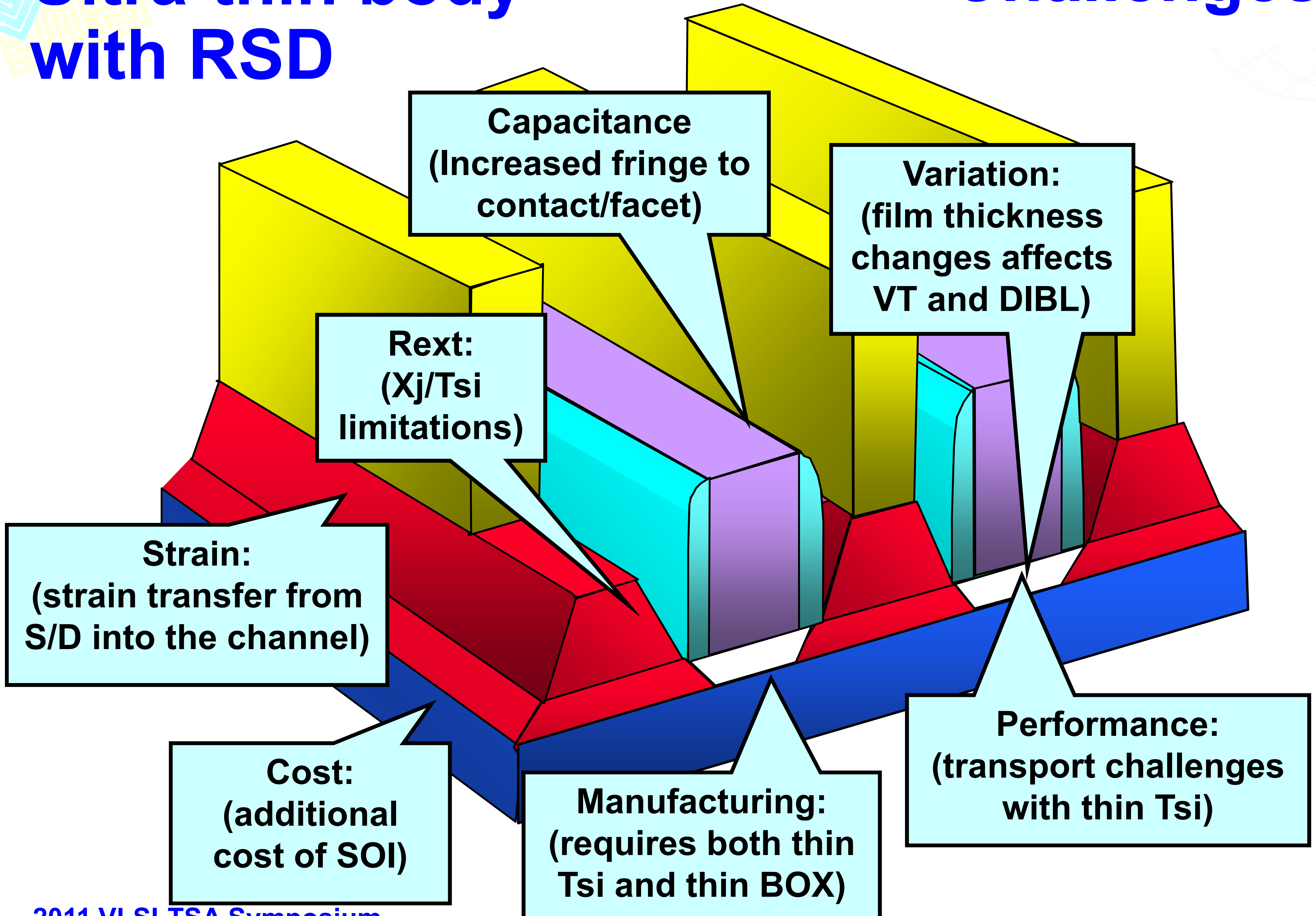
Ultra-thin body with RSD

Benefits



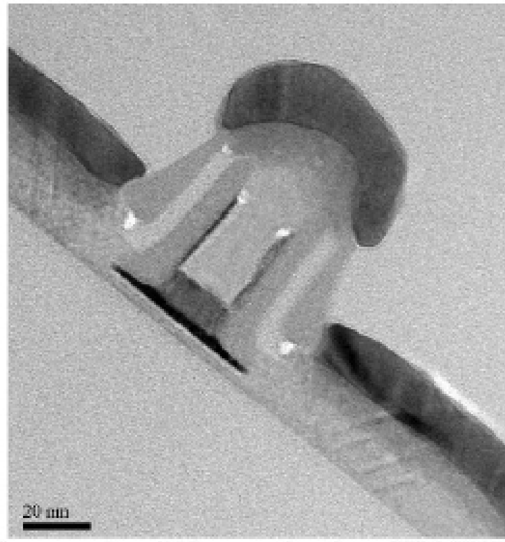
Ultra-thin body with RSD

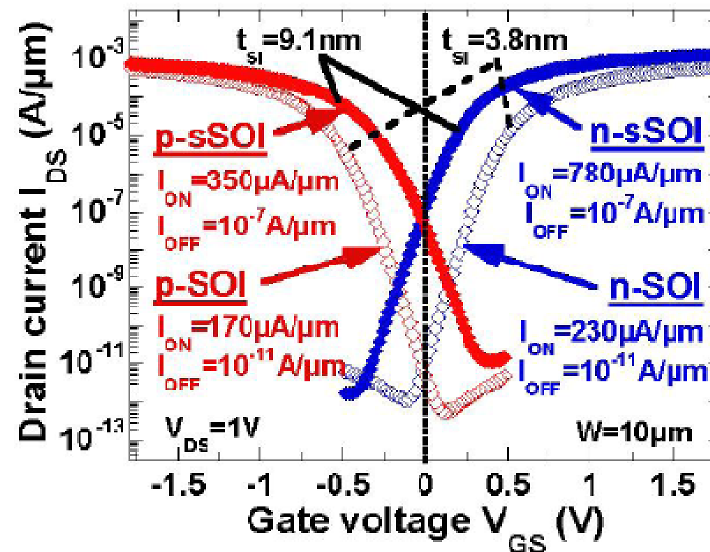
Challenges

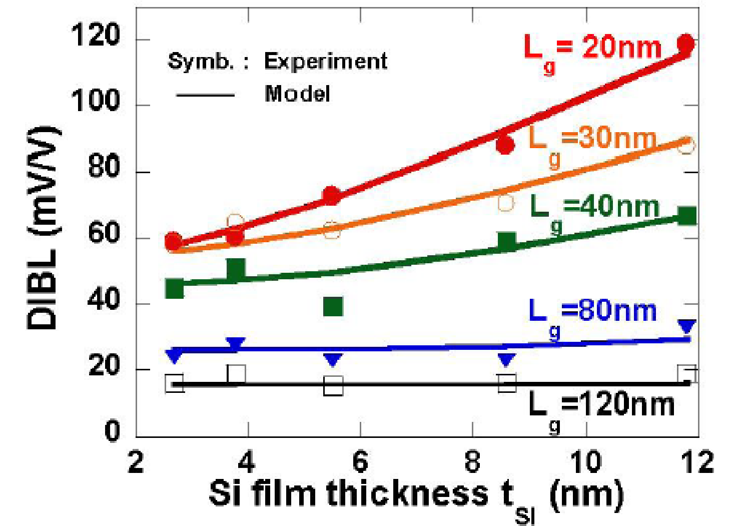


Ultra-thin body

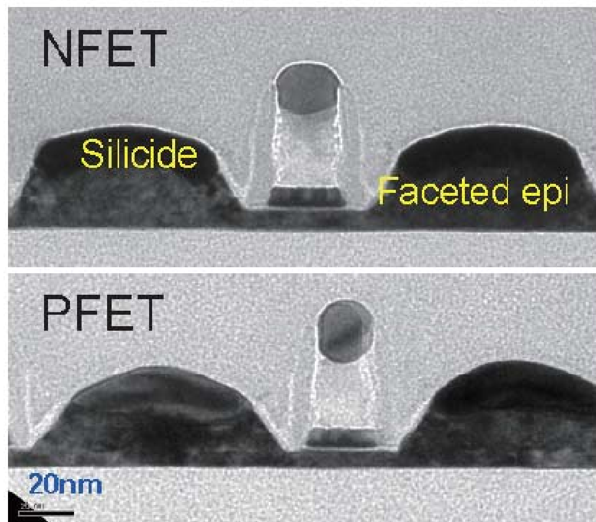
Barral – IEDM 2007

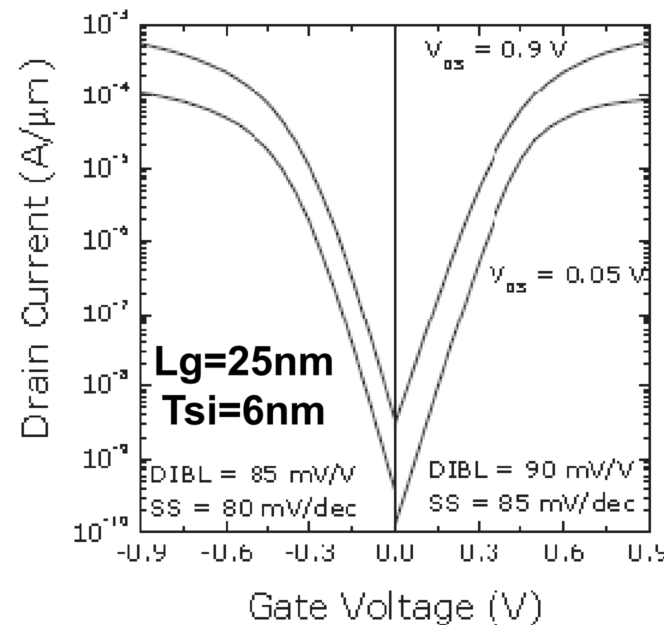


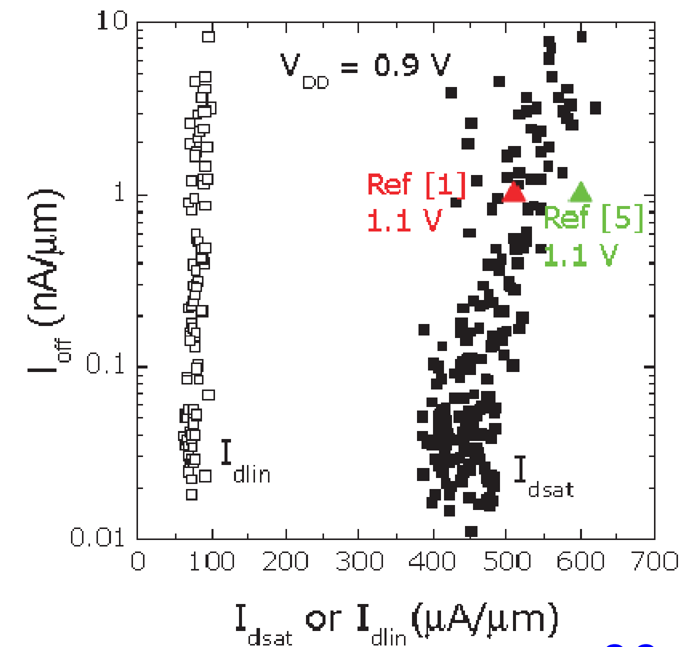




Cheng – VLSI 2009

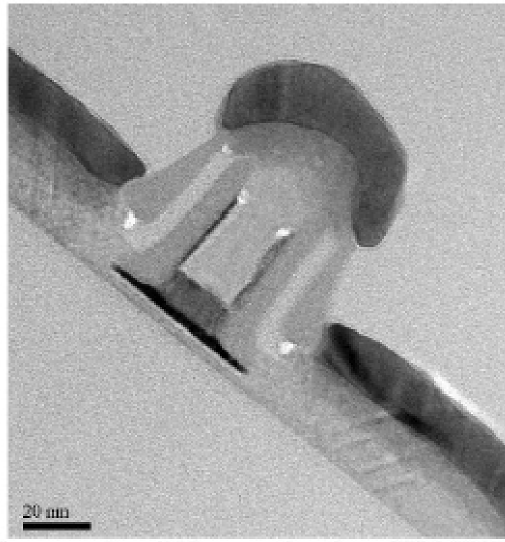


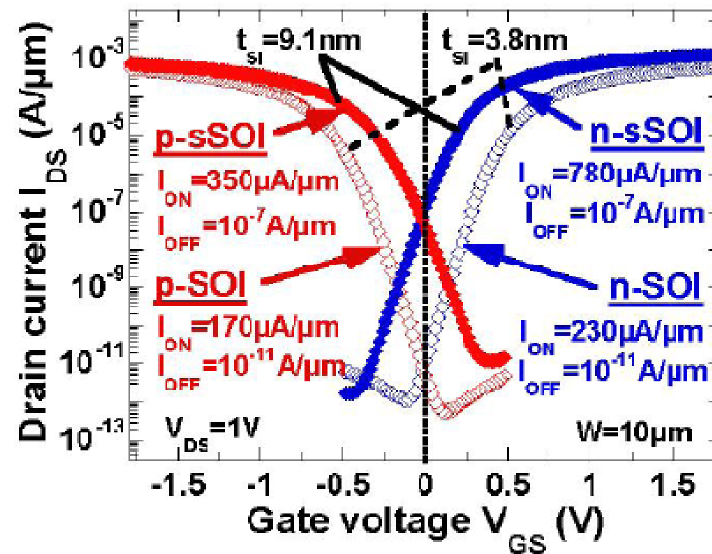


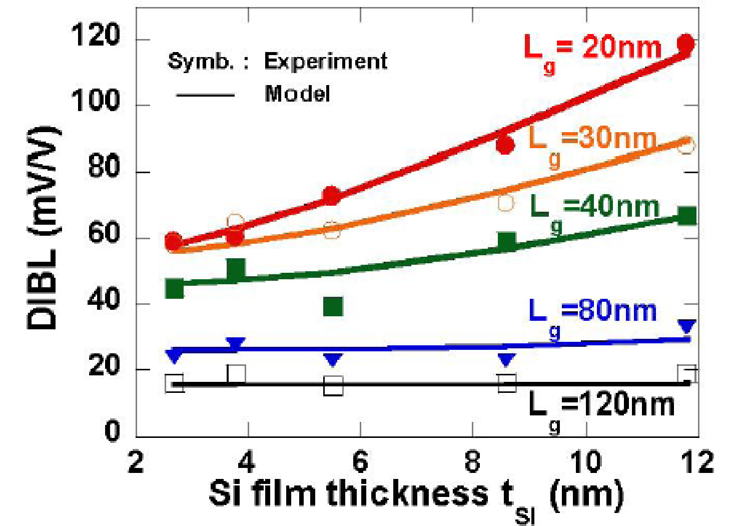


Ultra-thin body

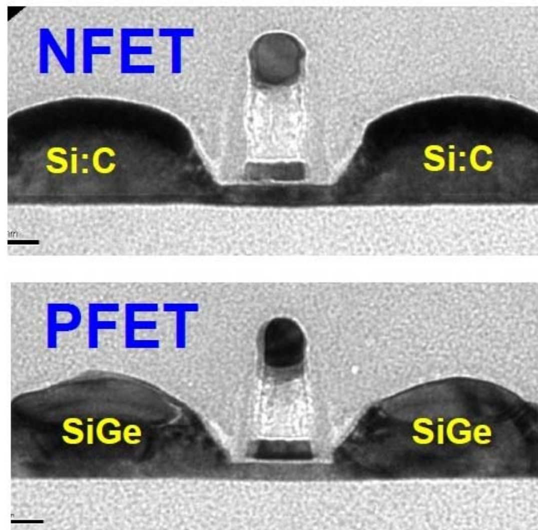
Barral – IEDM 2007

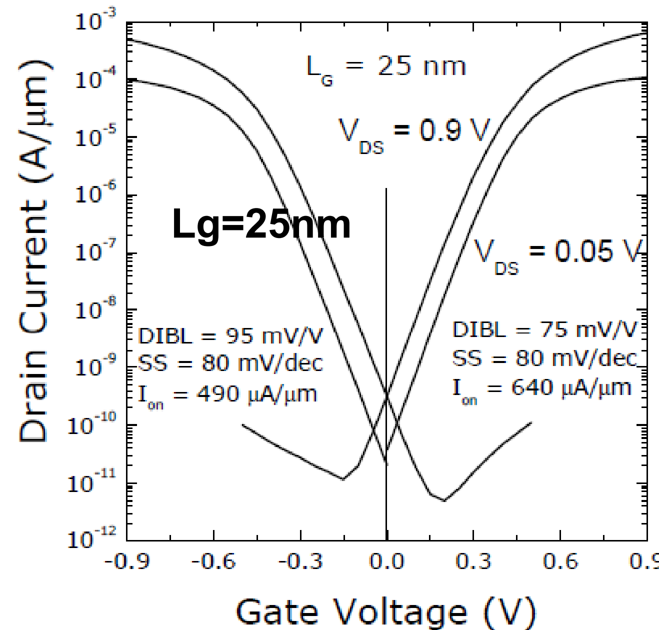


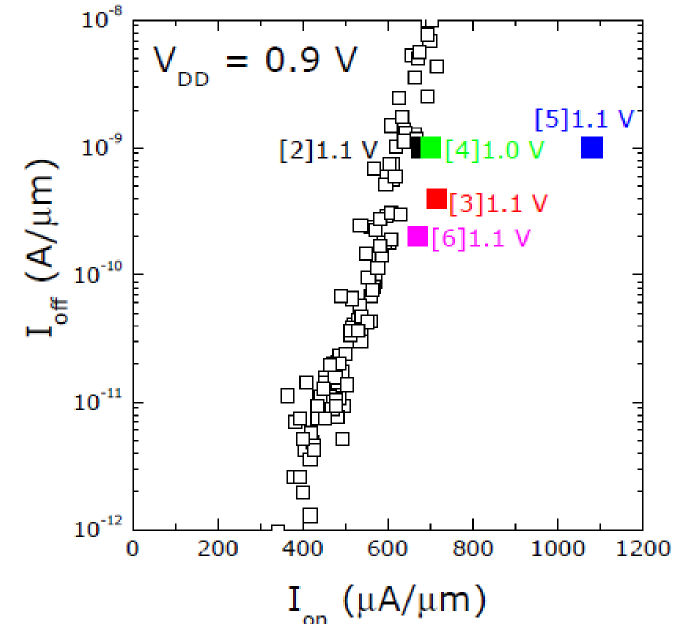




Cheng – IEDM 2009

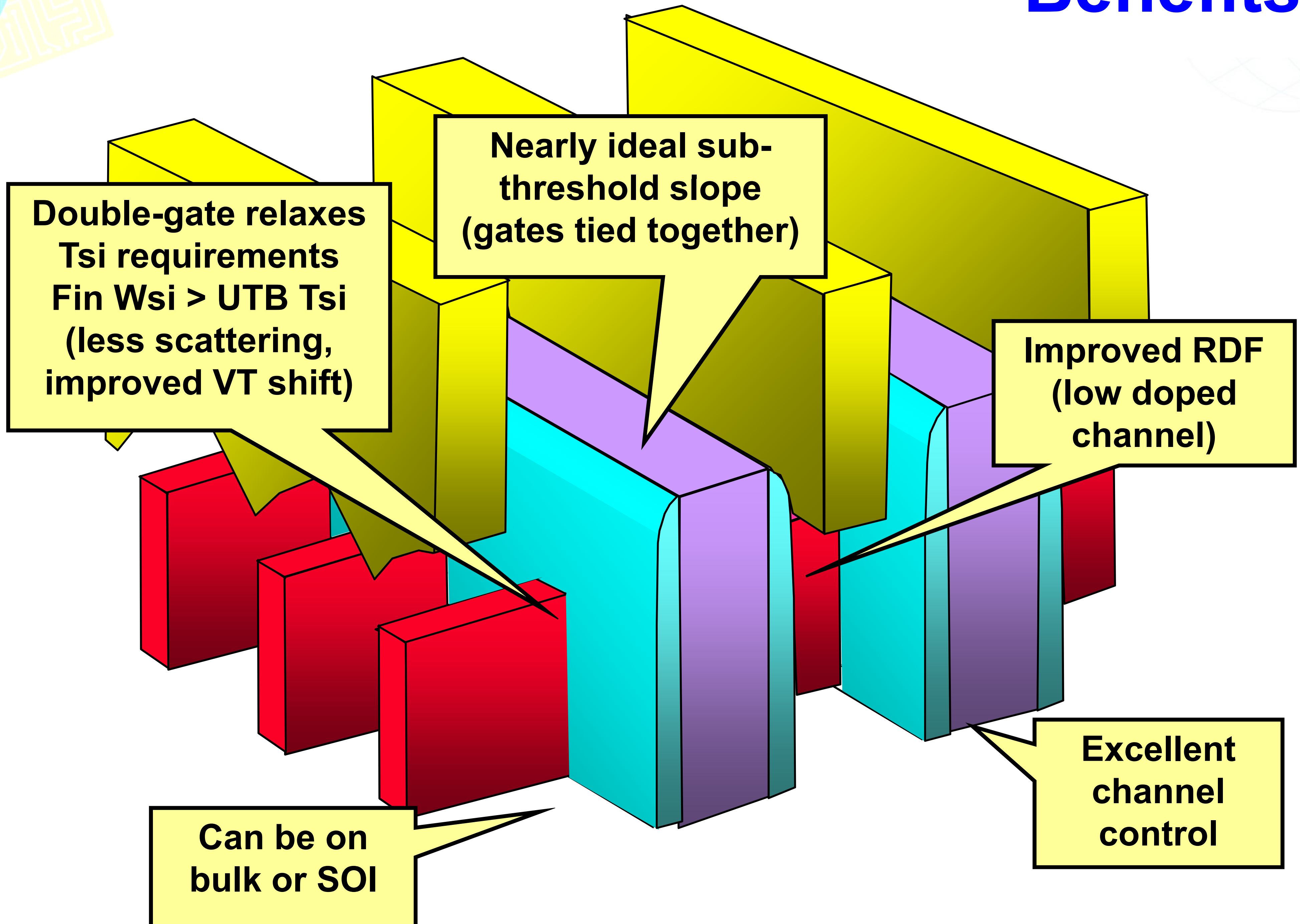






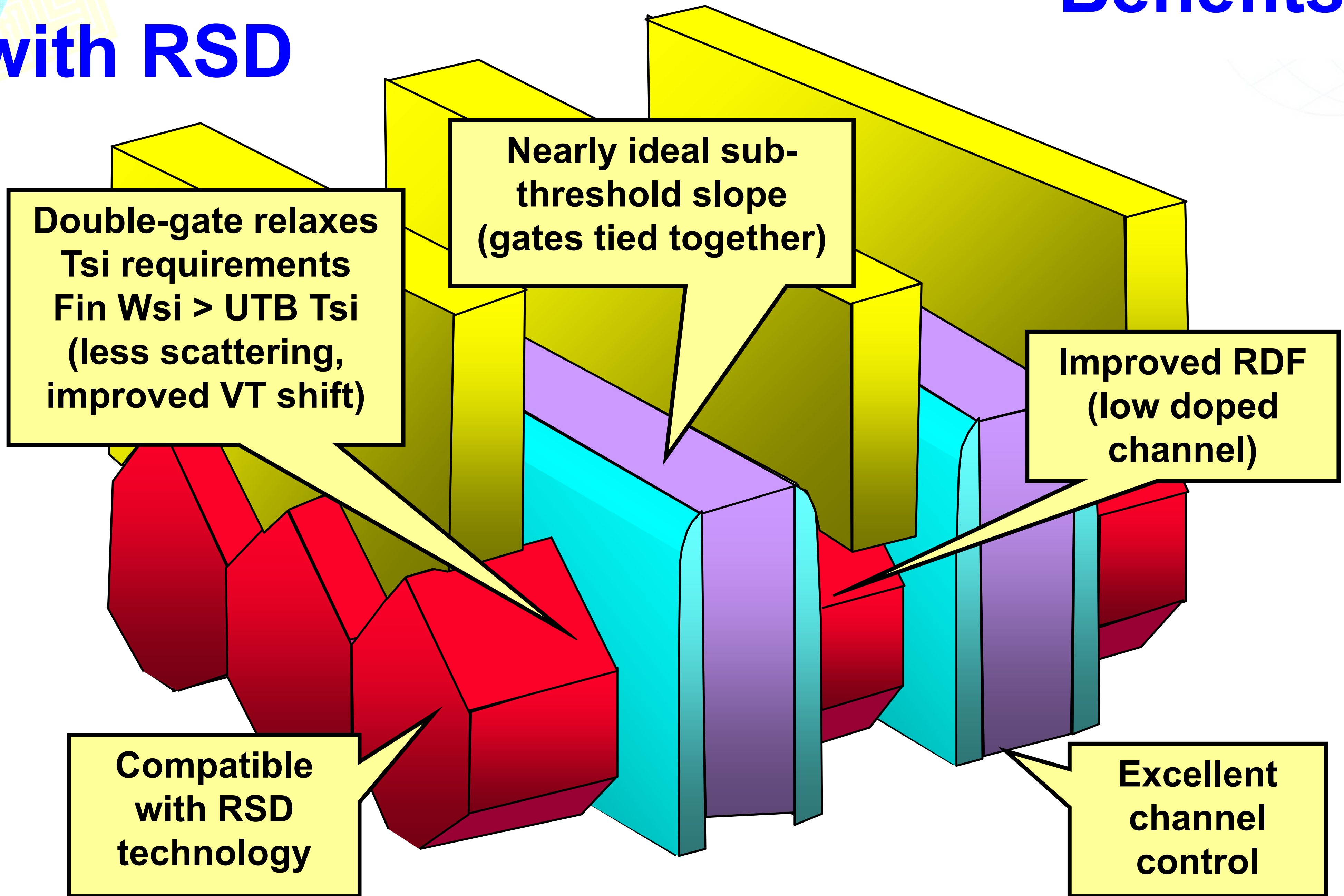
MuGFET

Benefits

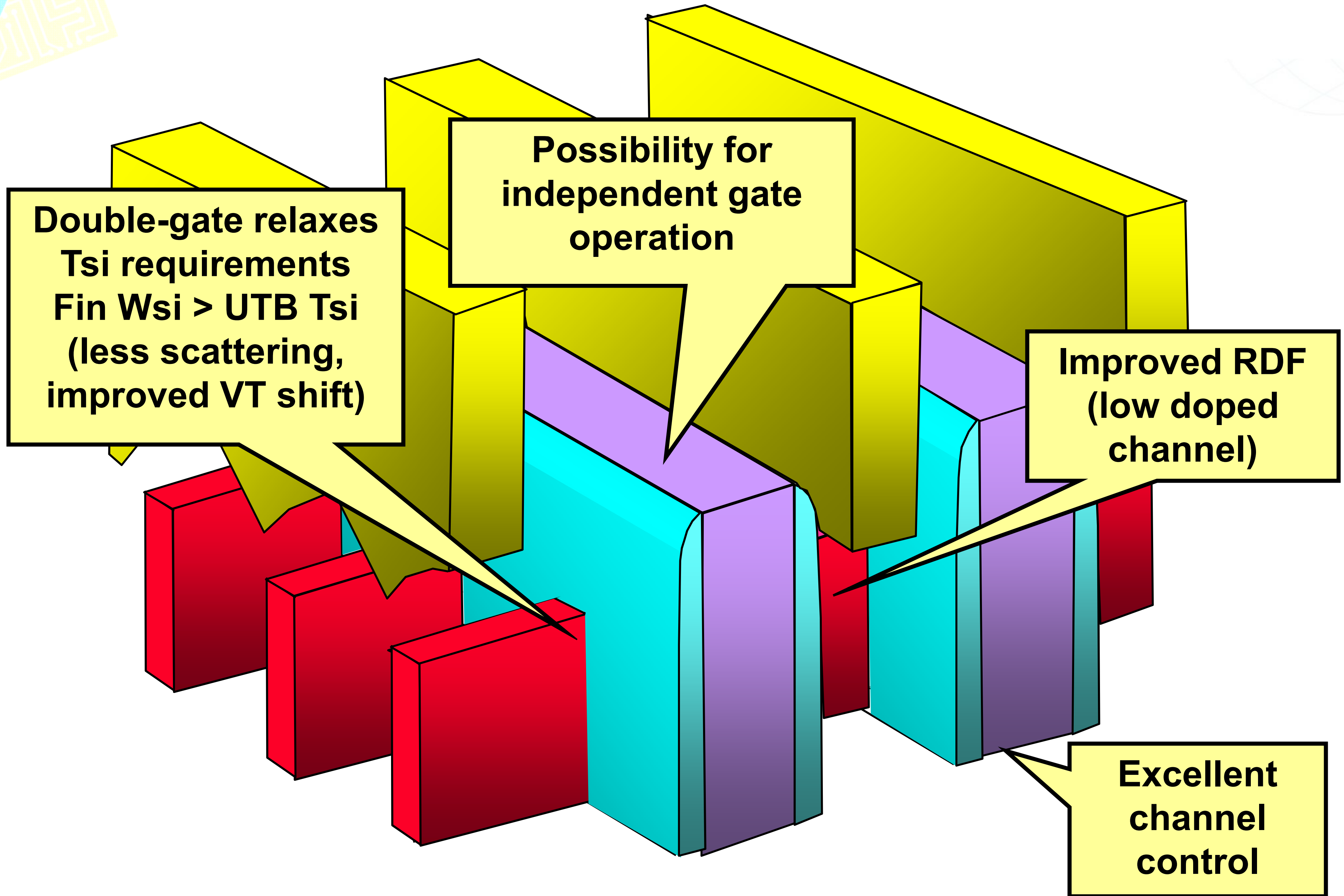


MuGFET with RSD

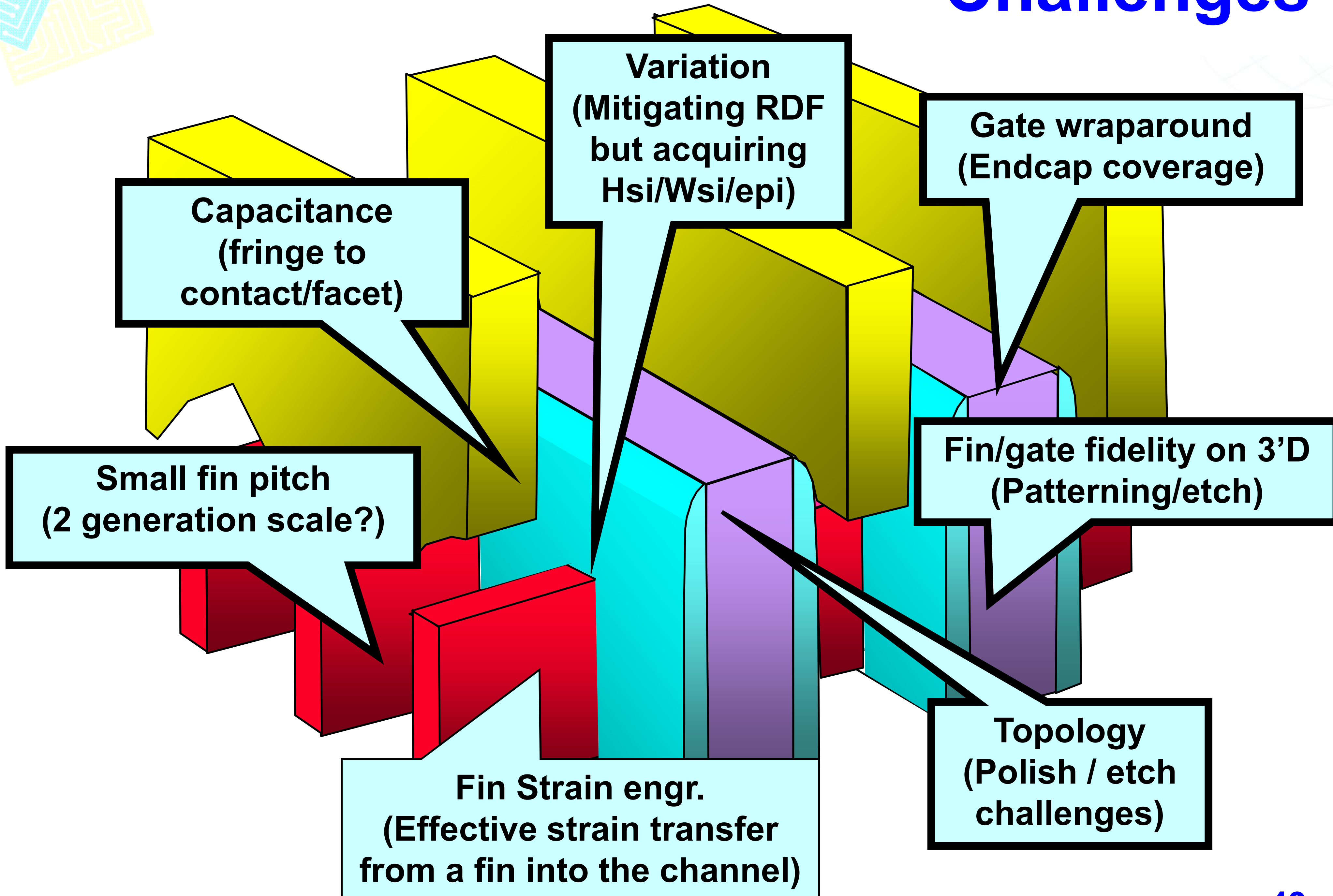
Benefits



MuGFET

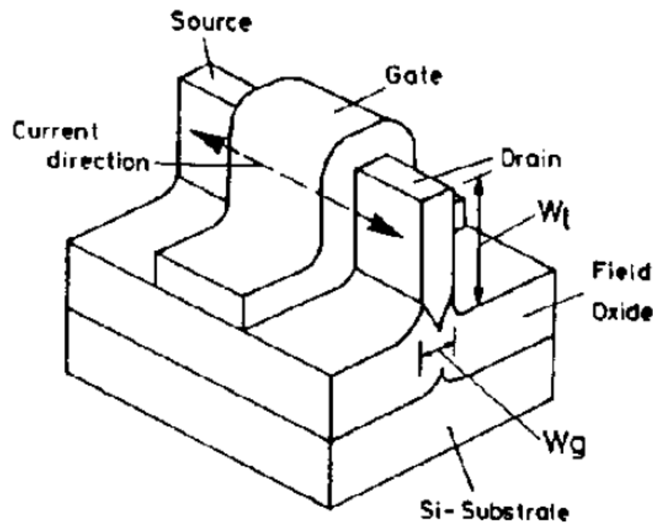


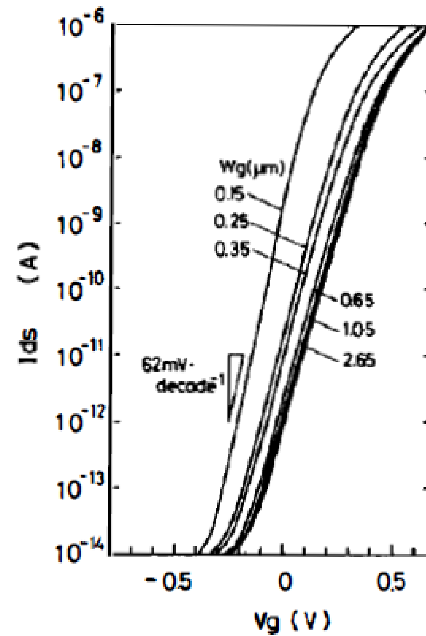
MuGFET Challenges

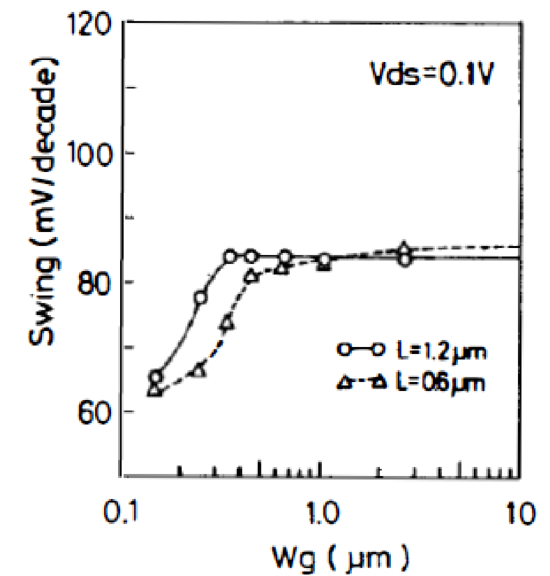


MuGFET

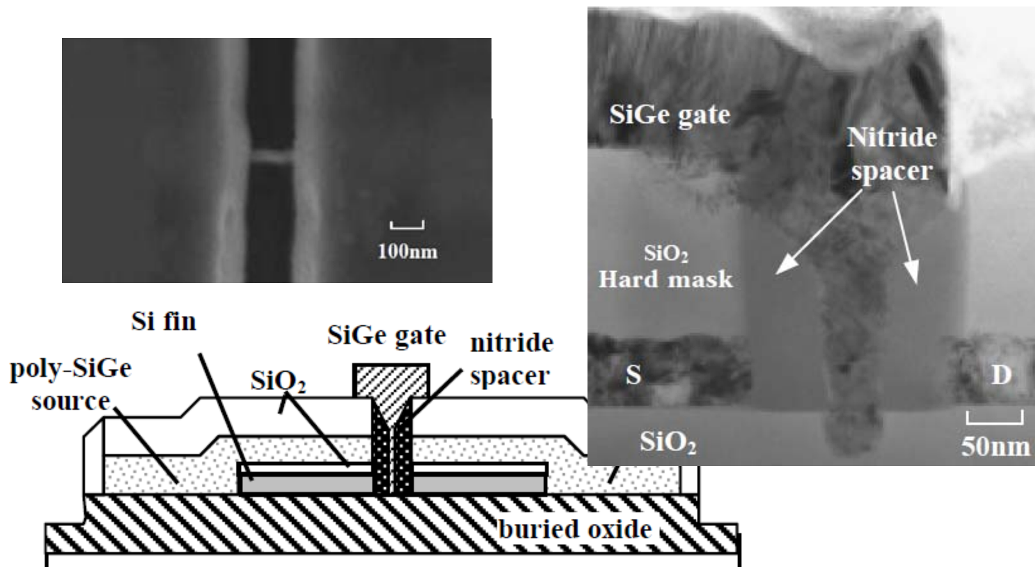
Hisamoto – IEDM 1989

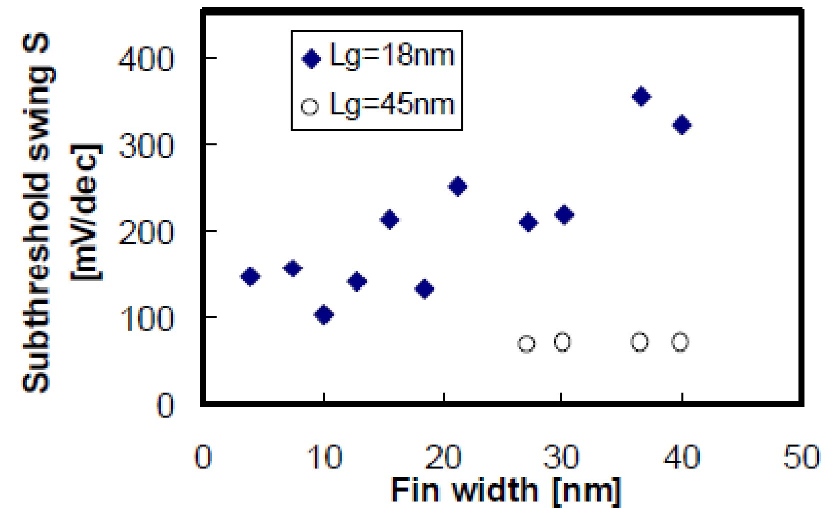






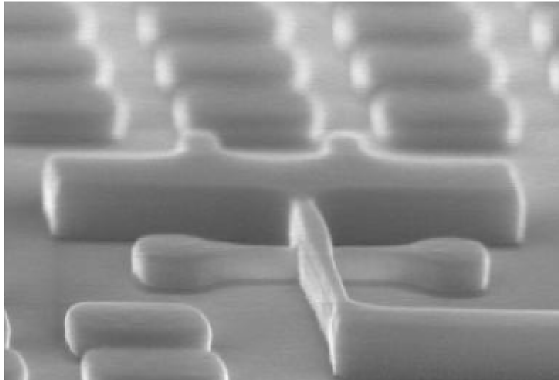
Huang (Hu) – IEDM 1999

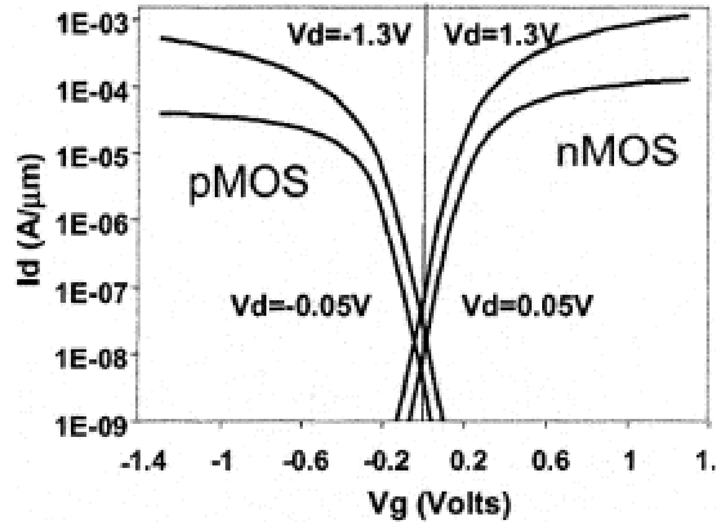


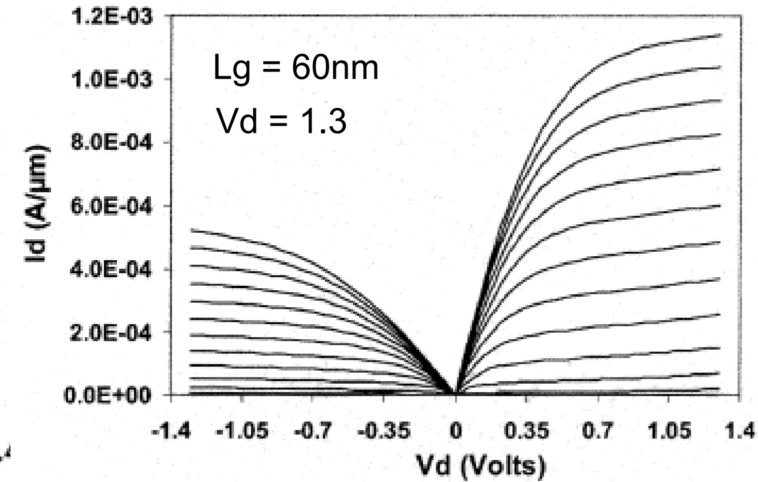


Trigate

Chau – ISSDM 2002

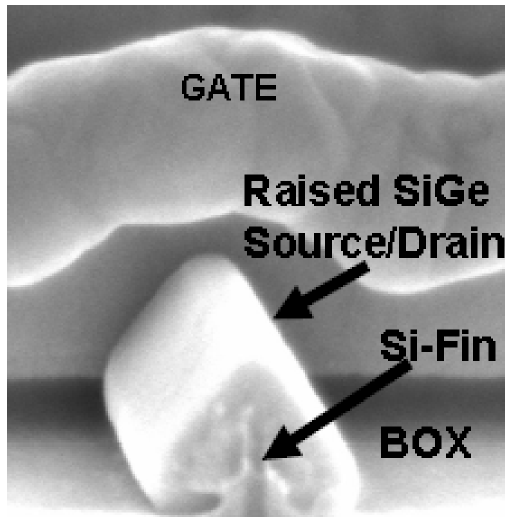


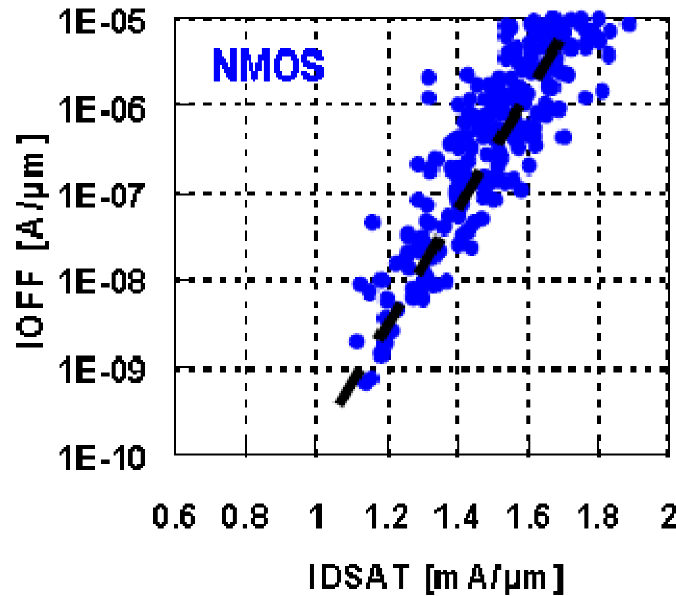


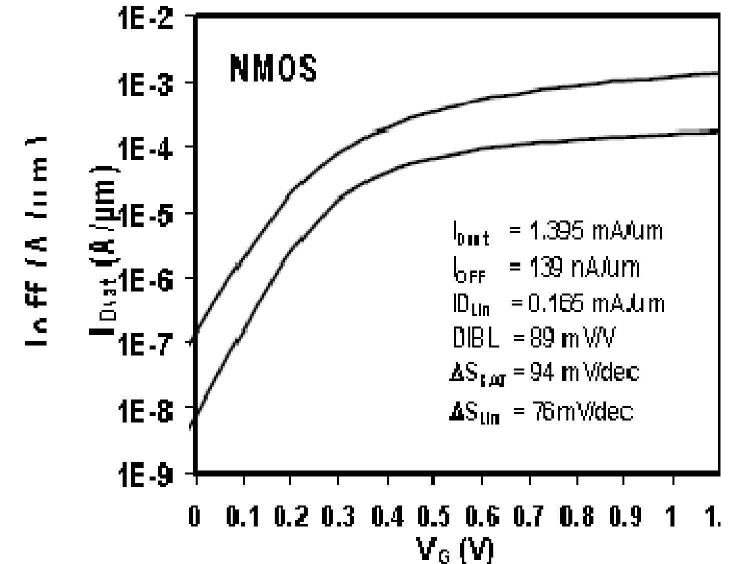


Kavalieros - IEDM 2006

Advanced Depleted-Substrate Transistors

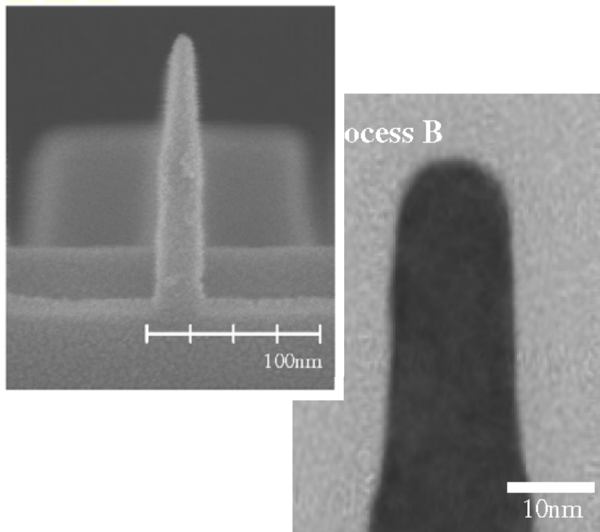


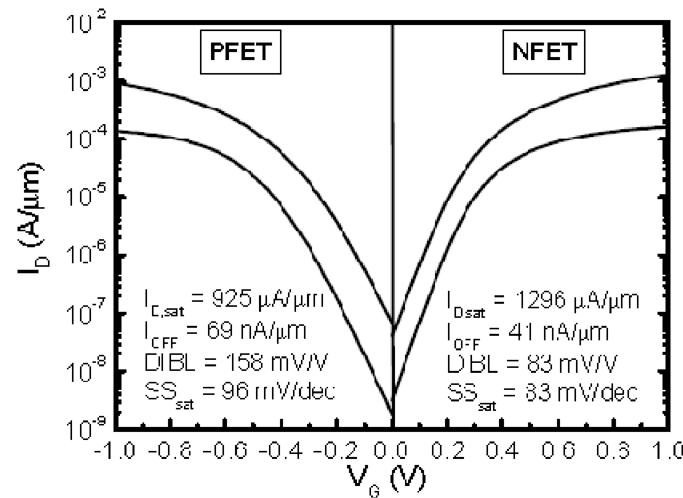


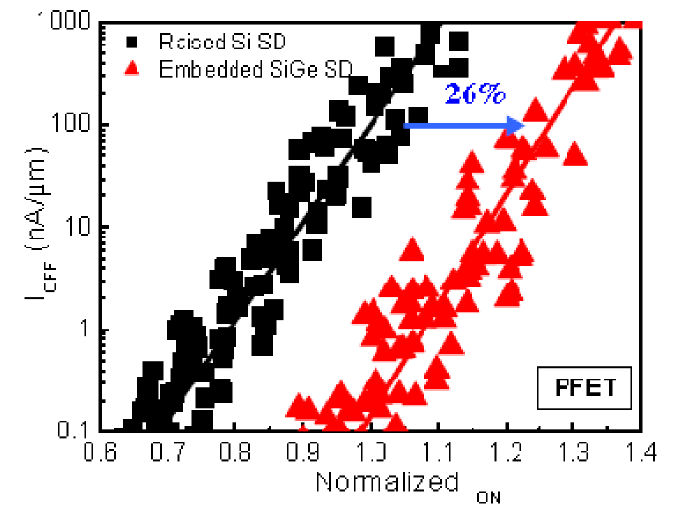


MuGFET

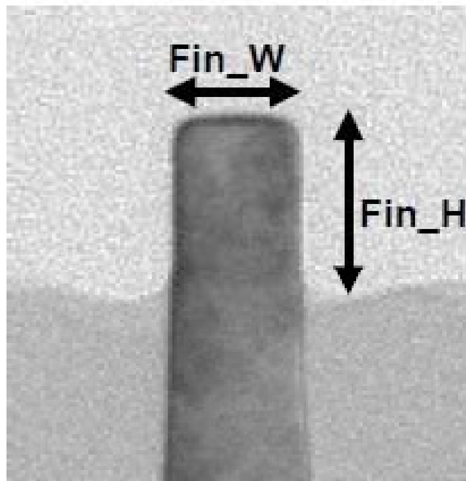
Chang – IEDM 2009



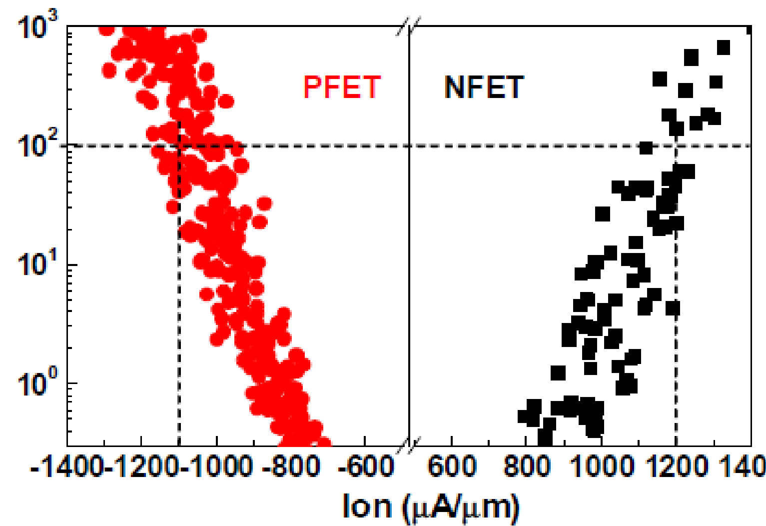


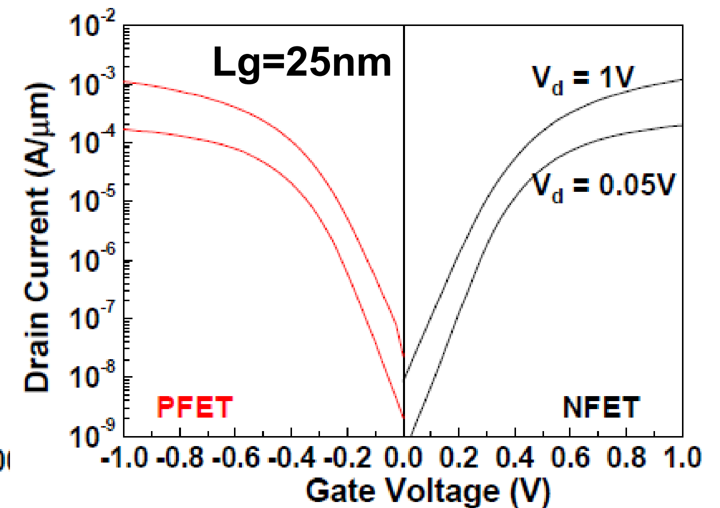


Wu – IEDM 2010

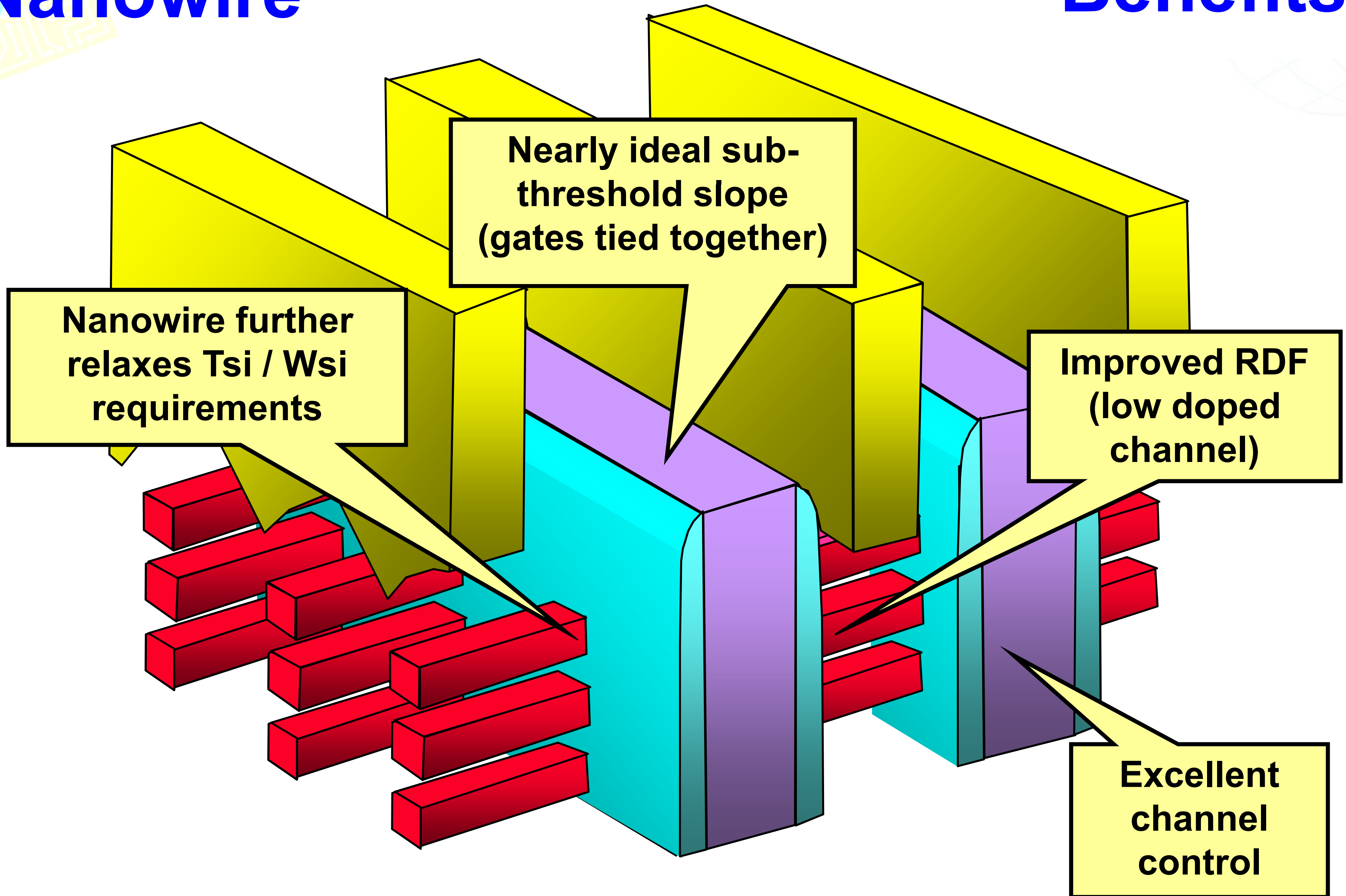


Weff = 2 x Fin_H + Fin_W

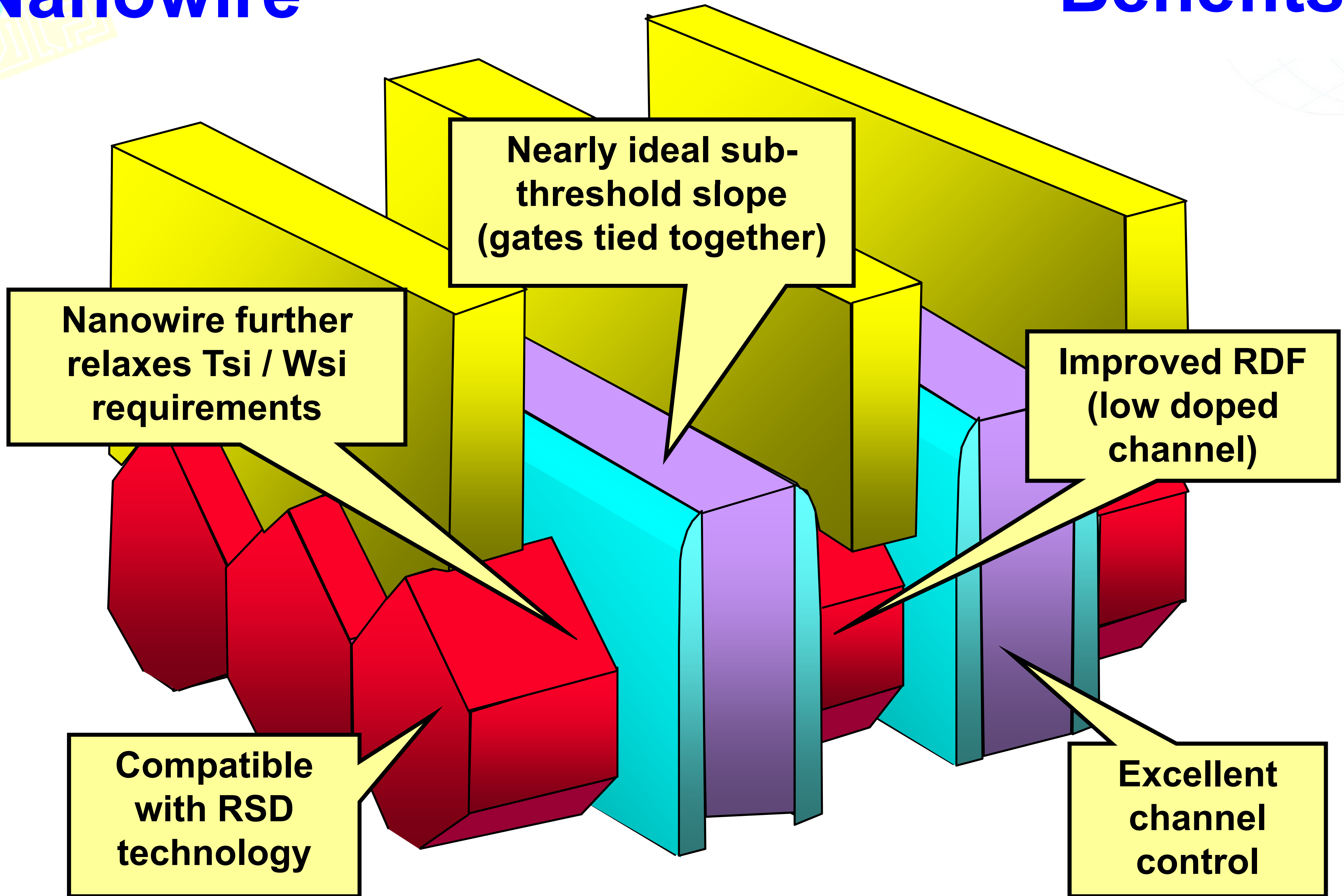




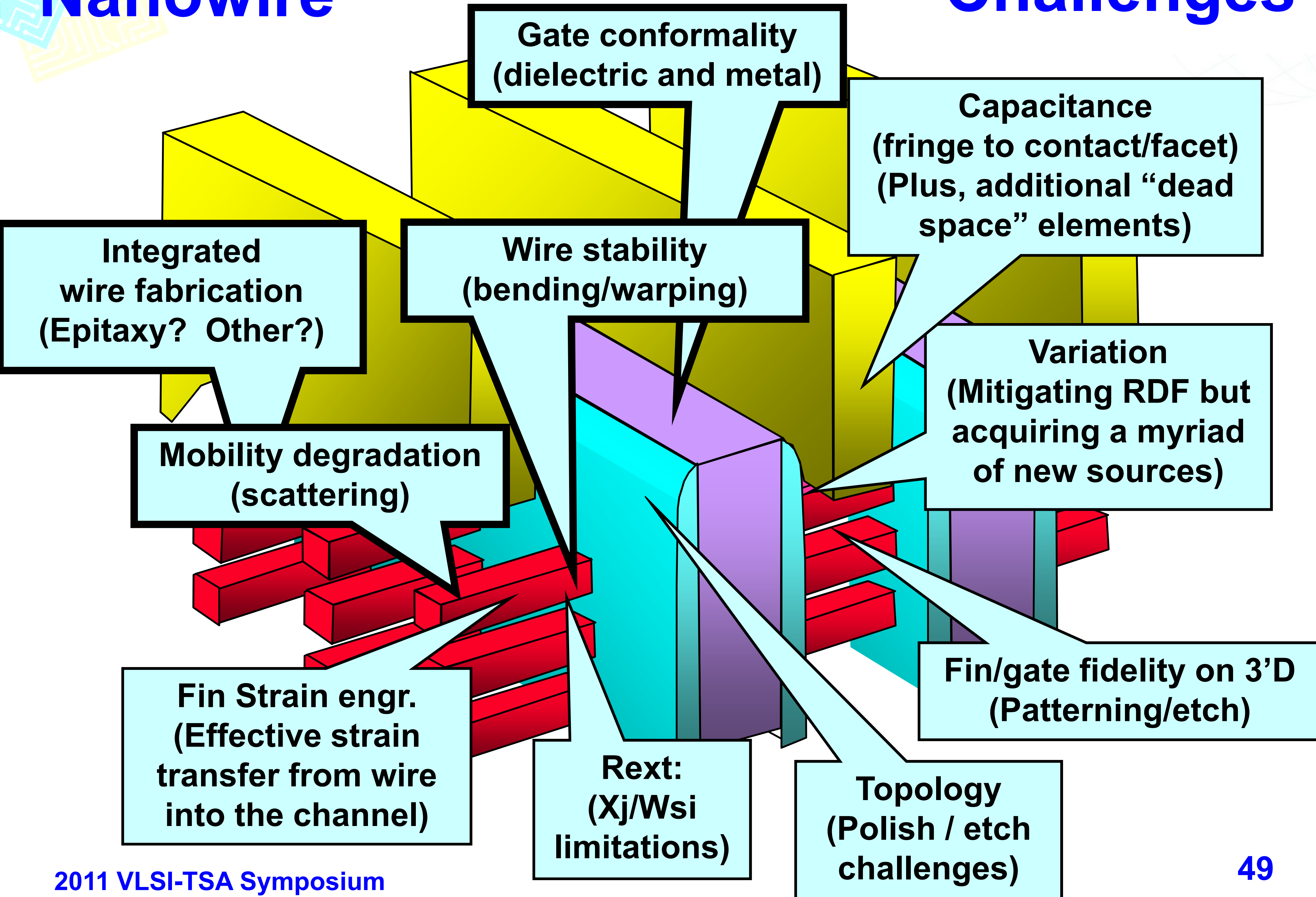
Nanowire Benefits



Nanowire Benefits

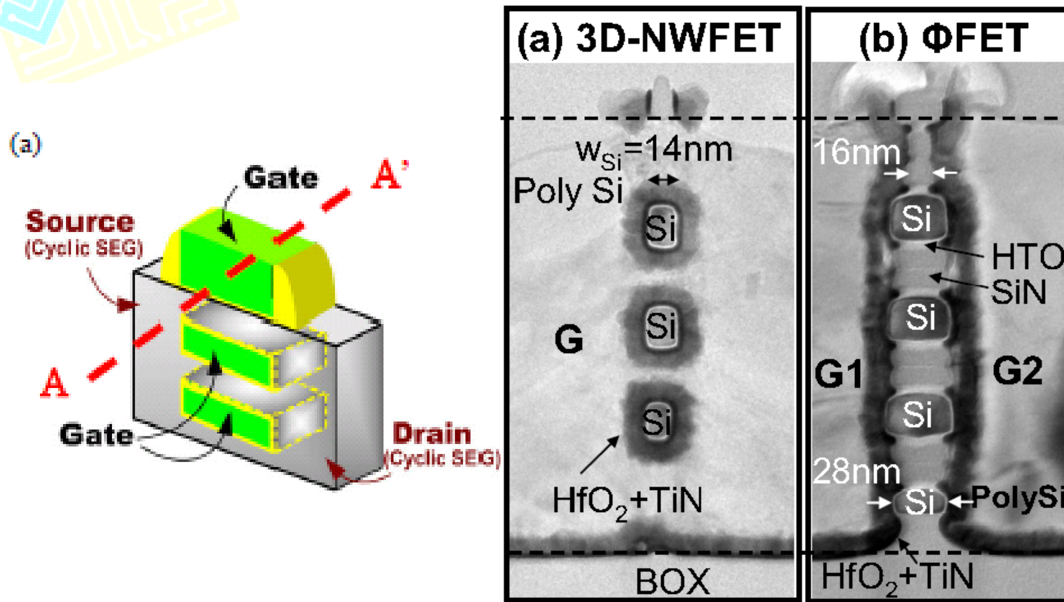


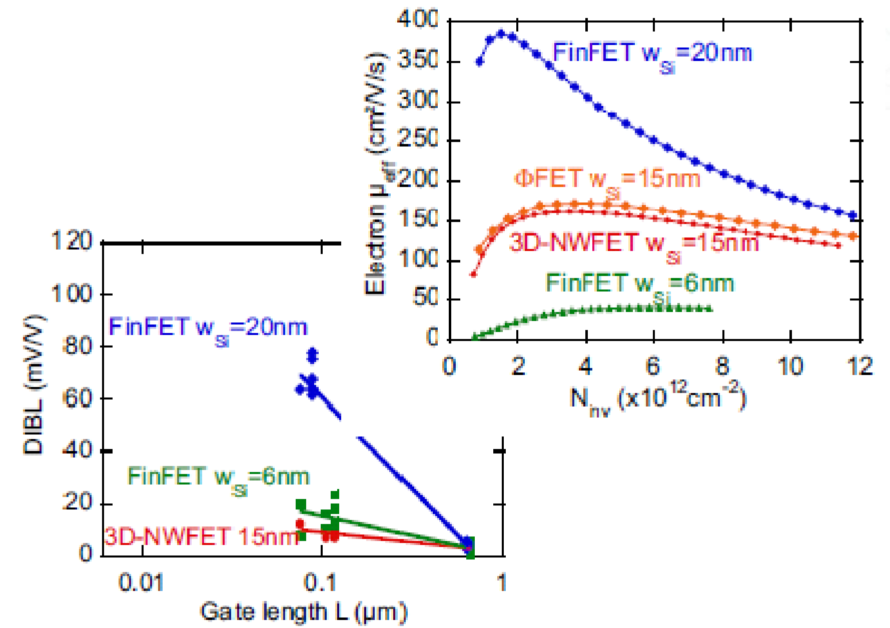
Nanowire Challenges



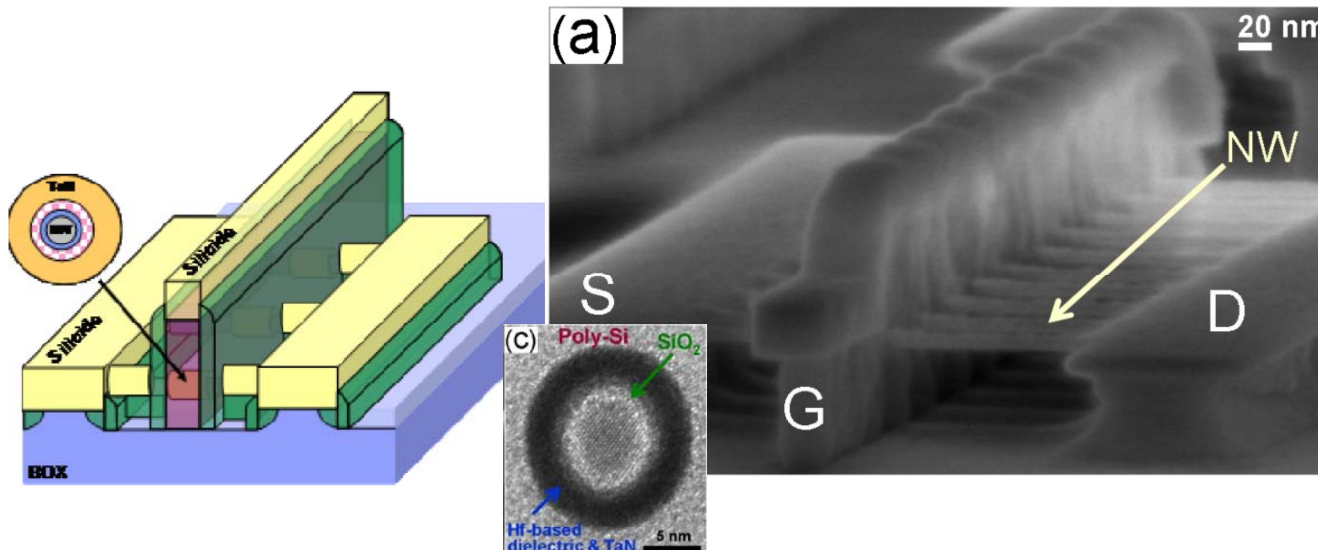
Nanowire FETs

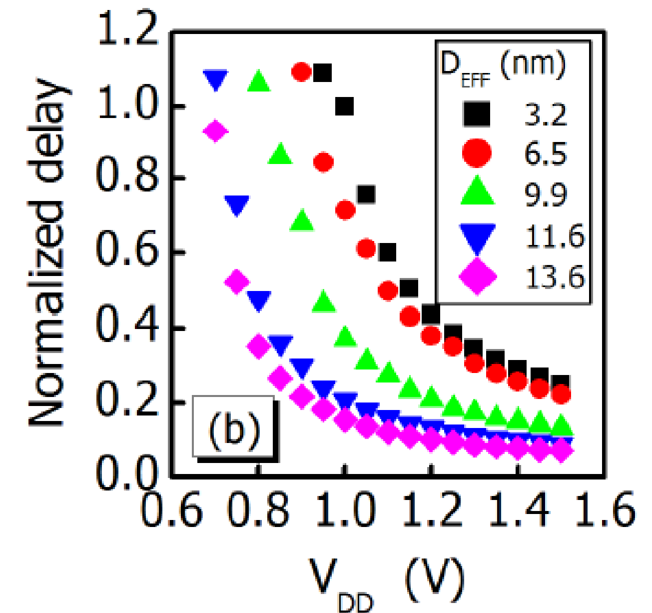
Dupre – IEDM 2008





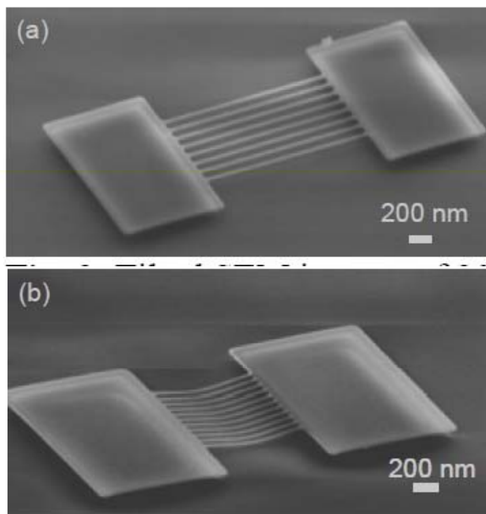
Bangsaruntip - IEDM 2009 / VLSI 2010

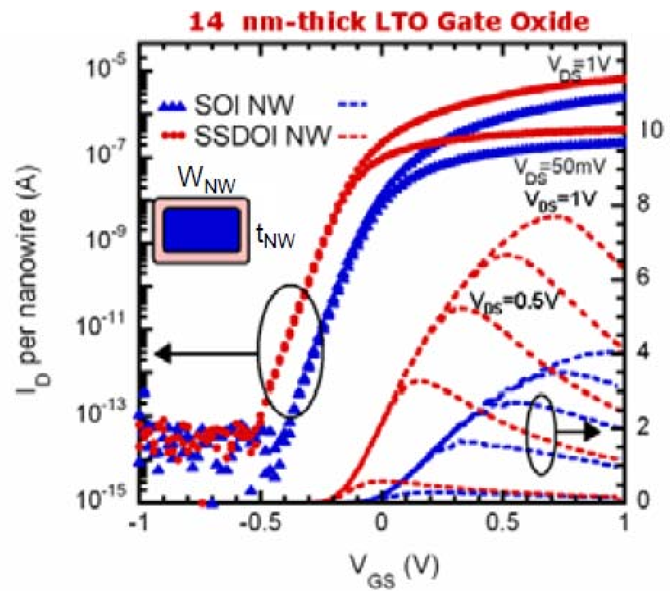


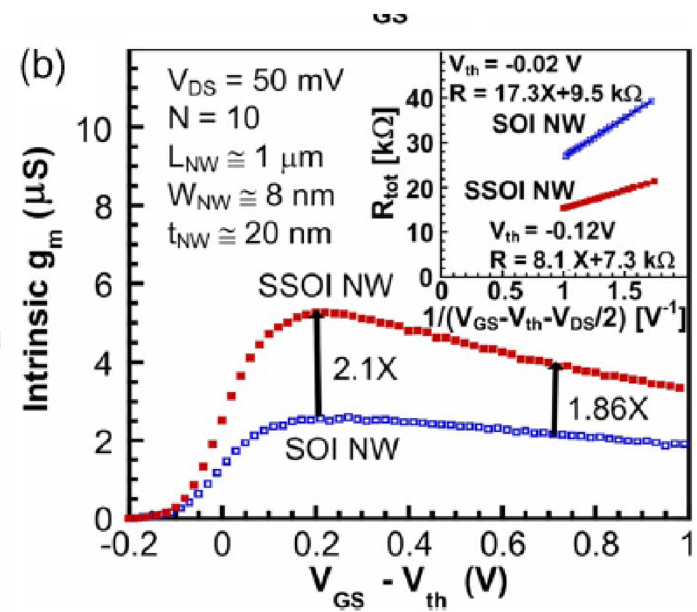


Nanowire FETs

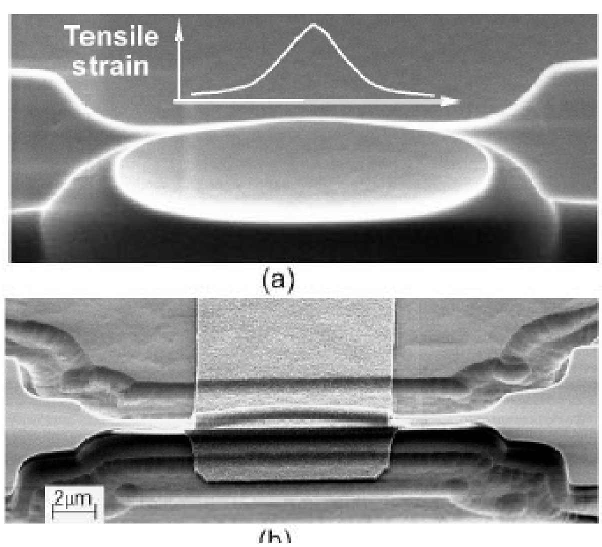
Hashemi/Hoyt
IEDM 2008 EDL/ESSDRC 2009

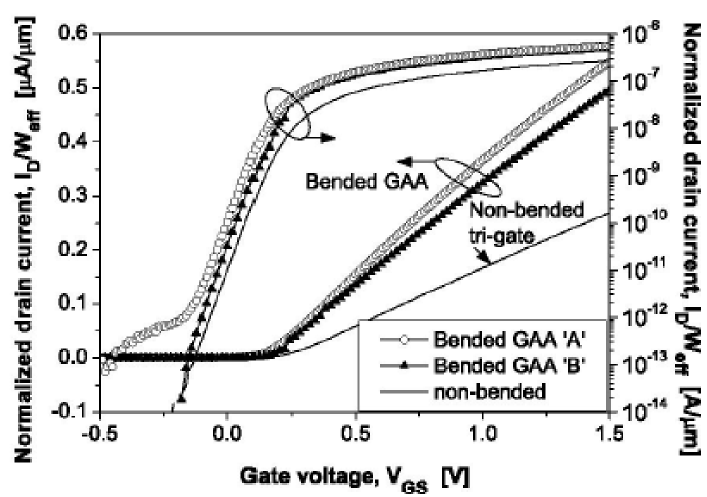


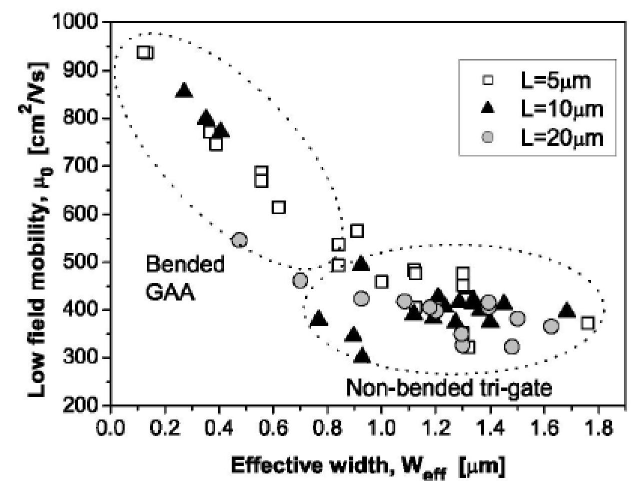




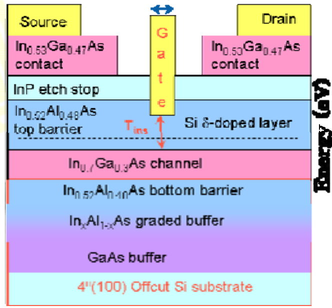
Moselund – IEDM 2007



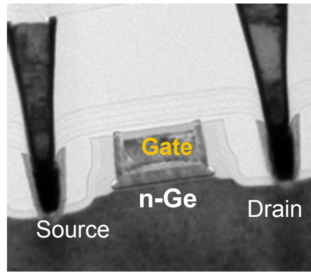




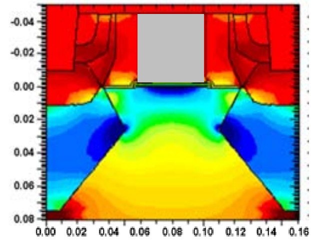
MOBILITY



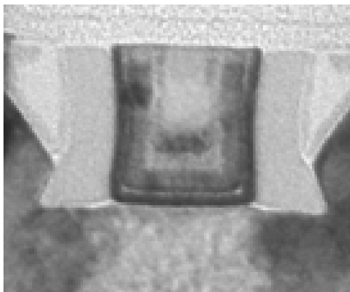
III-V



Ge



Strain



32nm

VLSI SINCE 1983

I/O
Cache
Core
Video
Display
Graphics
I/O

System-on-chip

System-in-package

STRUCTURE

UTB SOI

Fins

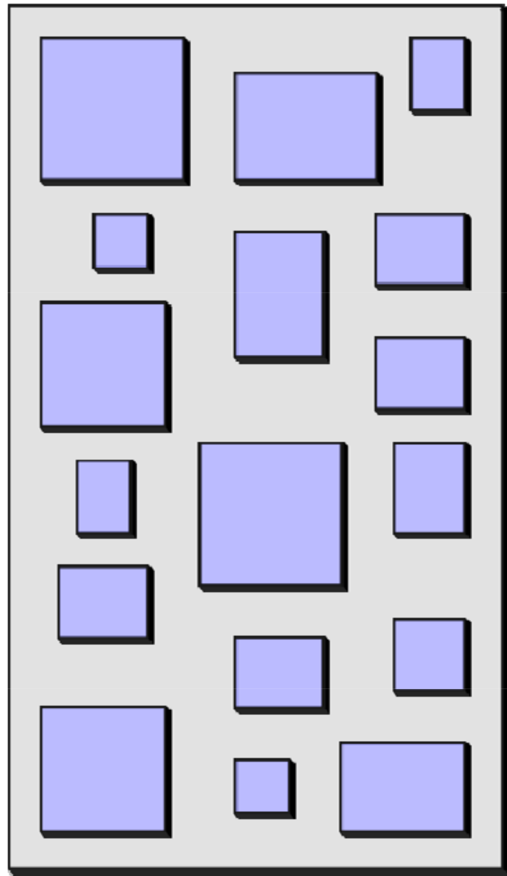
Wires/Ribbons

ELECTROSTATIC CONFINEMENT

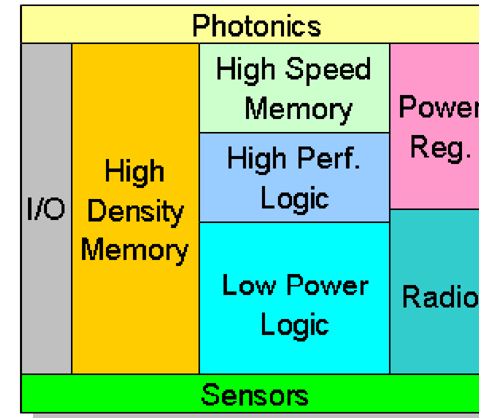
2011 VLSI-TSA Symposium

System Integration

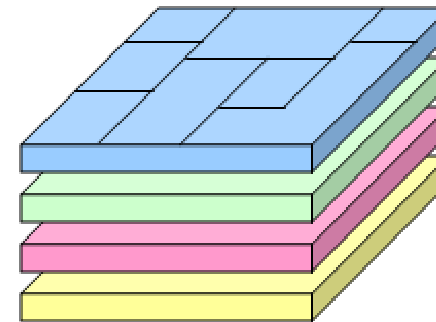
Discrete ICs



2-D Integration (SoC)



3-D Integration

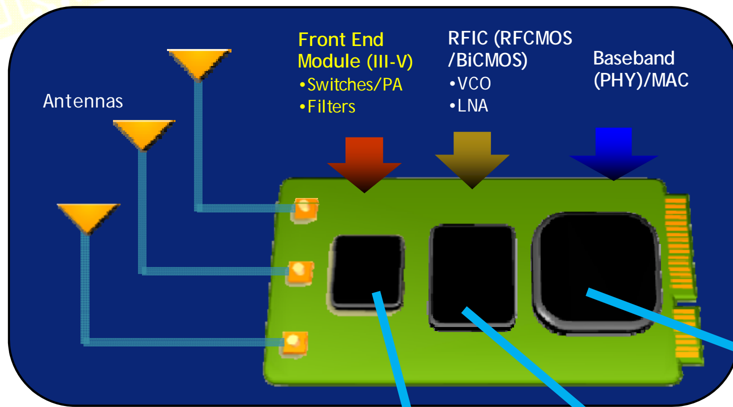


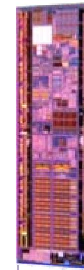
Logic
Memory
Power
Reg.
Radio
Sensors
Photonics

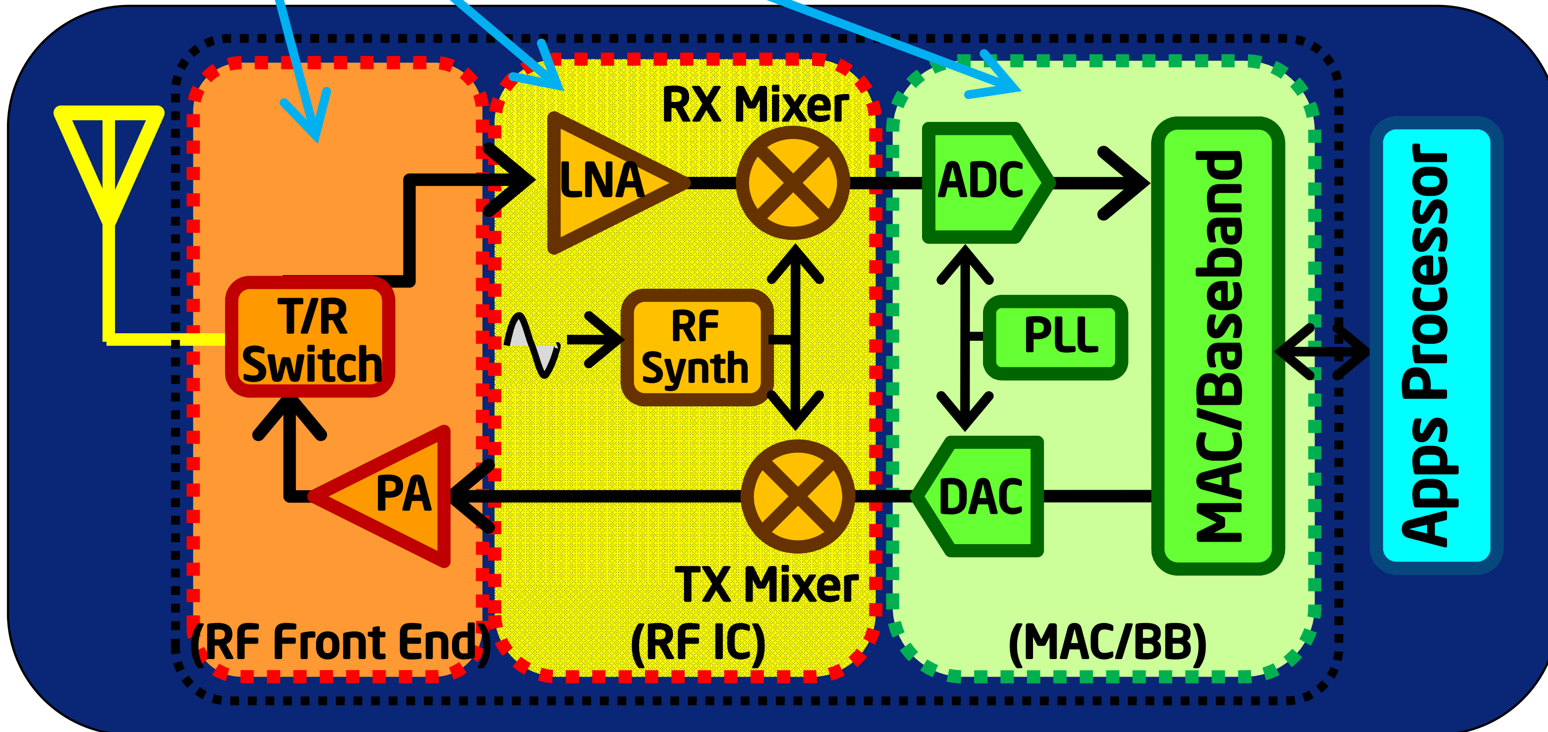
M. Bohr – Stanford 2011

System integration needed for performance, power, form factor
Challenge is to integrate wider range of heterogeneous elements

The Vision of RF SOC



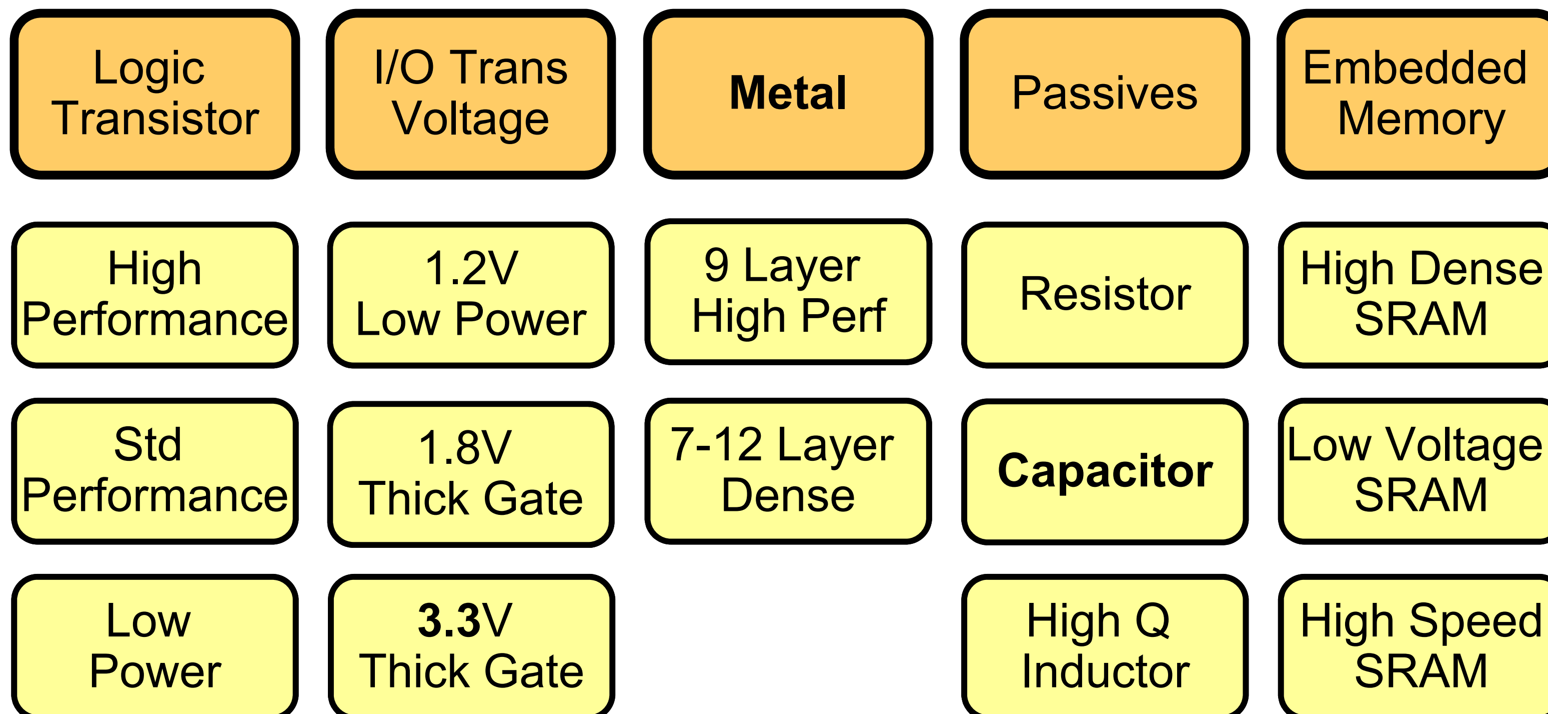




Full integration of RF components into monolithic silicon chips

C.-H. Jan – IEDM 2010

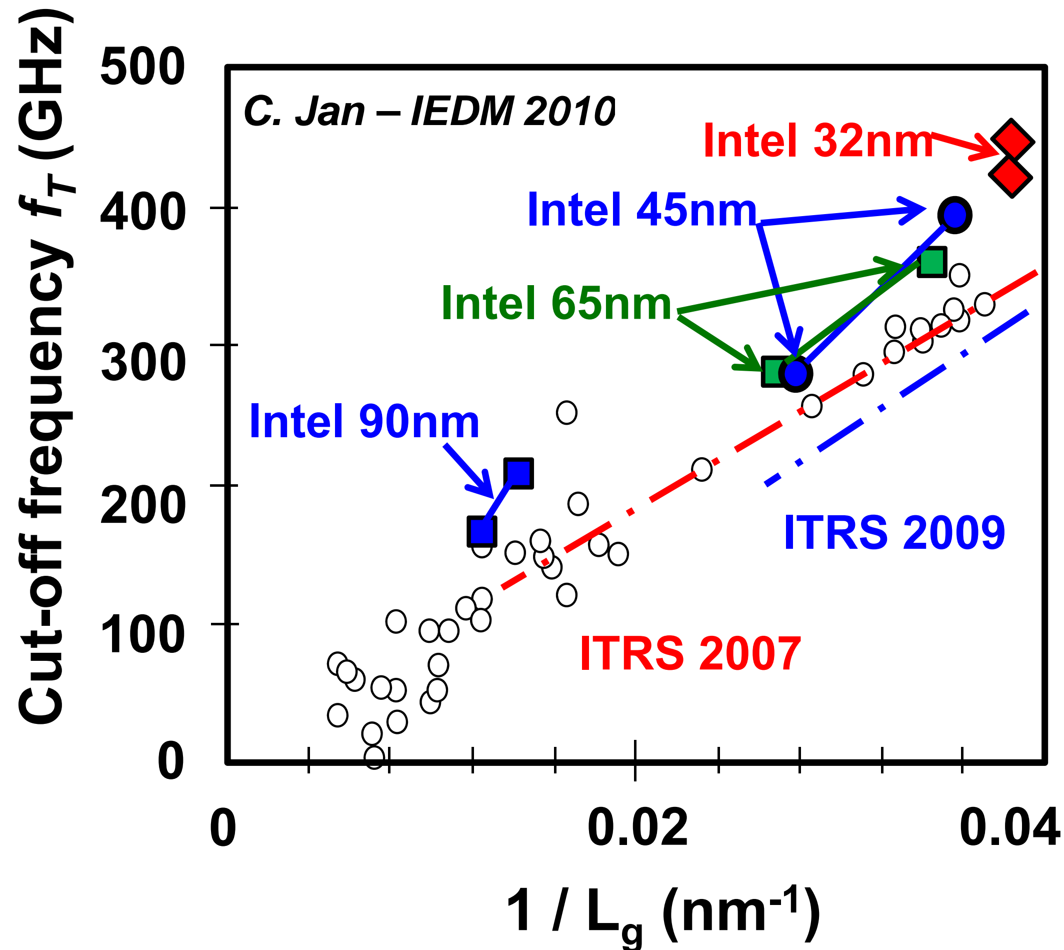
32 nm SoC Process Features



M. Bohr – Stanford 2011

Intel’s 32 nm SoC process
Illustrates the breadth of an SoC feature set

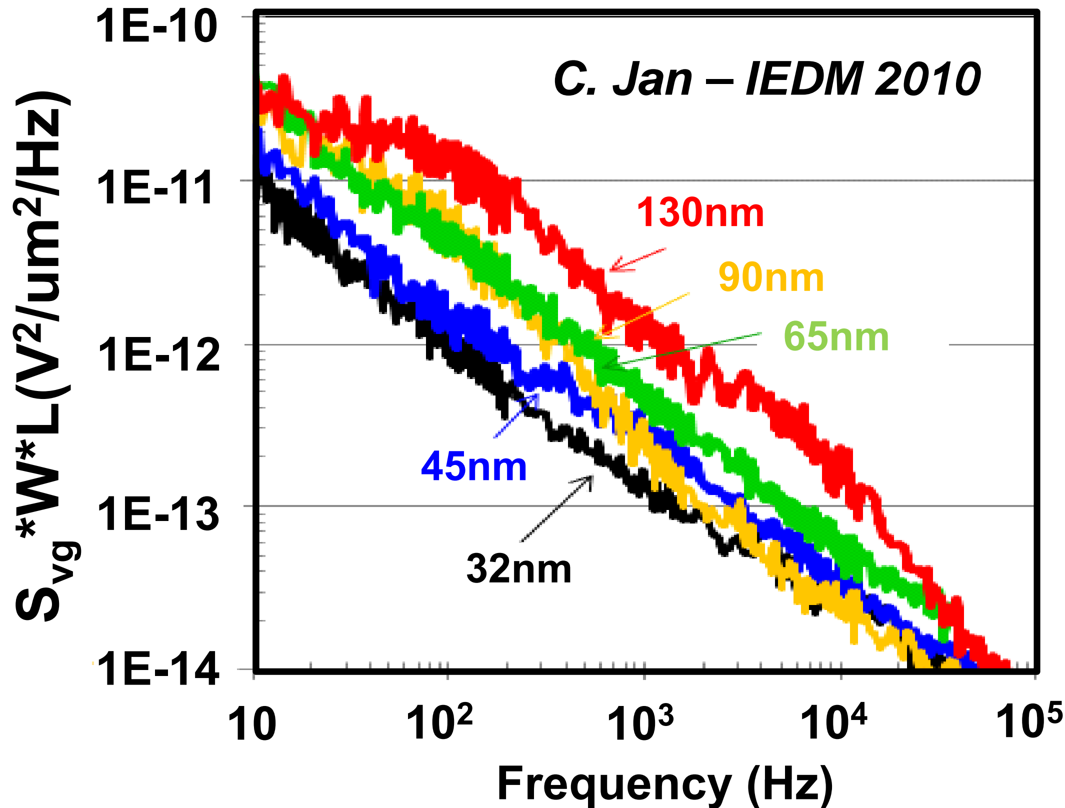
CMOS: A critical platform for for RF SoC integration



CMOS competitive with III-V for some applications, 32nm peak f_T ~ 445 GHz

C.-H. Jan – IEDM 2010

CMOS: A critical platform for for RF SoC integration

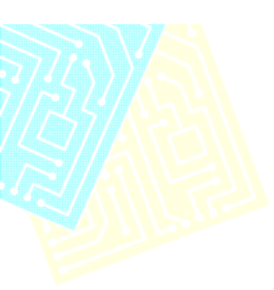


$$S_{vg} \cdot W \cdot L = \frac{S_{id}}{g_m^2} \cdot W \cdot L = \frac{K}{f} \frac{1}{C_{ox}^2}$$

- 10x *1/f* flicker noise improvement on five nodes
- Benefits from *Cox* scaling enabled by high-k
- Critical for phase noise and other mixed signal designs

Flicker noise not degraded by HiK/MG Transition

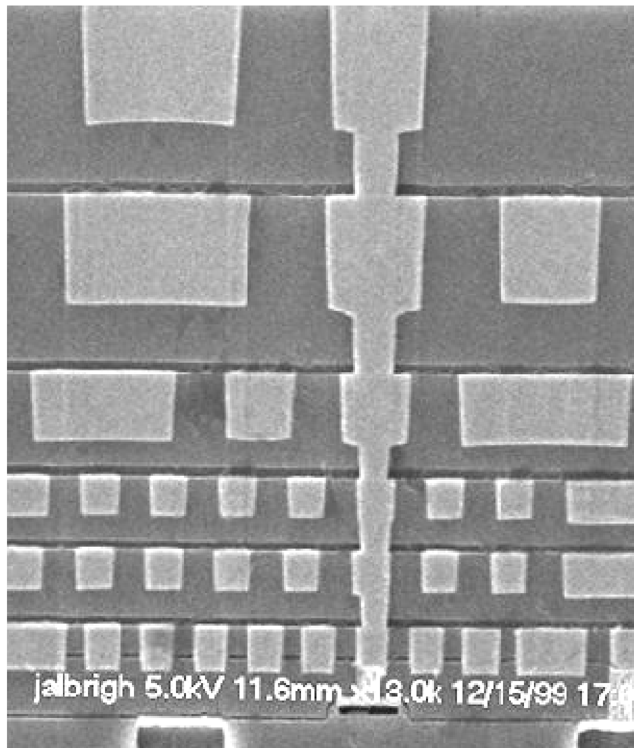
C.-H. Jan – IEDM 2010



VLSI SINCE 1983

SOC and Interconnect

0.13 um 6 layers



Polymer

4.5 um

TM1
(Thick Metal)
Cu

32 nm 8 layers

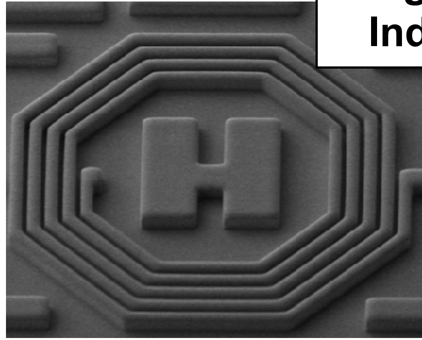
M1 – M8
Interconnects

Thick metal improves the quality of RF passives

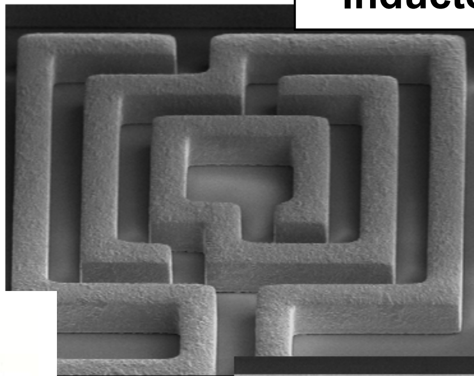
C.-H. Jan – IEDM 2010

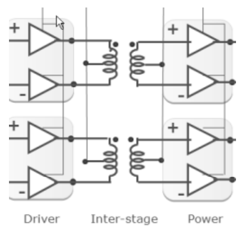
Inductors Enabled by Thick Metal

Single End Inductor

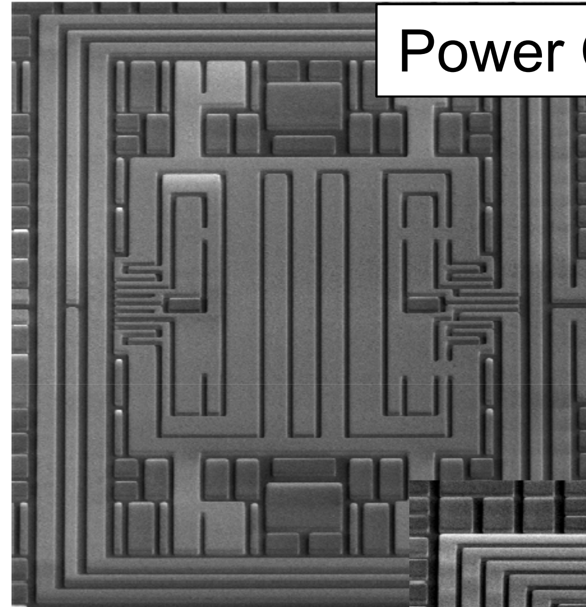


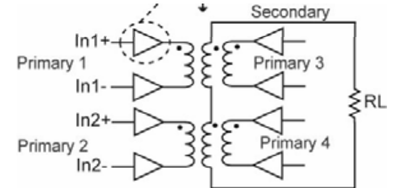
Differential Inductor

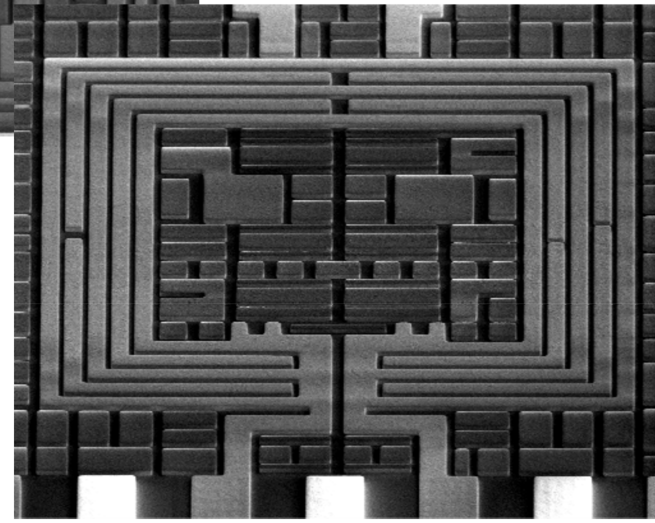


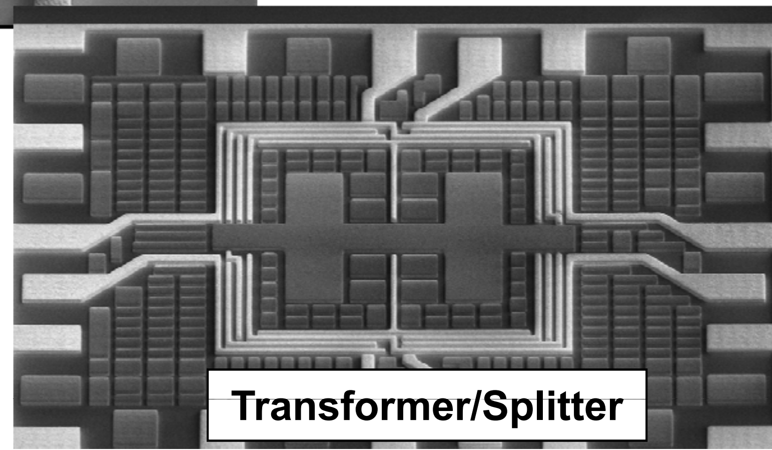


Power Combiner



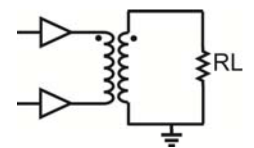






Transformer/Splitter

Balun



C.-H. Jan – IEDM 2010

Vertical Architectures

Benefits

Vertical orientation may enable new circuit concepts

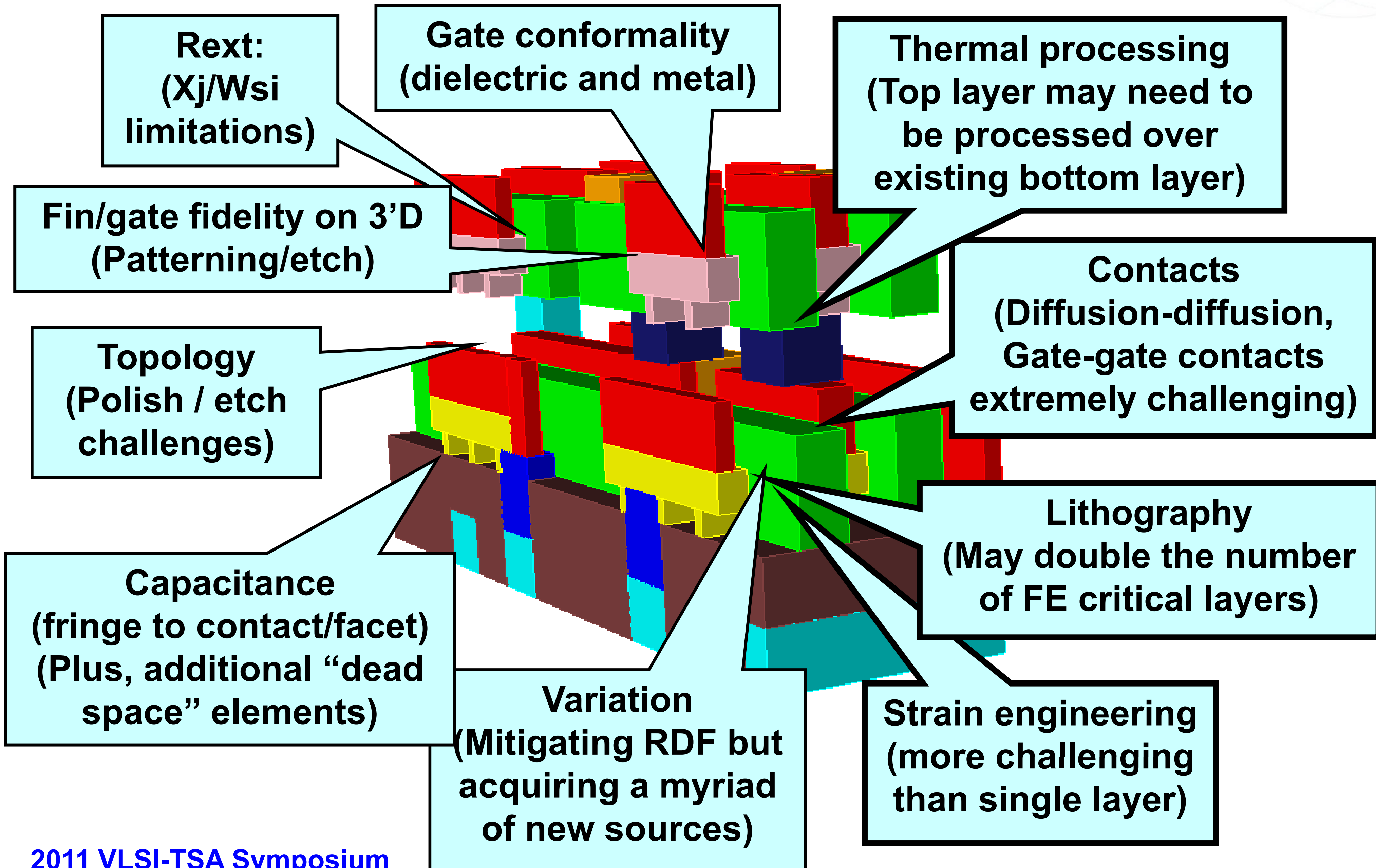
50% reduction in "plan view" density

Possibility for different N/P materials/orientations

Reduced vertical interconnect capacitance

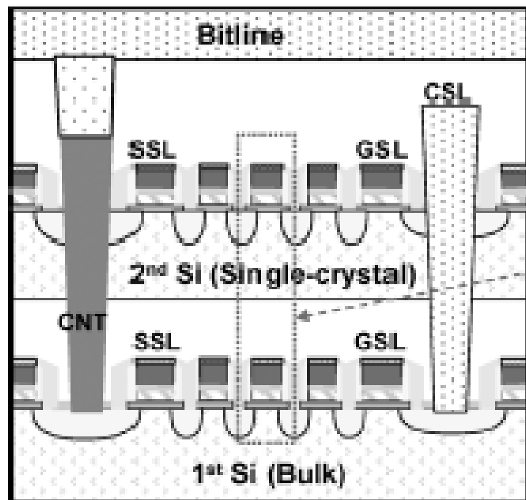
Vertical Architectures

Challenges



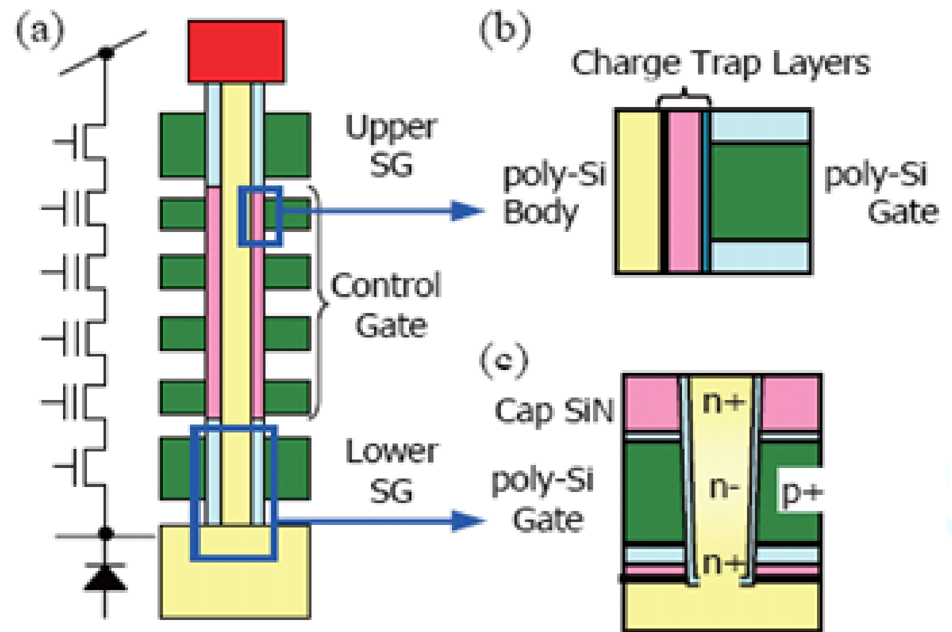
3D NAND

Deck-by-Deck - Planar NAND + SOI



K-T Park, et al. Solid State Ckt 2009

Vertical NAND - Vertical Pillar with Surround Gate Structure

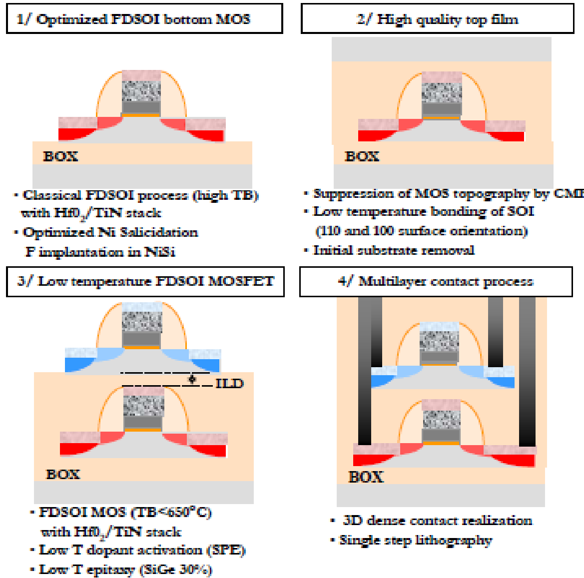


H.Tanaka, et al. VLSI Tech Dig 2007

Two categories of 3'D NAND: – Deck by Deck and Vertical

Vertical

Batude – IEDM 2009 – stacked 110/100



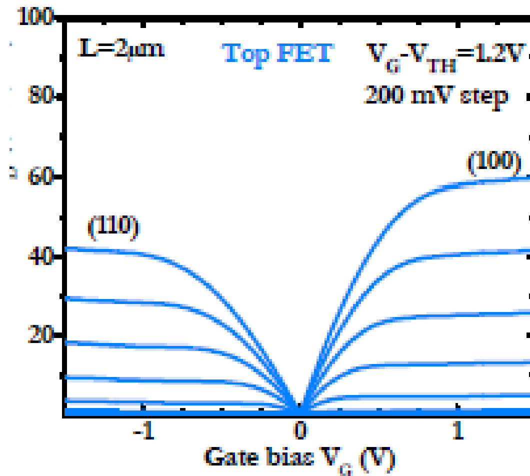


Fig.15: ID-VD characteristics of top FET

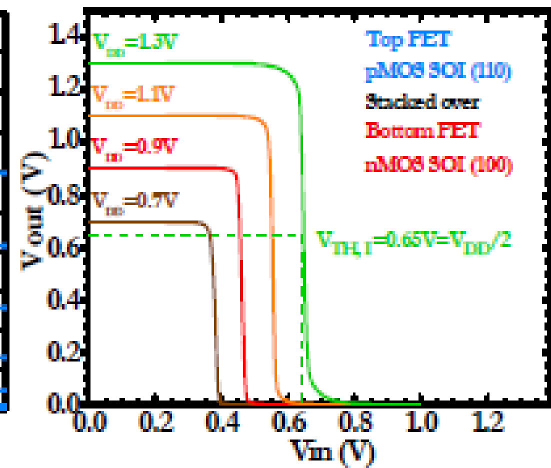
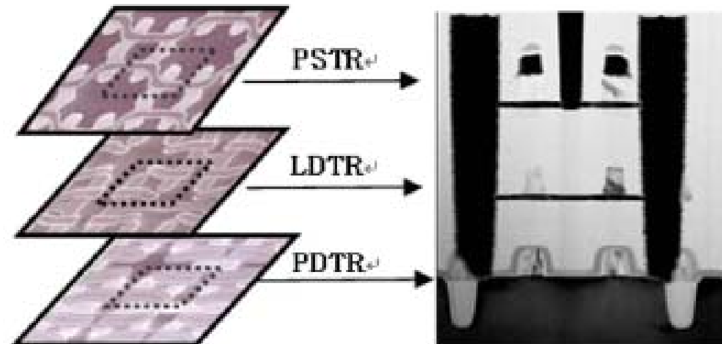
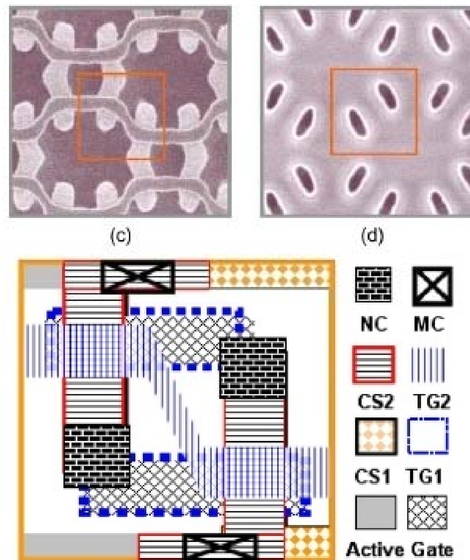
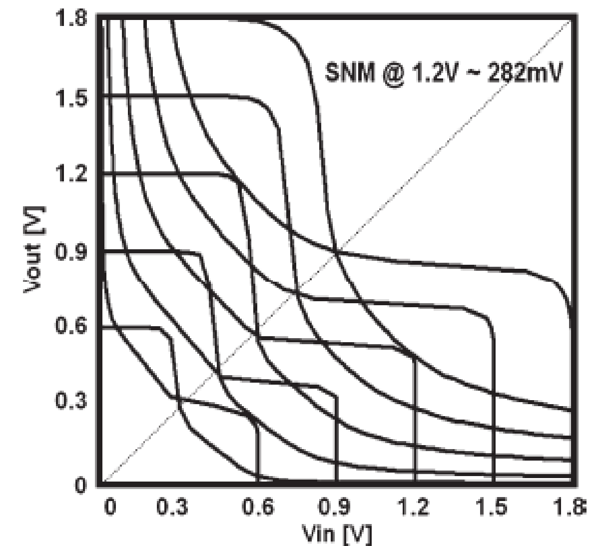


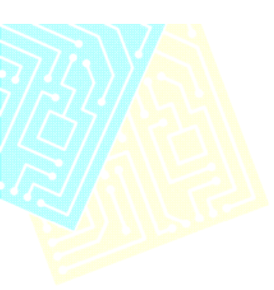
Fig.16:Transfer Voltage characteristic of an inverter: top SOI (110) pFET and bottom SOI (100) nFET

Jung – IEEE TED 2010 – 3'D stacked 6T





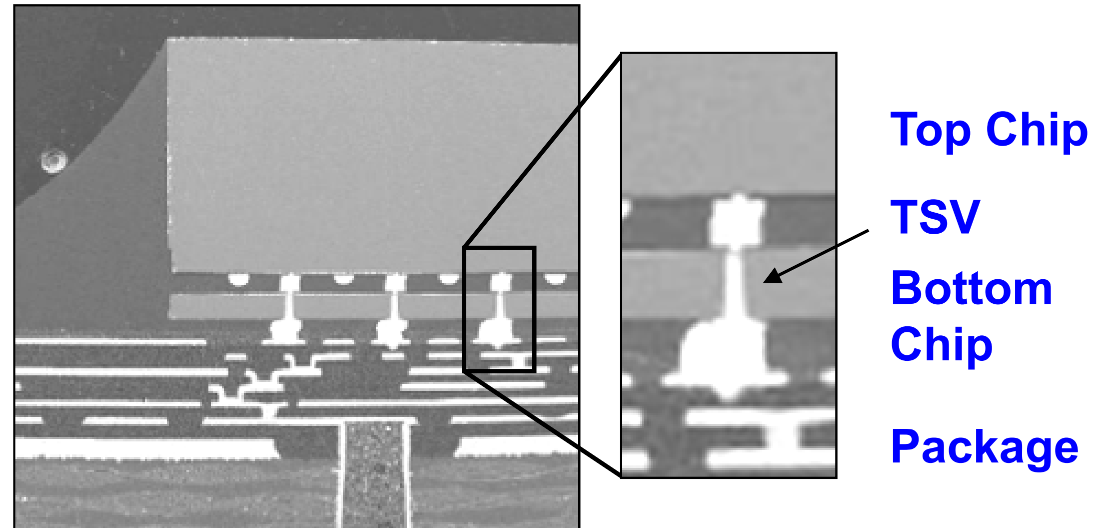




System-in-Package
3'D Chip Stacking

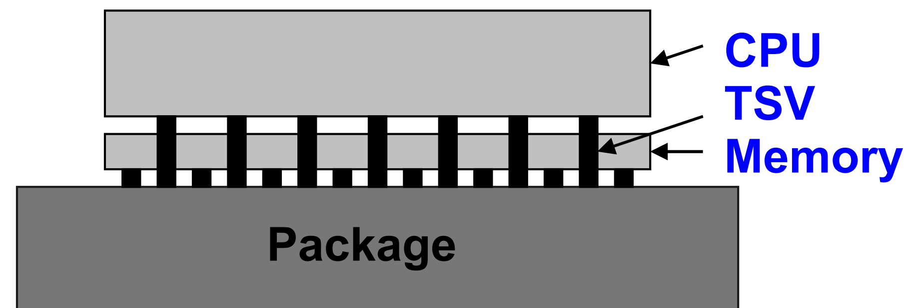
BENEFITS:

- High density chip-chip connections
- Small form factor
- Combines dissimilar technologies



CHALLENGES:

- Added cost
- Degraded power delivery, heat sinking
- Area impact on lower chip



M. Bohr – Stanford 2011

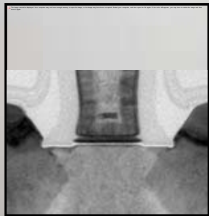
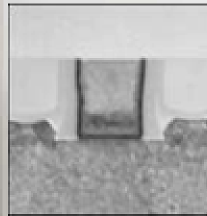
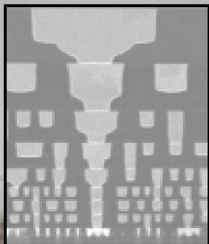
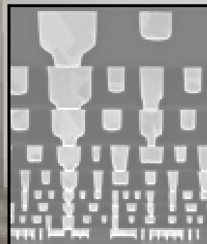
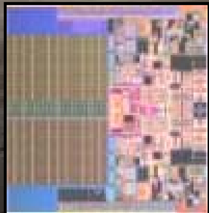
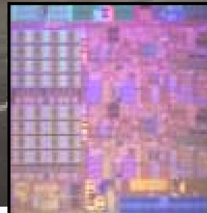
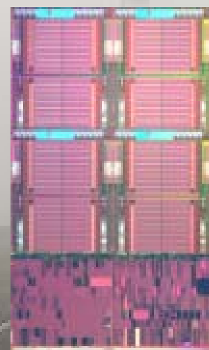
3-D chip stacking using through-silicon vias

Limit to visibility remains ~ decade

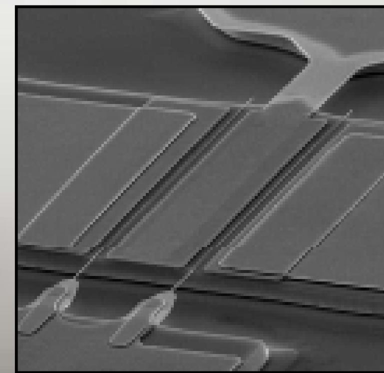
TECHNOLOGY GENERATION

45nm	32nm	22nm	14nm	10nm	7nm	Beyond
2007	2009	2011	2013	2015	2017	2020

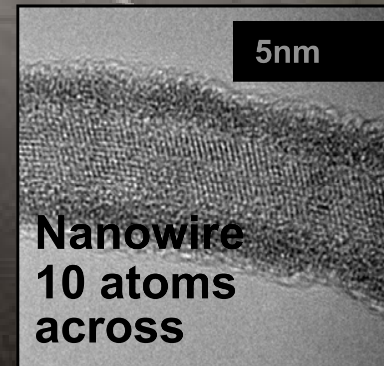
MANUFACTURING | DEVELOPMENT | RESEARCH

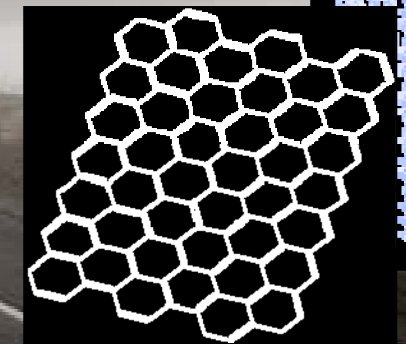
Not to scale



QW III-V Device



Carbon
Nanotube
~1nm diameter



Graphene
1 atom thick