Moore's Law past 32nm:
Future Challenges in Device Scaling

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Intel Corporation

Agenda

- History
- Architecture
- Capacitance
- Resistance
- HiK-MG
- Orientation
- Strain
- Strain + Orientation
- Summary

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- **History**
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Lithography Scaling Limitations
From Broers [1] IEDM Plenary Session 1980

In the limit, microscope objectives with 0.95 N.A. are available and, provided very small fields (200μ x 200μ) are adequate, linewidths < 0.4μ should be achievable under carefully controlled laboratory conditions, and in very thin resist layers.

Depth of field will be reduced to about ± 0.2μ. Deep U.V. (λ = 200nm - 260nm) lenses will be difficult to build because of the lack of materials that are transparent at these wavelengths and yet have relatively high refractive indices.

1980:
Optical Lithography Limit
~ 400nm

Transistor Scaling Limitations
From Meindl [2] IEDM Plenary Session 1983

For conservative design margins, typical results suggest that IGFET channel lengths can be reduced to approximately 0.40 microns in E/D NMOS logic gates; 0.30 microns in CMOS transmission gates; and 0.20 microns in E/E CMOS logic gates. Smaller channel lengths can be projected for more aggressive designs. The dominant mechanism imposing these limits is subthreshold drain current due to short channel charge sharing and drain induced barrier lowering.

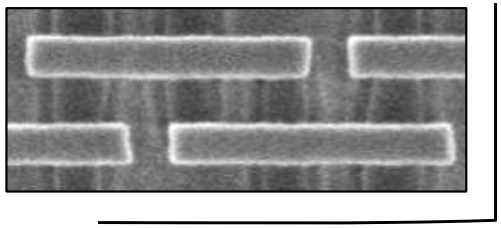
1983:
Transistor architecture limit
200-400nm (SCE)

Transistor Scaling Limitations
From Heilmeier [4] IEDM Plenary Session 1984

other factors limiting the scaling of ICs come into play. Some of these factors are interconnect capacitance, channel capacitance, interconnect resistance, parasitic resistances, velocity saturation, ionizing radiation, drain breakdown, gate oxide breakdown, hot carrier injection, subthreshold current, punch through, and statistical control of oxide thickness and channel doping. It appears that minimum geometries for high-volume ICs will saturate in the range of 0.3 to 0.5 microns.

1984:
Transistor architecture limit
300-500nm (laundry list of reasons…)

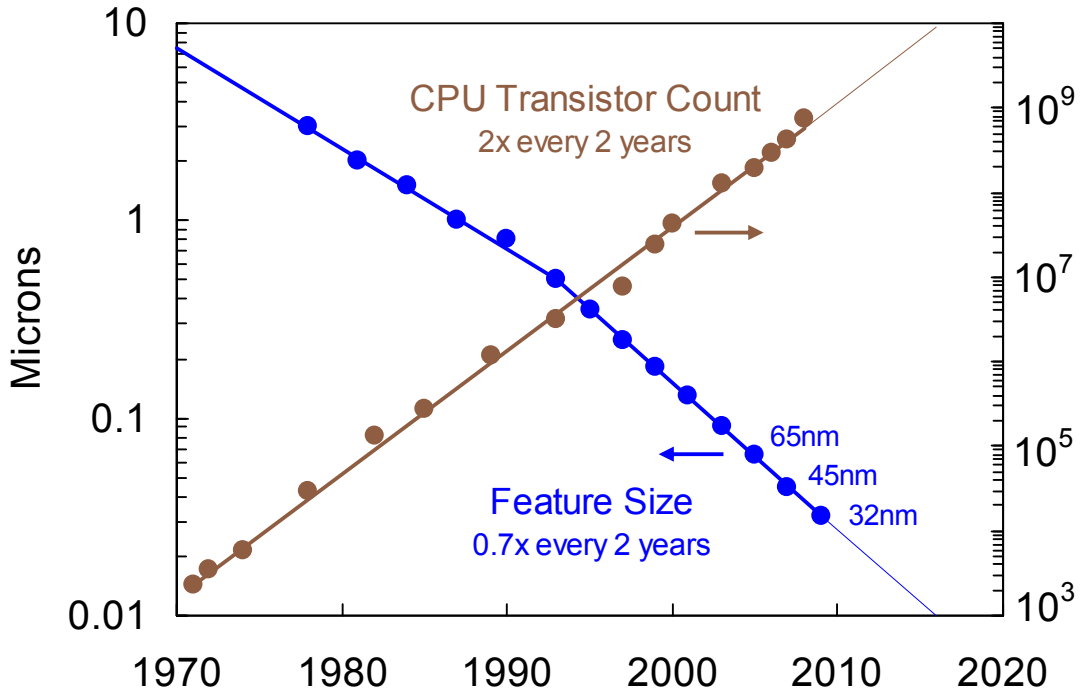
Moore's Law Scaling



~300nm

~500nm

1983-84 limits on gate size, are commensurate with the dimensions of 2008's entire 32nm SRAM cell!

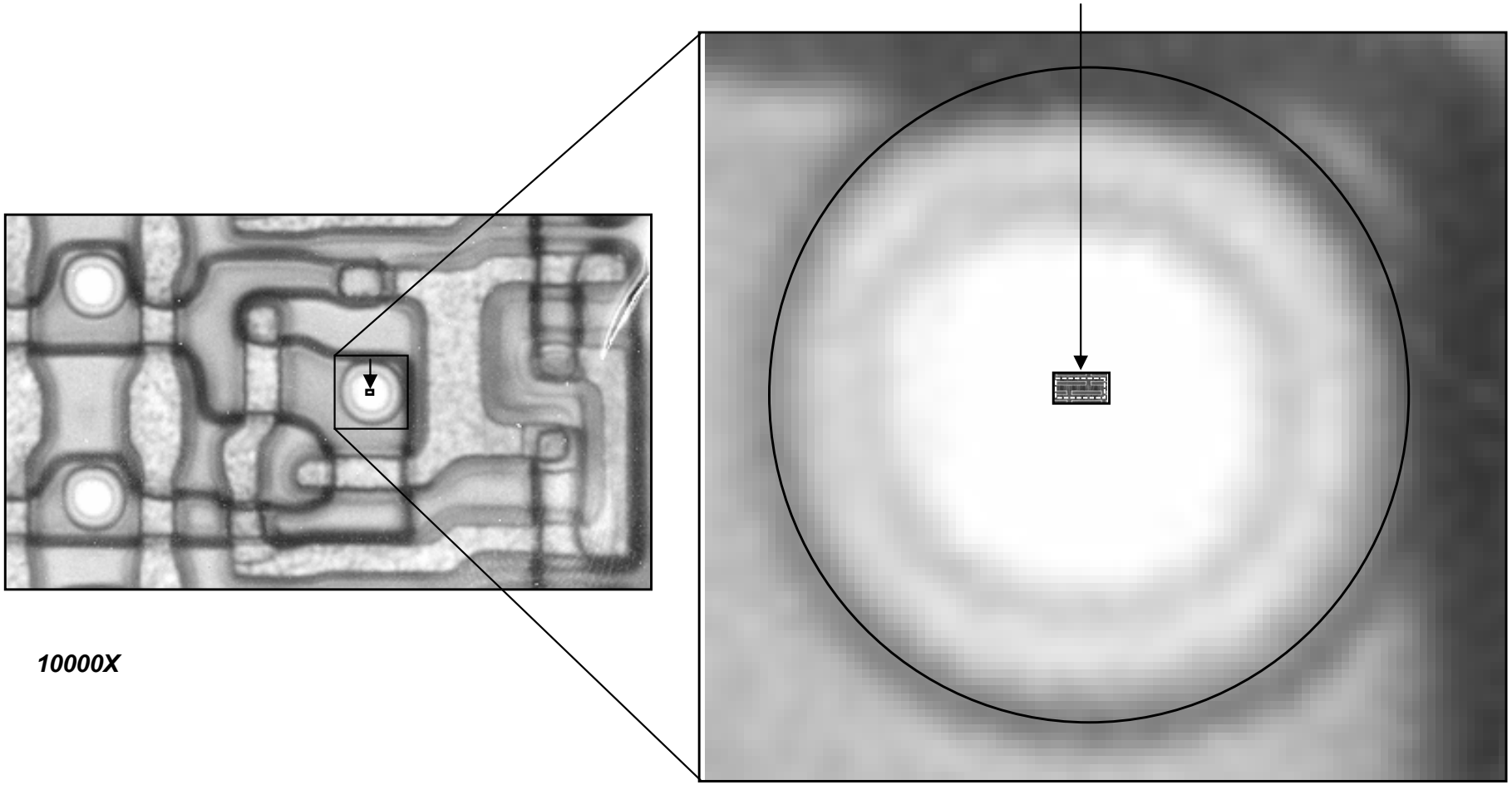


Transistor dimensions scale to improve performance, reduce power, and reduce cost per transistor

1980 to 2008

1980 SRAM Cell: 1700 um^2

32nm SRAM Cell: 0.171 um^2

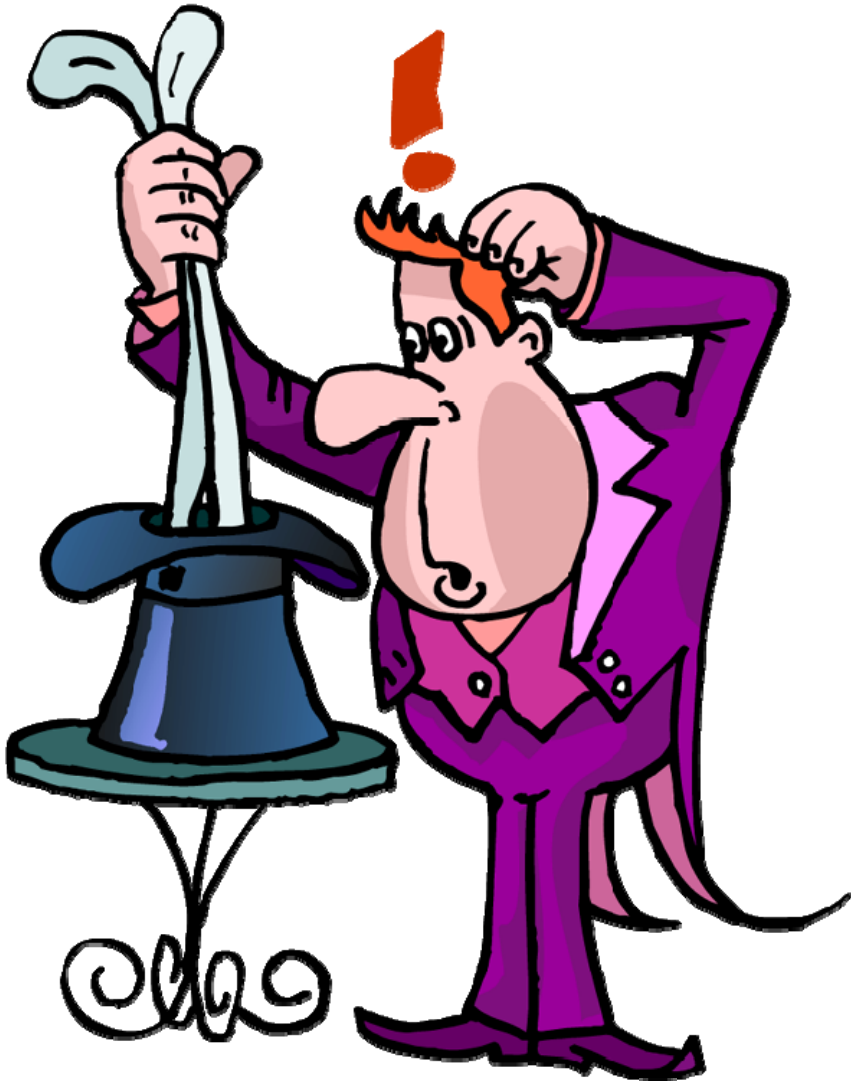


10000X

A 2008 32nm SRAM cell is dwarfed by a 1980 SRAM cell CONTACT

M. Bohr 2007

Agenda



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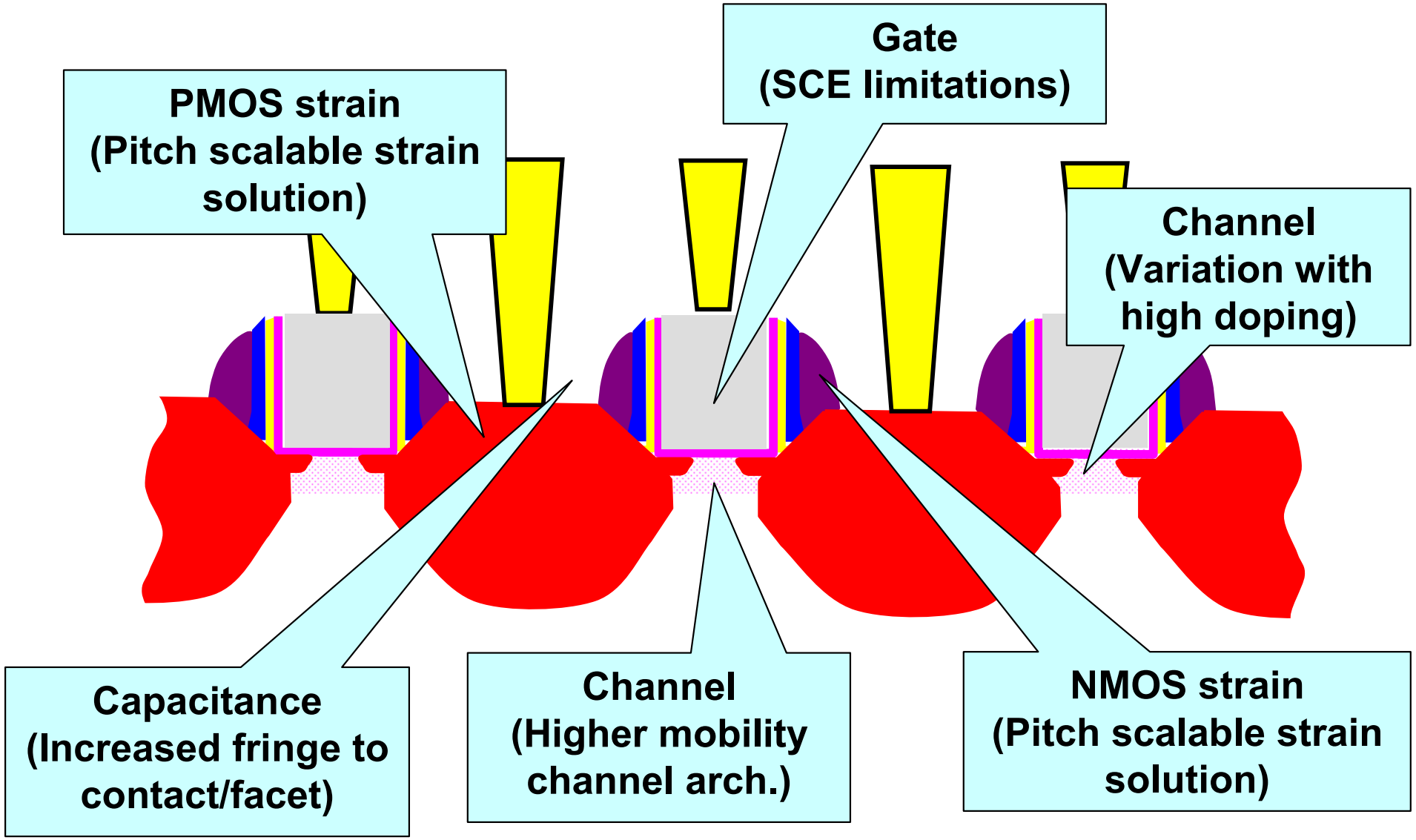
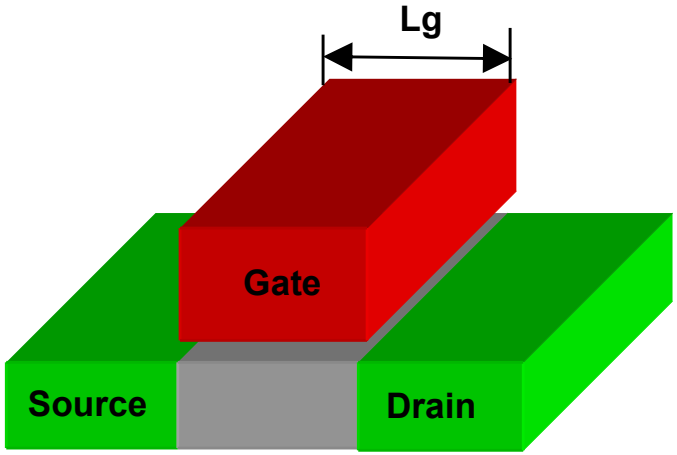
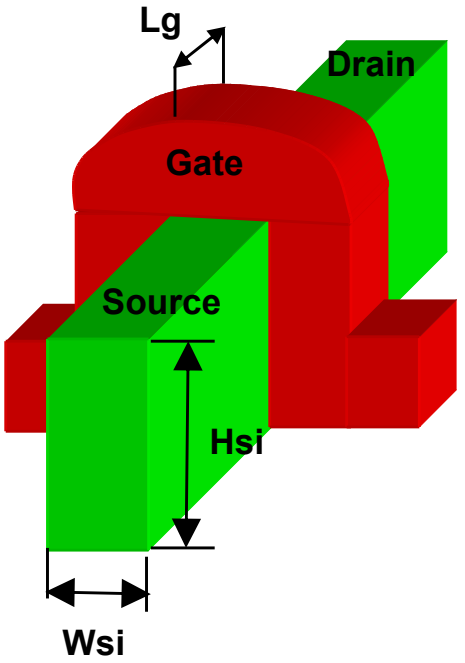
Planar Challenges



Electrostatics Benefit



Conventional Planar FET

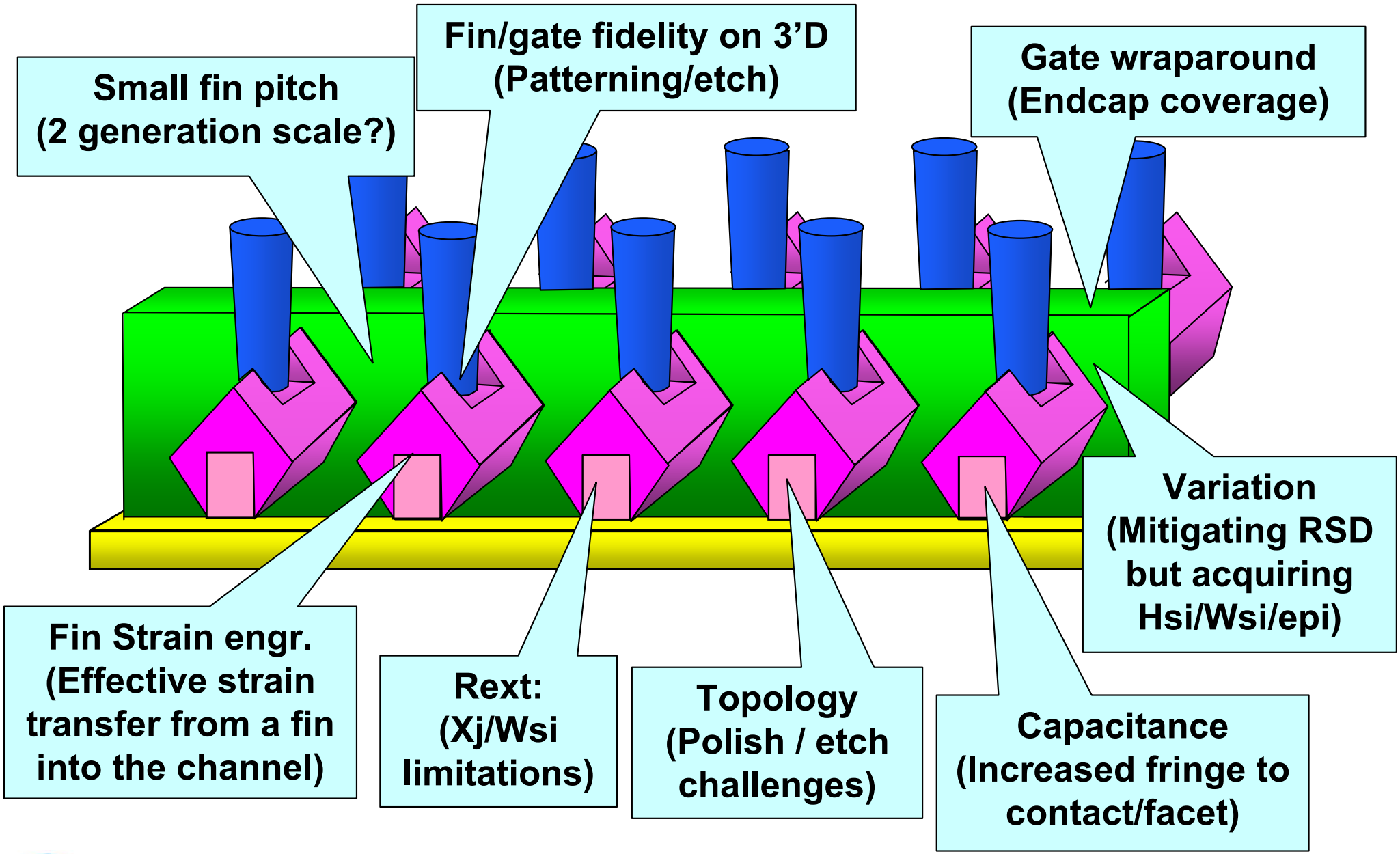


MuGFET

MuGFET electrostatics allows either:

1) Lg Scaling (support smaller Leff at same Ioff)
2) Vg-Vt scaling (support smaller Vt at same Ioff)

Additional MuGFET Challenges



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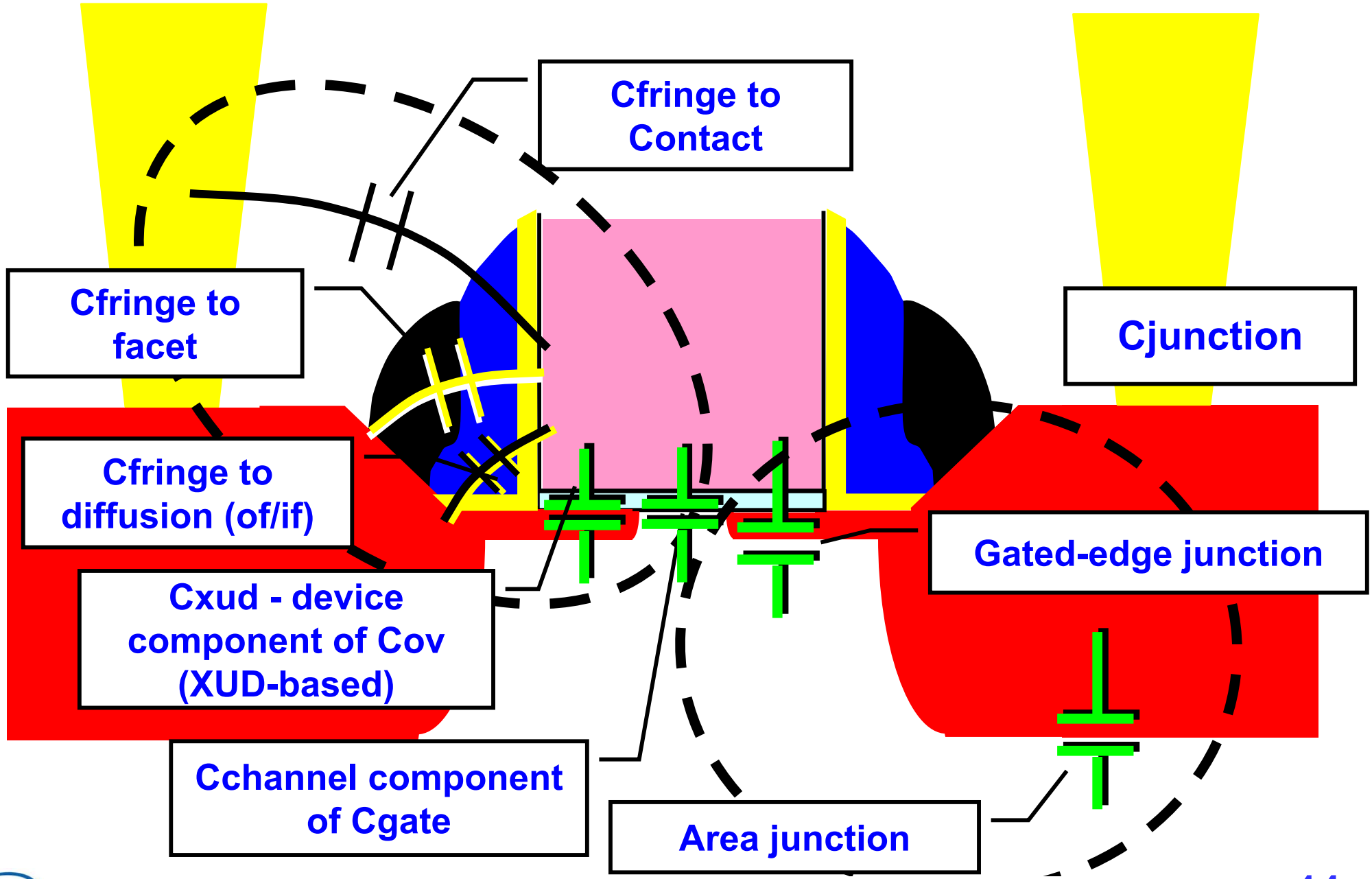
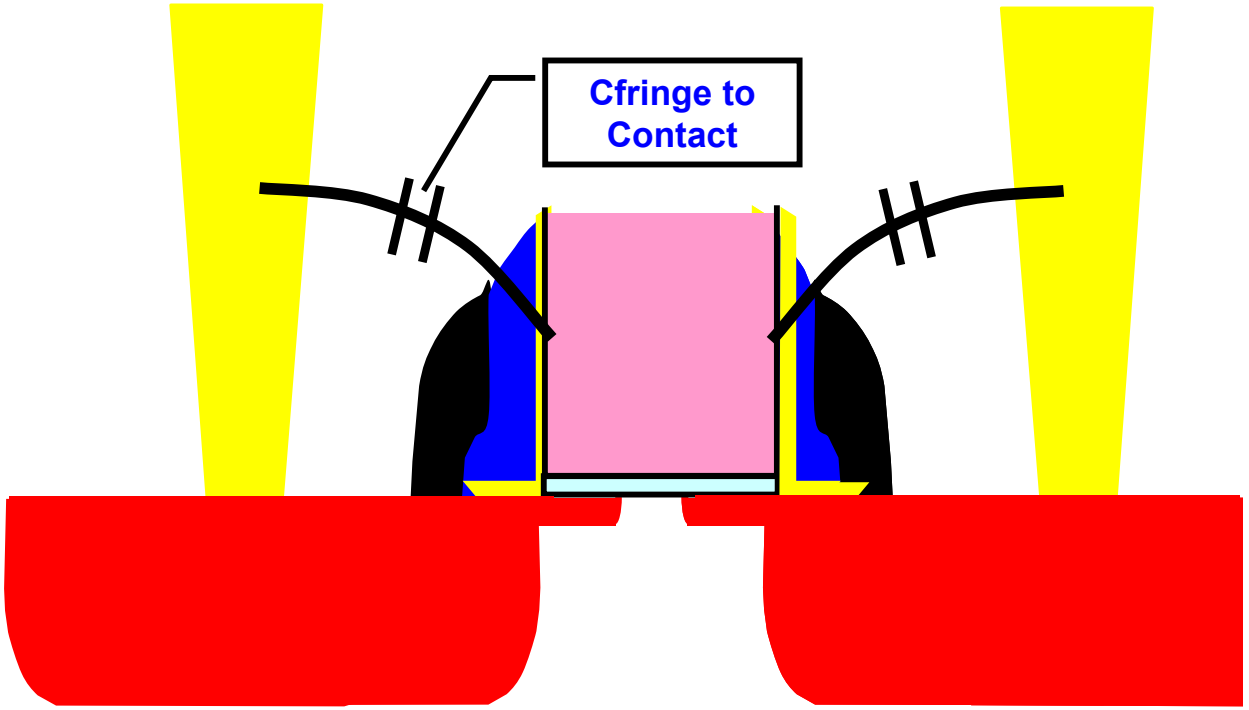
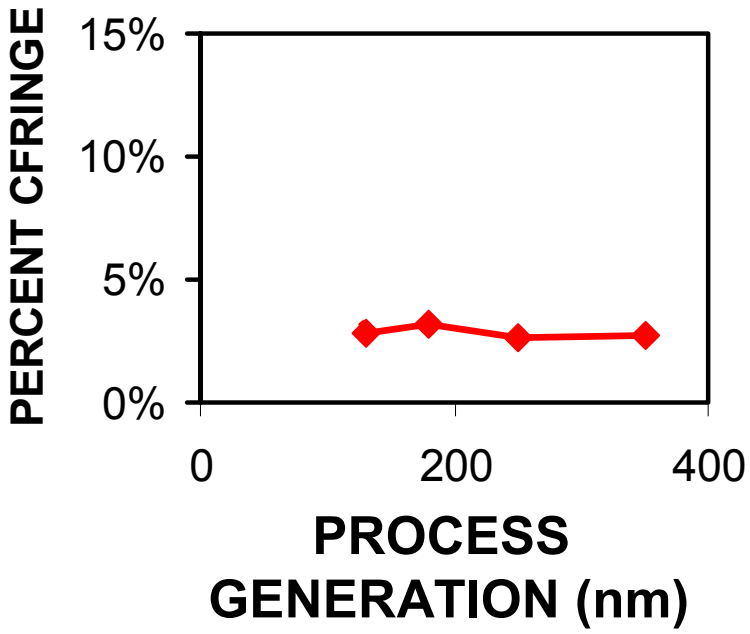
Planar Capacitive Elements



K. Kuhn – IEDM 2008

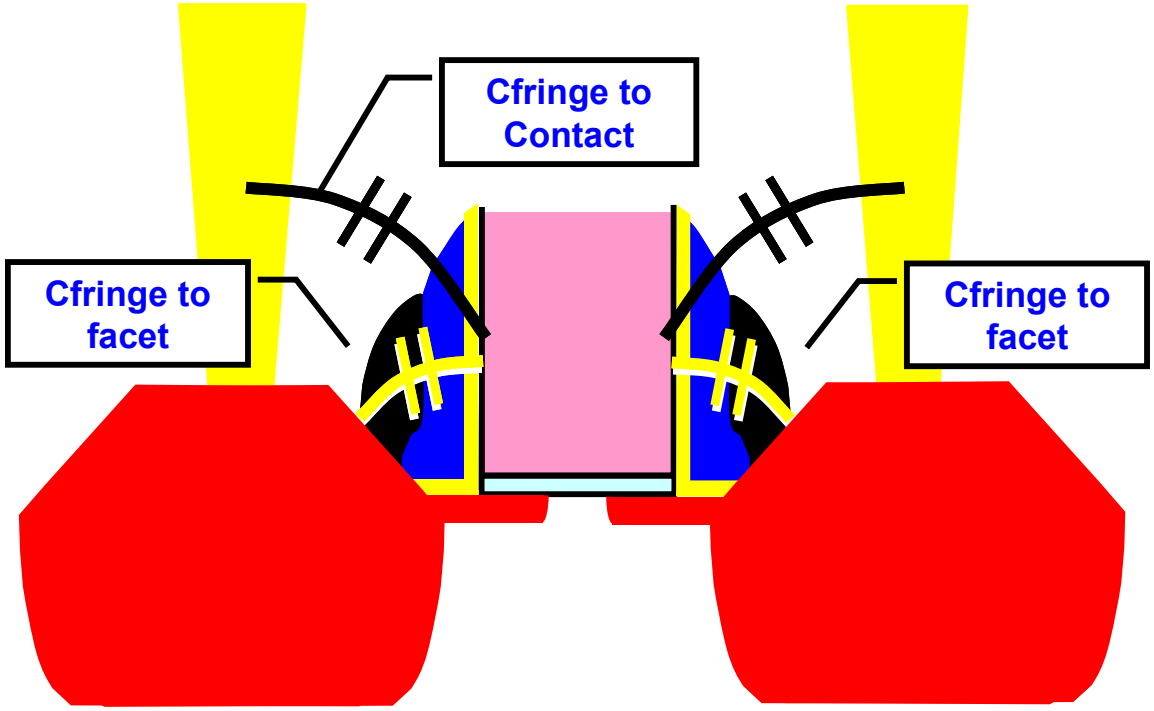
Planar Capacitive Elements

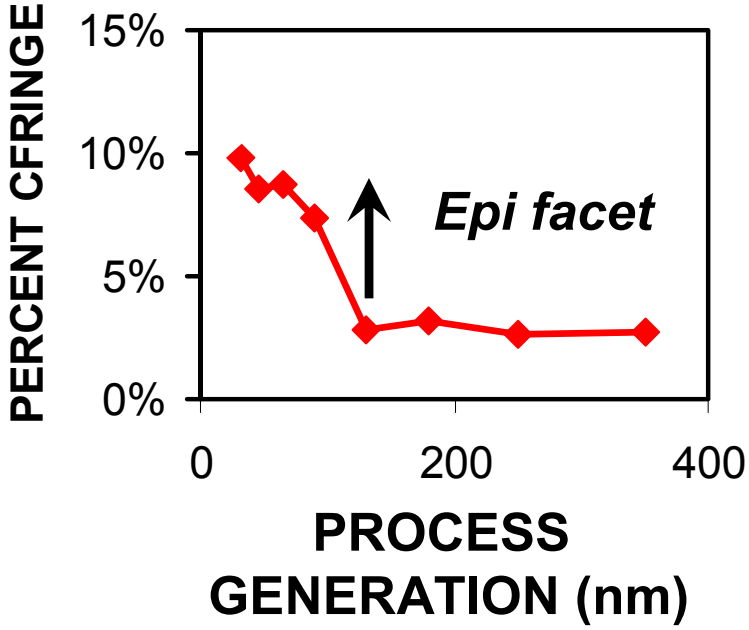




"Golden" days of scaling:
Who worried about Cfringe?

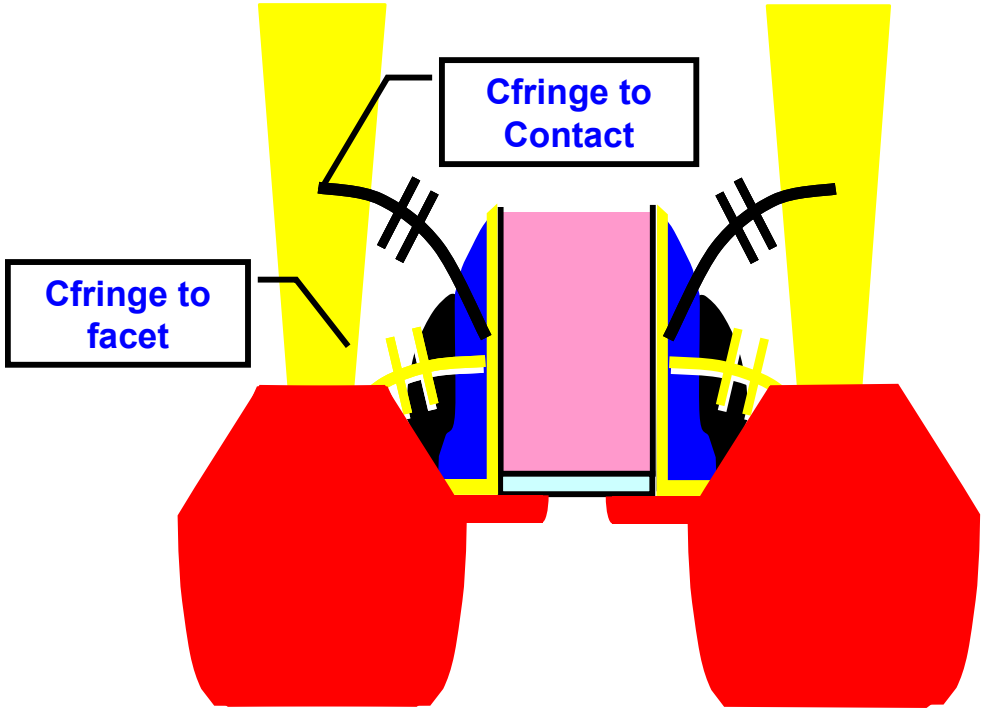
Planar Capacitive Elements

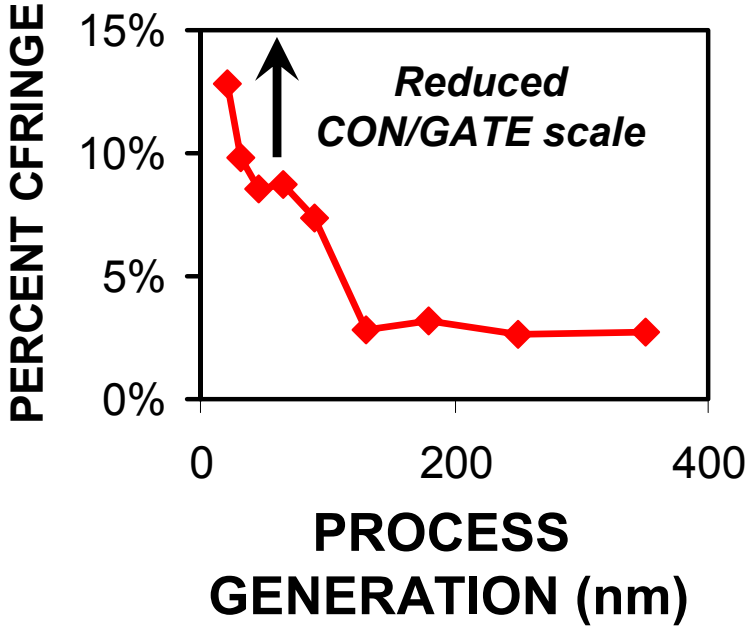




"Silver" days of scaling: Introduction of epi: Increased fringe due to facet

Planar Capacitive Elements



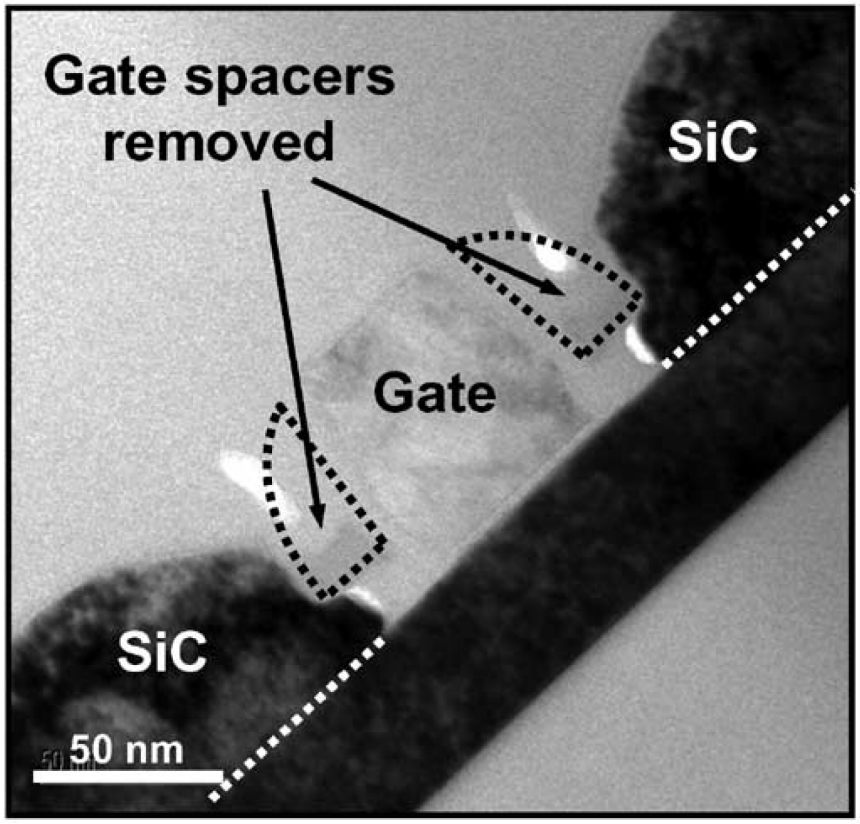


"Bronze" days of scaling

Gate and contact CD dimensions scaling slower than contacted gate pitch – fringe matters

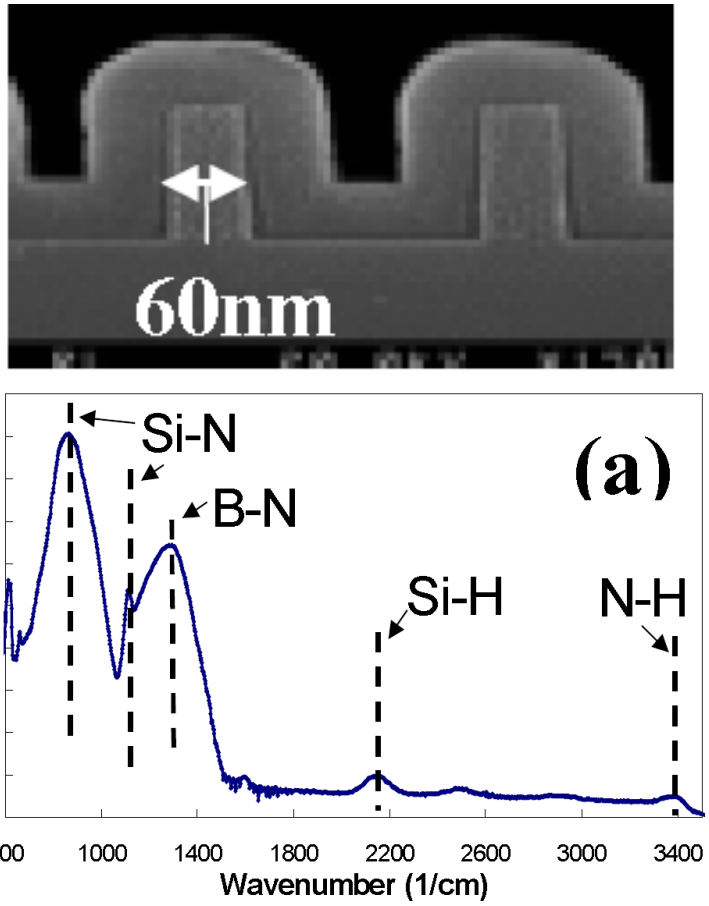
K. Kuhn – IEDM 2008

Innovative Spacer Technologies



SPACER REMOVAL

Liow – NUS Singapore
EDL 2008 [11]



SiBCN (Low-K) SPACER

Ko –TSMC
VLSI 2008 [12]

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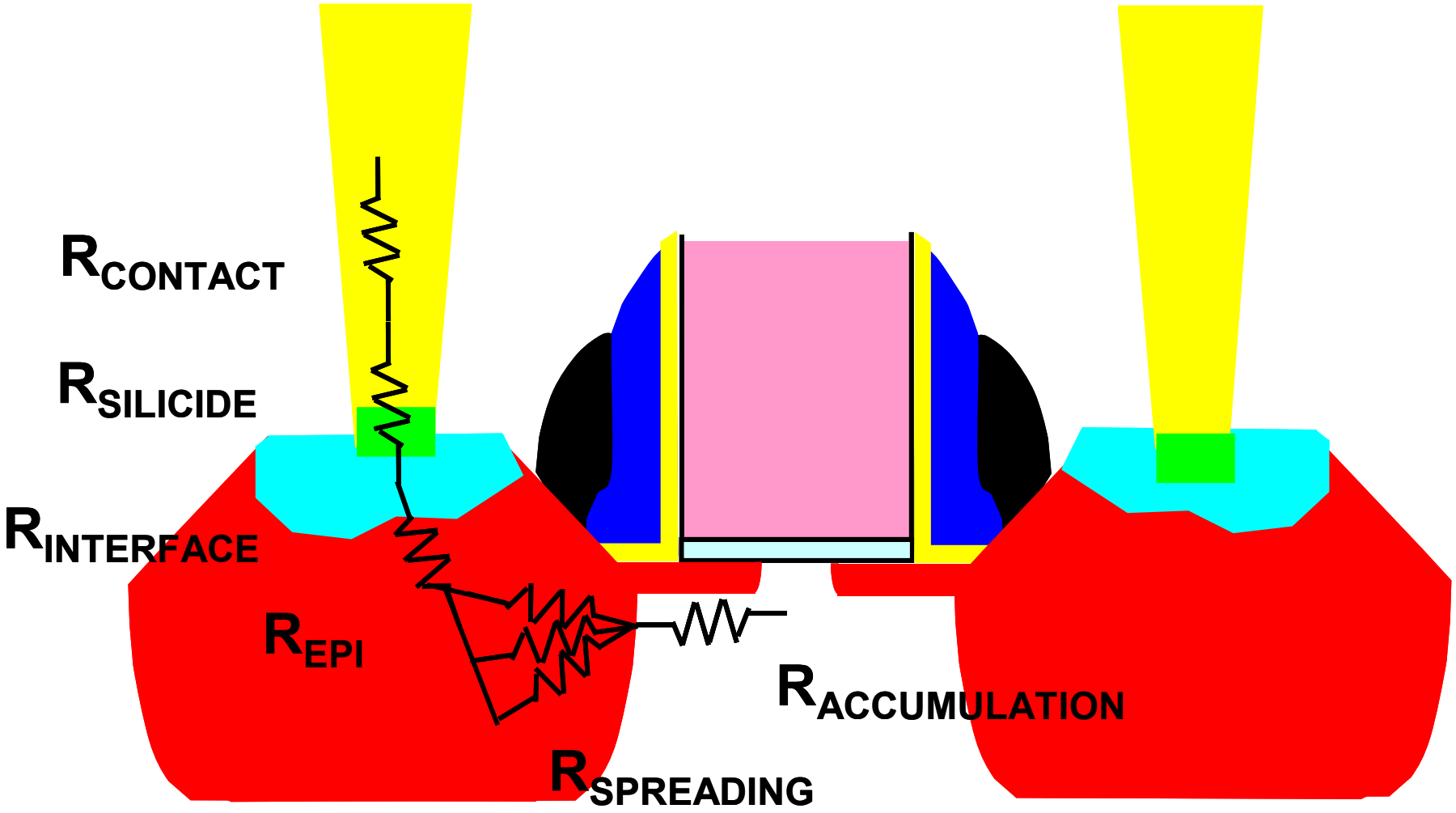
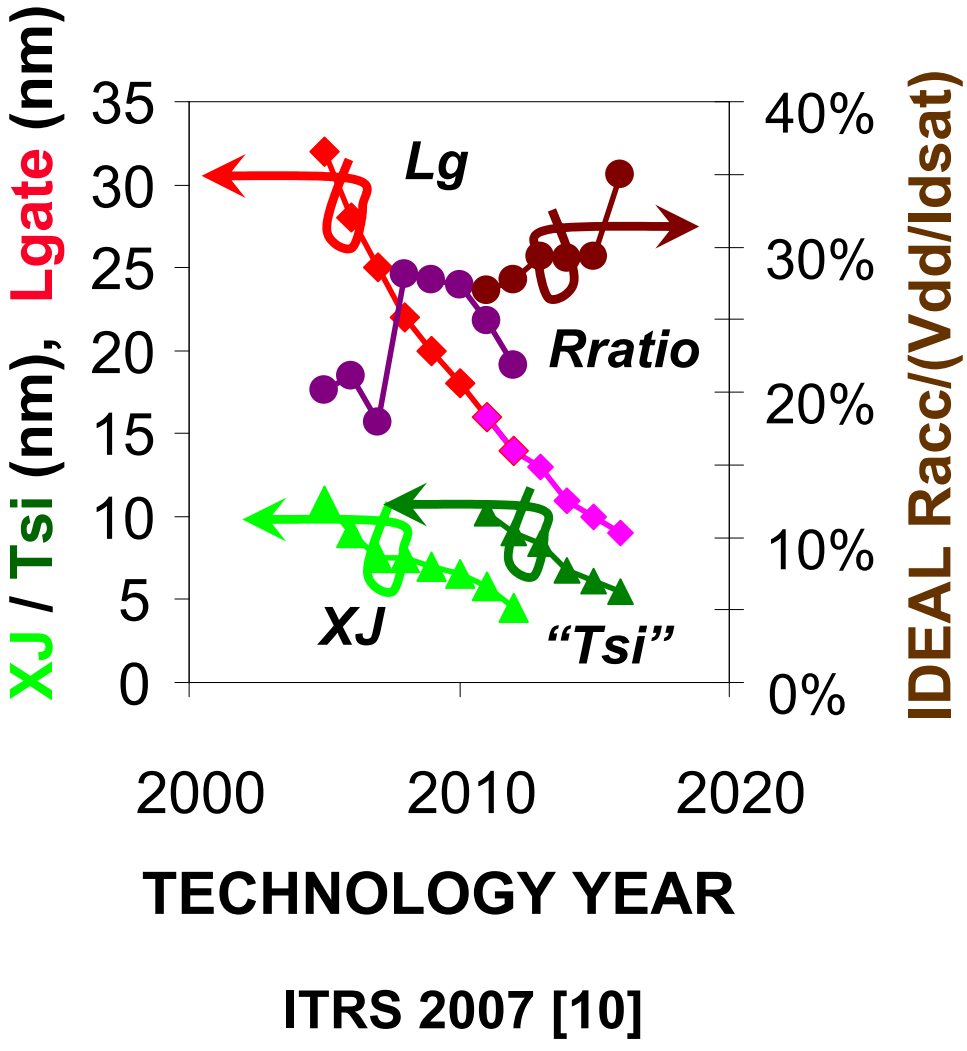
Planar Resistive Elements

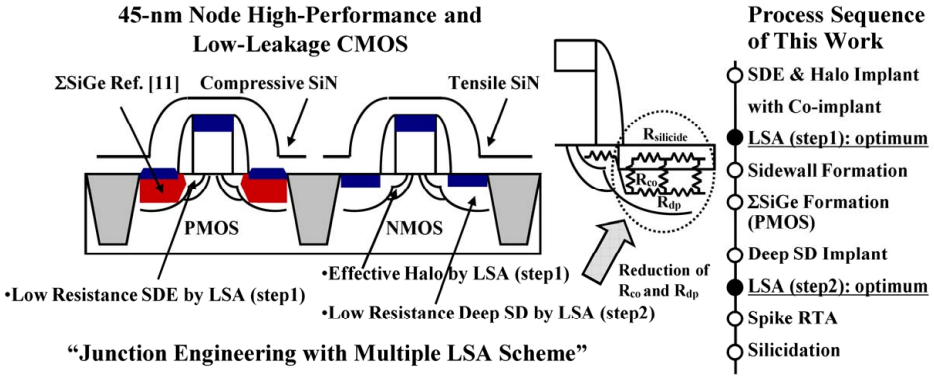


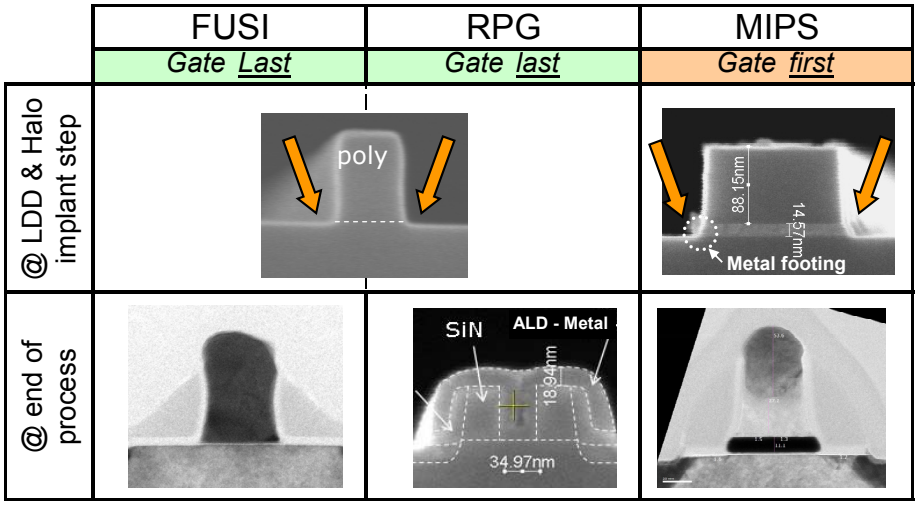
Technology trends
Xj/Tsi, Lg, Racc

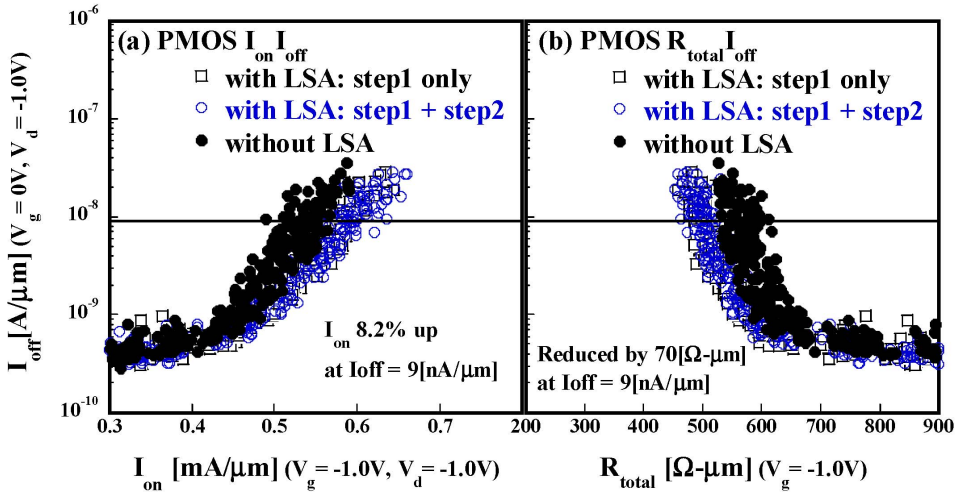


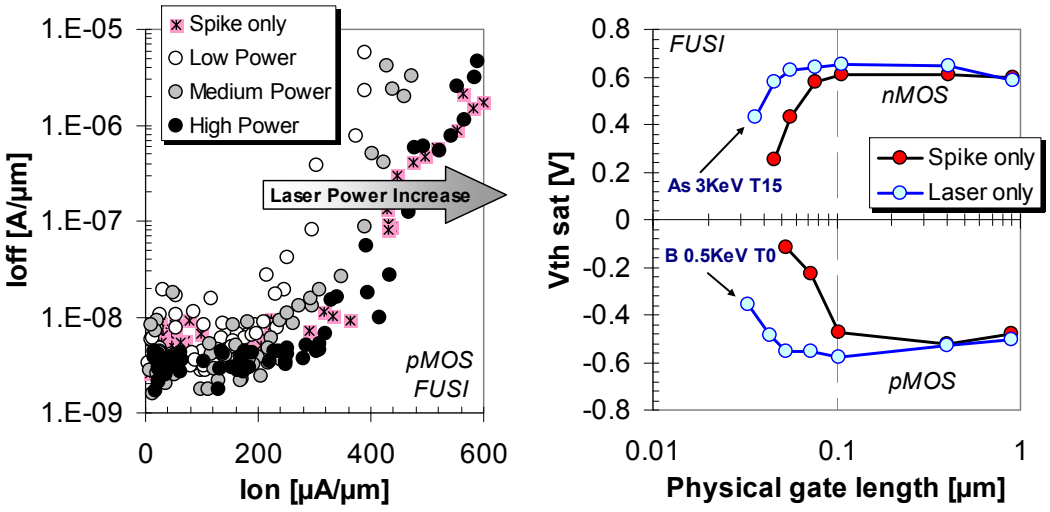
ITRS 2007 [10]

Advanced Laser Anneal Technologies





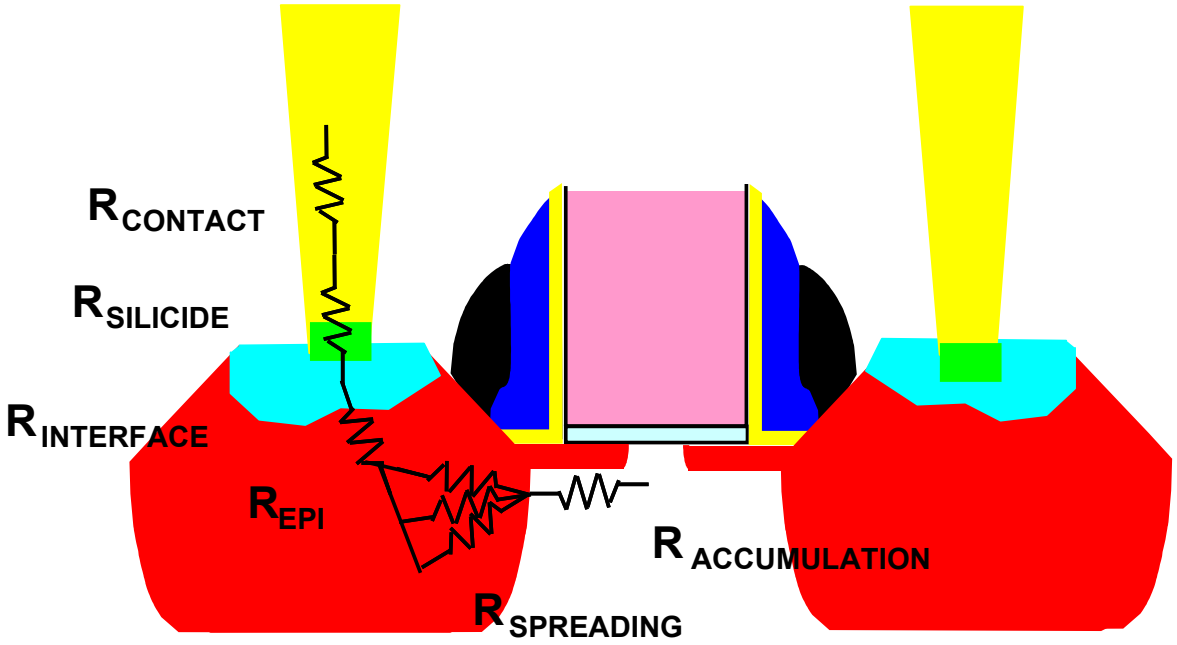




Yamamoto – Fujitsu - IEDM 2007 [15]
Multiple laser spikes + RTA

Ortolland – IMEC - VLSI 2008 [16]
Non-melt LSA with adv. gate stacks

Low Barrier Height Contacts



$$R_{\text{interface}} \propto \exp\left(\frac{q\phi_B}{\sqrt{N_D}}\right)$$

$$R_{\text{interface}} \propto \frac{1}{A}$$

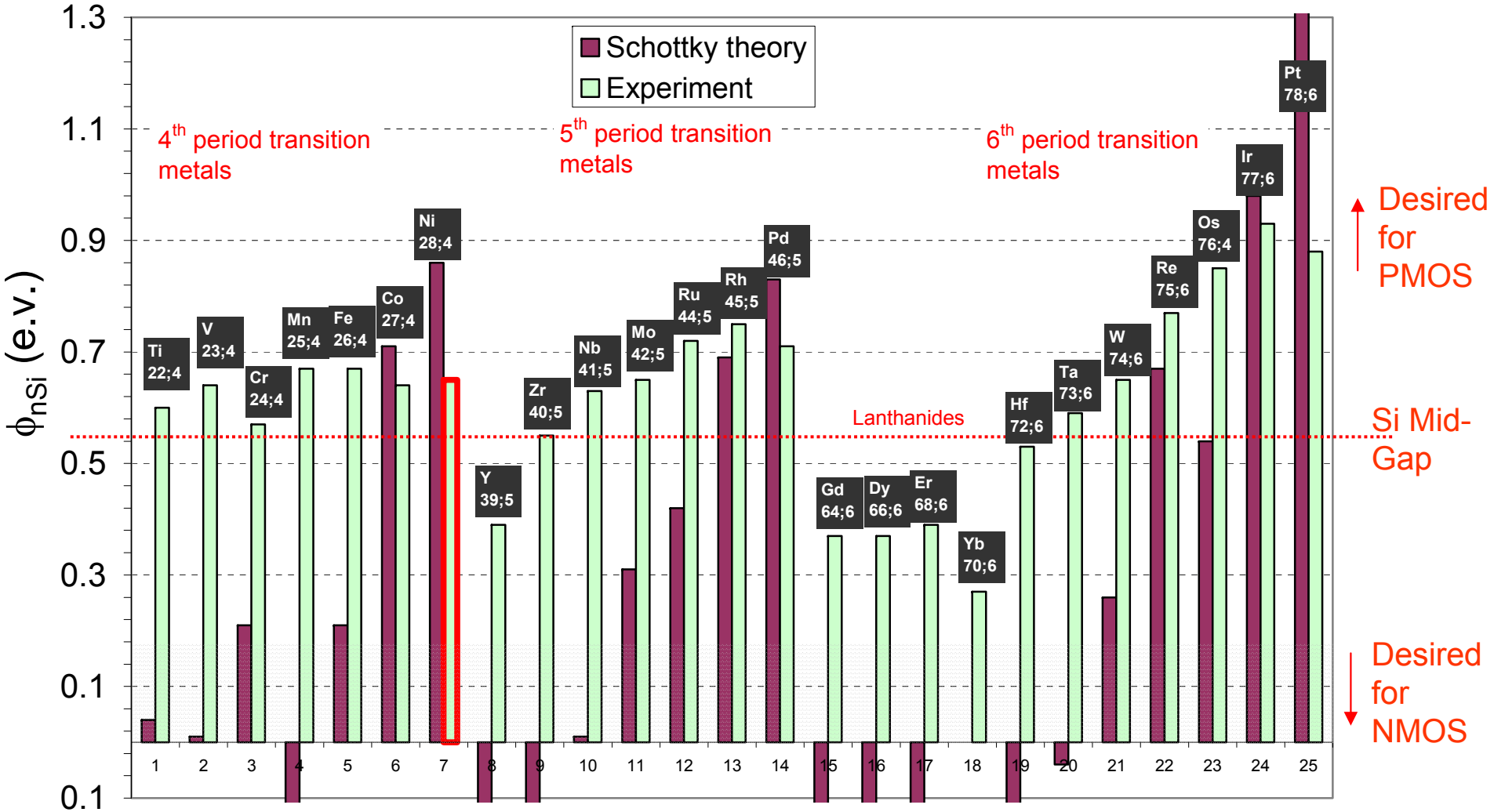
$q\phi_B - Schottky\ \ Barrier\ \ Height\ (SBH)$

$N_D - Substrate\ \ doping\ \ conc.$

$A - Contact\ \ area$

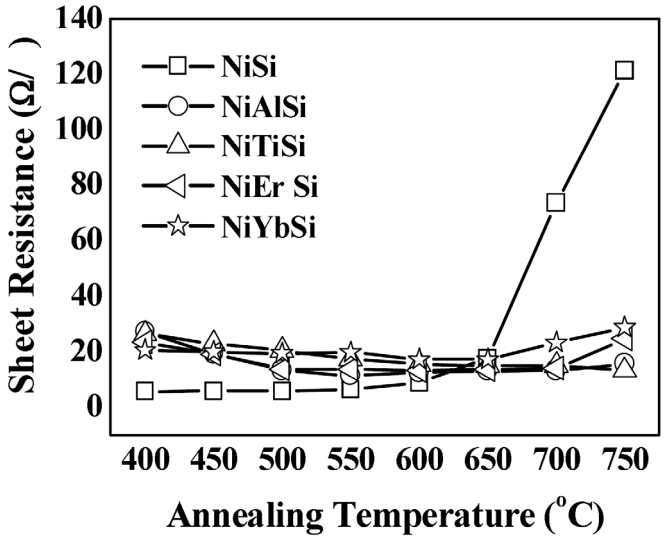
- Limited additional improvement with $R_{silicide}$ (NiSi has the lowest known resistivity at 10.5 μohm-cm)
- SBH optimization has potential for $R_{interface}$ reduction

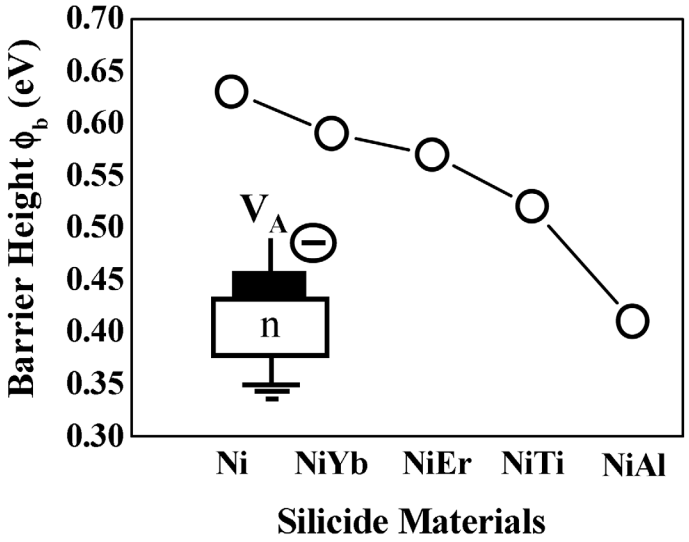
Schottky theory vs. experimental SBHs for metals on nSi
Mukherjee – Intel



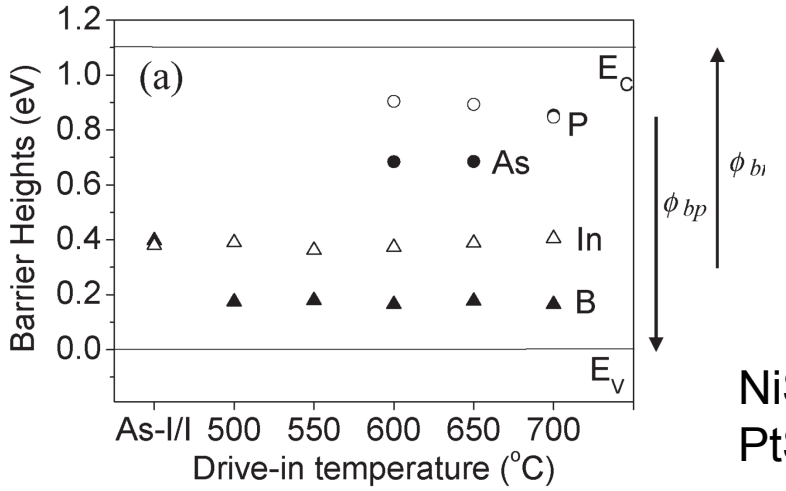
Fermi level pinned to mid-gap for most metals on Si

Alloy and Implant Modifications to Silicides

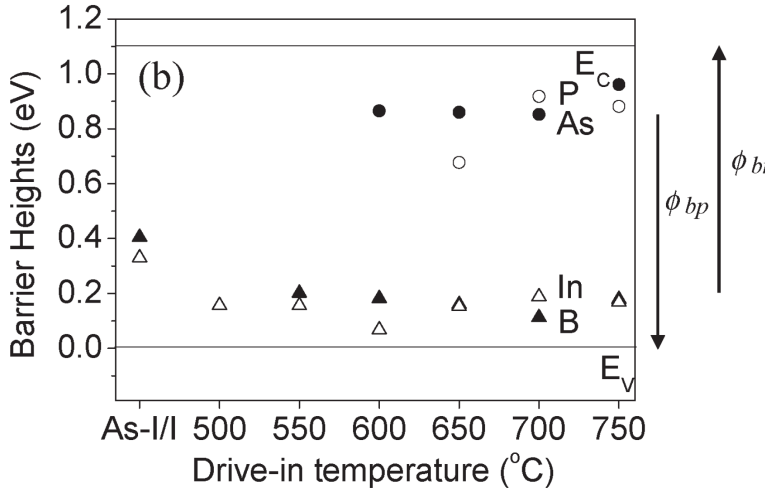




Lee –NUS-Singapore
IEDM 2006 [18]
Ni-alloy silicides

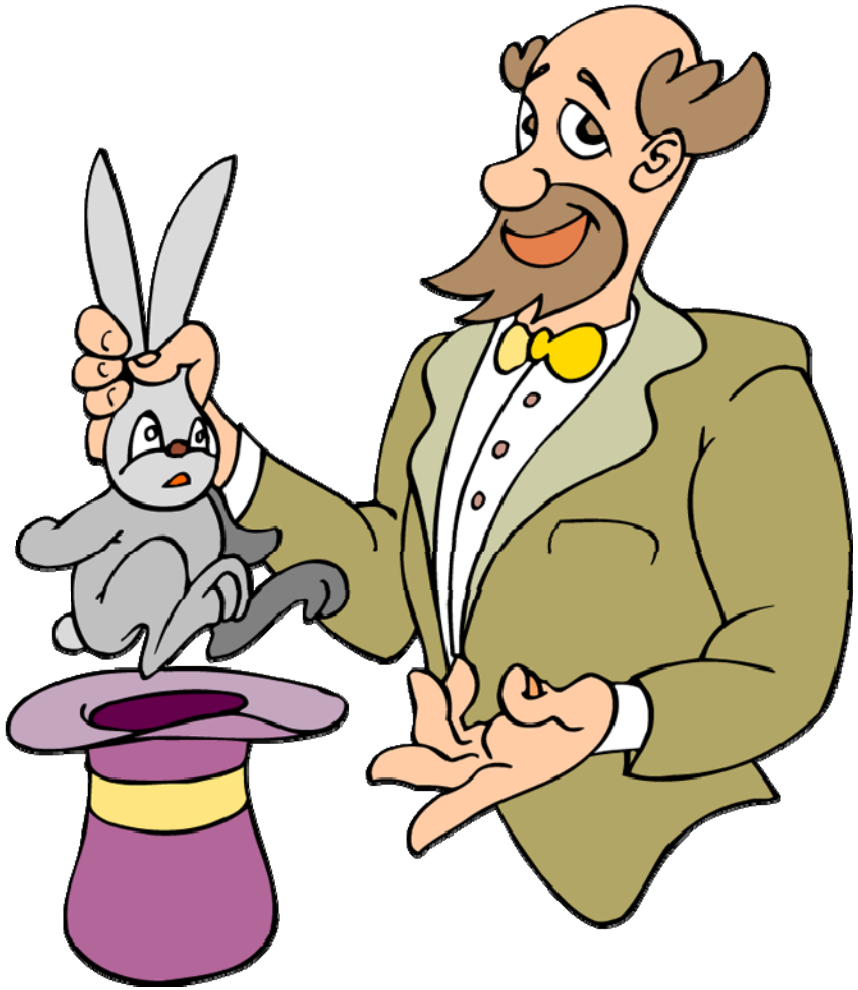


NiSi
PtSi



Zhang – KTH Sweden
EDL 2007 [20]
Implant modification of SBH
(SB FET paper)

Agenda



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High-k Metal Gate

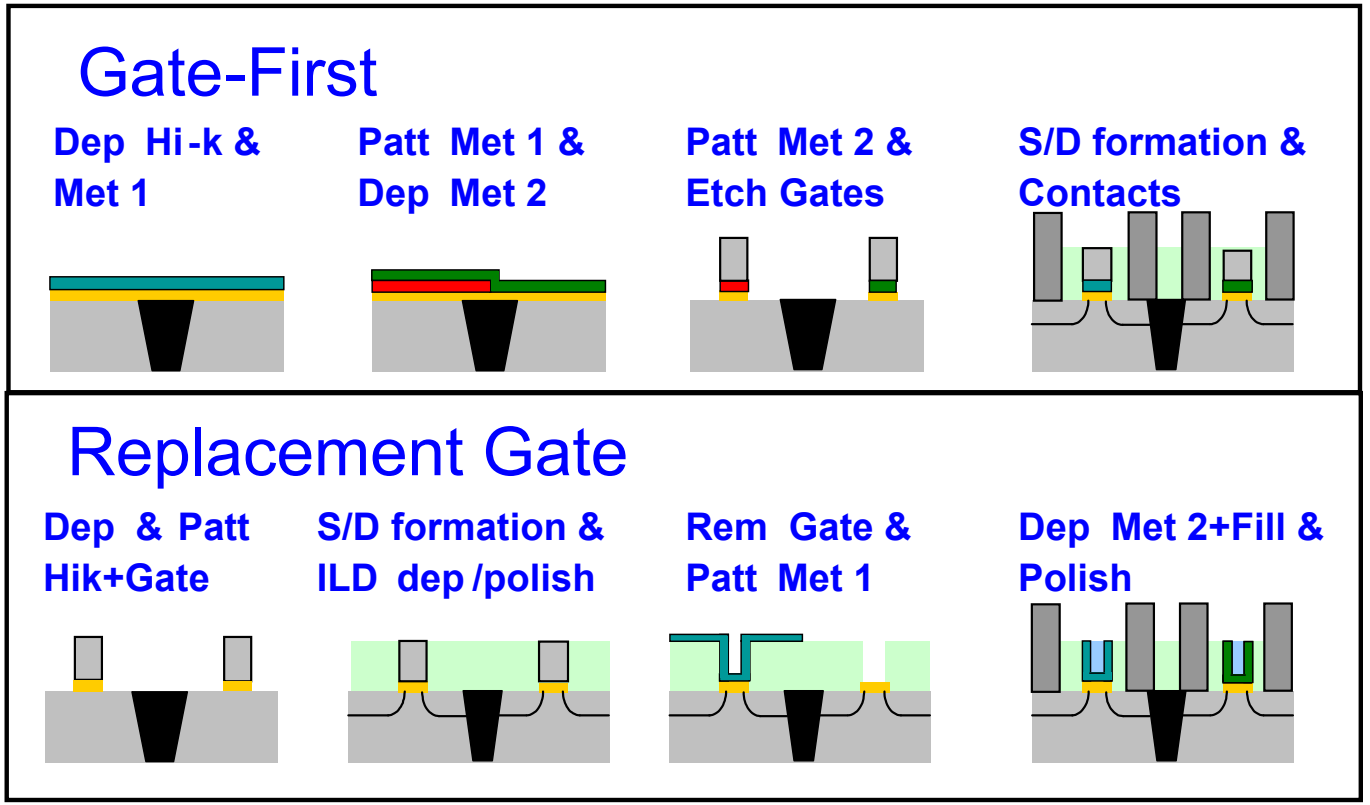
BENEFITS

- **High-k gate dielectric**
  - Reduced gate leakage
  - Continued T_{OX} scaling
- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolve V_T pinning for high-k gate dielectrics

CHALLENGES

- **High-k gate dielectric**
  - Reduced reliability
  - Reduced mobility
- **Metal gates**
  - Dual bandedge workfunctions
  - Thermal stability
  - Process integration

Gate First vs Replacement Gate

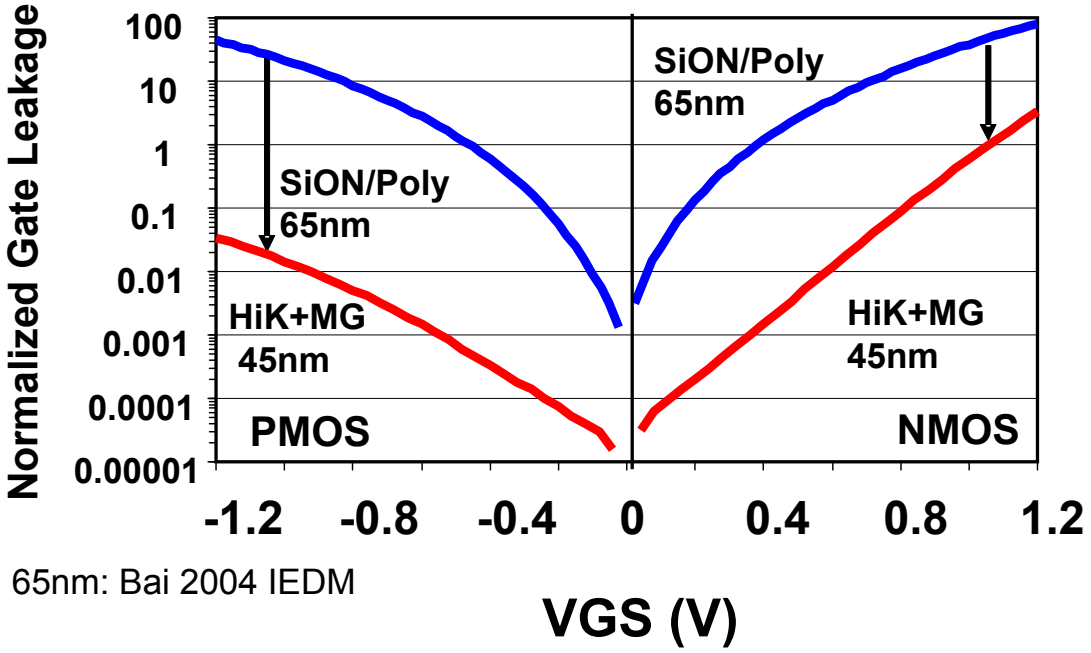


Advantages of replacement gate flow

- **High Thermal budget available for Midsection**
  - Better Activation of S/D Implants
- **Low thermal budget for Metal Gate**
  - Large range of Gate Materials available
- **Significant enhancement of strain**
  - Both NMOS and PMOS benefit

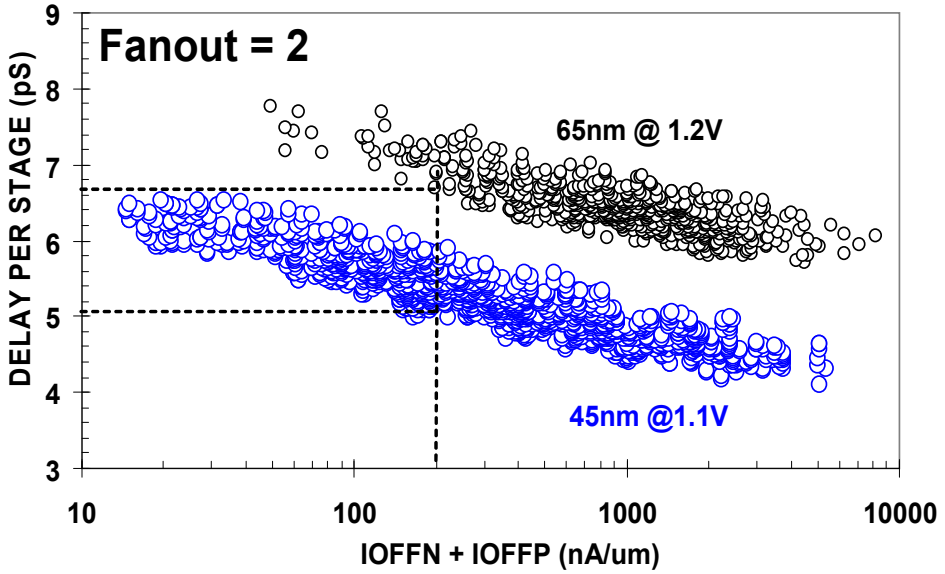
Auth - Intel –VLSI 2008 [23]

High-k Metal Gate: ToxE and Ig



65nm: Bai 2004 IEDM

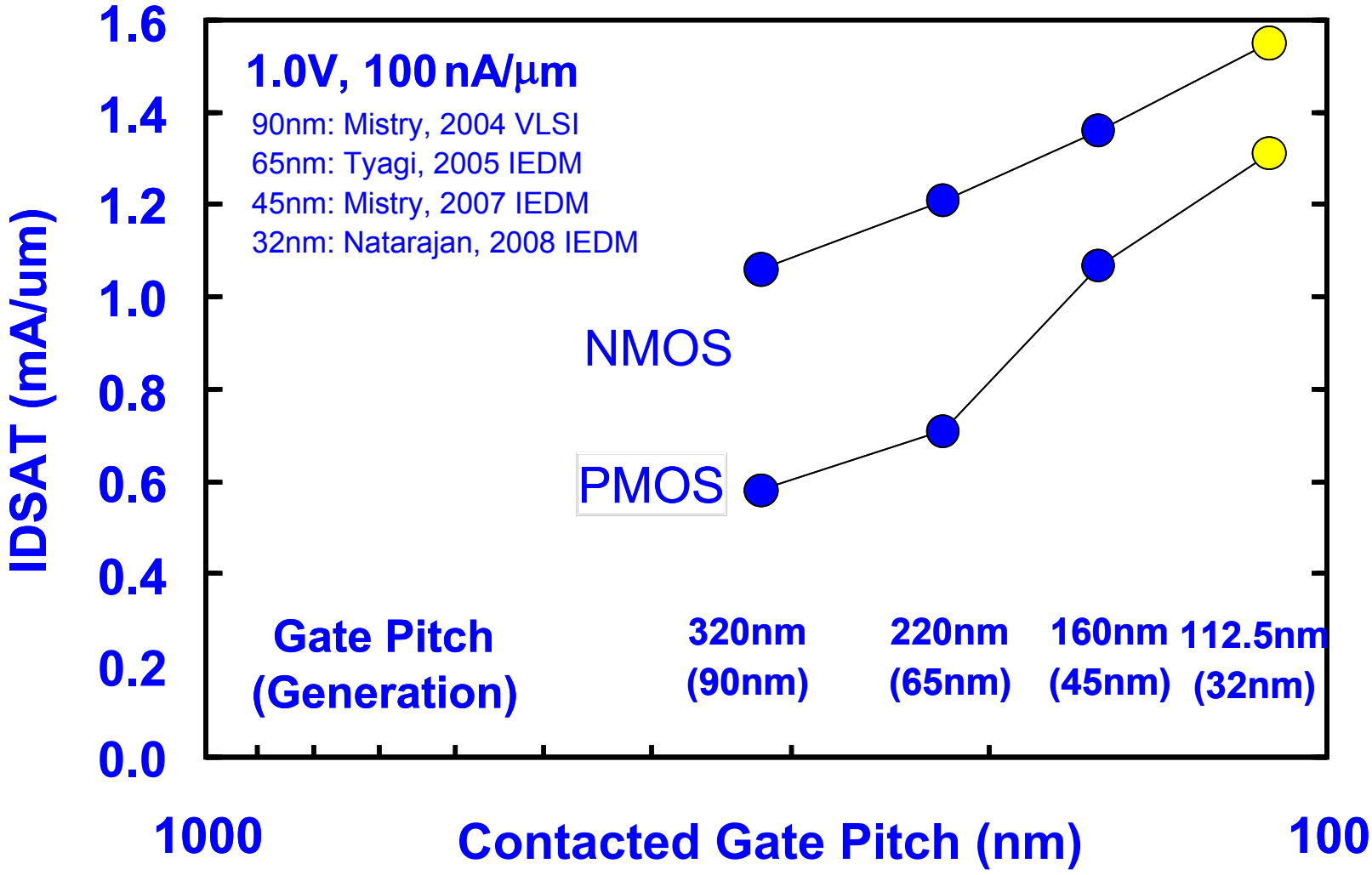
High-k/MG enables 0.7X ToxE scaling while reducing Ig > >25X for NMOS and 1000X for PMOS



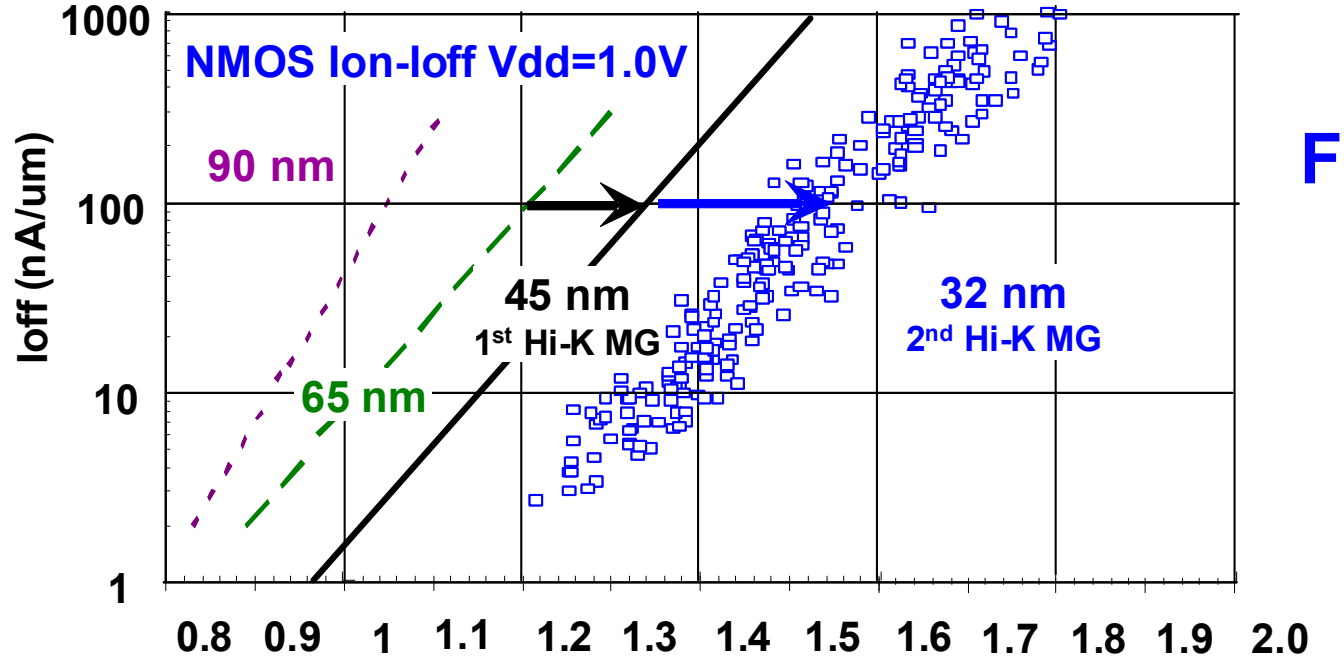
FO=2 delay of 5.1 ps at I_{OFFN} = I_{OFFP} = 100 nA/mm 23% better than 65 nm at the same leakage and 100mV lower Vcc.

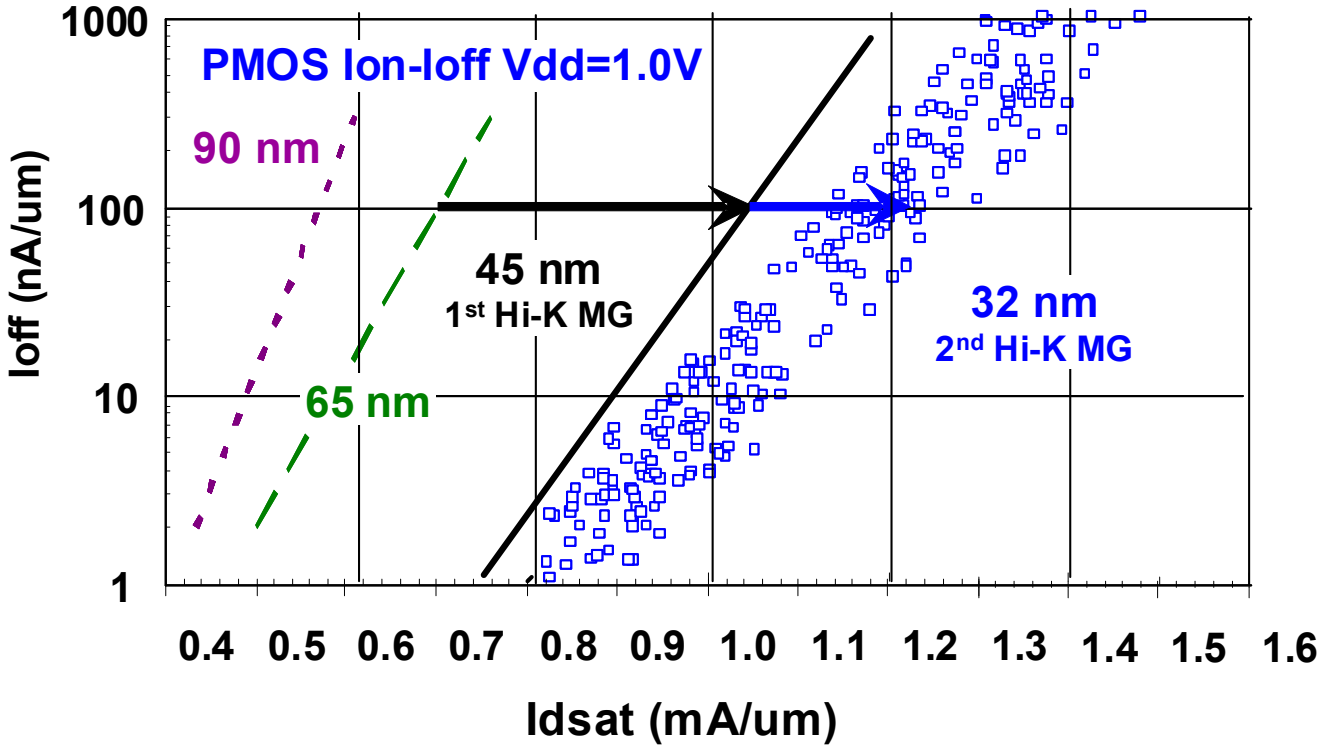
Mistry - Intel - IEDM 2007 [8]

32nm Transistor Performance
vs. Gate Pitch



Highest reported drive current at tightest reported gate pitch
Simultaneous performance and density improvement [9]



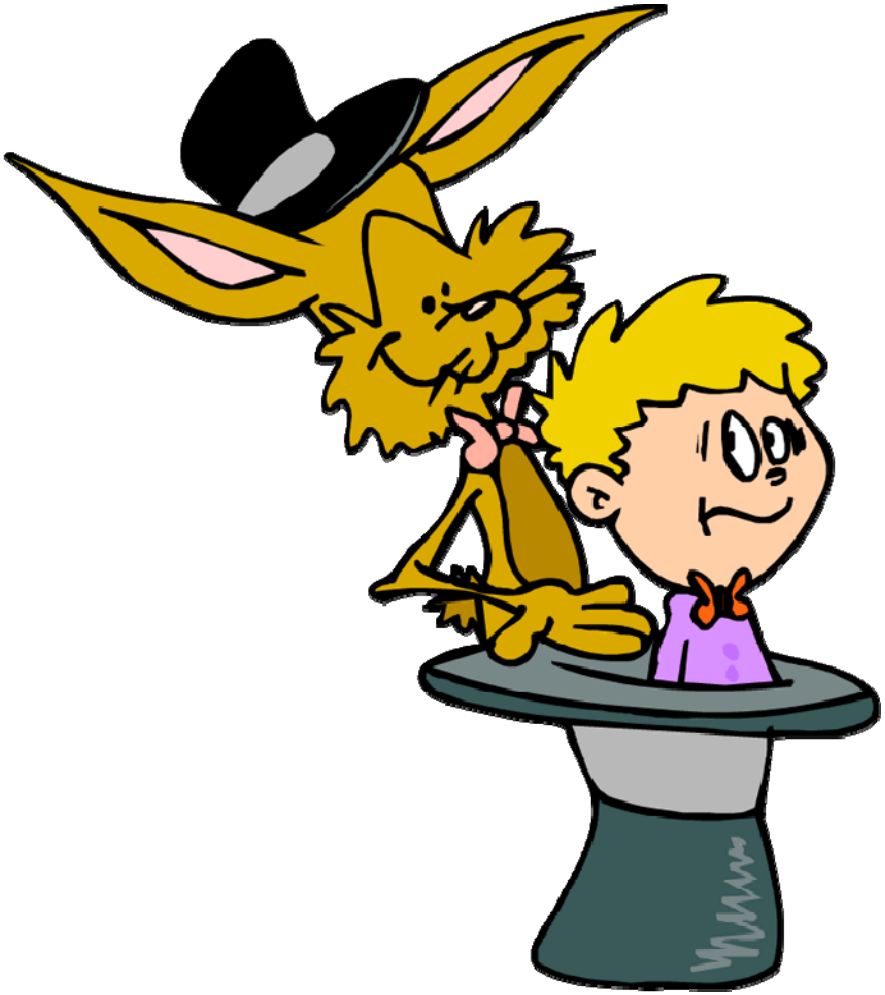


FOUR GENERATION COMPARISON

45nm:
1st gen. HiK-MG [8]

32nm:
2nd gen. HiK-MG [9]

Agenda



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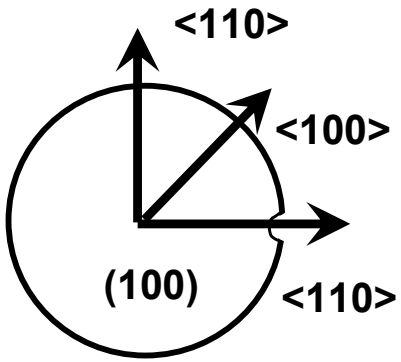
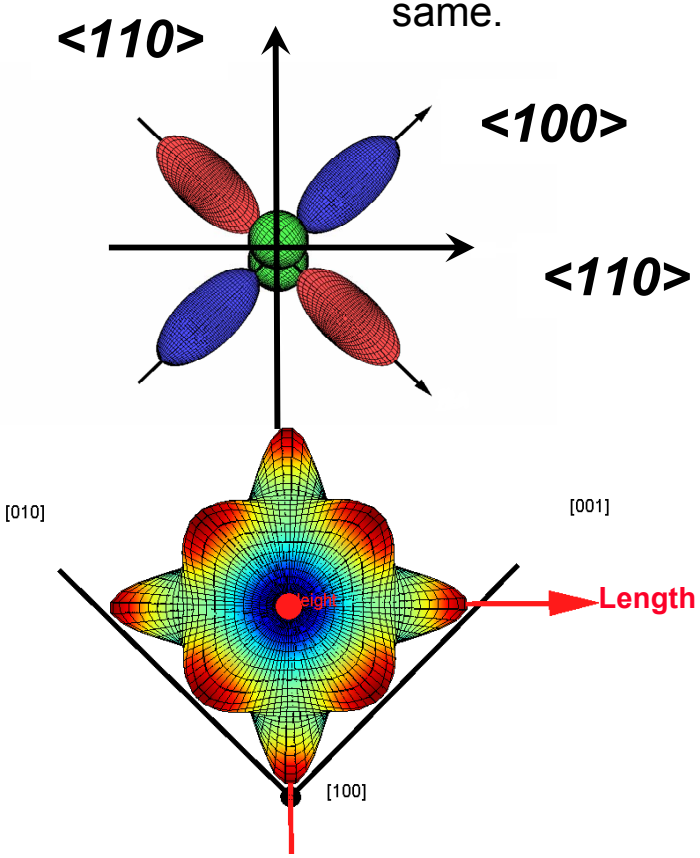
(100) surface – top down



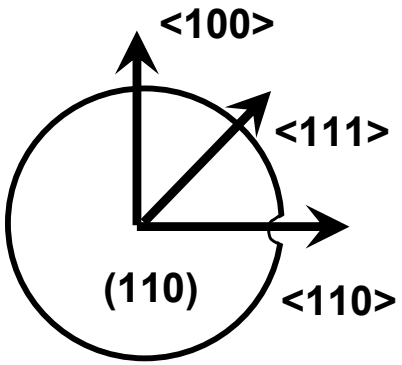
Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a “45 degree” wafer)

Both <110> directions are the same.



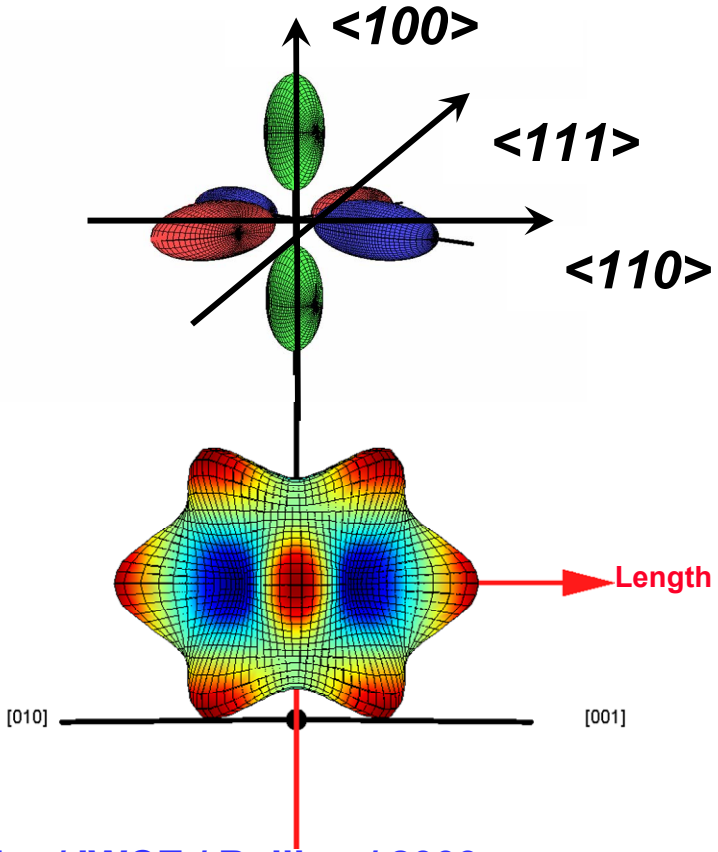
(110) surface – top down



Non-standard

(110) Surface

Three possible channel directions
<110> <111> and <100>

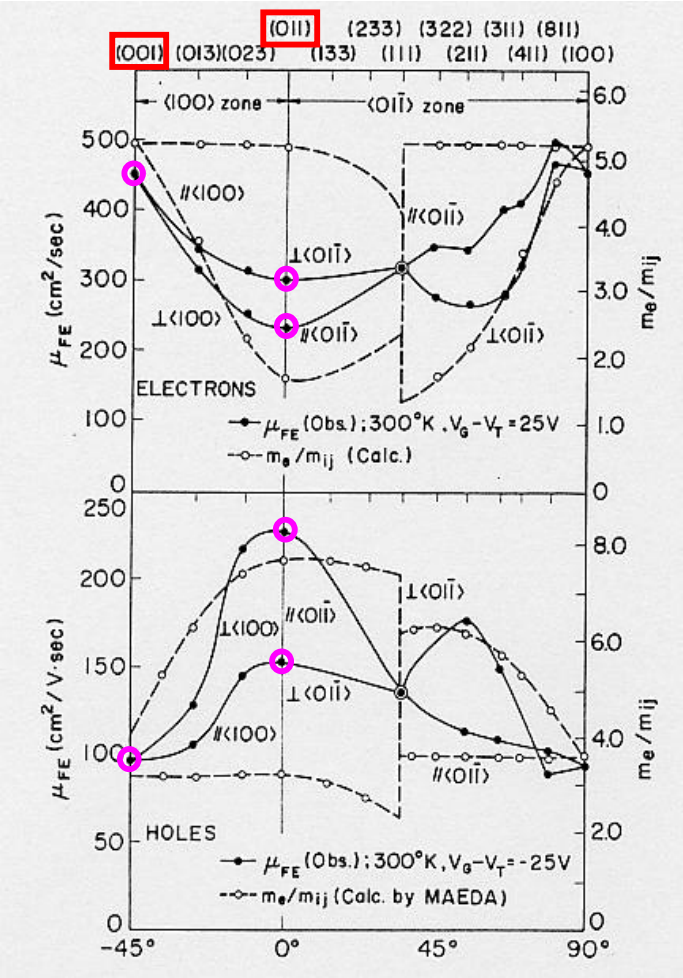


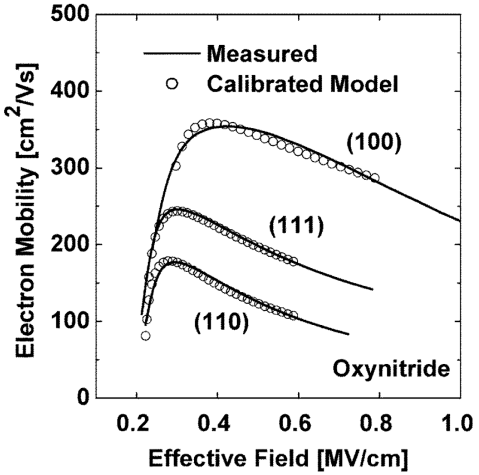
OVERALL BEST?

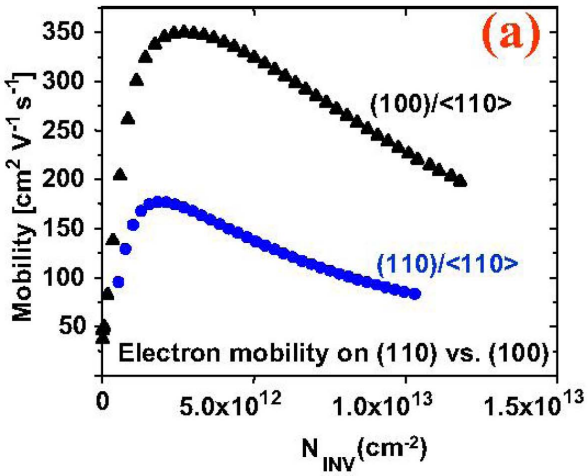
(100) and (110) comparisons (no strain)
NMOS (100) <110>, PMOS (110) <110>

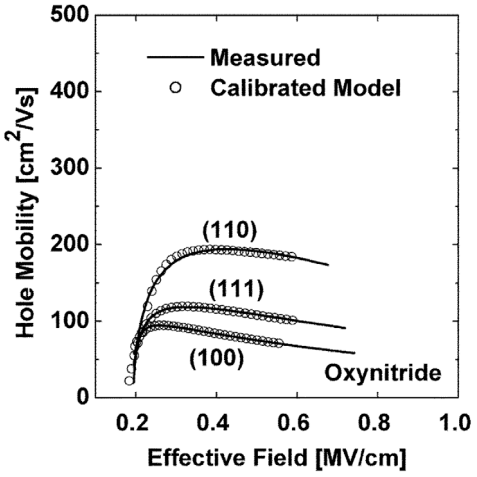
electron

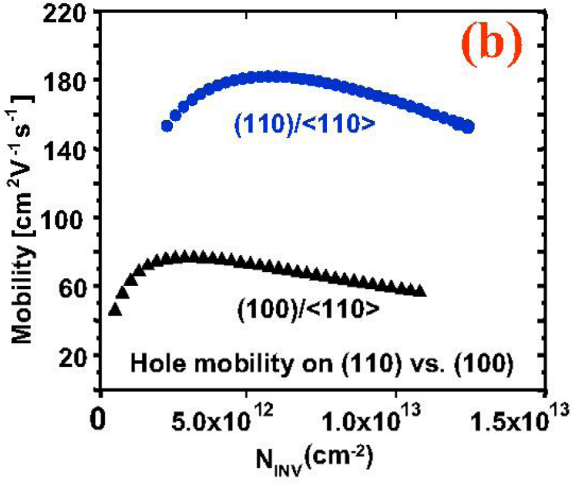
hole









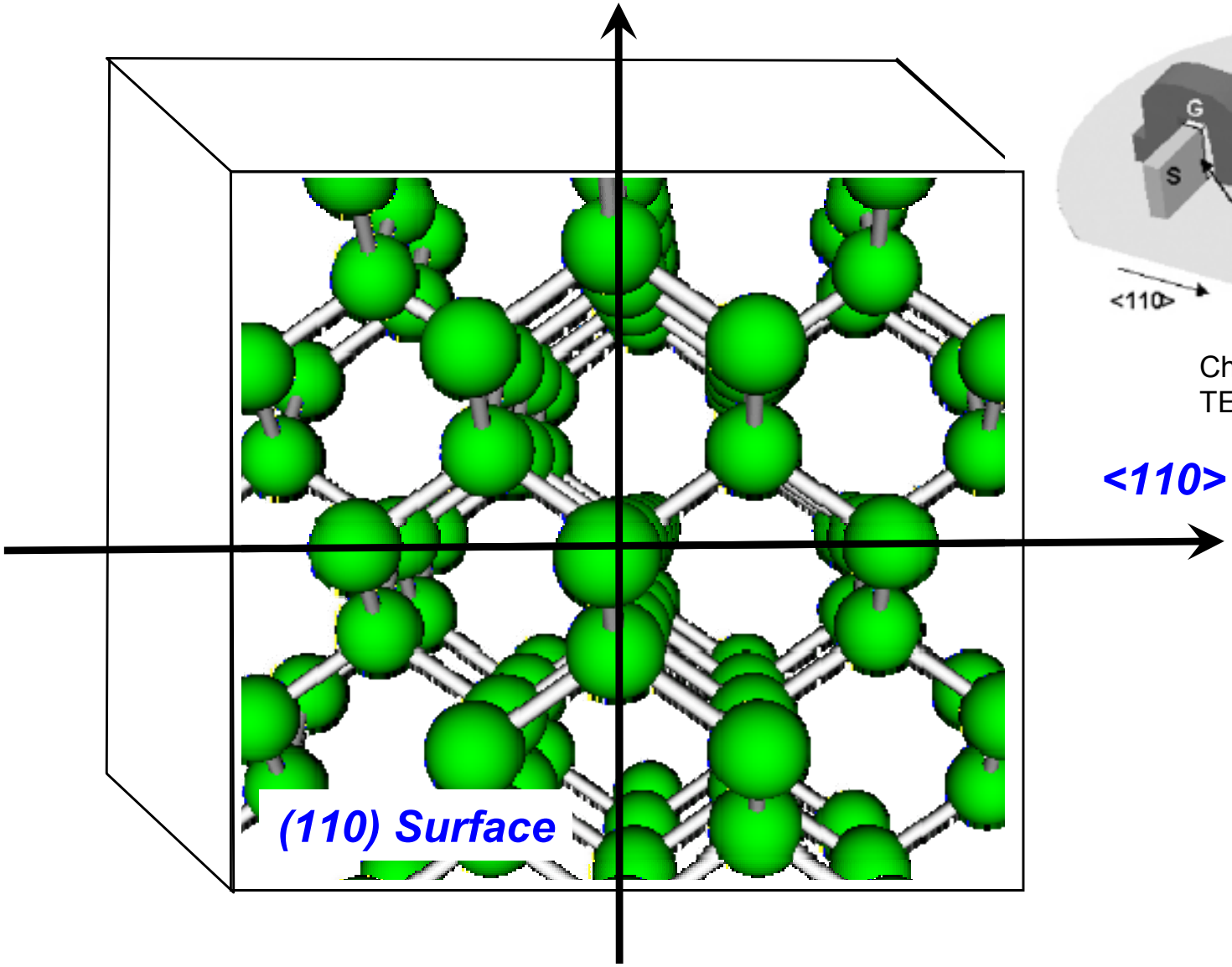


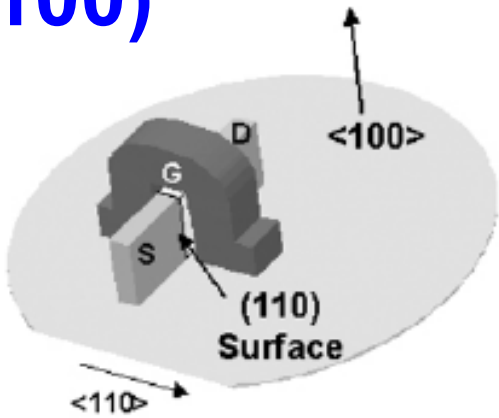
Sato [25]
Phys. Rev. (1971)

Chang - IBM
TED 2004 [26]

Yang – AMD/IBM
EDST 2007 [27]

PMOS VERTICAL DEVICES on (100)





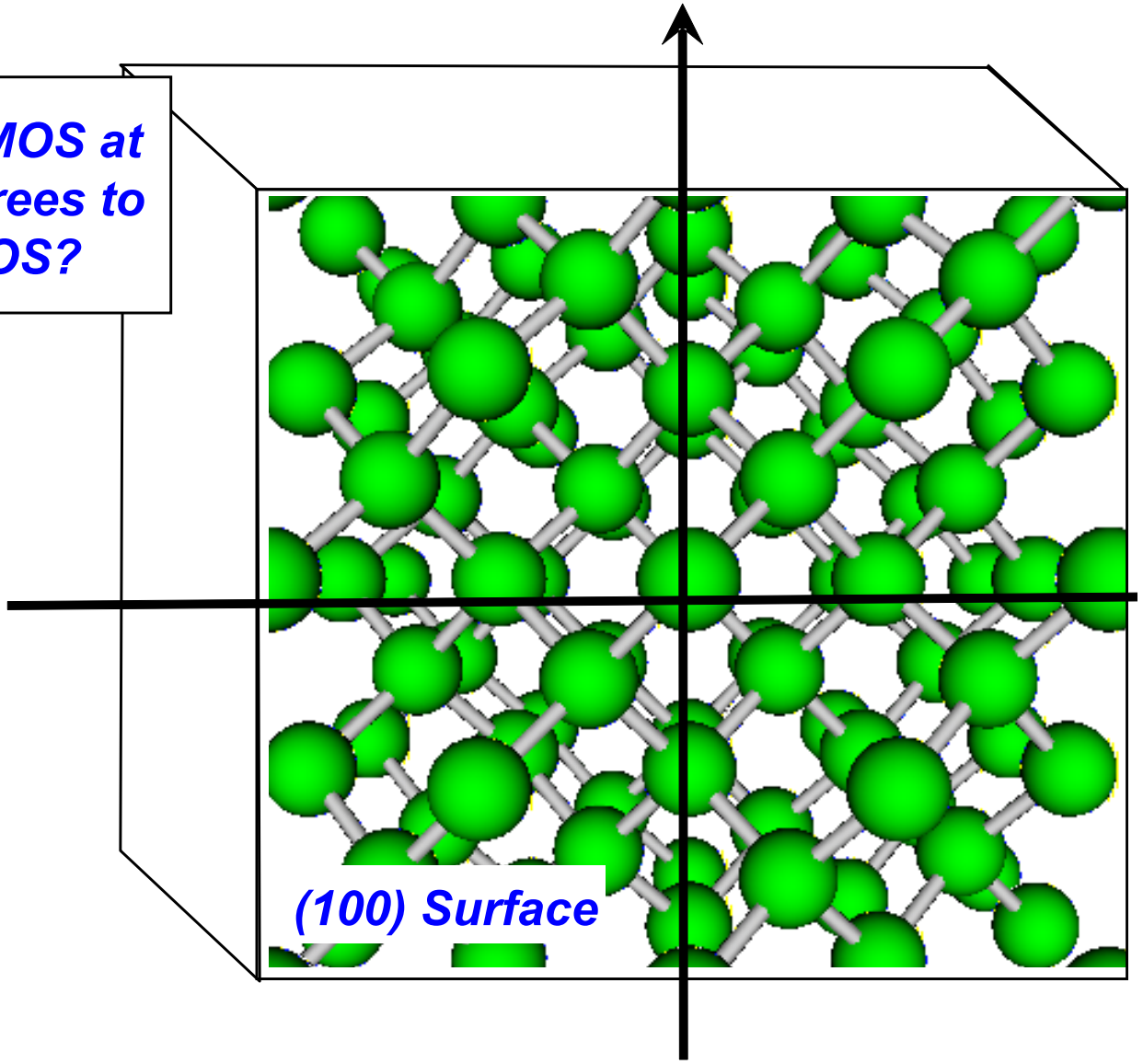
Chang - IBM – TED 2004

<110> channel

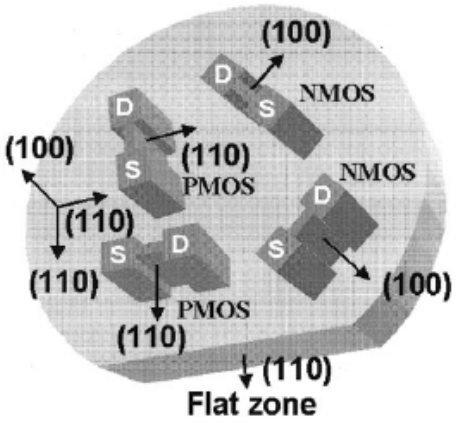
(110) surface <110> channel results when a VFET is fabricated on typical (100) Si - good for PMOS, not for NMOS

NMOS VERTICAL DEVICES on (100)

Put NMOS at 45degrees to PMOS?



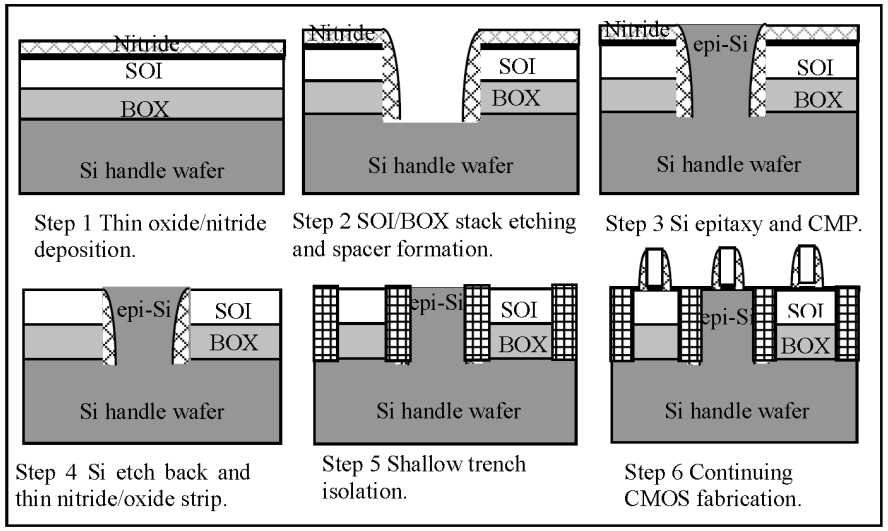
<100> channel

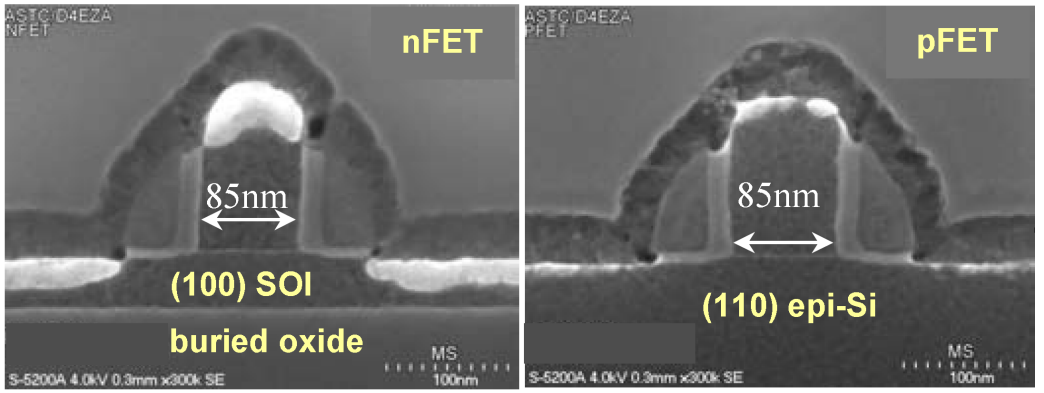


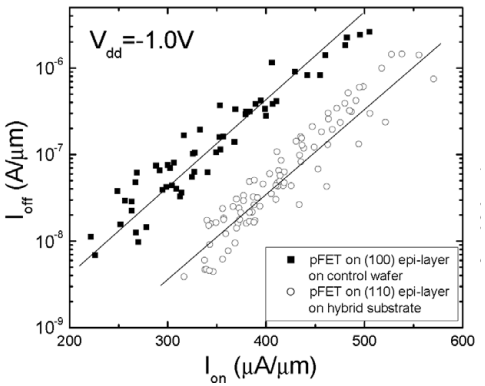
Chang - Berkeley
Proc. IEEE 2003 [26]

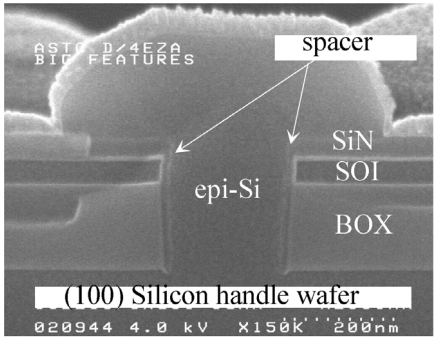
(100) surface <100> channel for a VFET fabricated at 45 degrees typical (100) Si – very challenging for lithography at 22nm node

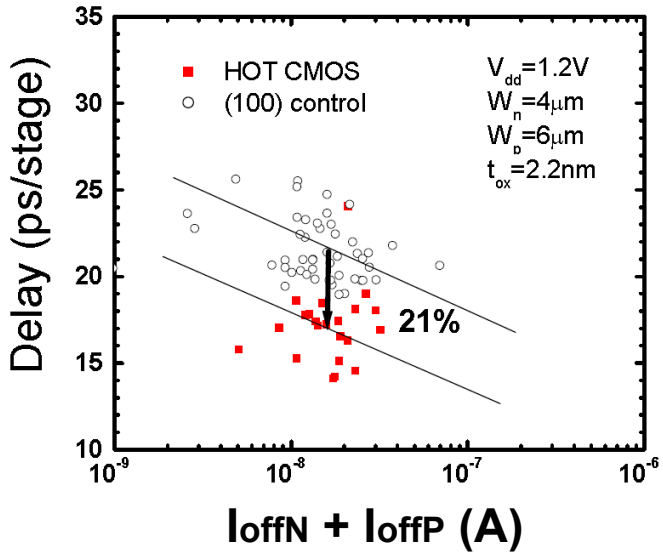
Elegant solution! Early HOT









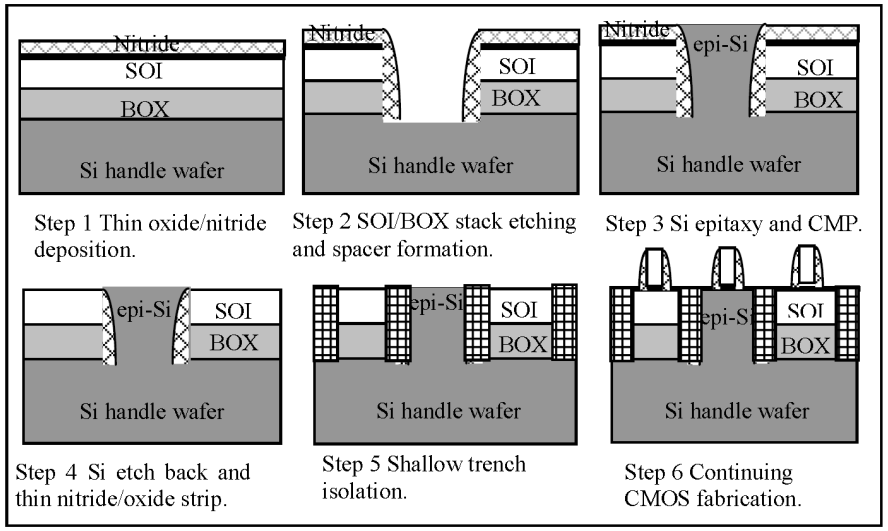


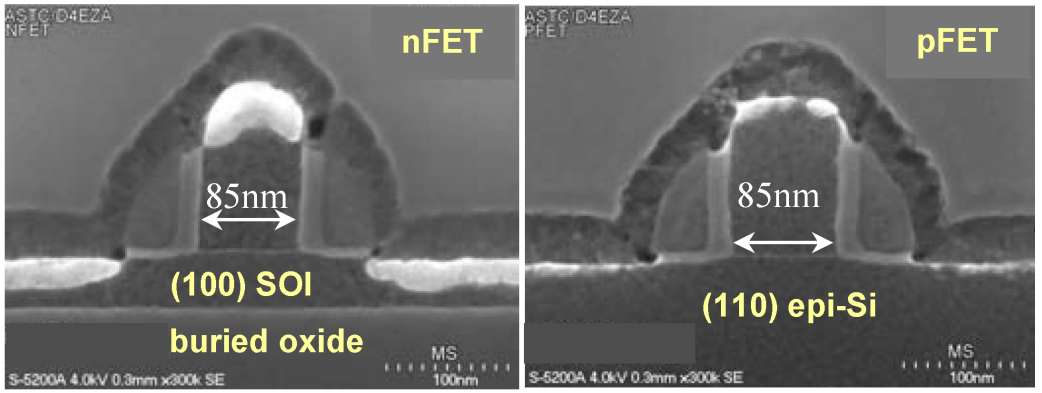
Yang – IBM
IEDM 2003 [27]
First HOT

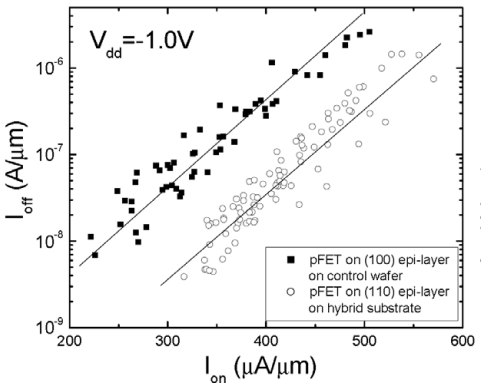
Yang – AMD/IBM
VLSI 2004
HOT RO

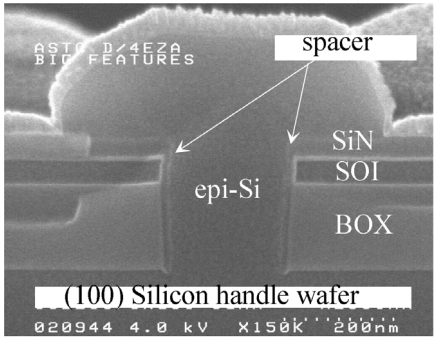
Wafer bonding; SOI of opposite type of handle wafer; both options (N and PMOS SOI explored)

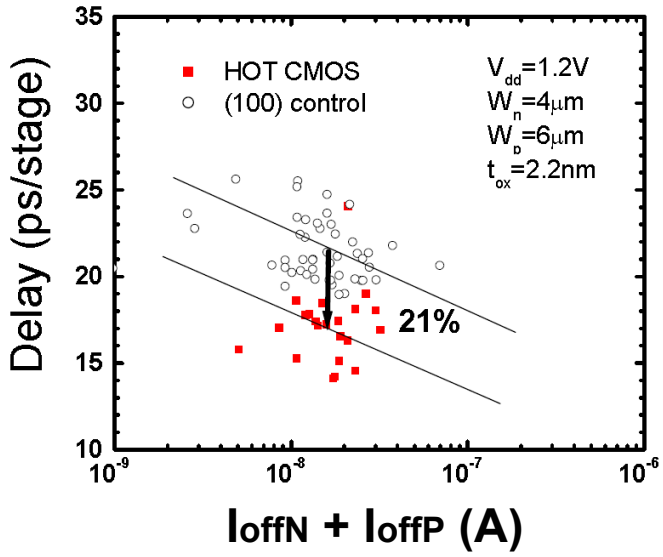
Early HOT









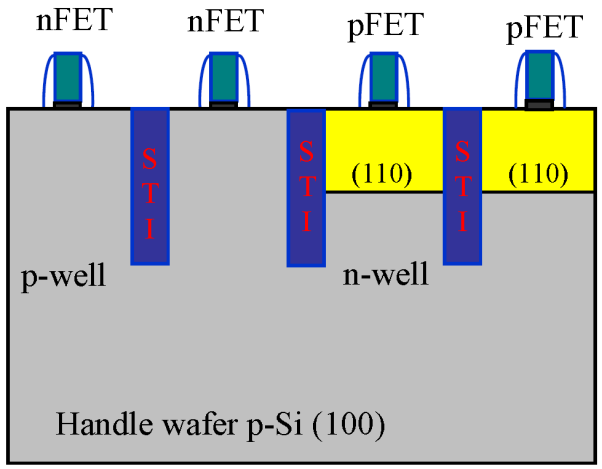


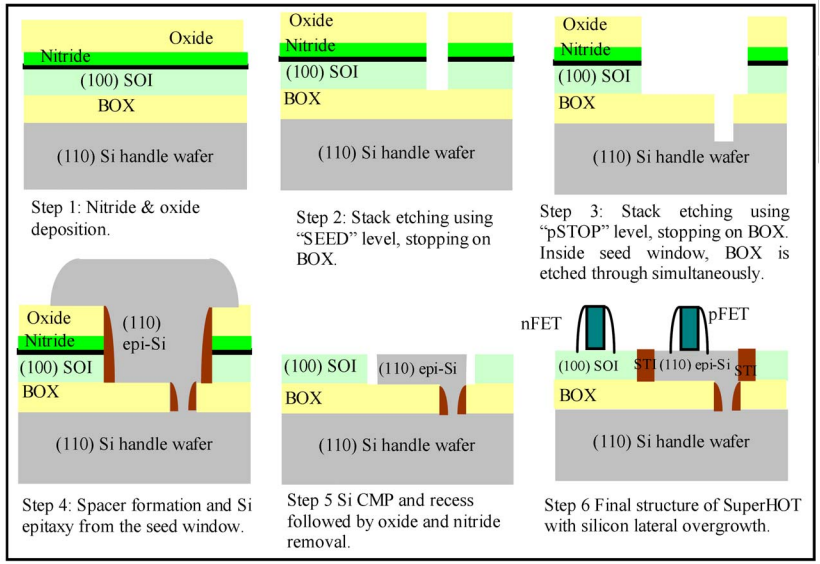
Yang – IBM
IEDM 2003 [27]
First HOT

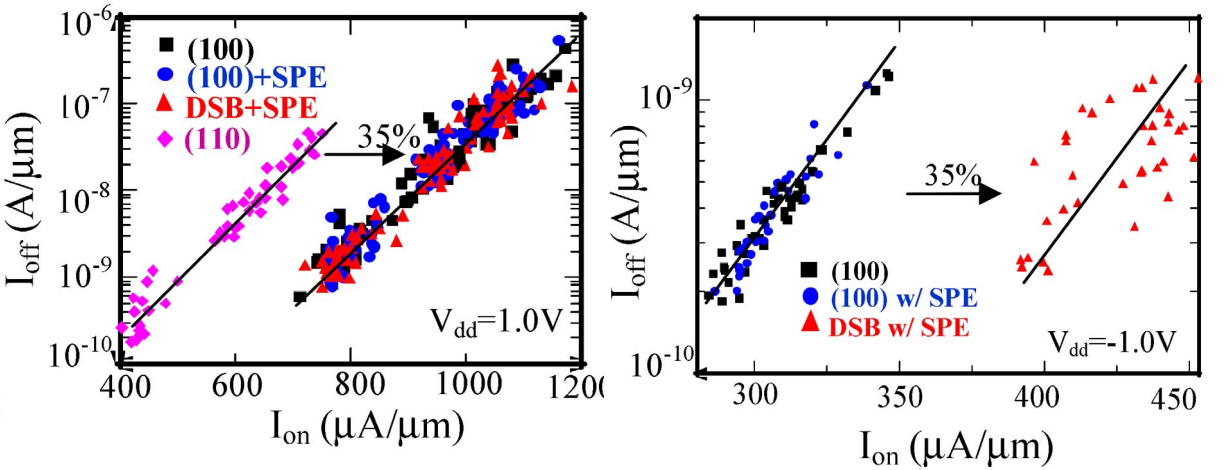
Yang – AMD/IBM
VLSI 2004
HOT RO

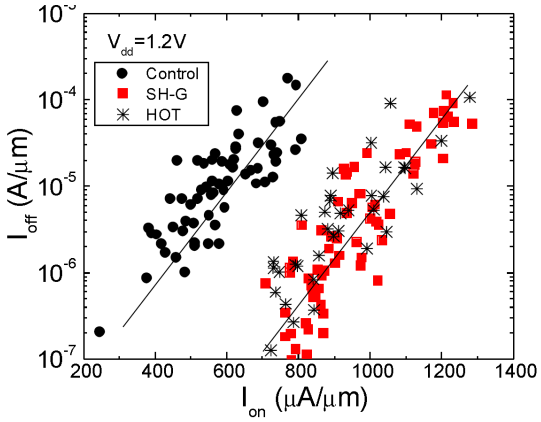
HOT architecture options

SuperHot





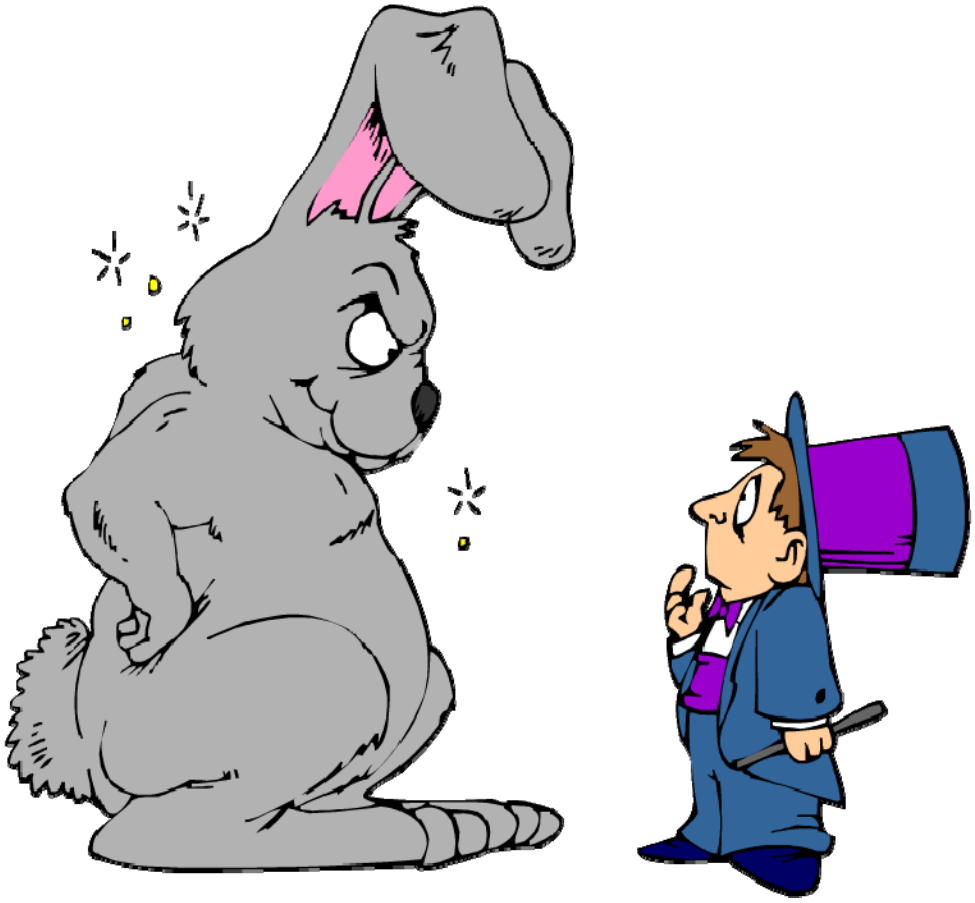




Sung – IBM
IEDM 2005 [28]
Direct silicon-bond HOT

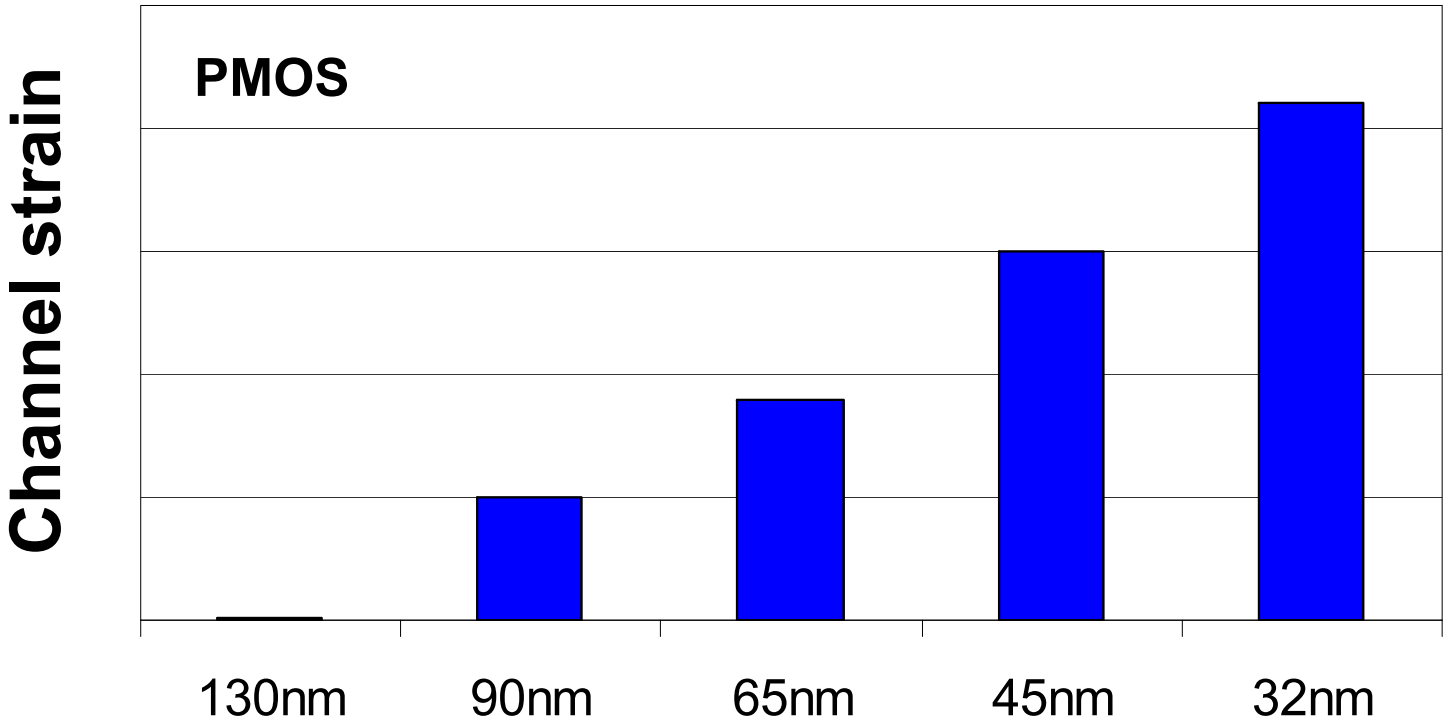
Yang – IBM
VLSI 2006 [29]
~Dual SOI HOT

Agenda



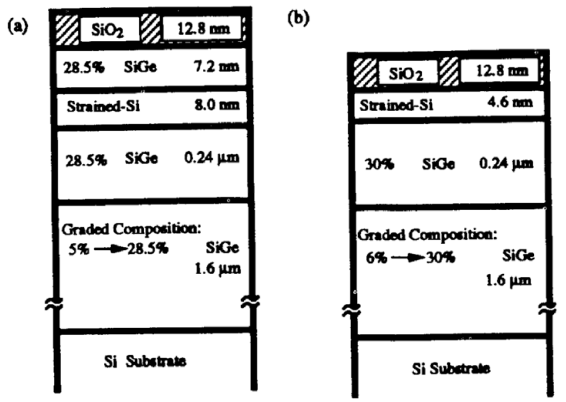
- History
- Architecture
- Capacitance
- Resistance
- HiK-MG
- Orientation
- Strain
- Strain + Orientation
- Summary

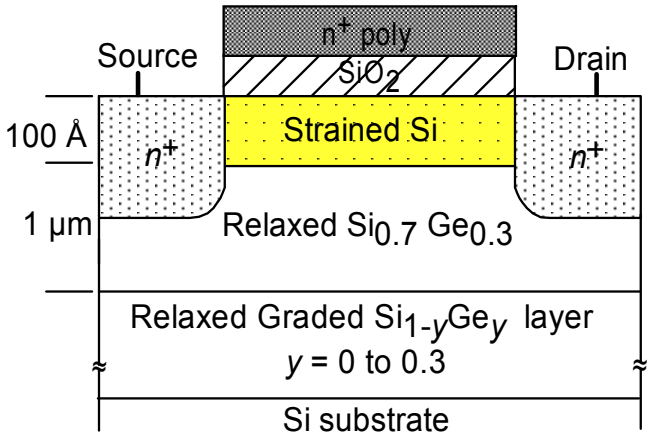
Strain: Importance in scaling

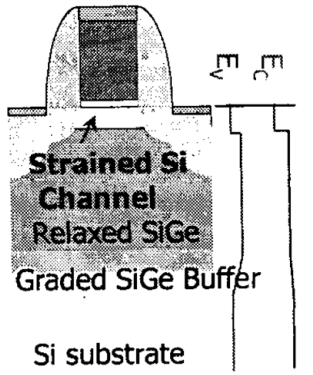


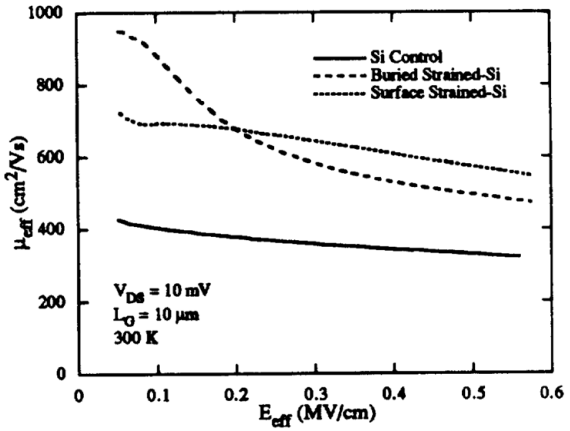
Strain (first introduced at 90nm) is a critical ingredient in modern transistor scaling

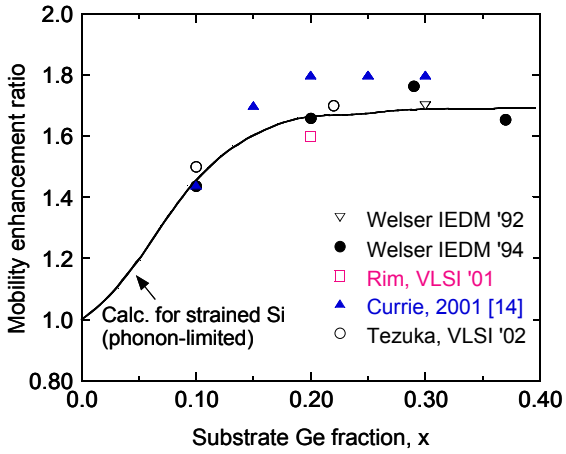
Electron mobility enhancement: Biaxial

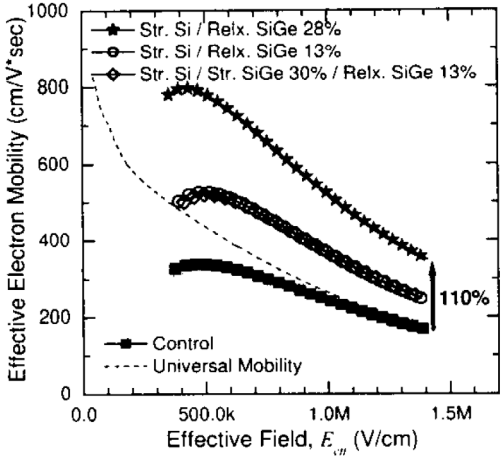












Welser – Stanford
IEDM 1992/1994 [30]
Strained Si/
Relaxed SiGe

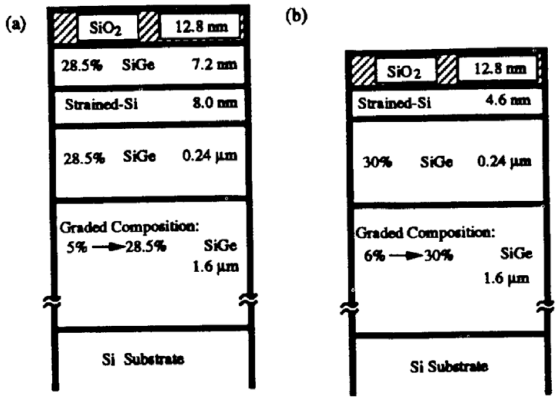
Hoyt – MIT
IEDM 2002 [31]
Strained Si/
Relaxed SiGe

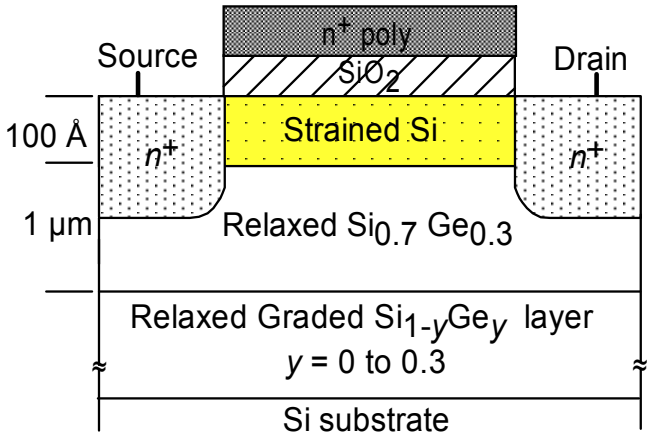
Rim – IBM
VLSI 2002 [32]
Strained Si/
Relaxed SiGe

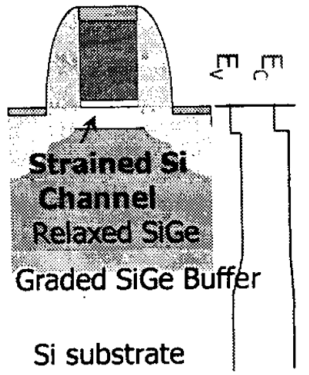
Electron mobility ent:

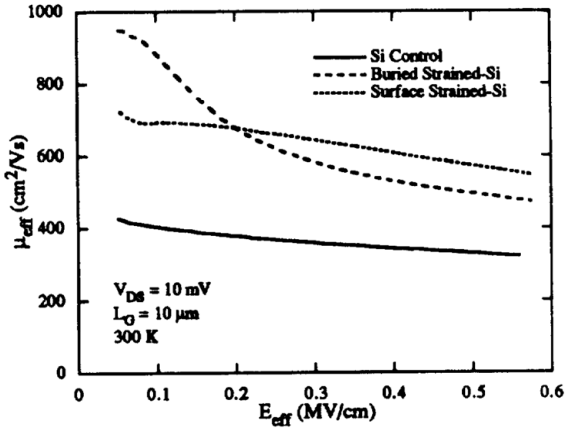
Further quantifying the strain enhancement, including vertical effective field and doping

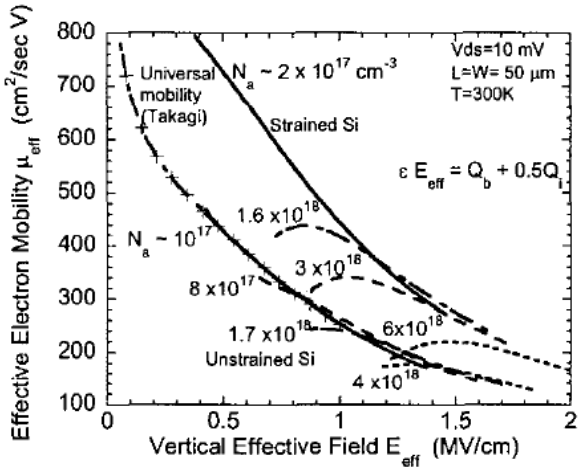
Exploring and controlling the lower VT associated with short channel strained NMOS

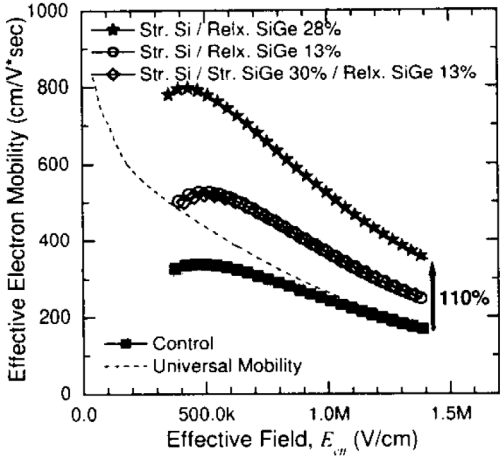










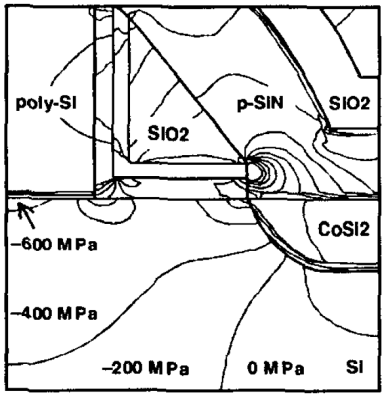


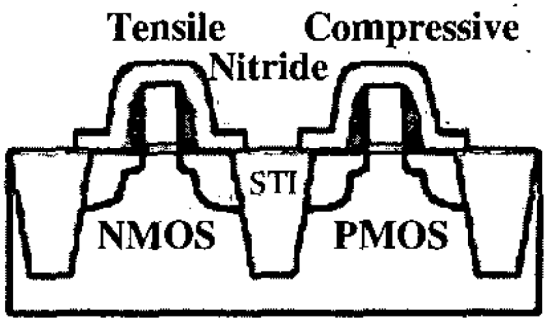
Welser – Stanford
IEDM 1992/1994 [30]
Strained Si/
Relaxed SiGe

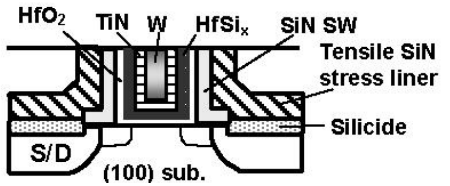
Hoyt – MIT
IEDM 2002 [31]
Strained Si/
Relaxed SiGe

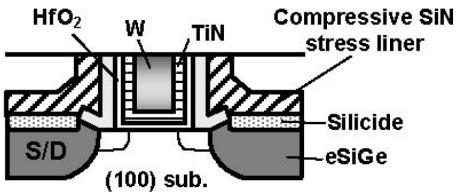
Rim – IBM
VLSI 2002 [32]
Strained Si/
Relaxed SiGe

Etch-stop nitride (CESL)

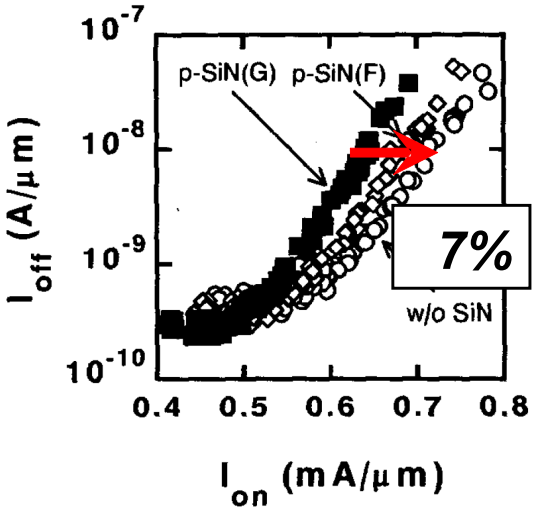


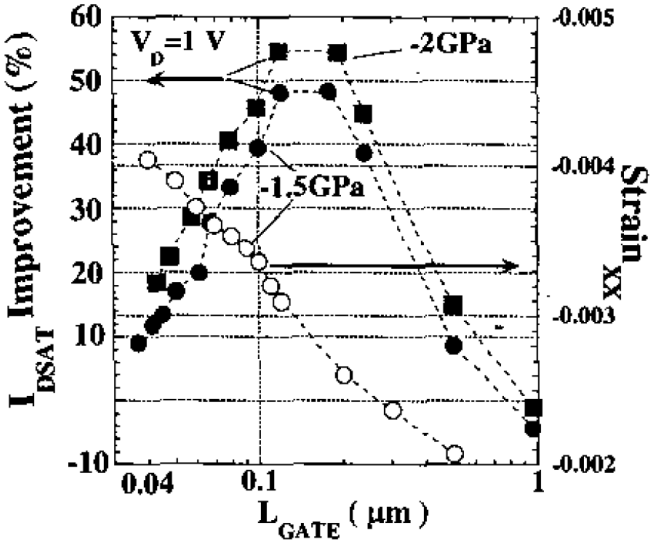


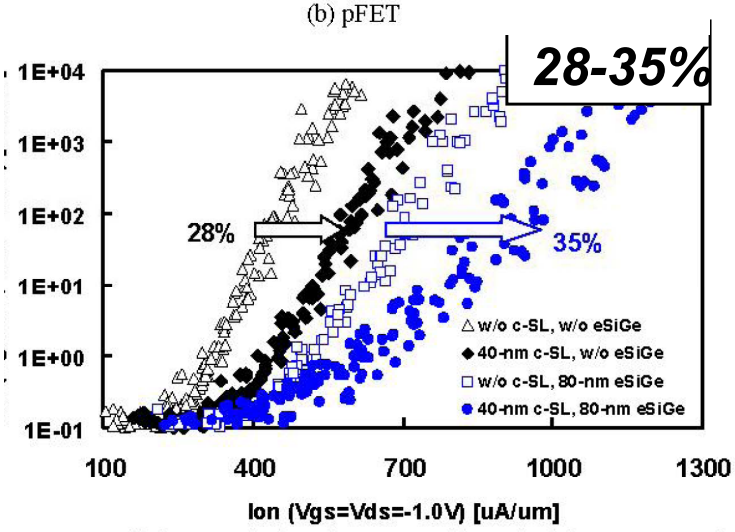




(b) pFET





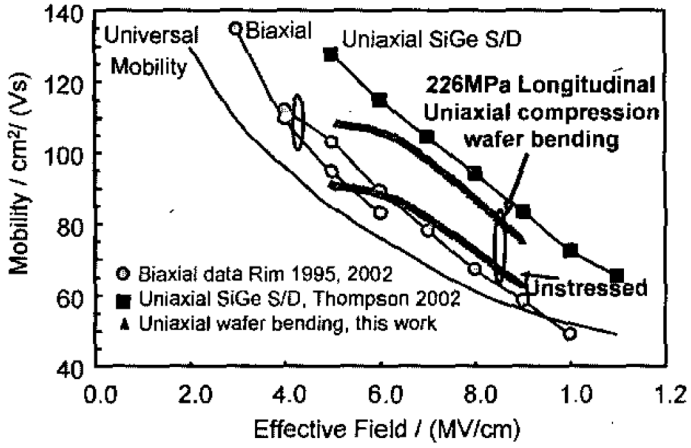


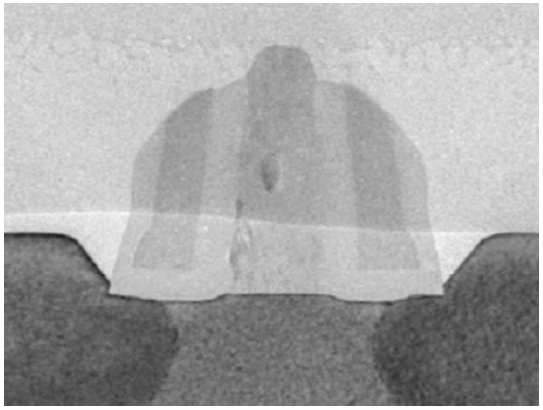
Ito – NEC
IEDM 2000 [33]
NMOS SiN strain

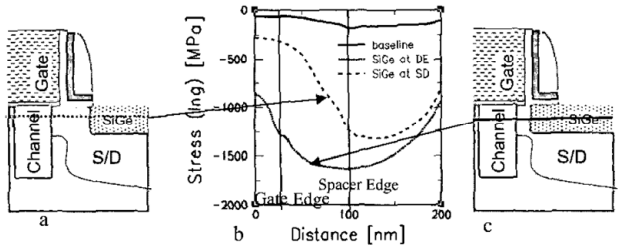
Pidin – Fujitsu
IEDM 2004 [34]
N and PMOS

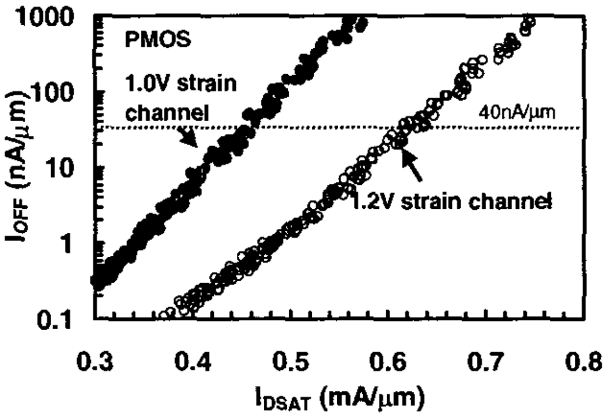
Mayuzumi – Sony
IEDM 2007 [35]
Dual-cut stress liners
(MG process)

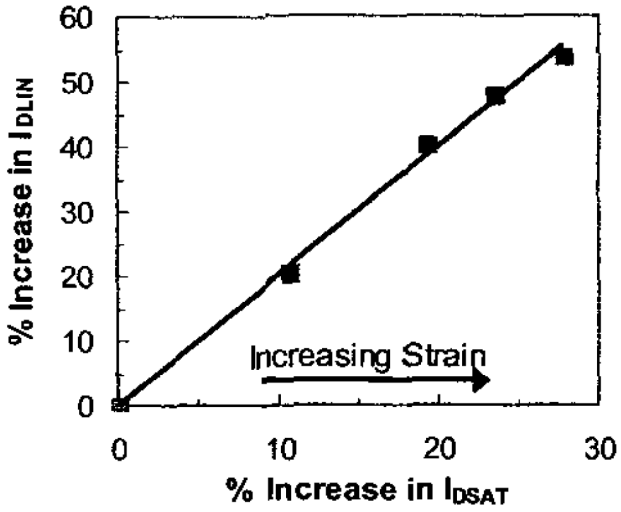
Embedded SiGe (PMOS)

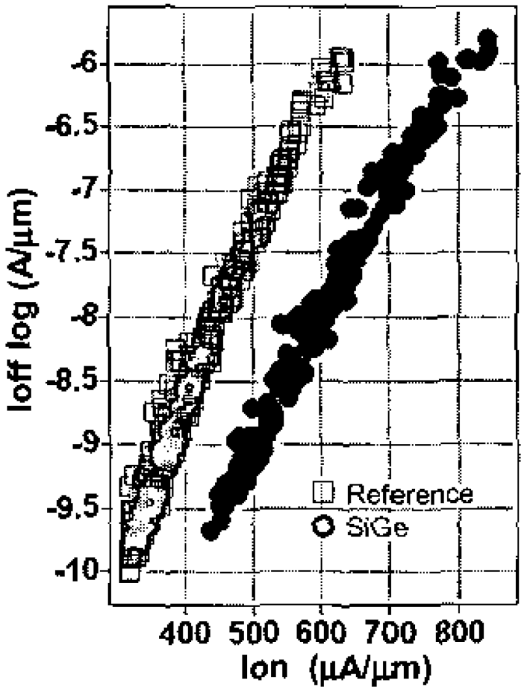










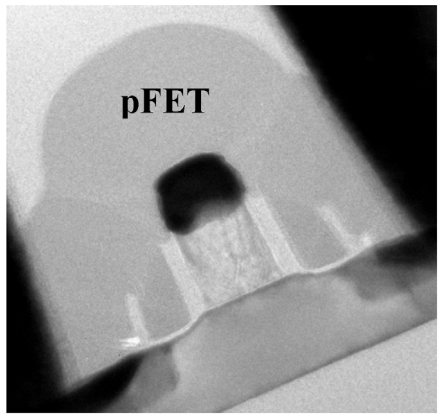


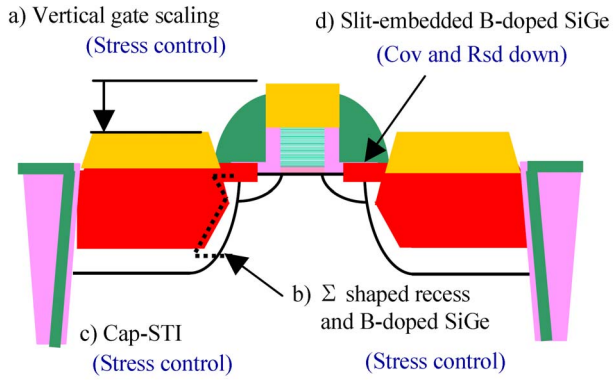
Thompson – Intel
IEDM 2002 / 2004 [6]

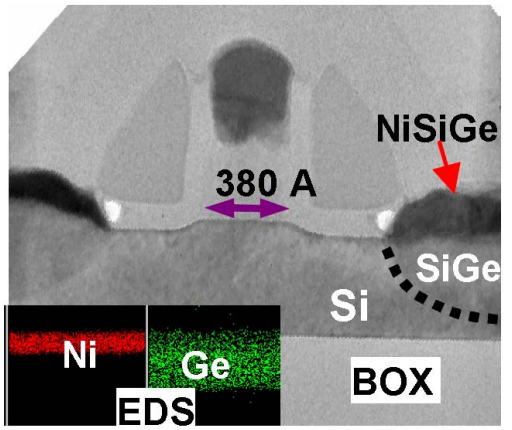
Ghani – Intel
IEDM 2003 [36]

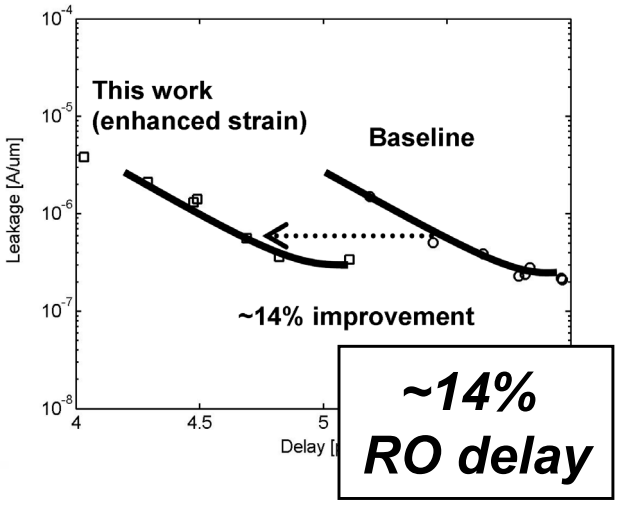
Chidambaram
TI / Applied Materials
VLSI - 2004 [37]

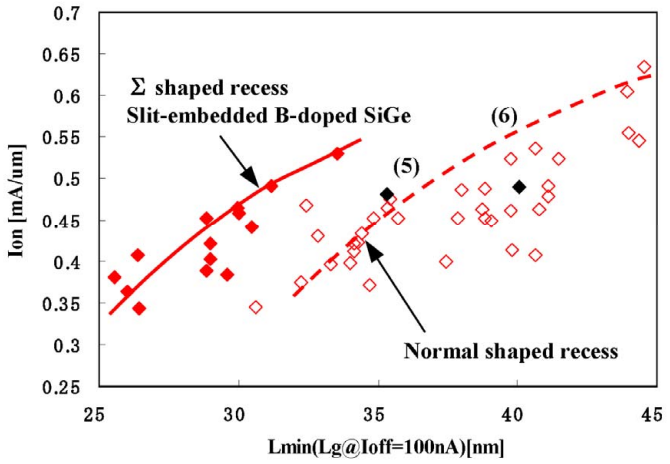
Embedded SiGe (PMOS)

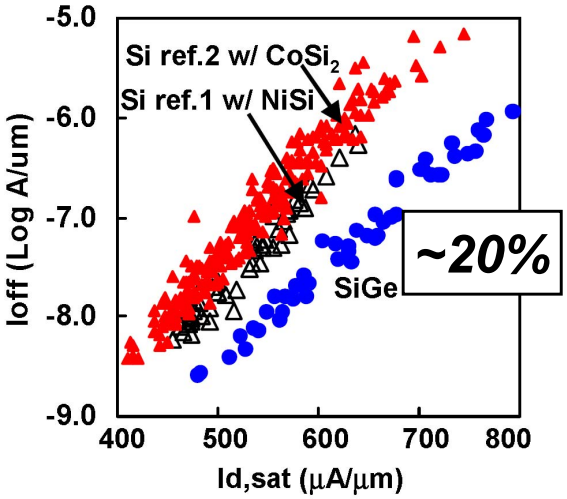










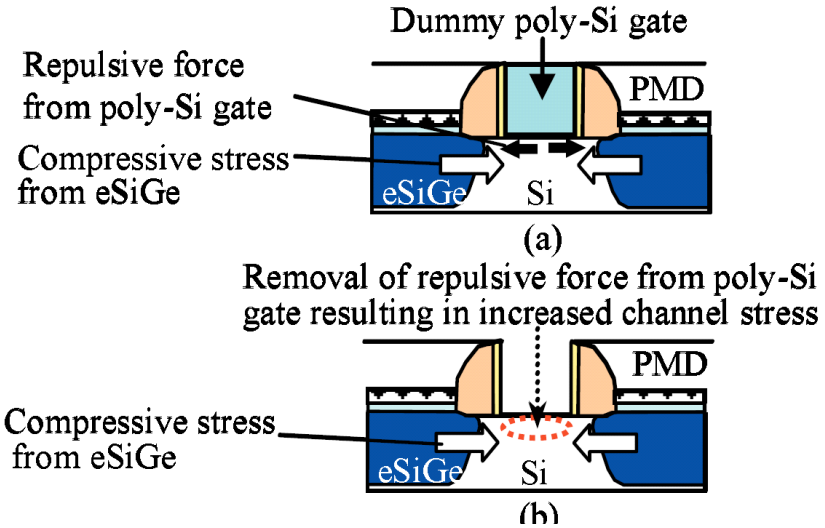


Lee - IBM
IEDM 2005 [38]
SOI and e-SiGe

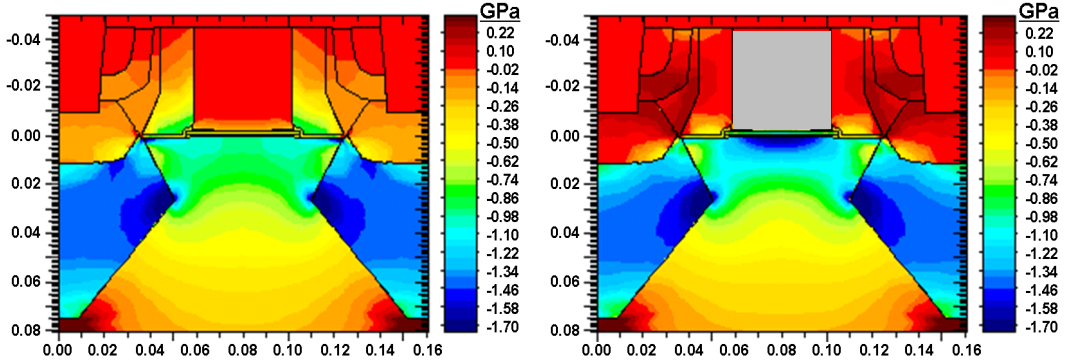
Ohta – Fujitsu
IEDM 2005 [39]
Profile engr.

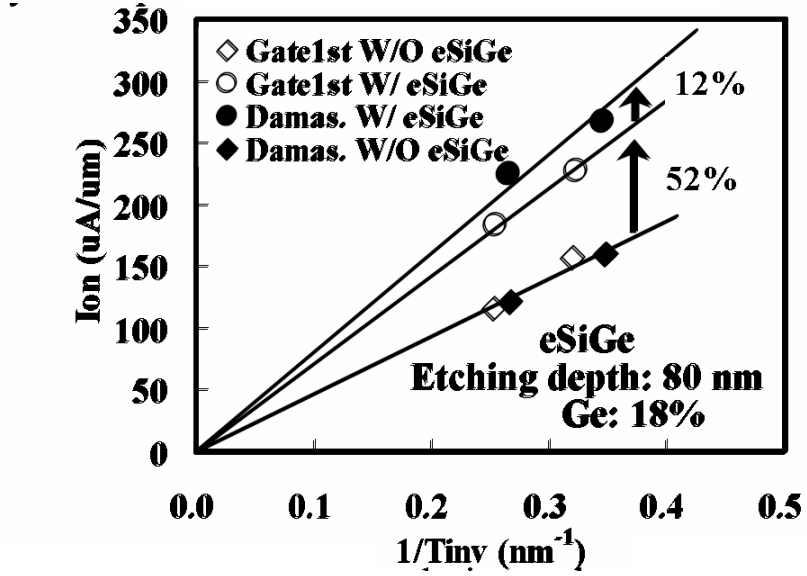
Zhang – Freescale
VLSI 2005 [40]
Thin body SOI

Enhanced PMOS strain: Gate last HiK-MG

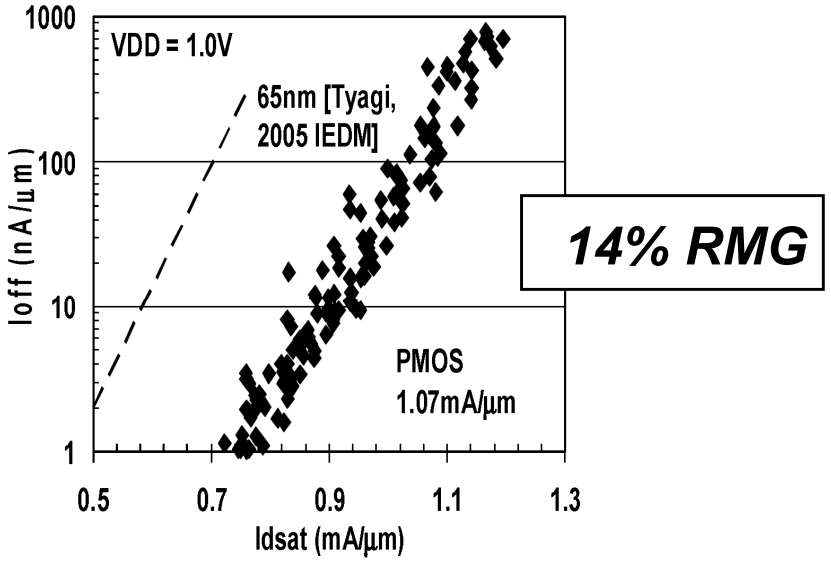


Before gate removal **After gate removal**



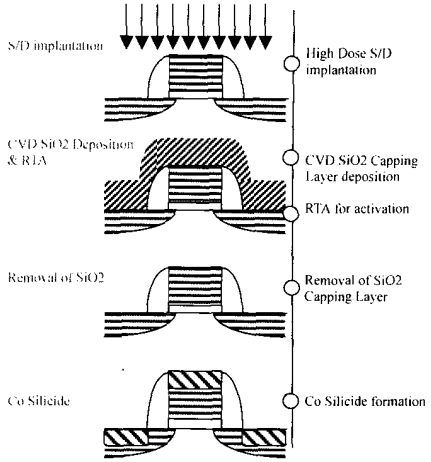


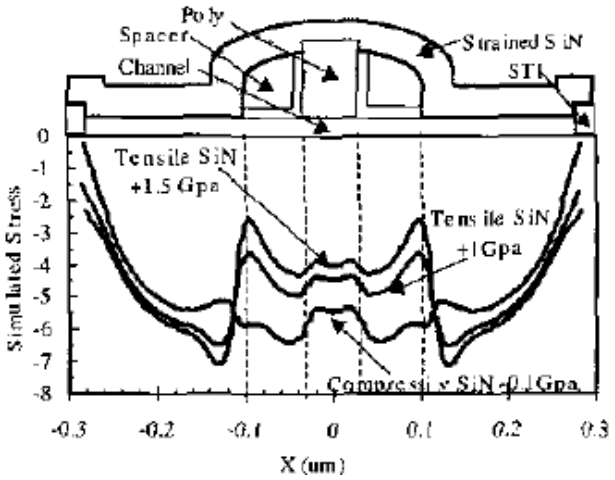
Wang – Sony
VLSI 2007 [41]

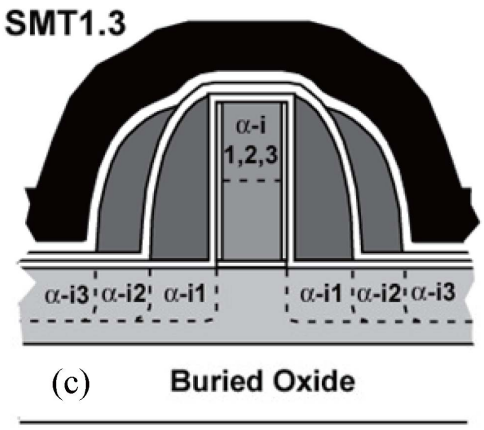


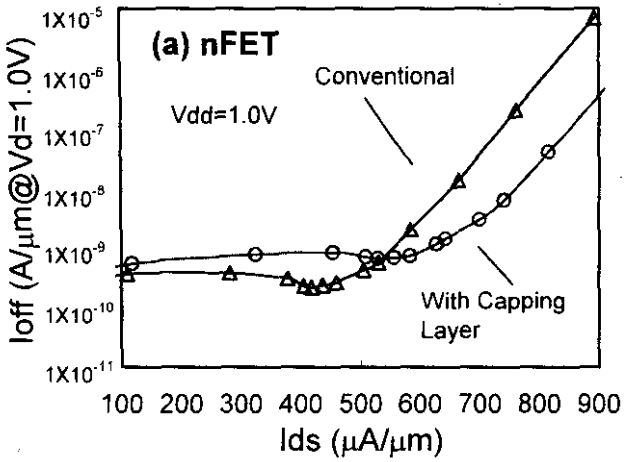
Auth – Intel
VLSI 2008 [23]

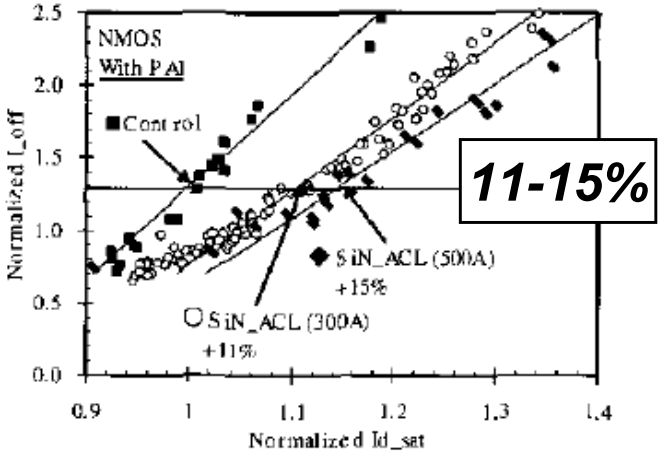
Stress Memorization (SMT)

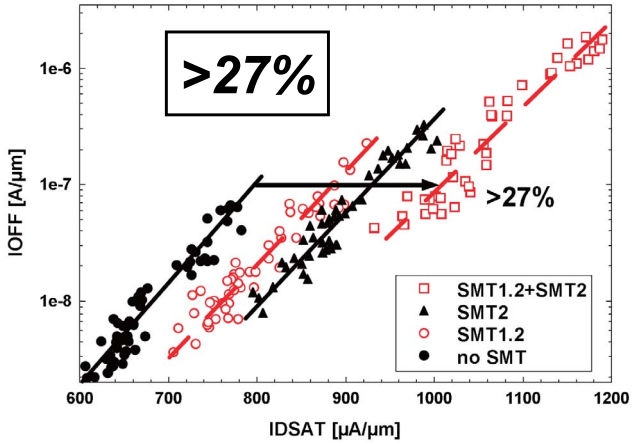












Ota – Mitsubishi
IEDM 2002 [42]
NMOS SMT

Chen – TSMC
VLSI 2004 [43]
NMOS SMT

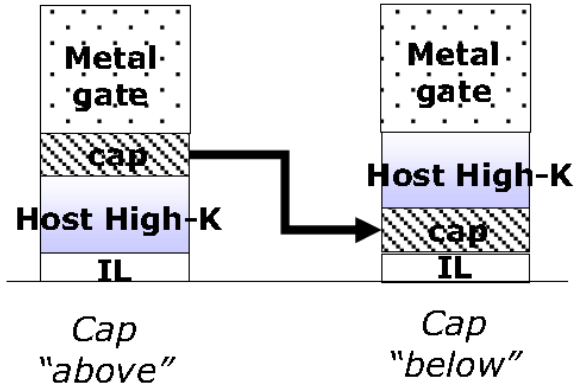
Wei – AMD
VLSI 2007 [44]
Multiple liners

SMT enhancement with HiK-MG
Kubicek – IMEC – VLSI 2008 [45]

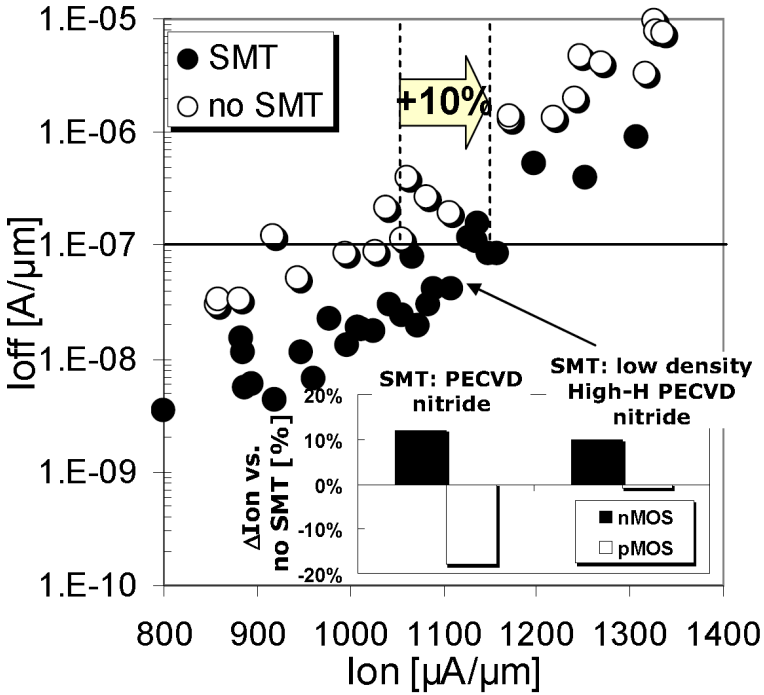
Strain enhanced Low-V_T CMOS featuring La/Al-doped HfSiO/TaC and 10ps Invertor Delay

S. Kubicek, T.Schram, E.Rohr, V.Paraschiv, R.Vos, M.Demand, C.Adelmann, T.Witters, L.Nyns, A.Delabie , L.-Å.Ragnarsson, T.Chiarella, C.Kerner, A.Mercha, B.Parvais, M.Aoulaiche†, C.Ortolland, H.Yu, A.Veloso, L.Witters, R.Singanamalla†, T. Kauerauf†, S.Brus, C.Vrancken, V.S.Chang[1], S-Z.Chang[1], R.Mitsuhashi[2], Y.Okuno[2], A.Akheyar[3], H.-J.Cho[4], J.Hooker[5], B. J. O'Sullivan, S.Van Elshocht, K.De Meyer†, M.Jurczak, P.Absil, S.Biesemans and T.Hoffmann

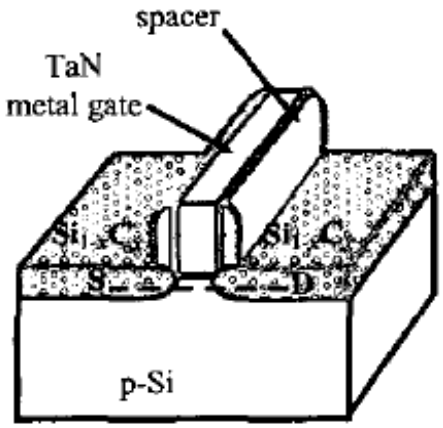
- STI
- 1st high-k
- 1st dielectric cap
- 1st metal + HM
- selective dry/wet etch
- 2nd high-k
- 2nd dielectric cap
- 2nd metal + HM
- selective dry etch
- gate etch
- . . .

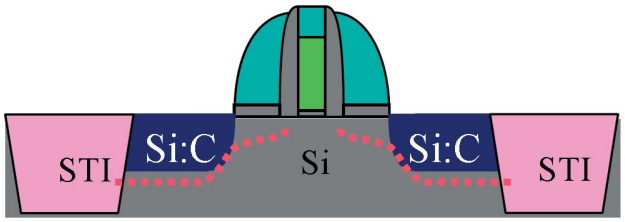


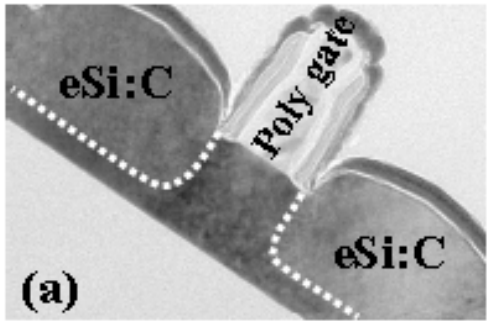
From the paper: *"…* the gain from traditional stress boosters (CESL, embedded-SiGe, channel orientation) was maintained on High-κ/Metal gate.."

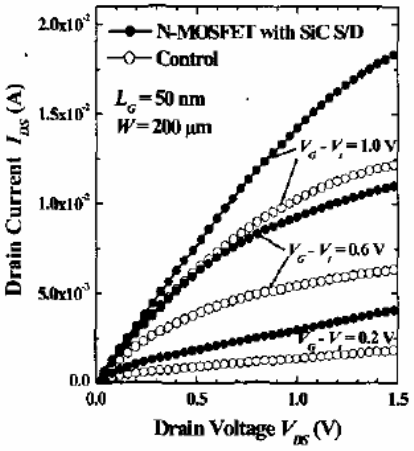


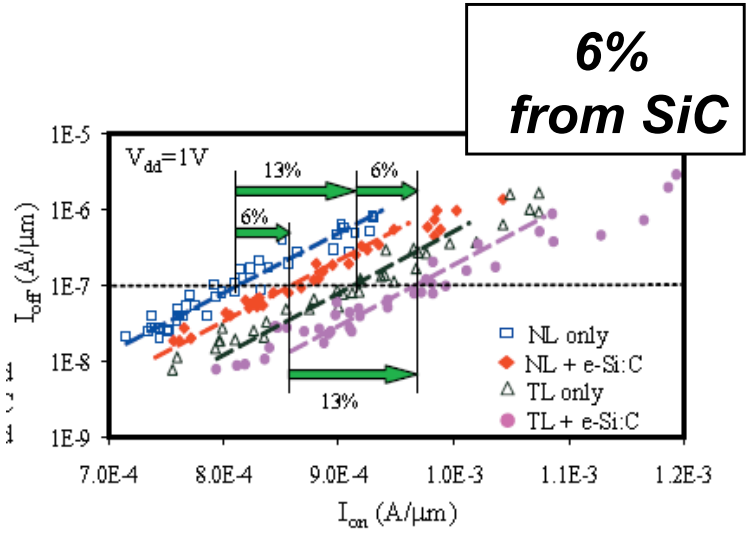
Embedded Si:C (NMOS)

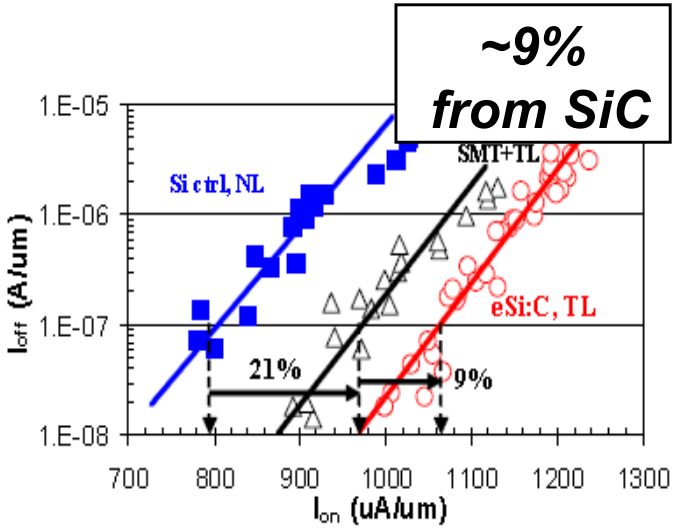










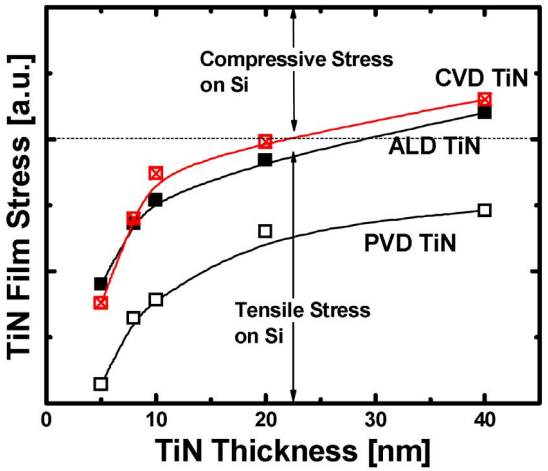


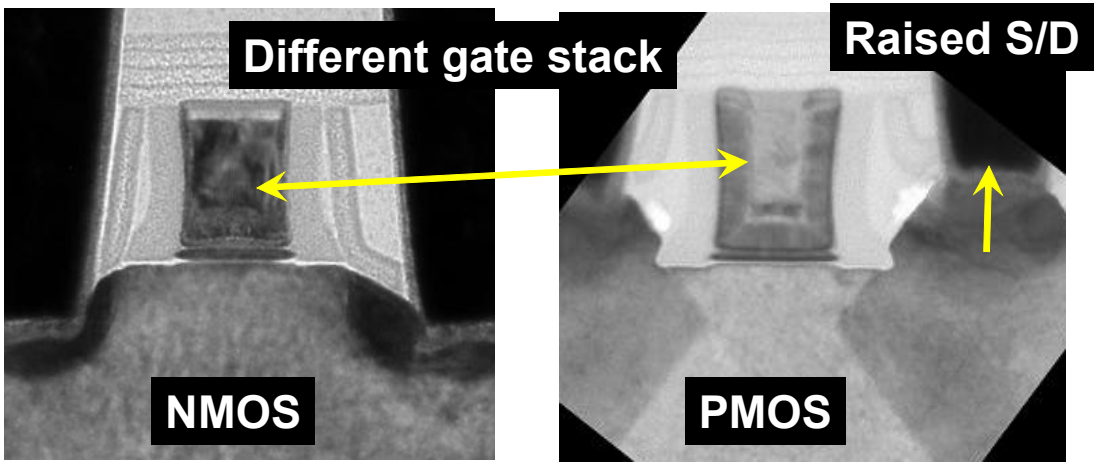
Ang – NUS-Singapore
IEDM 2004 [46]
Selective epi SiC (undoped)

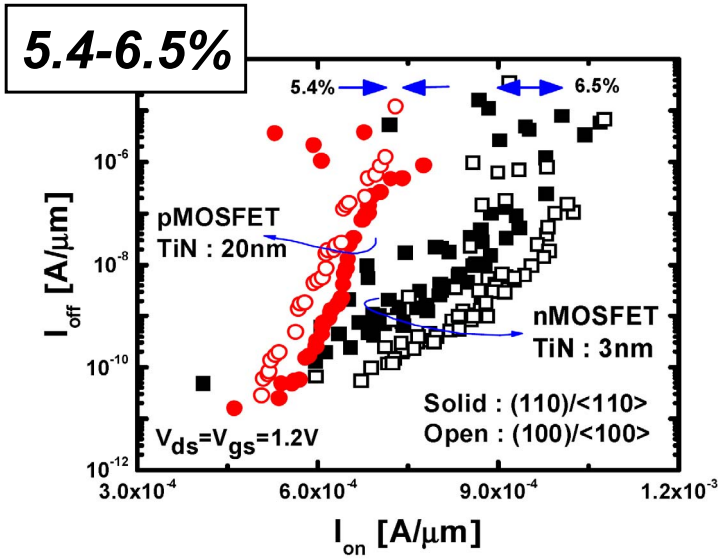
Liu – IBM
VLSI 2007 [47]
Implant + SPE

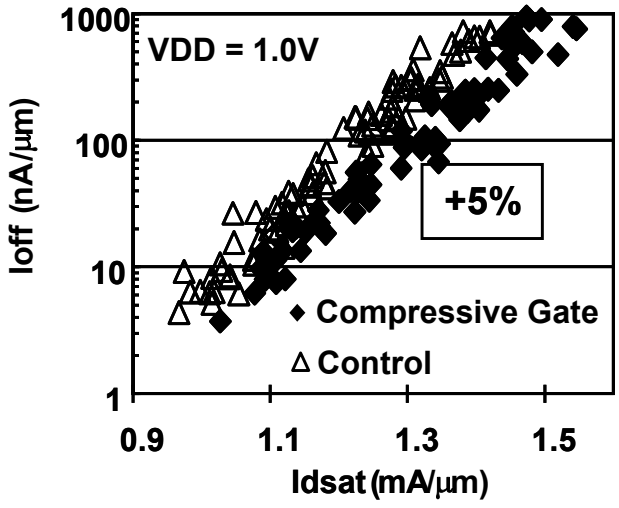
Yang – IBM
IEDM 2008
In-situ epi P-SiC

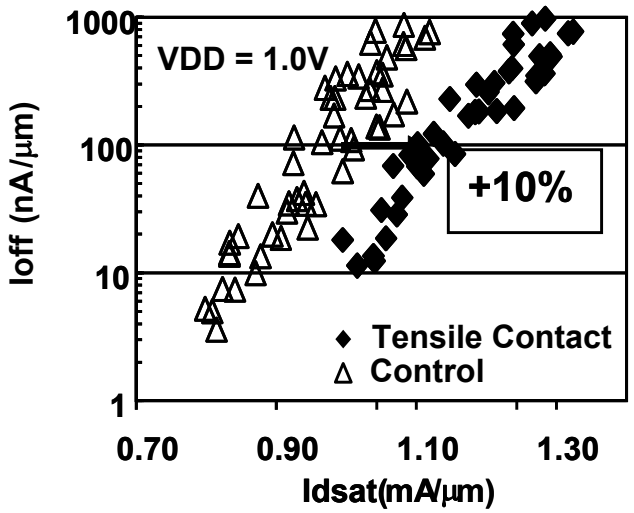
Metal stress (gate and contact)











Kang – Sematech
IEDM 2006 [49]

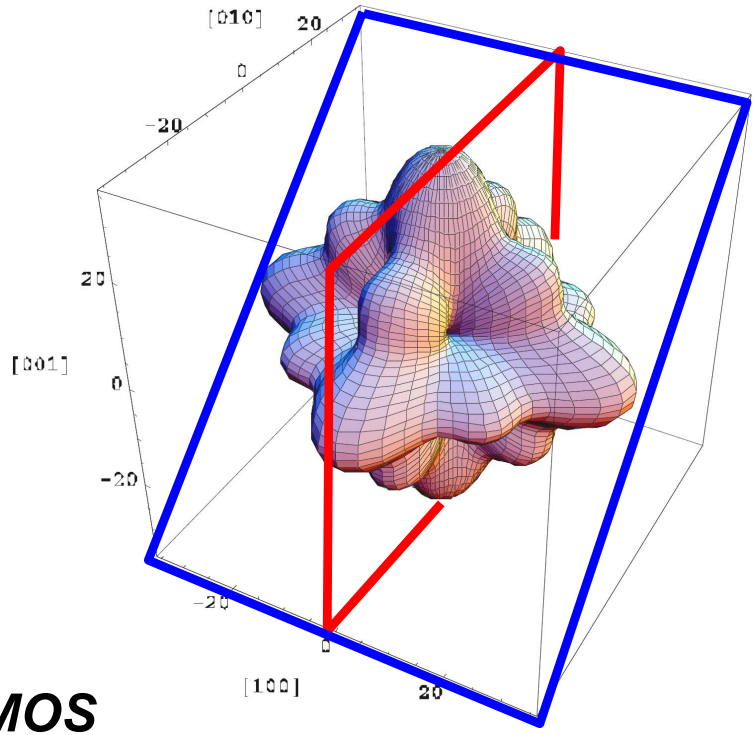
Auth – Intel
VLSI 2008 [23]

Agenda

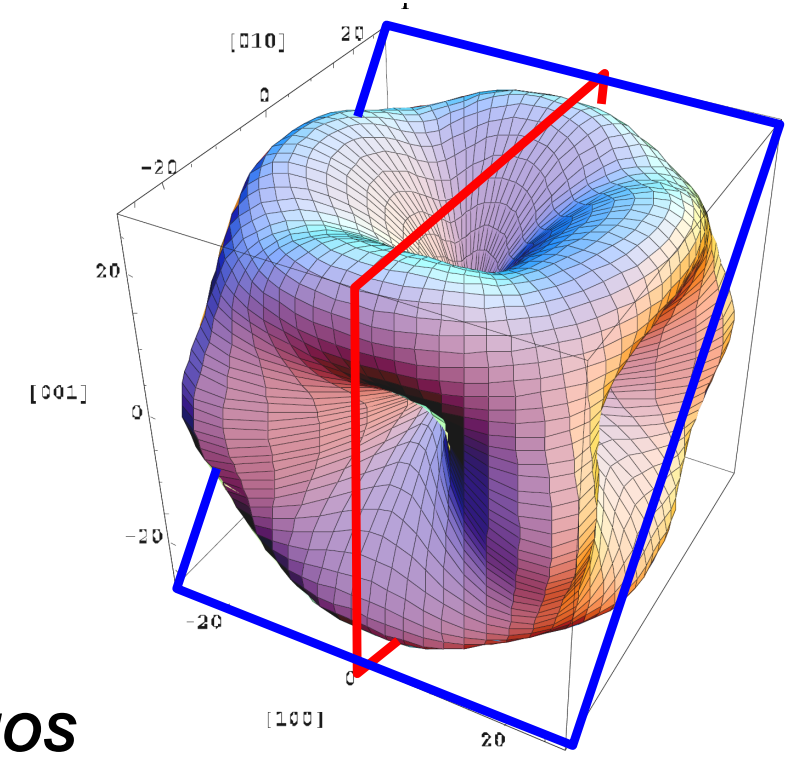
- History
- Architecture
- Capacitance
- Resistance
- HiK-MG
- Orientation
- Strain
- Strain + Orientation
- Summary

Strain and Orientation
Piezoresistive coefficient as a function of direction

Udo – Infineon – Proc. IEEE Sensors 2004



NMOS

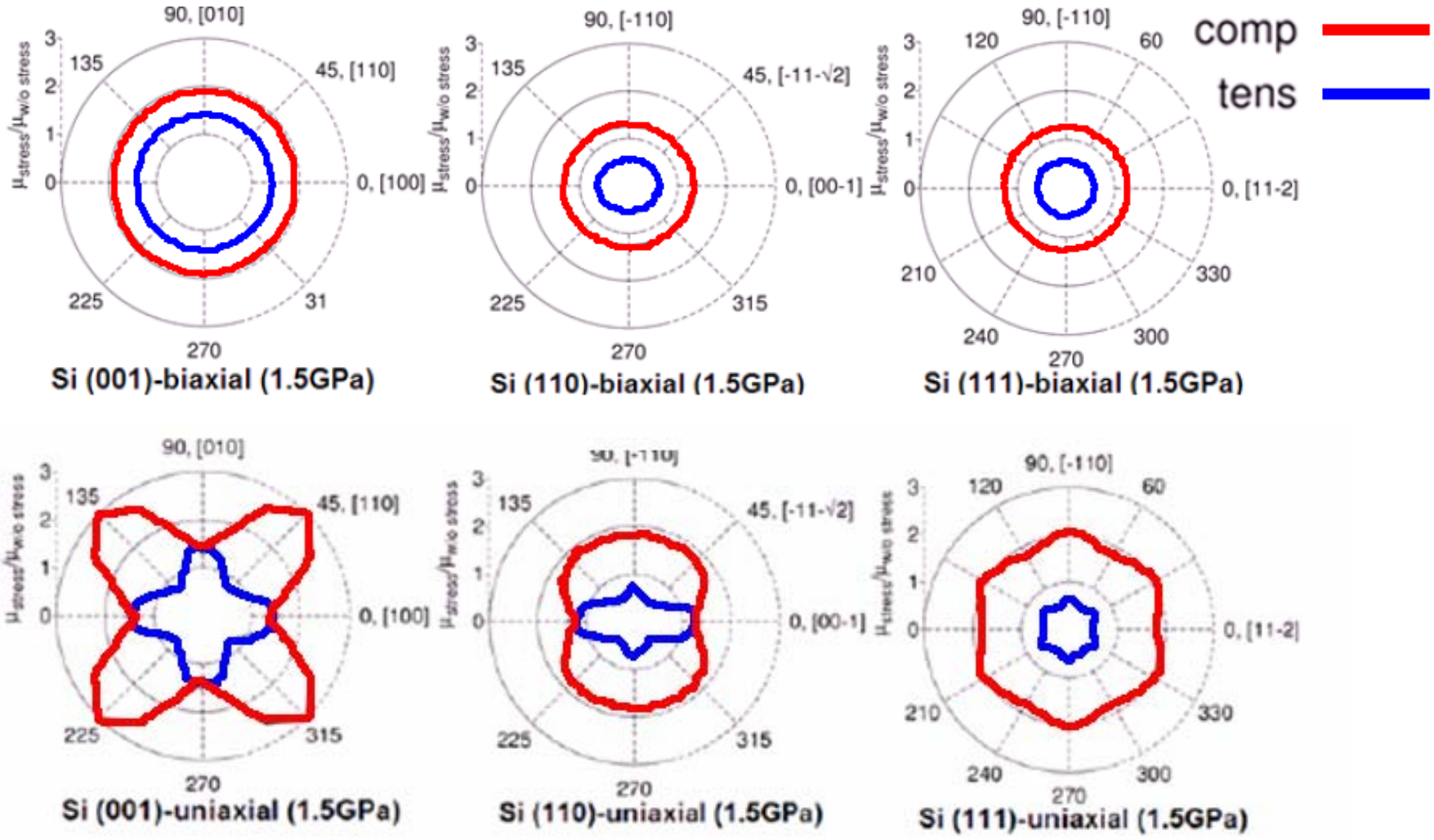


PMOS

Krishnamohan – Stanford – IEDM 2008

Comparison of (001), (110) and (111) Uniaxial- and Biaxial- Strained-Ge and Strained-Si PMOS DGFETs for All Channel orientations: Mobility Enhancement, Drive Current, Delay and Off-State Leakage

[1,4]Tejas Krishnamohan, [1]Donghyun Kim, [2]Thanh Viet Dinh, [3]Anh-tuan Pham,
[3]Bernd Meinerzhagen, [2]Christoph Jungemann, [1]Krishna Saraswat



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- History
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"Looking in the Crystal Ball"

CHANGE	COMMENTS
Further enhancements in strain technology	Low risk – evolutionary change – large suite of proven successful options
Further enhancements in HiK-MG technology	Low risk – continual improvement – driven by strong research/development efforts
Optimized substrate and channel orientation	Medium risk – requires some solution to the (100)<110>N vs (110)/<110>P issue
Reduction in MOS parasitic resistance	Medium risk – new annealing technologies, RE/NM silicide options
Reduction in MOS parasitic capacitance	Medium-high risk – low-k FE dielectrics pose significant process challenges
MuGFETs	High risk – significant challenges with parasitic R, parasitic C and strain

Q&A