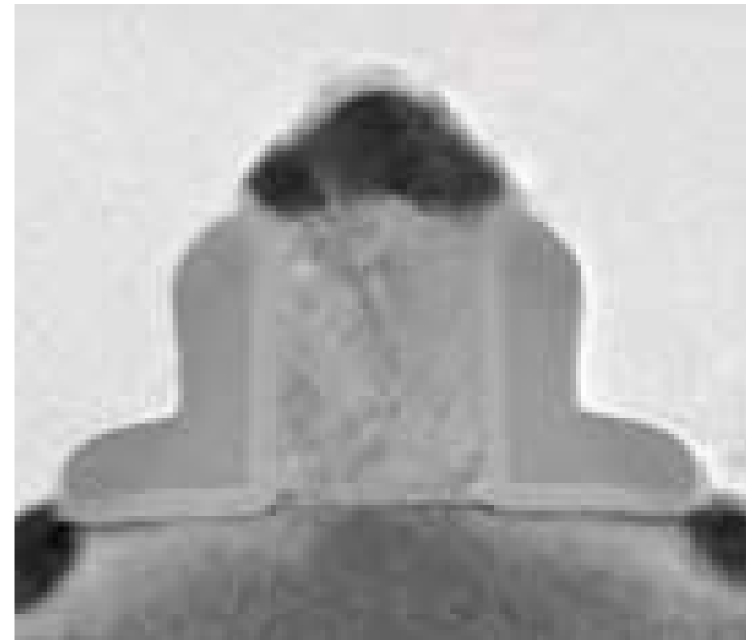
Moore's Law past 32nm: Future Challenges in Device Scaling

Kelin J. Kuhn
Intel Fellow
Director of Advanced Device Technology
Intel Corporation

Future Challenges in Device Scaling

As near as I can tell: THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size



130 nm

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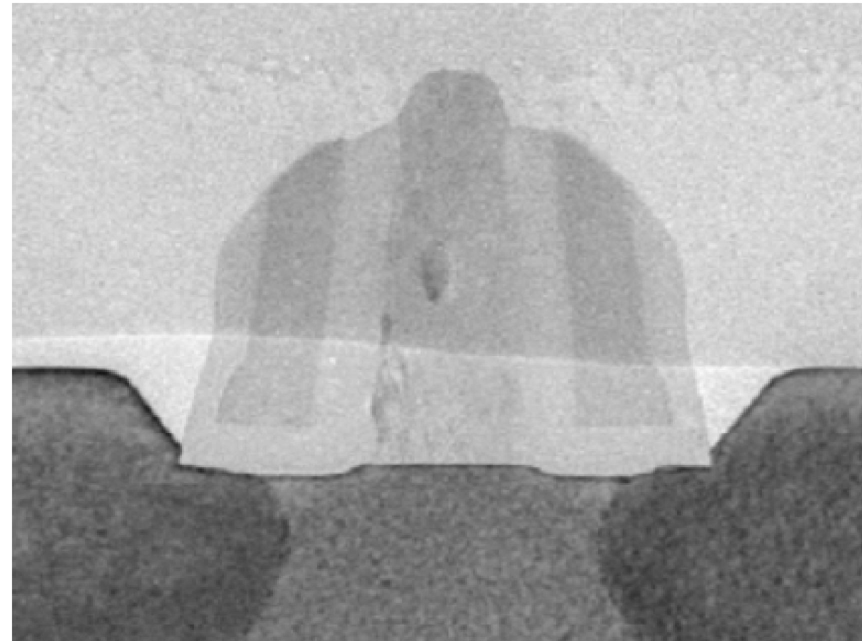

90 nm

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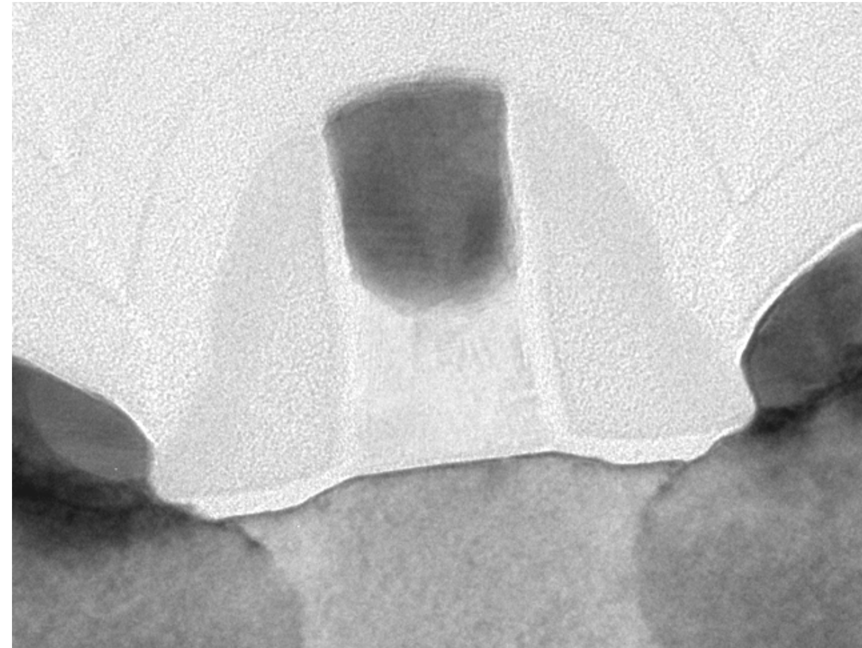

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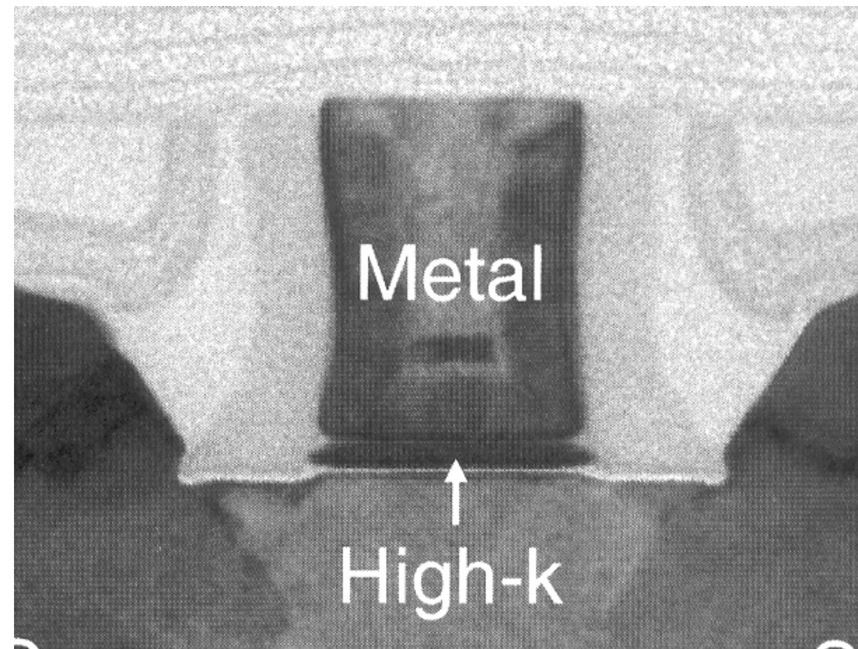

45 nm

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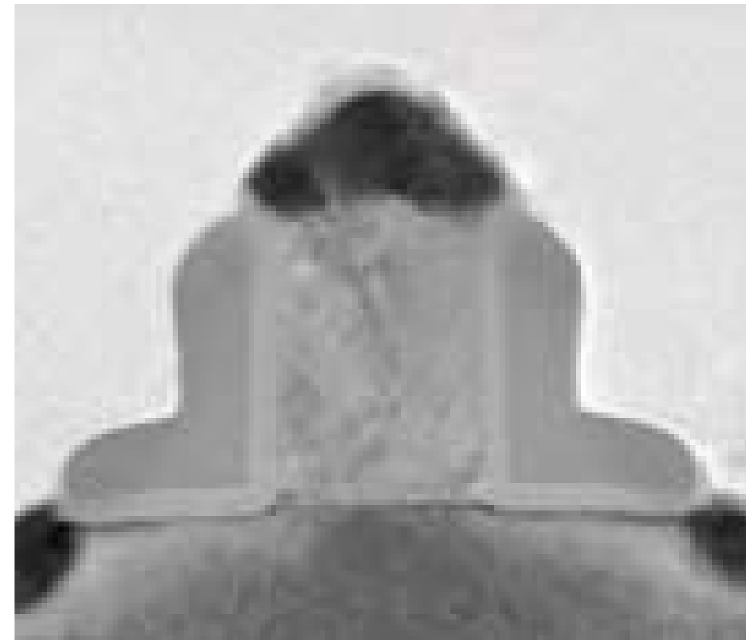

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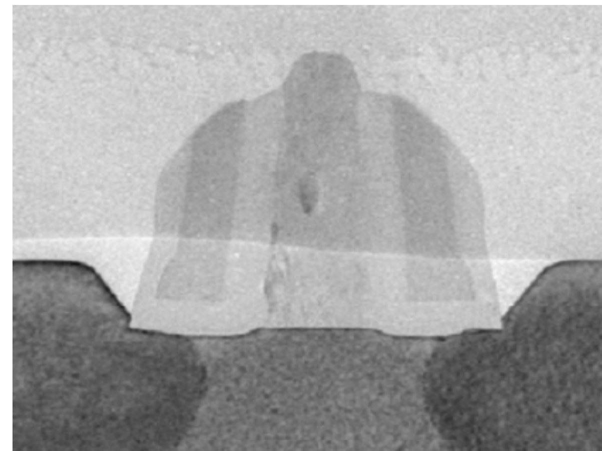

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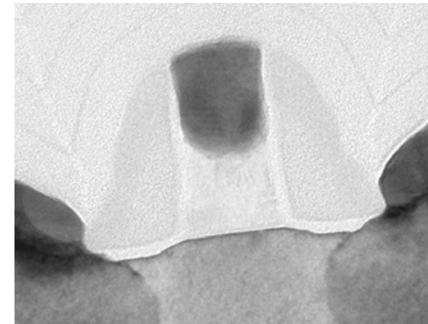

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K. Kuhn, MIT 2008

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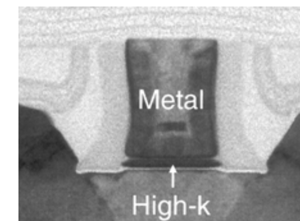

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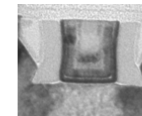

32 nm

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AGENDA

- Scaling history
- Gate control
  - High-k metal-gate
  - Structural enhancements
- Resistance
- Capacitance
- Mobility
  - Strain
  - Orientation
  - Advanced channel materials
- Summary

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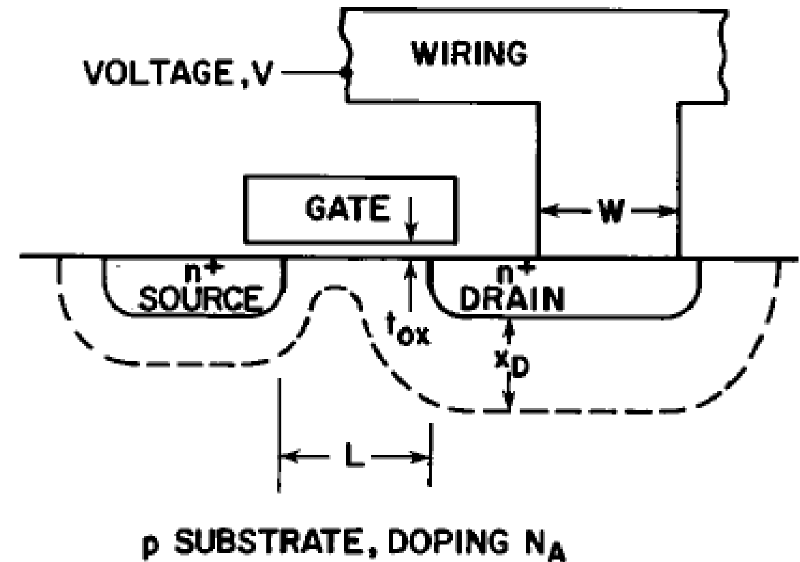
MOSFET Scaling

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	$1/\kappa$
Doping concentration *Na*	κ
Voltage *V*	$1/\kappa$
Current *I*	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit *VC/I*	$1/\kappa$
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1



R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling was first described by Dennard in 1974

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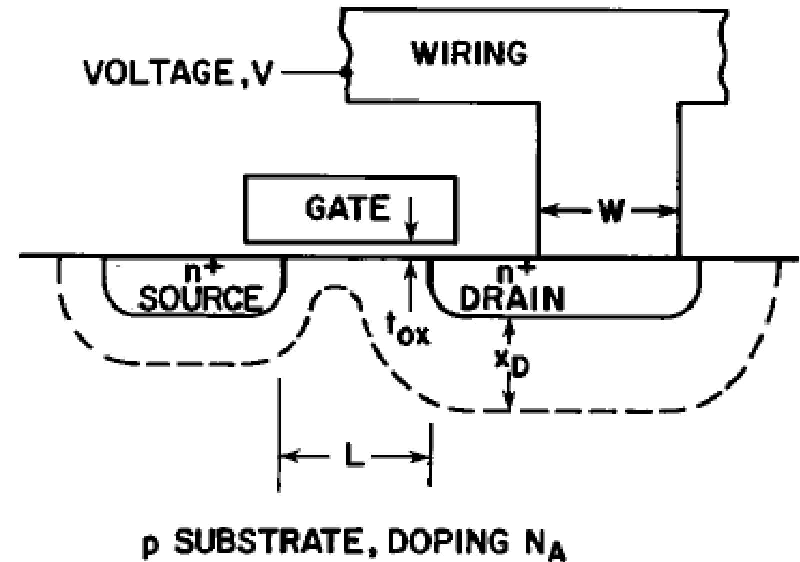
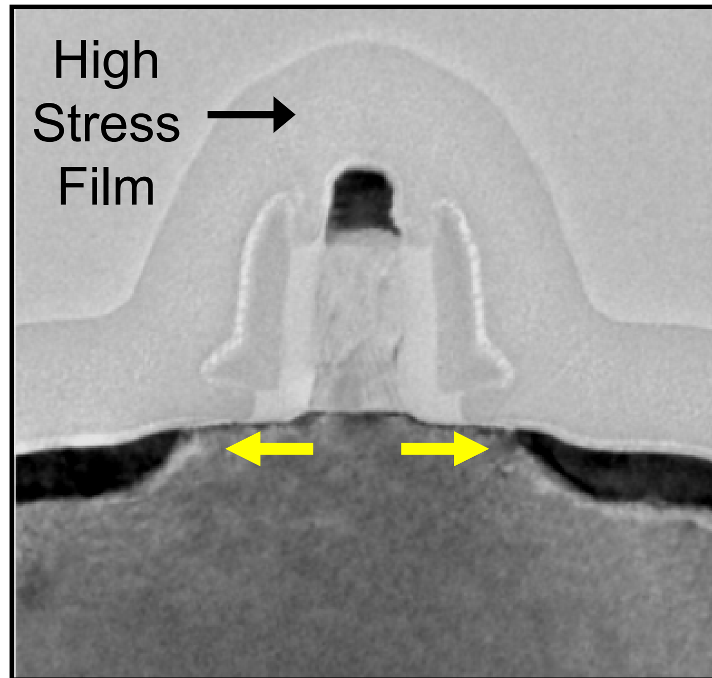


R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling ENDED at the 130nm node (and nobody noticed …)

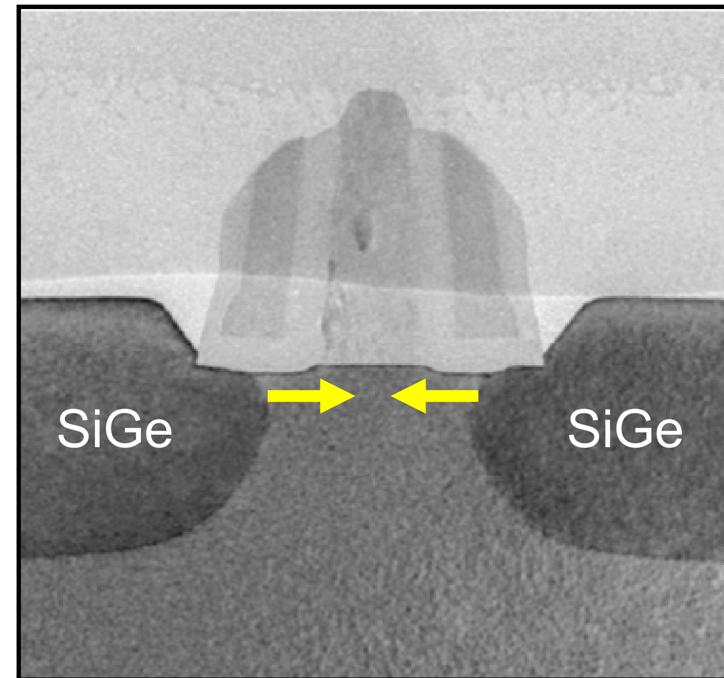
90 nm Strained Silicon Transistors

NMOS



SiN cap layer
Tensile channel strain

PMOS

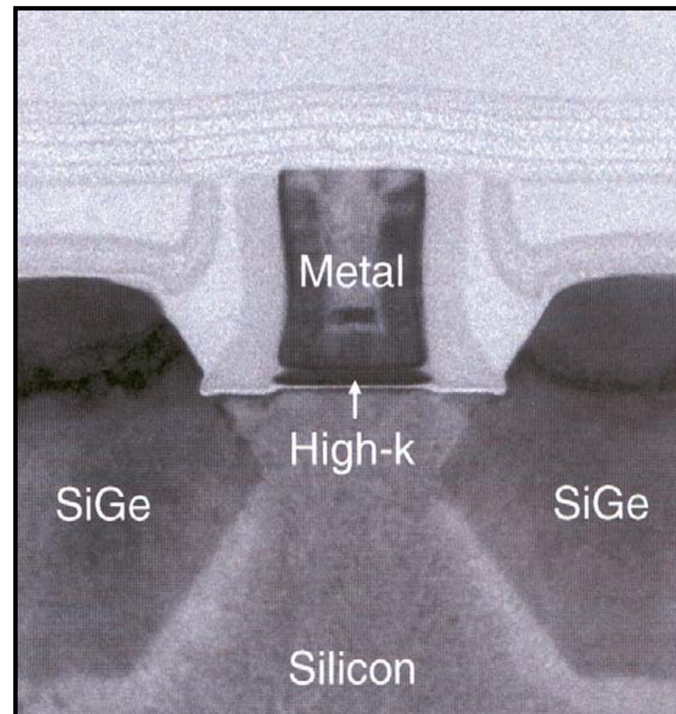


SiGe source-drain
Compressive channel strain

Strained silicon provided increased drive currents, making up for the loss of classical Dennard scaling

45nm High-k + Metal Gate Transistors

45 nm HK+MG



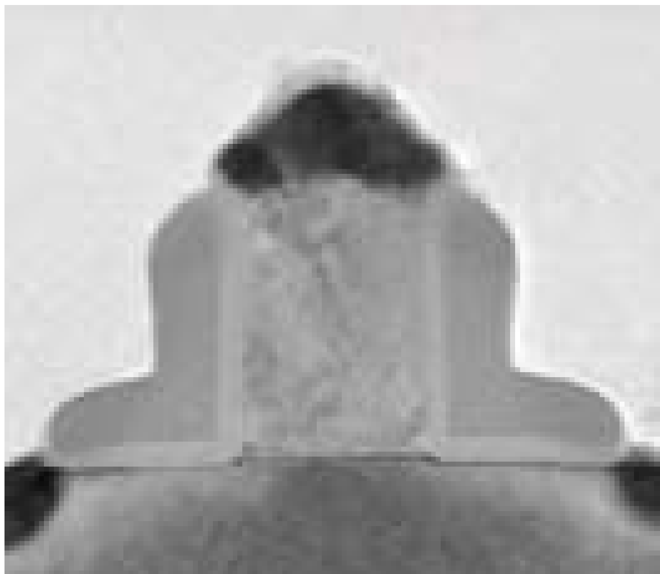
Hafnium-based dielectric
Metal gate electrode

High-k + metal gate transistors restored gate oxide scaling at the 45nm node

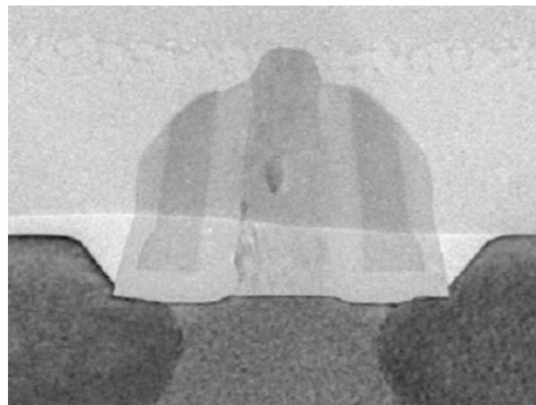
Changes in Scaling

THEN

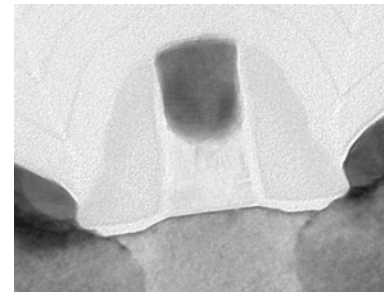
- Scaling drove down cost
- Scaling drove performance
- Performance constrained
- Active power dominates
- Independent design-process



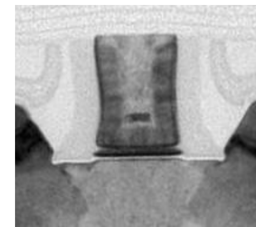
130nm



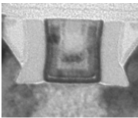
90nm



65nm



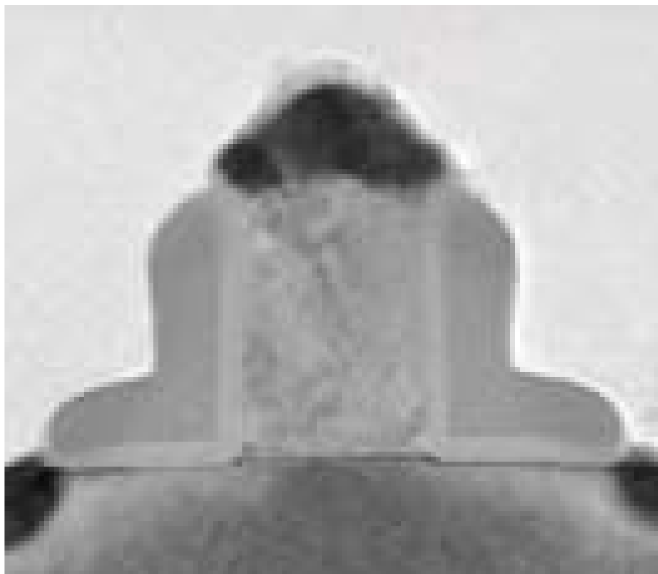
45nm



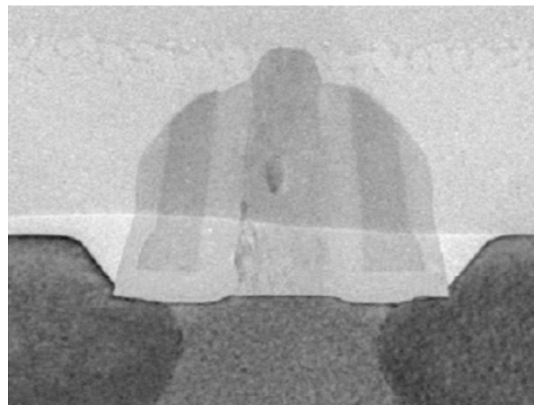
32nm

Changes in Scaling

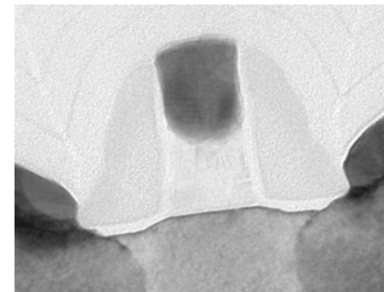
THEN	NOW
• Scaling drove down cost	• Scaling drives down cost
• Scaling drove performance	• Materials drive performance
• Performance constrained	• Power constrained
• Active power dominates	• Standby power dominates
• Independent design-process	• Collaborative design-process



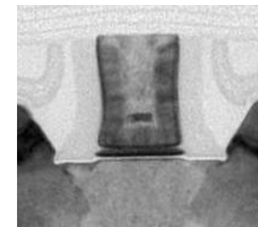
130nm



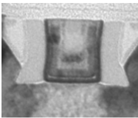
90nm



65nm



45nm



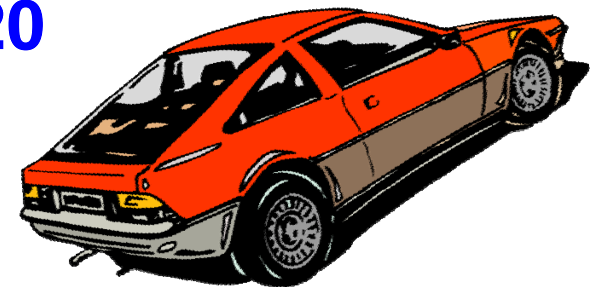
32nm

What if CARS
Were as Efficient as MICROPROCESSORS?

MIPS/watt: 1000, 100, 10, 1, 0.1

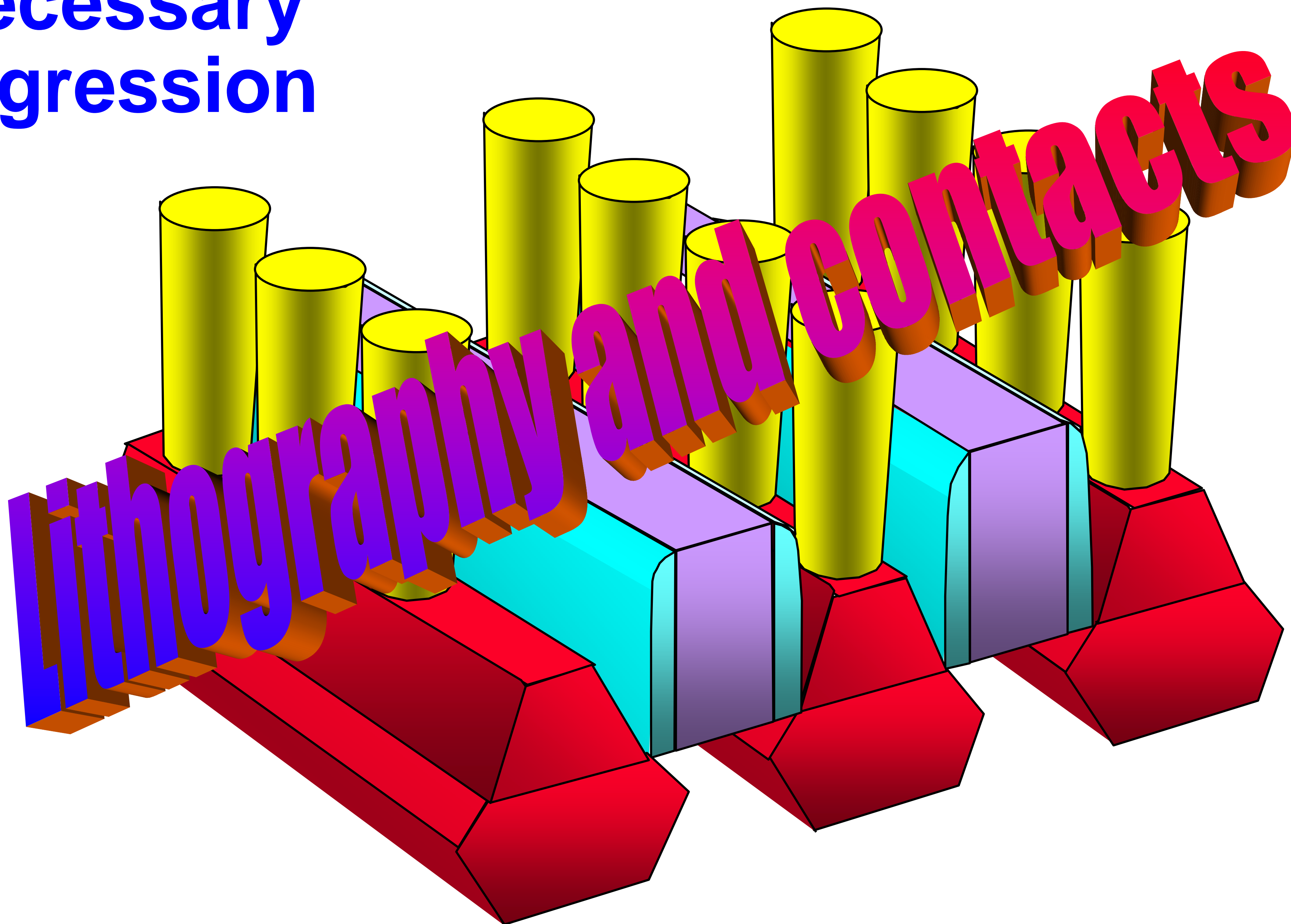
Miles per gallon: 100000, 10000, 1000, 100, 10, 1

YEAR: 1960, 1980, 2000, 2020

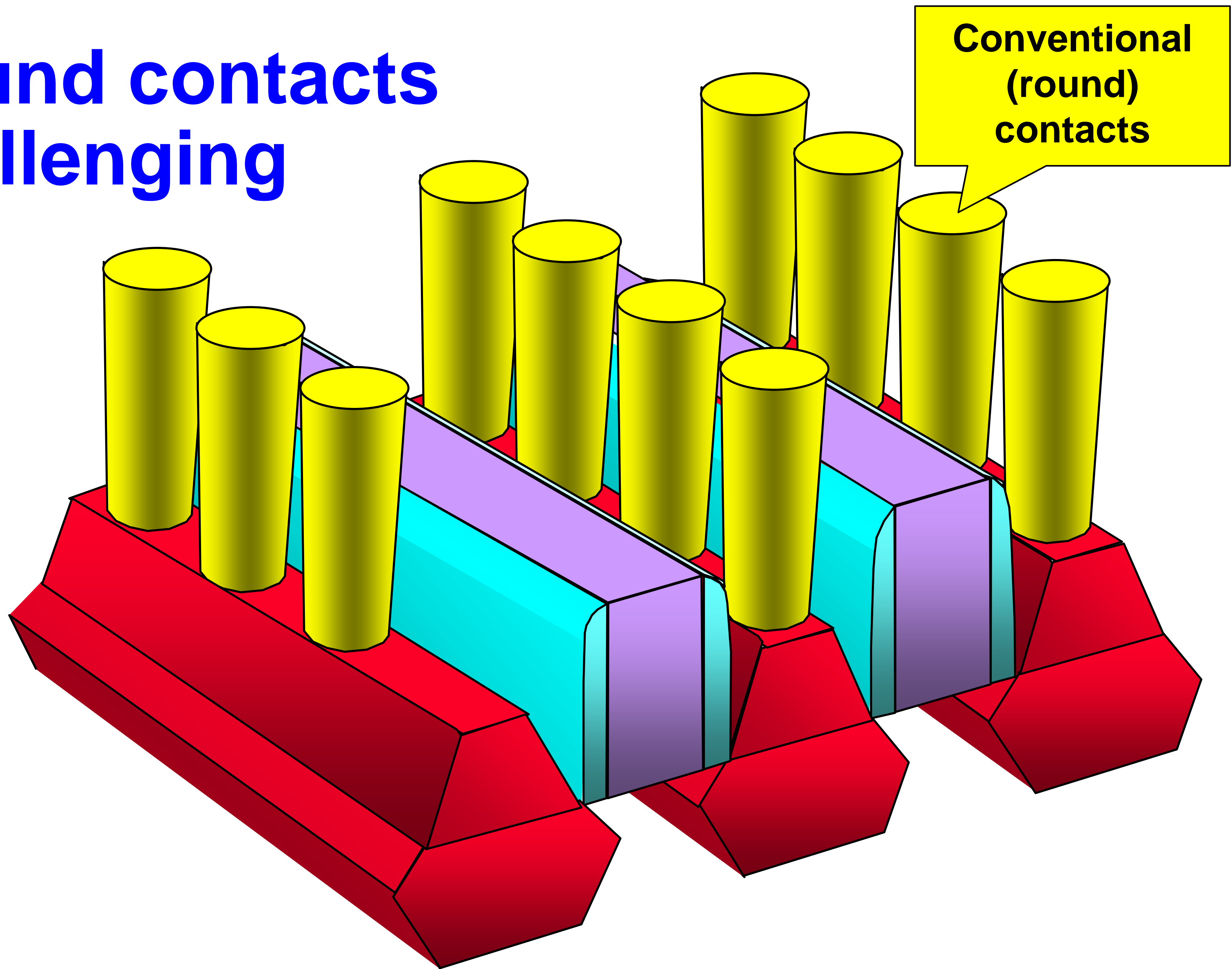


Images: © 2009 Jupiterimages Corp.

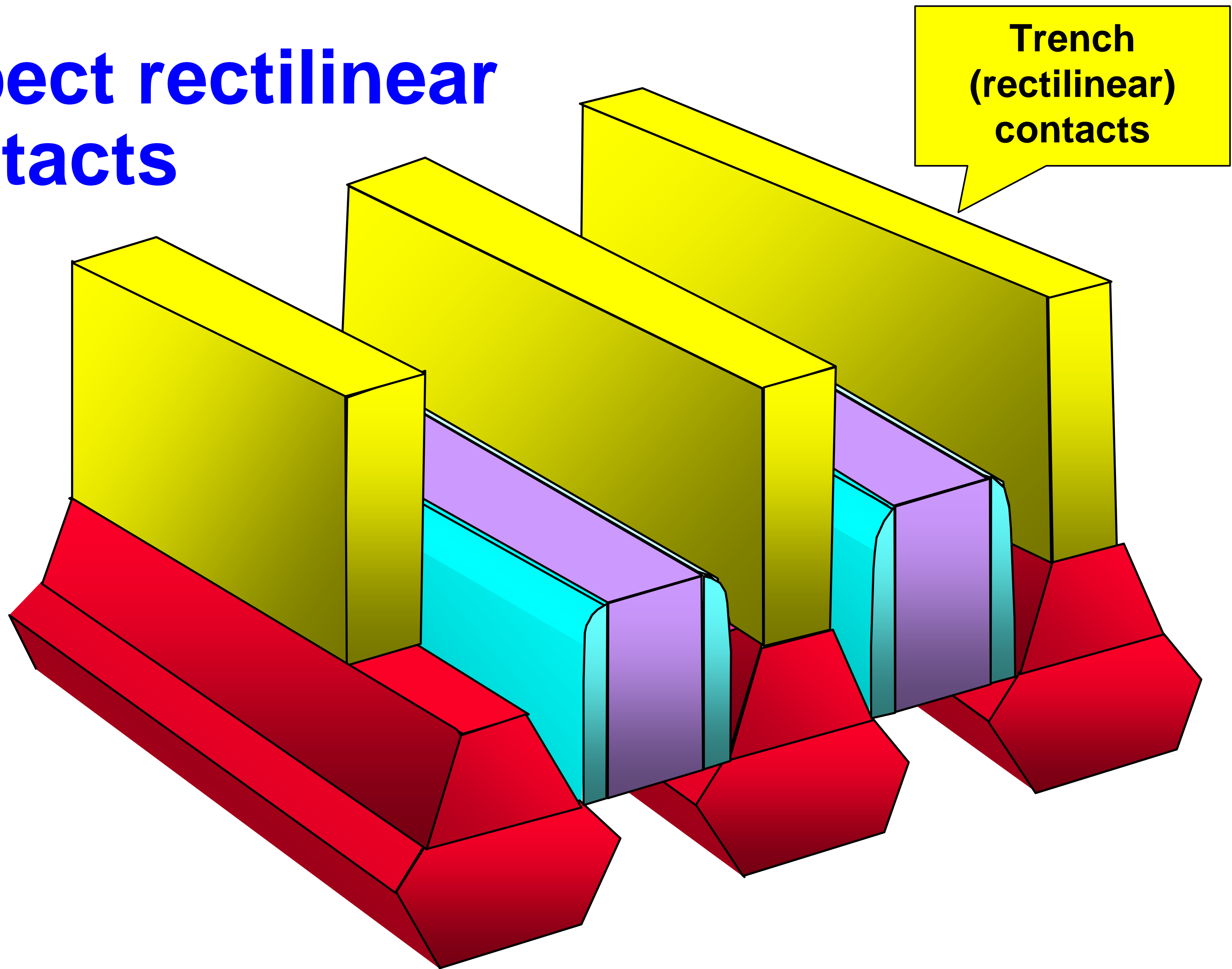
Necessary Digression



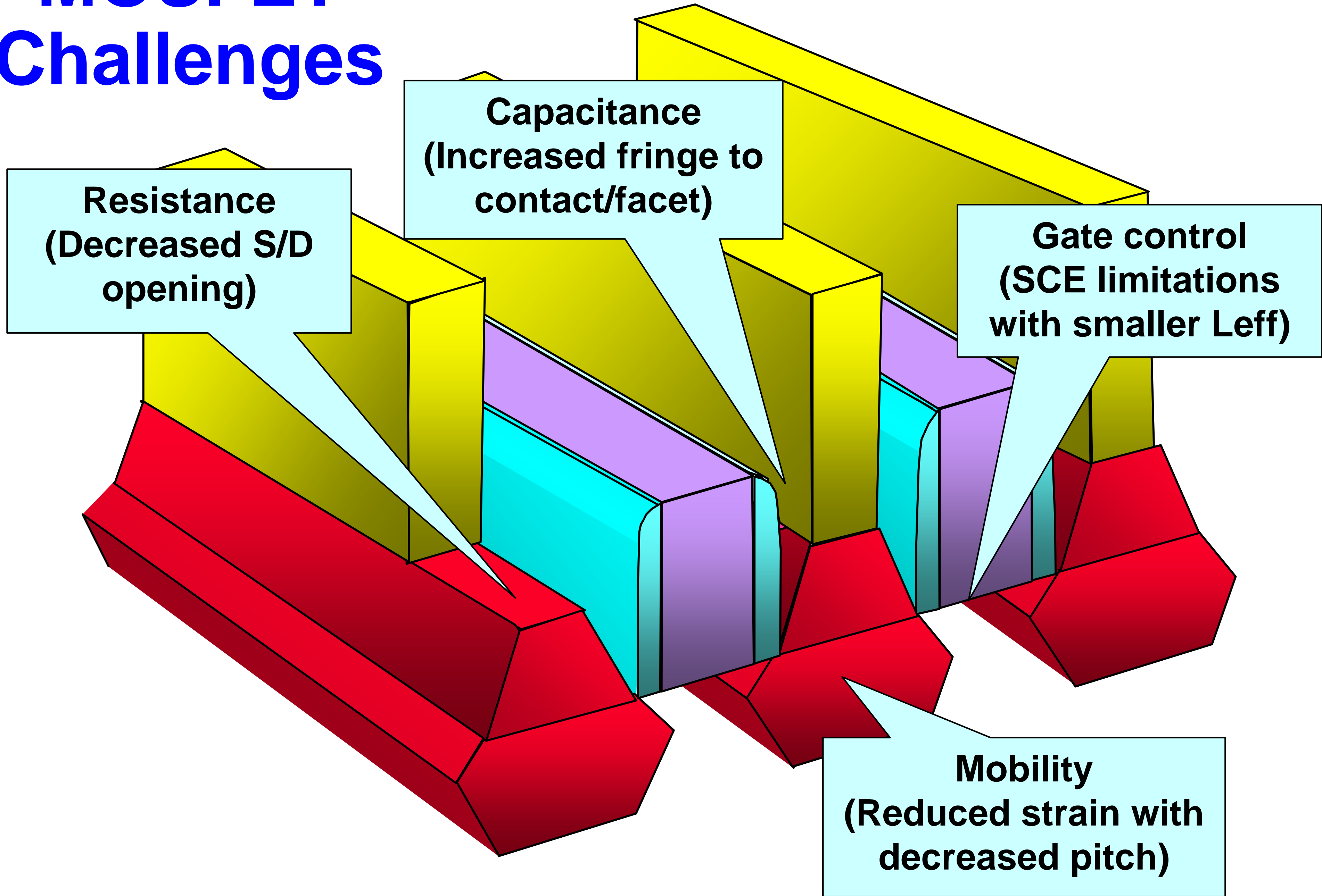
Round contacts challenging



Expect rectilinear contacts



MOSFET Challenges



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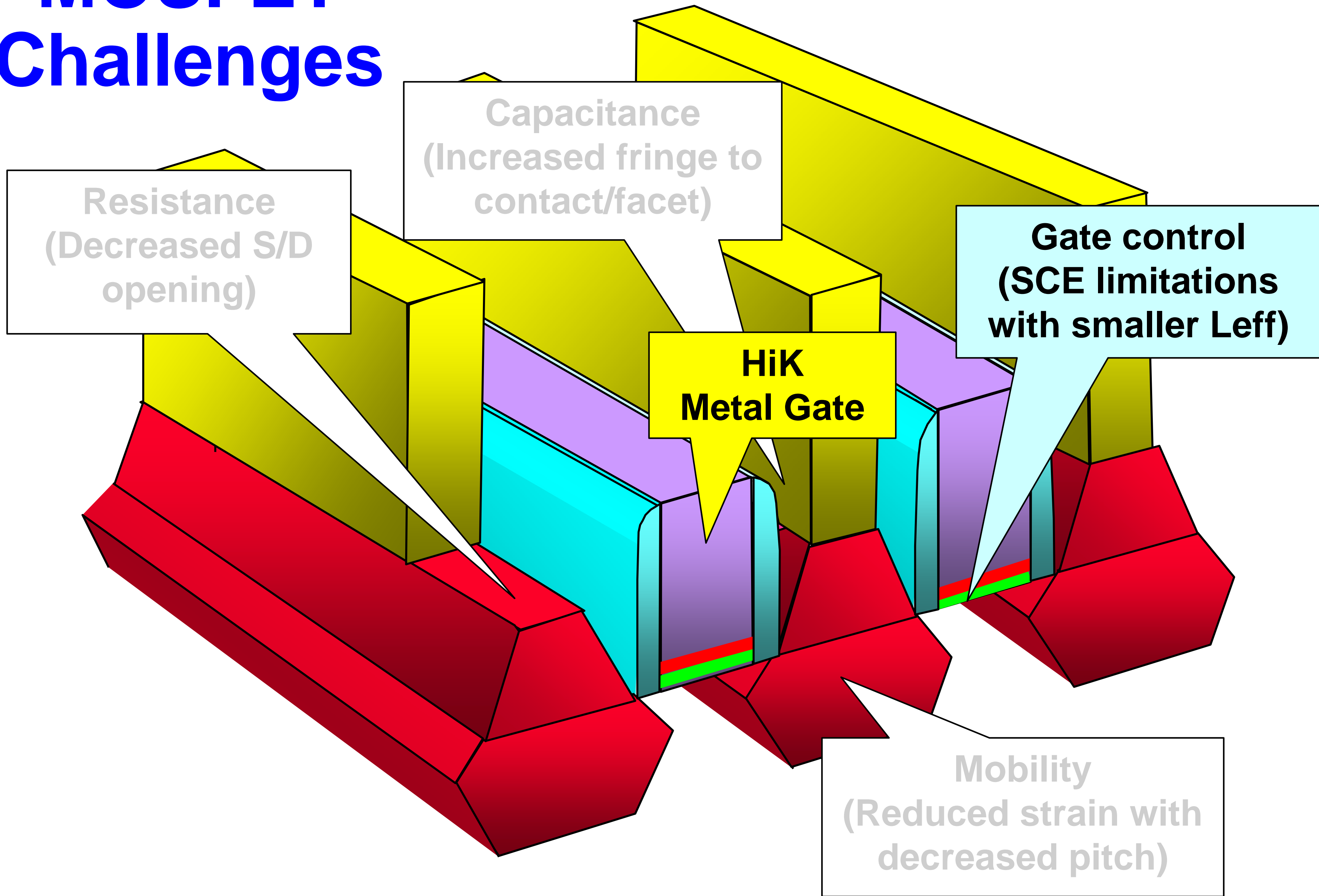


High-k Metal Gate

BENEFITS

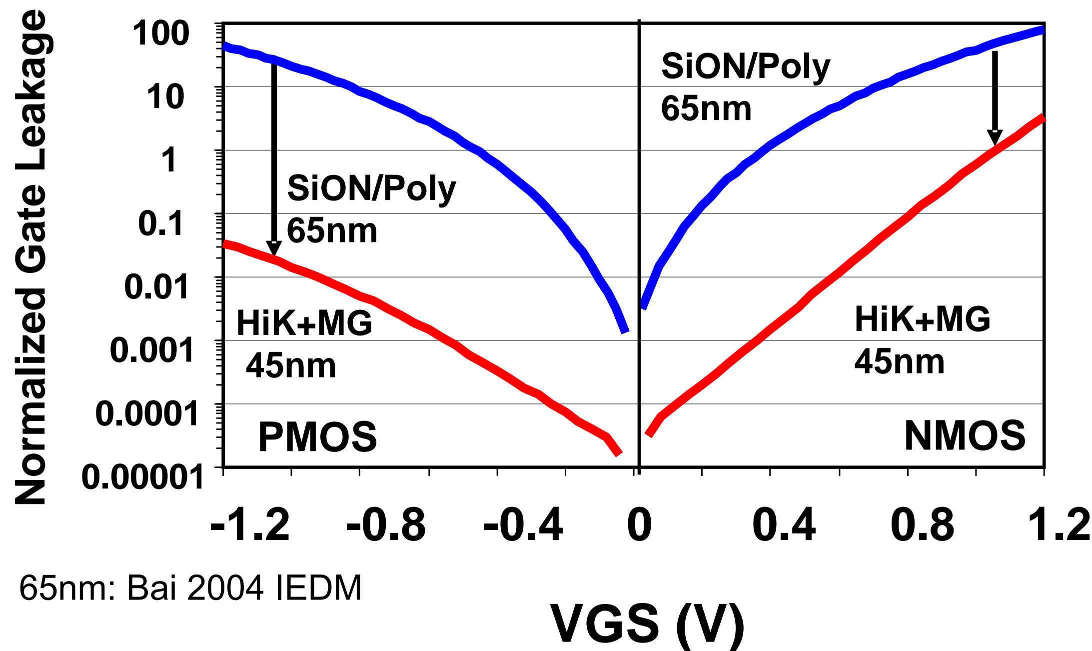
- **High-k gate dielectric**
  - Reduced gate leakage
  - Continued T_{OX} scaling
- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolve V_T pinning for poly on high-k gate dielectrics

CHALLENGES

- **High-k gate dielectric**
  - Reduced reliability
  - Reduced mobility
- **Metal gates**
  - Dual bandedge workfunctions
  - Thermal stability
  - Process integration

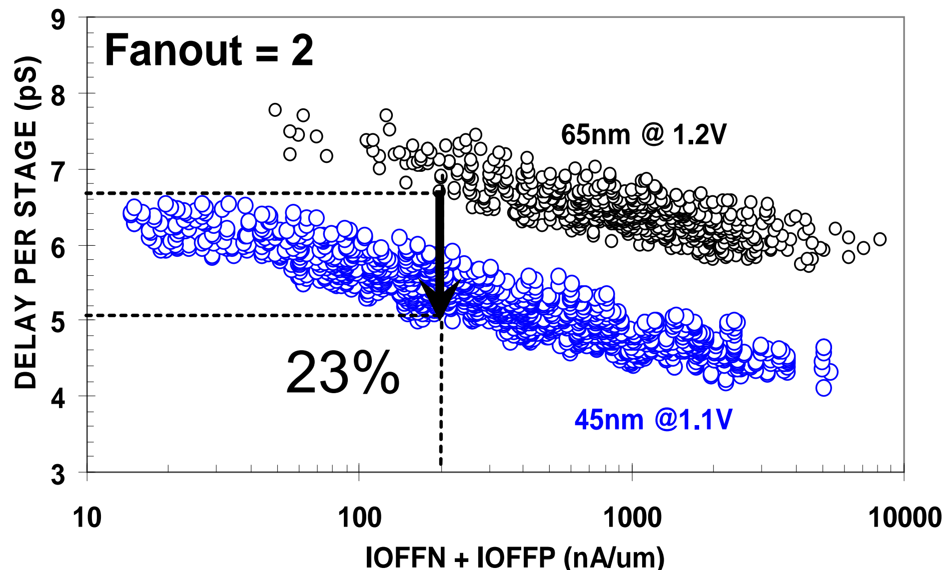
K. Mistry - IEDM 2007

High-k Metal Gate: ToxE and Ig



65nm: Bai 2004 IEDM

High-k/MG enables 0.7X ToxE scaling while reducing Ig >> 25X for NMOS and 1000X for PMOS



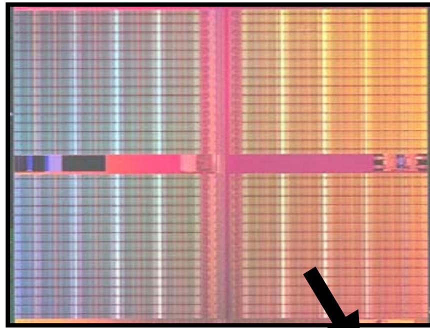
23% better than 65 nm at the same leakage and 100mV lower Vcc. (FO=2 delay of 5.1 ps at IOFFN = IOFFP = 100 nA/µm)

K. Mistry - IEDM 2007

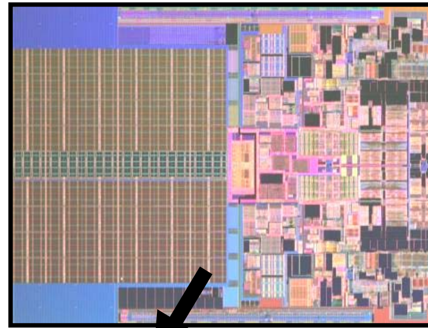
The Road to HK+MG Processors

1st Generation HK+MG

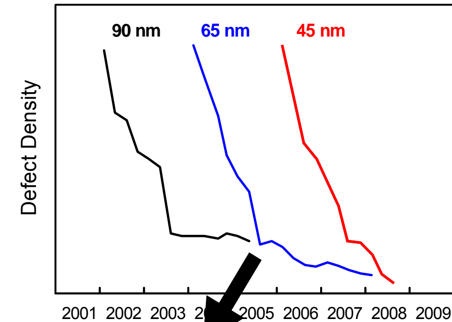
Jan. 2006
45 nm 153 Mb SRAM

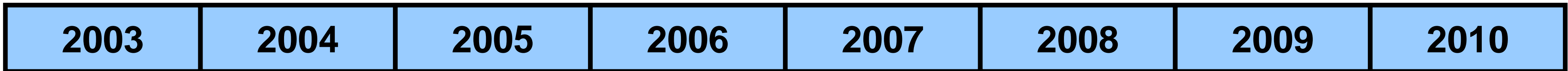


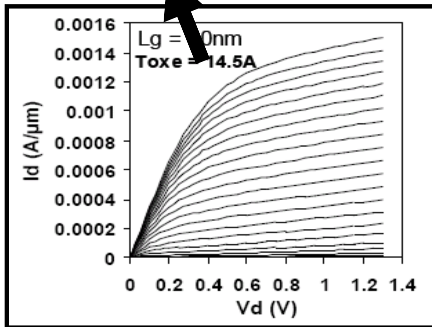
Jan. 2007
45 nm Penryn CPU



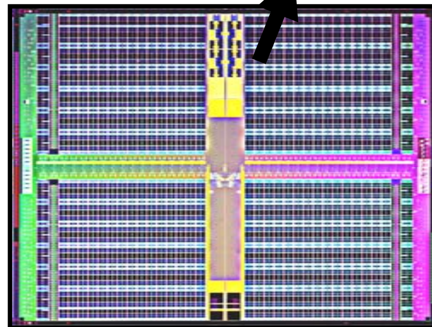
Jan. 2009
>100 million shipped



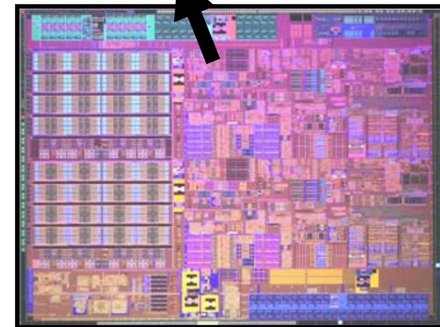




Nov. 2003
HK+MG Transistors



Sep. 2007
32 nm 291 Mb SRAM

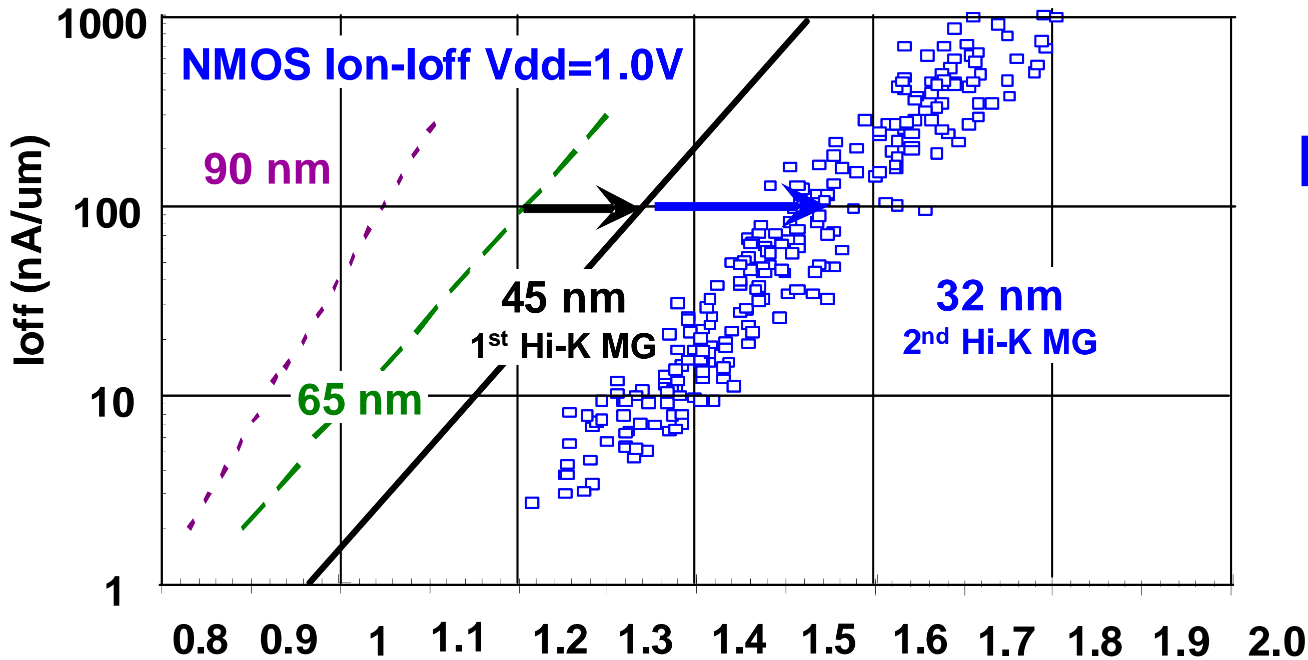


Jan. 2009
32 nm Westmere CPU

HK+MG Research

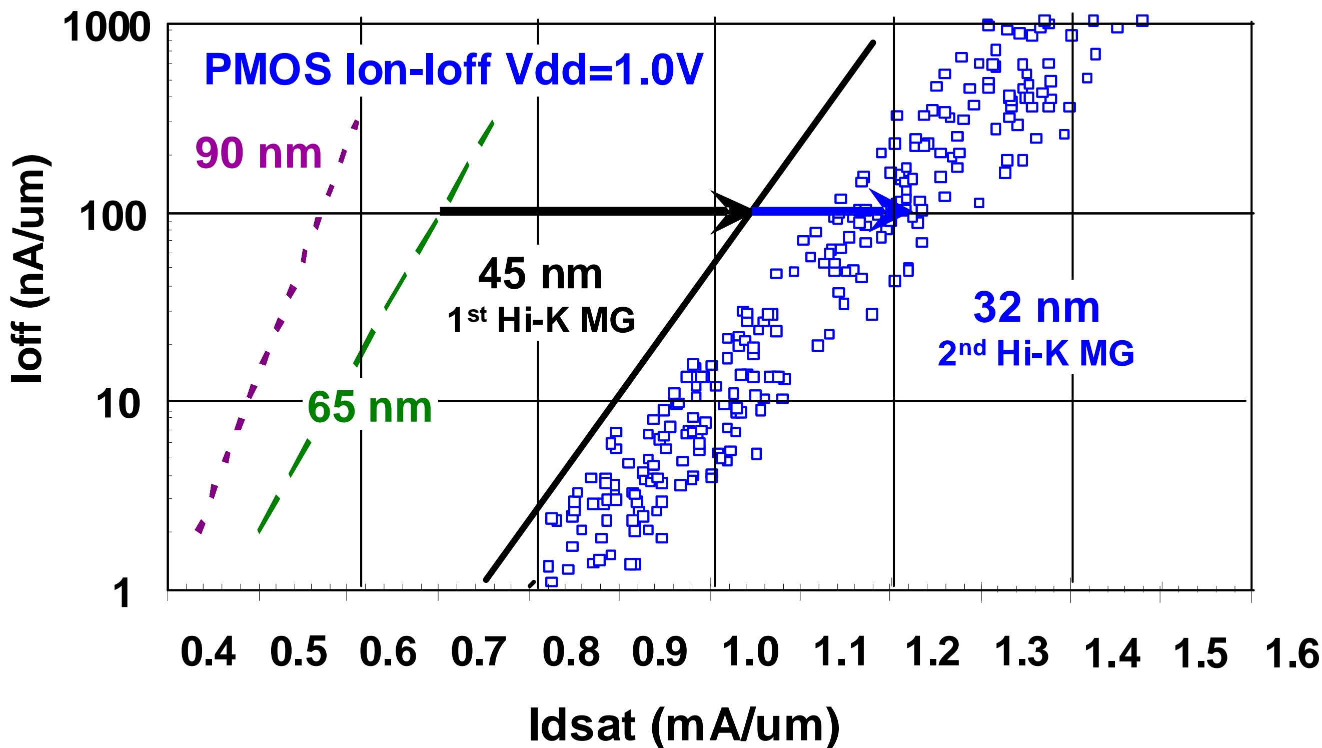
2nd Generation HK+MG

Bohr, Intel, 6/09



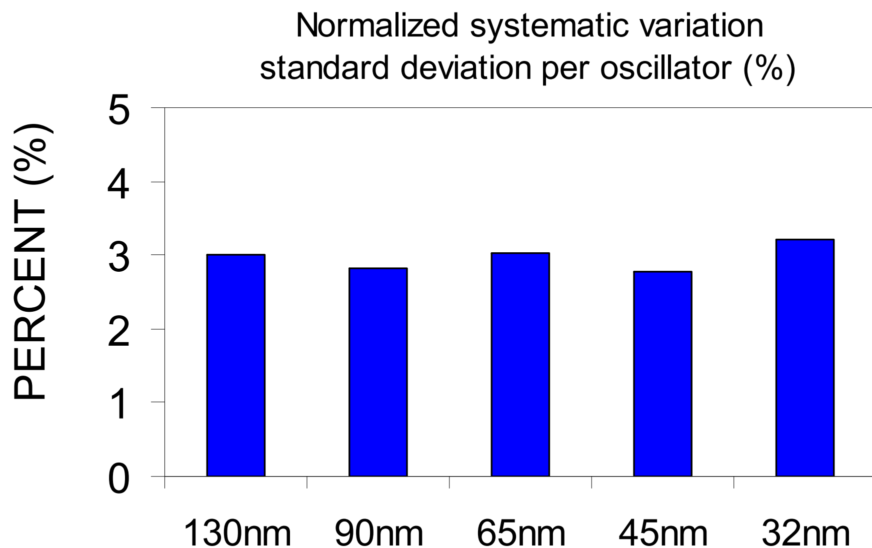
FOUR GENERATION COMPARISON

45nm:
1st gen. HiK-MG
Mistry, Intel, IEDM 2007

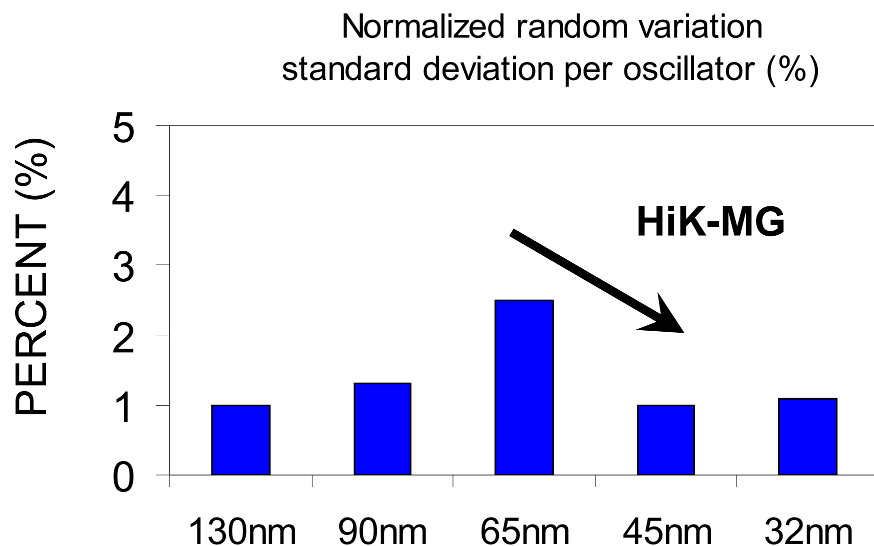


32nm:
2nd gen. HiK-MG
Natarajan, Intel, IEDM 2008

Random and Systematic Variation Trends



Systematic WIW variation is comparable from one generation to the next



Random WIW variation in 32nm is comparable to 45nm and significantly improved over 65nm and 90nm due to HiK-MG

Yield: The best measure of Systematic Variation

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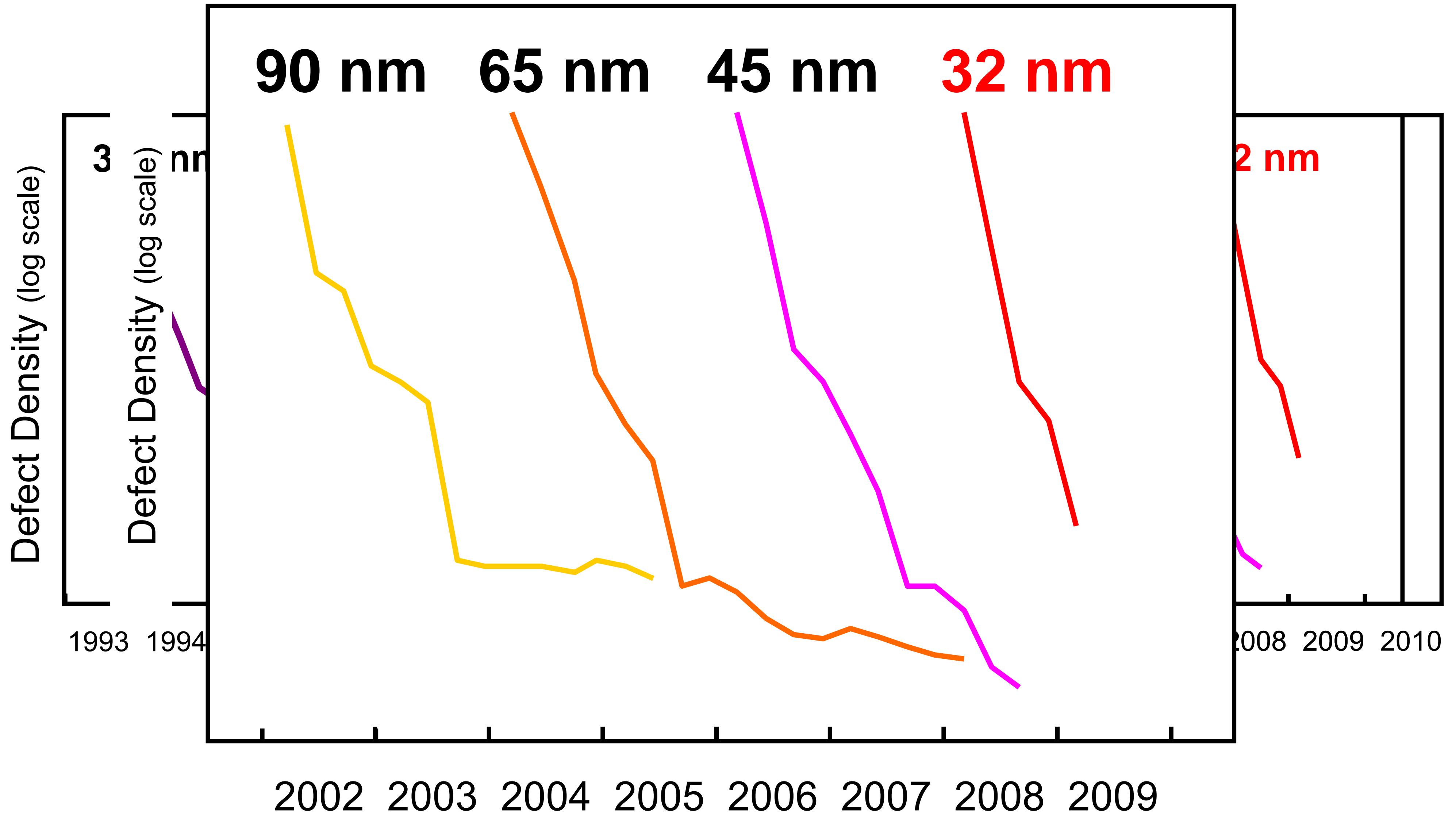
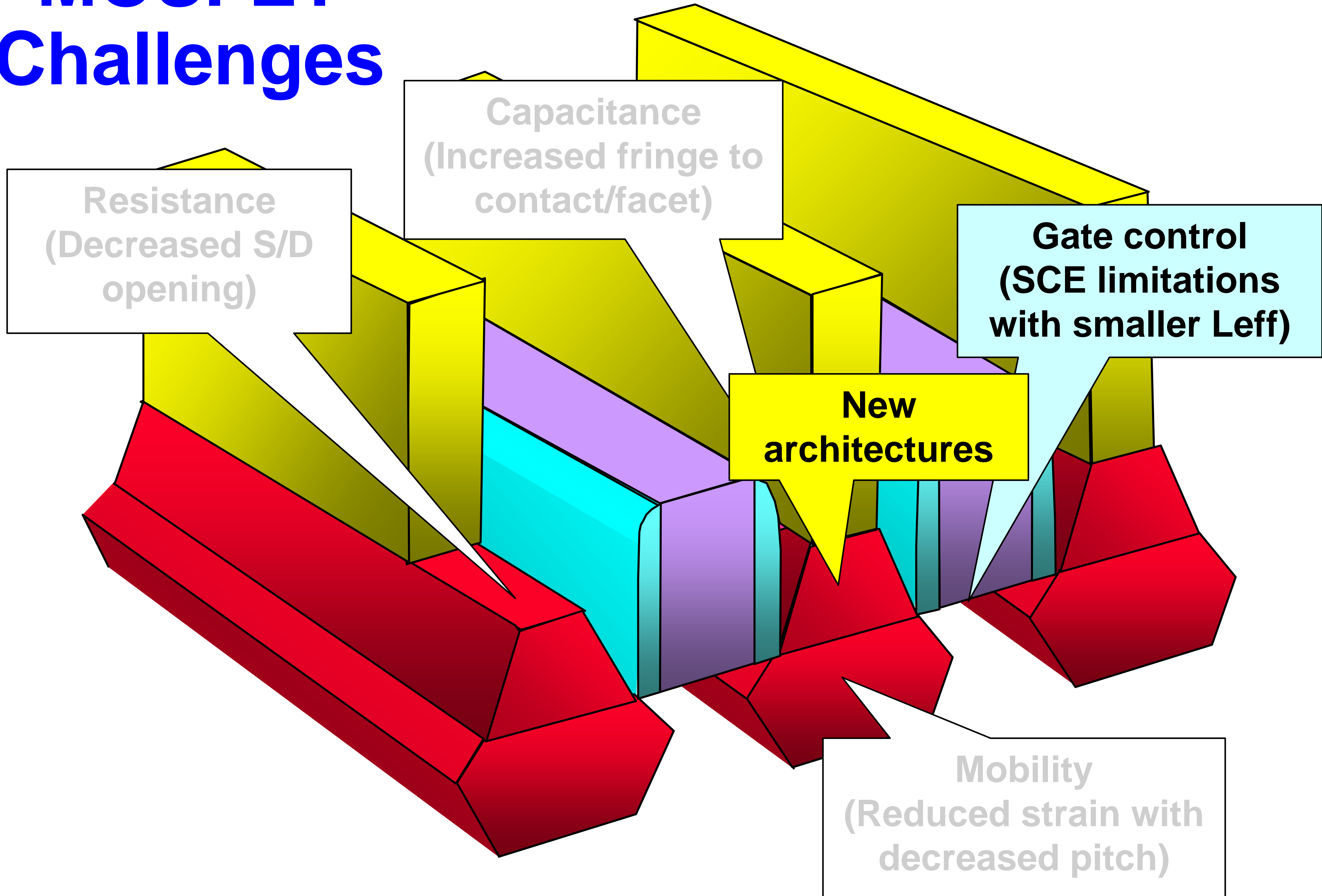
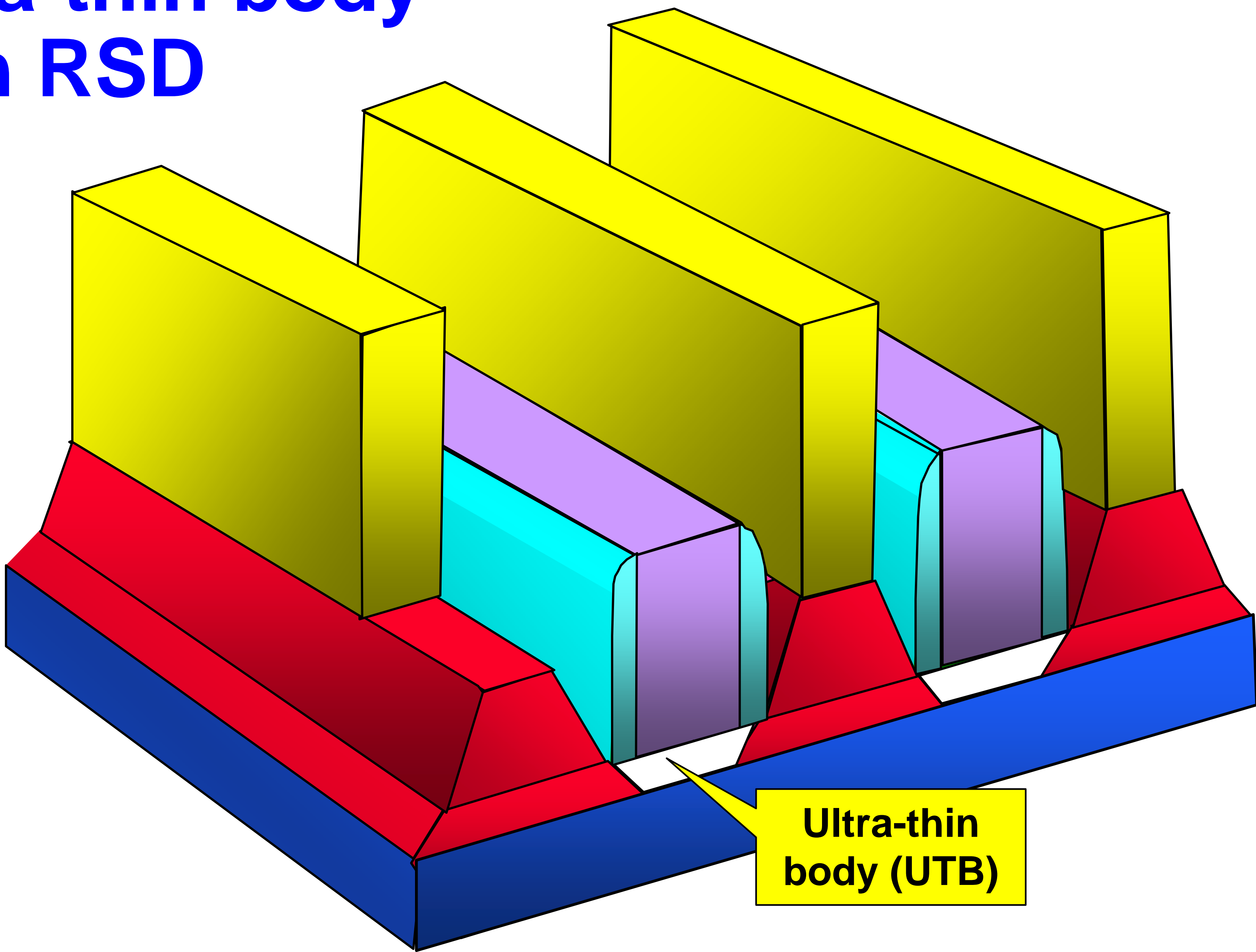


MOSFET Challenges



Ultra-thin body with RSD



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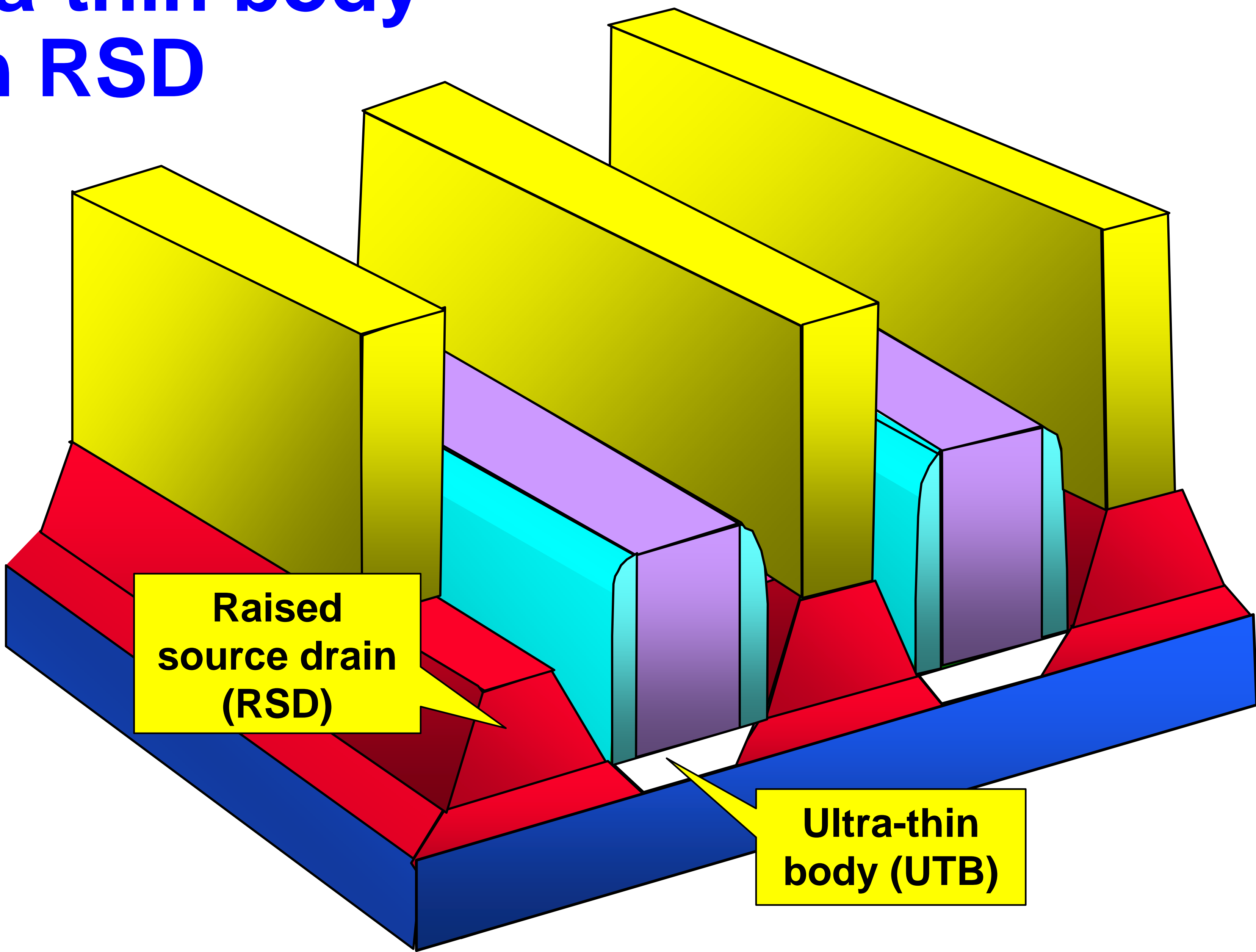
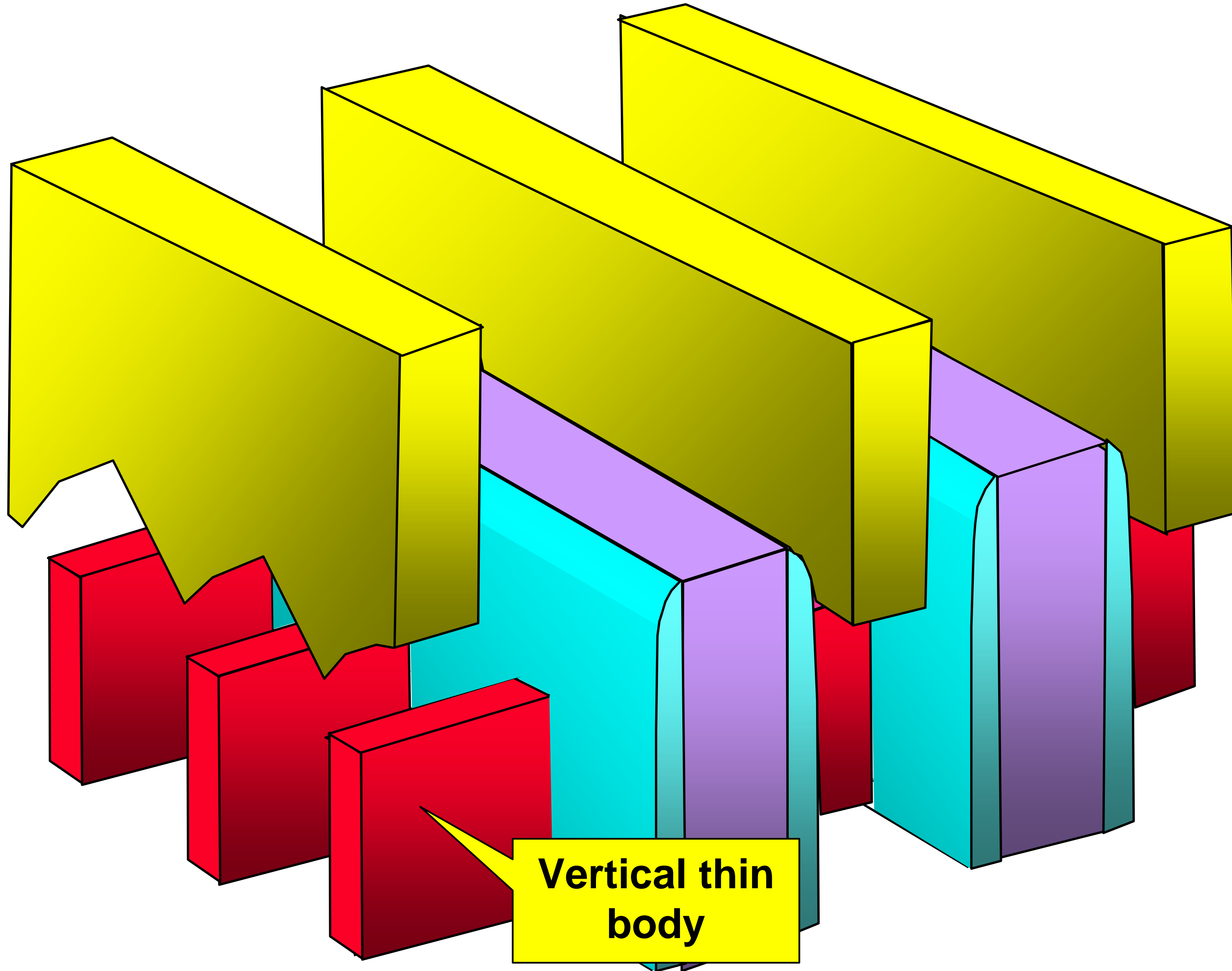
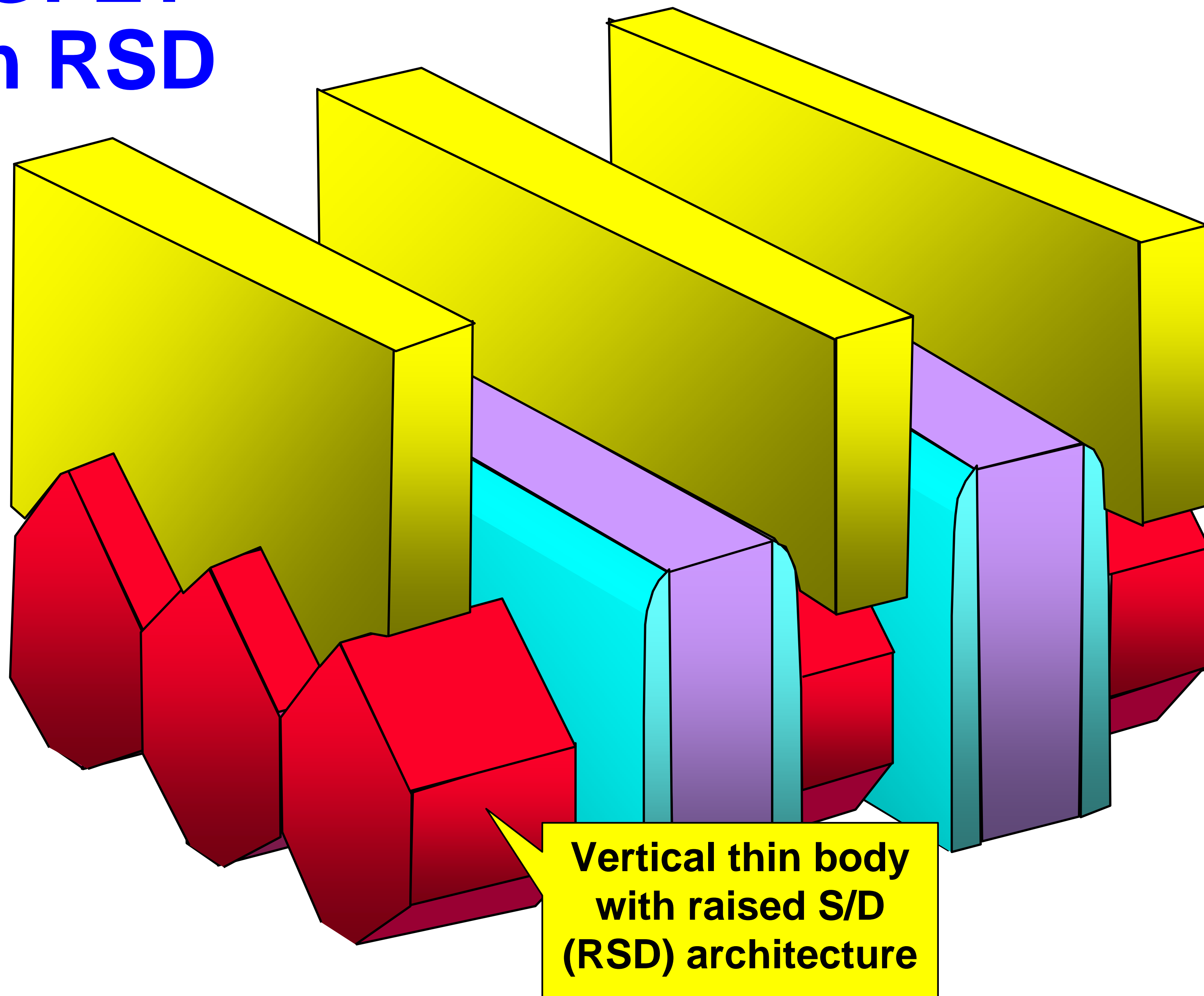


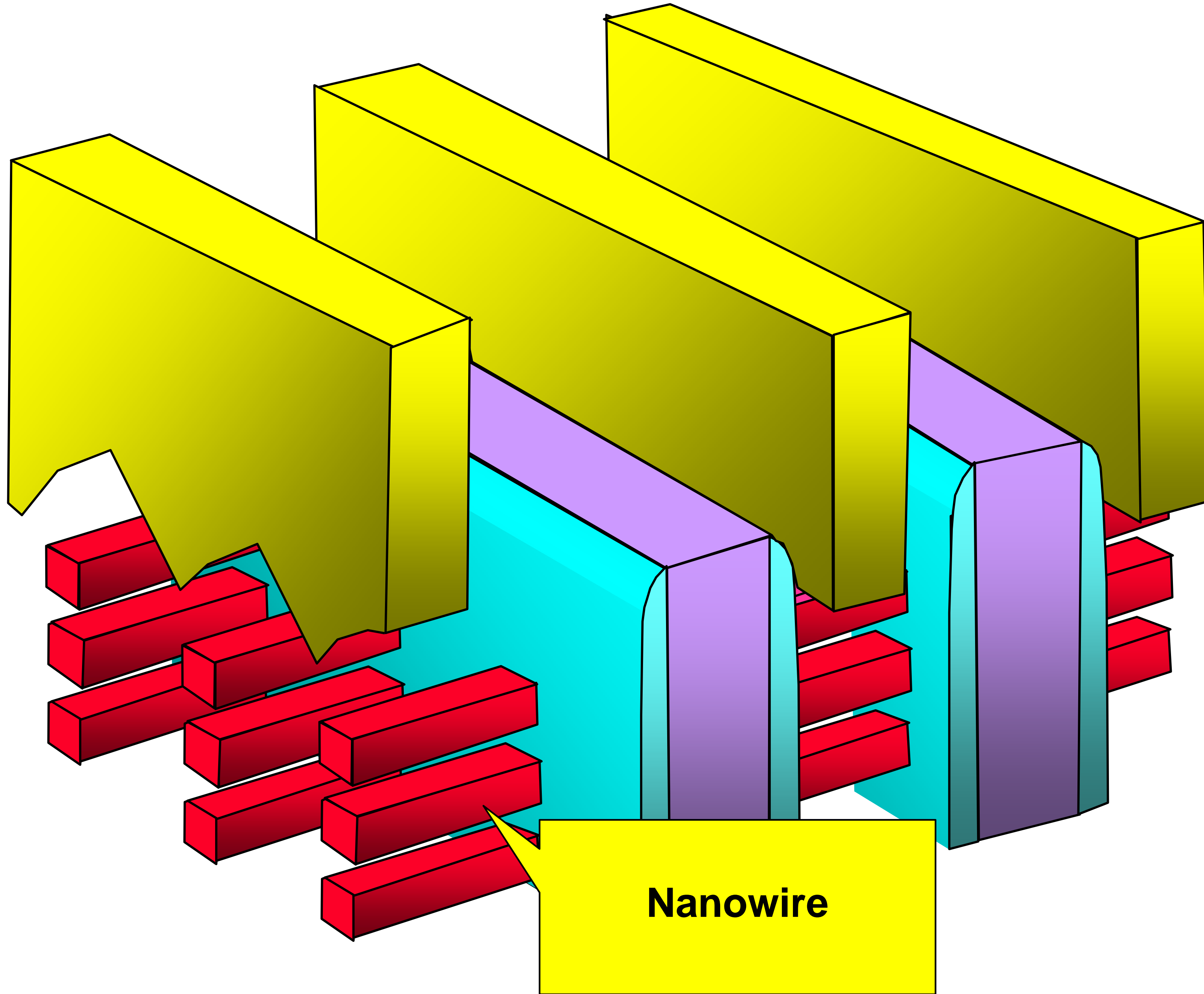
MuGFET



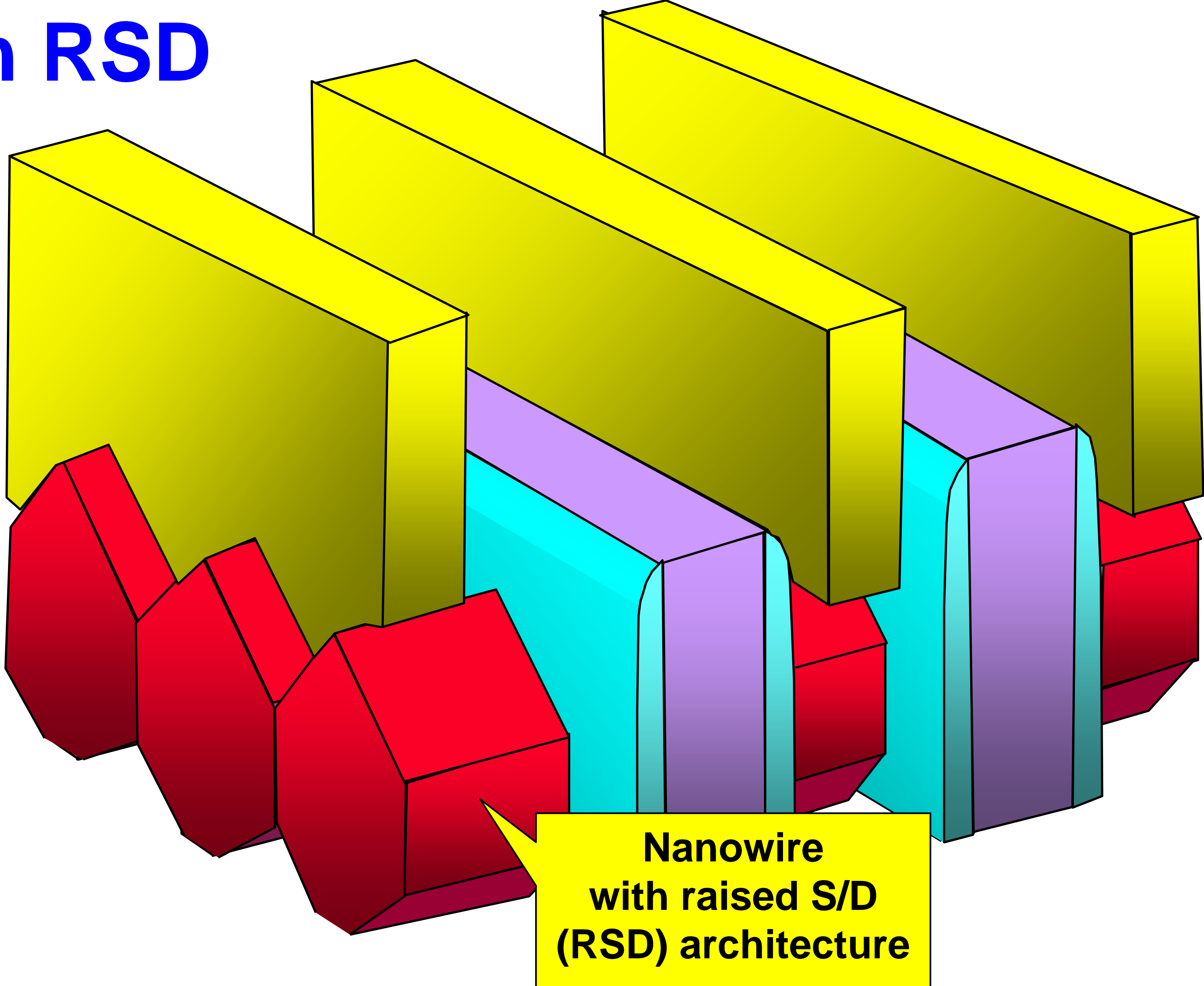
MuGFET with RSD



Nanowire



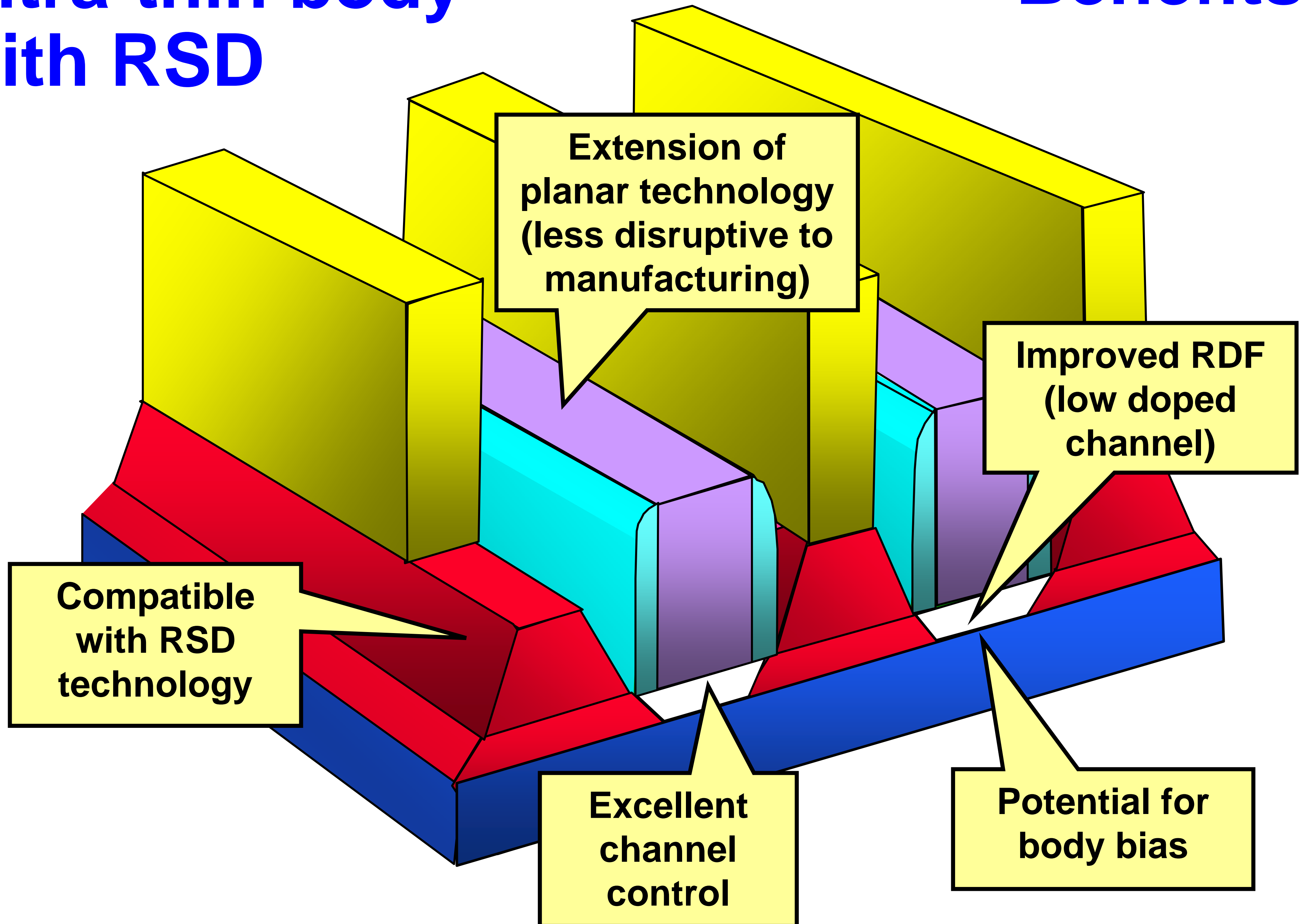
Nanowire with RSD



Looking at all these in more detail

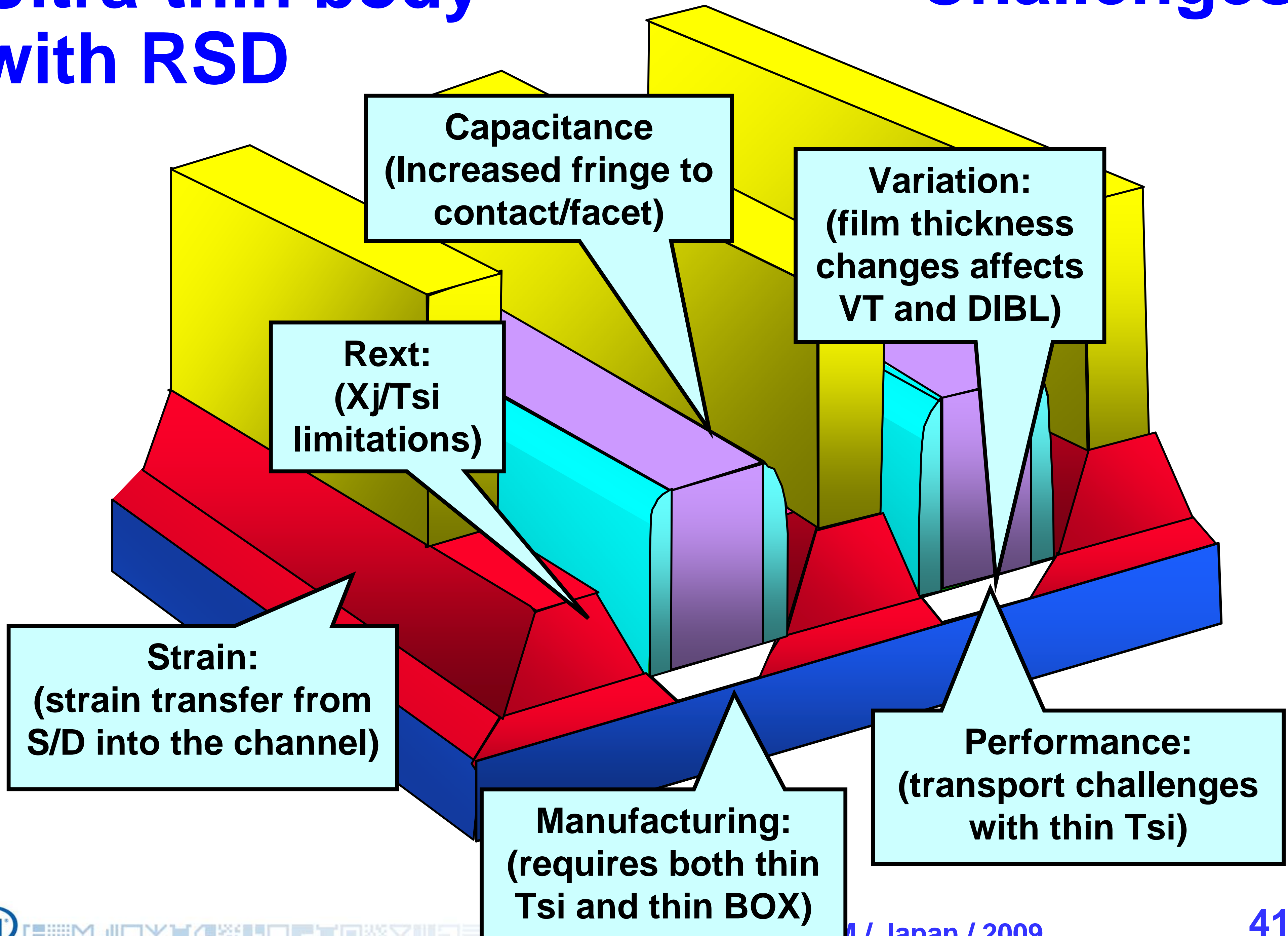
Ultra-thin body with RSD

Benefits



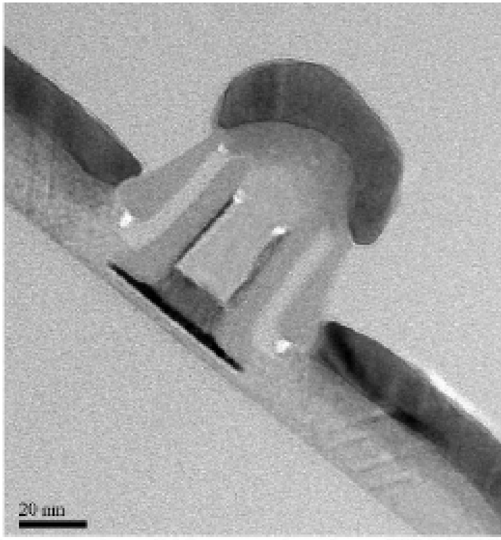
Ultra-thin body with RSD

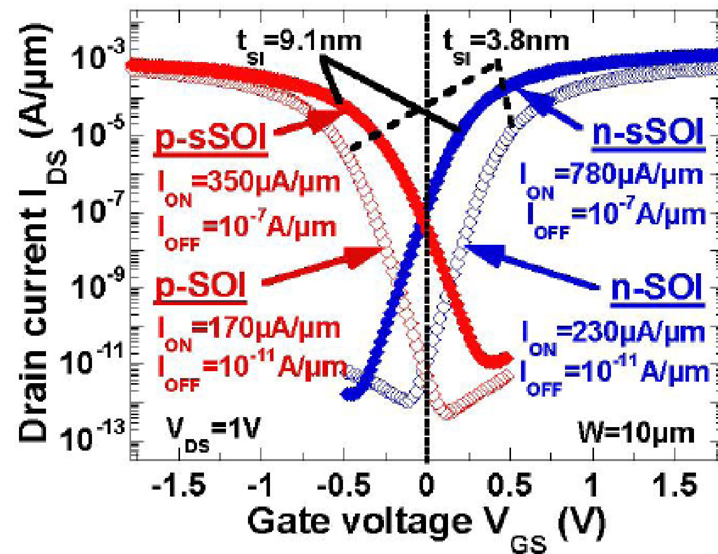
Challenges

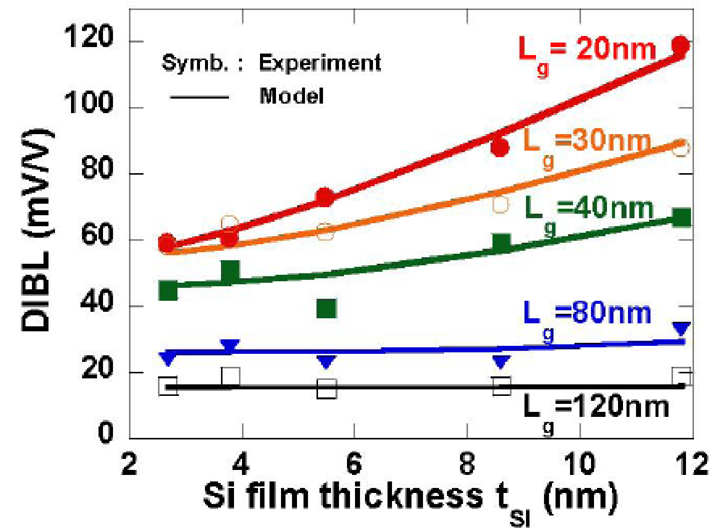


Ultra-thin body

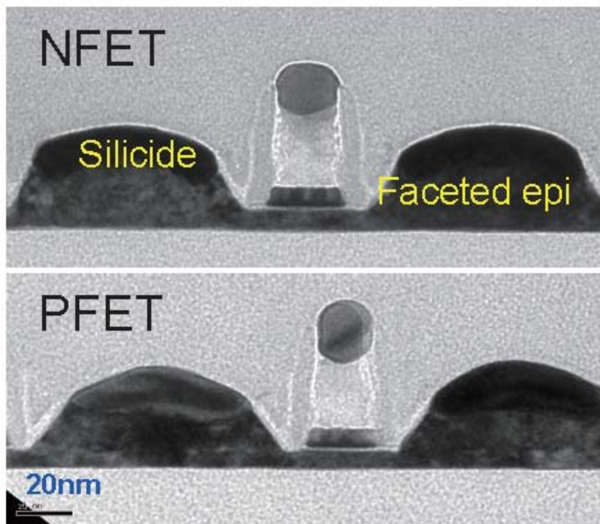
Barral – CEA-LETI– IEDM 2007

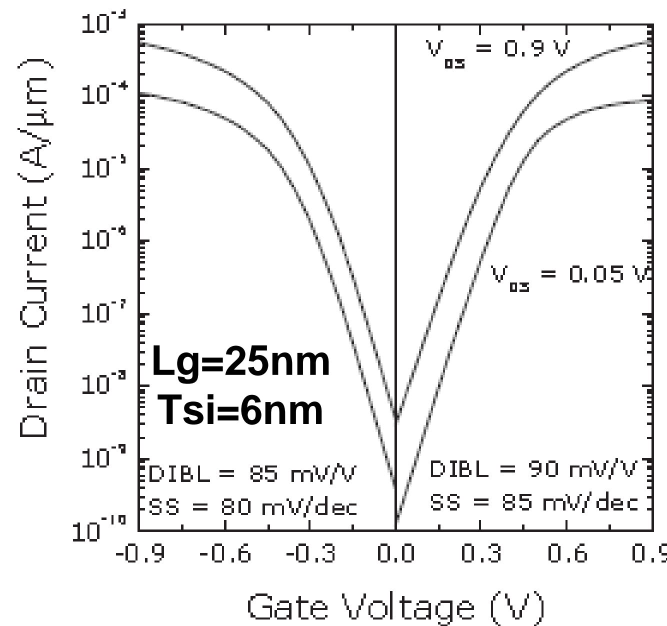


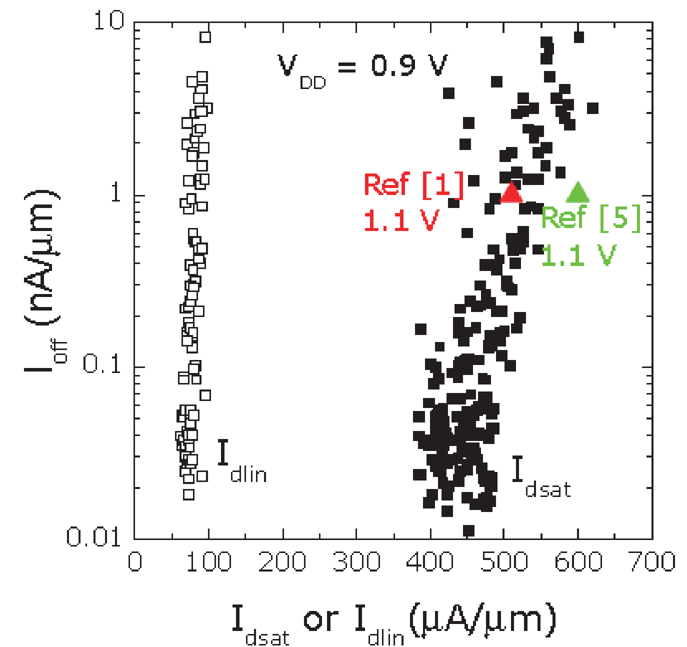




Cheng – IBM – VLSI 2009

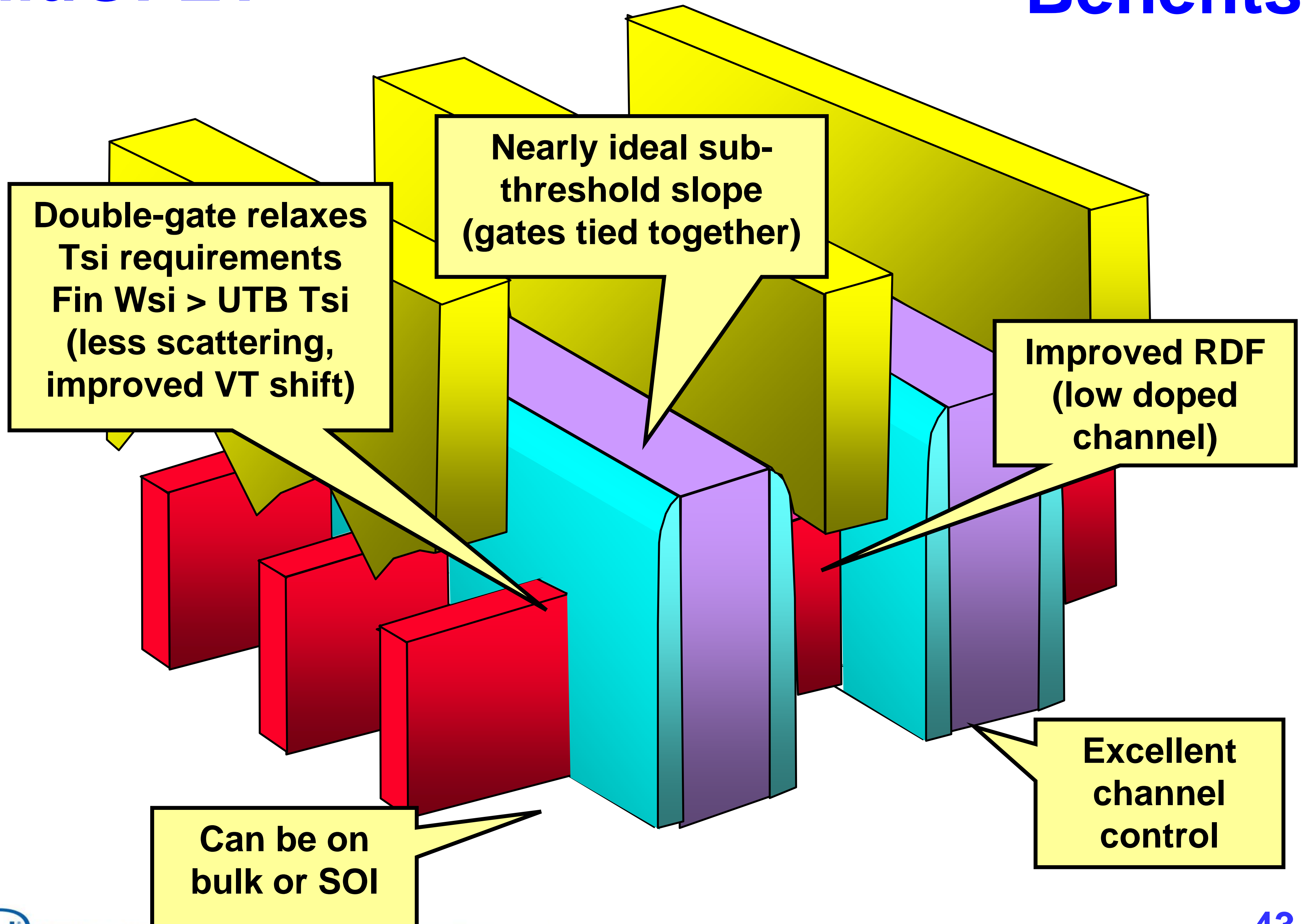






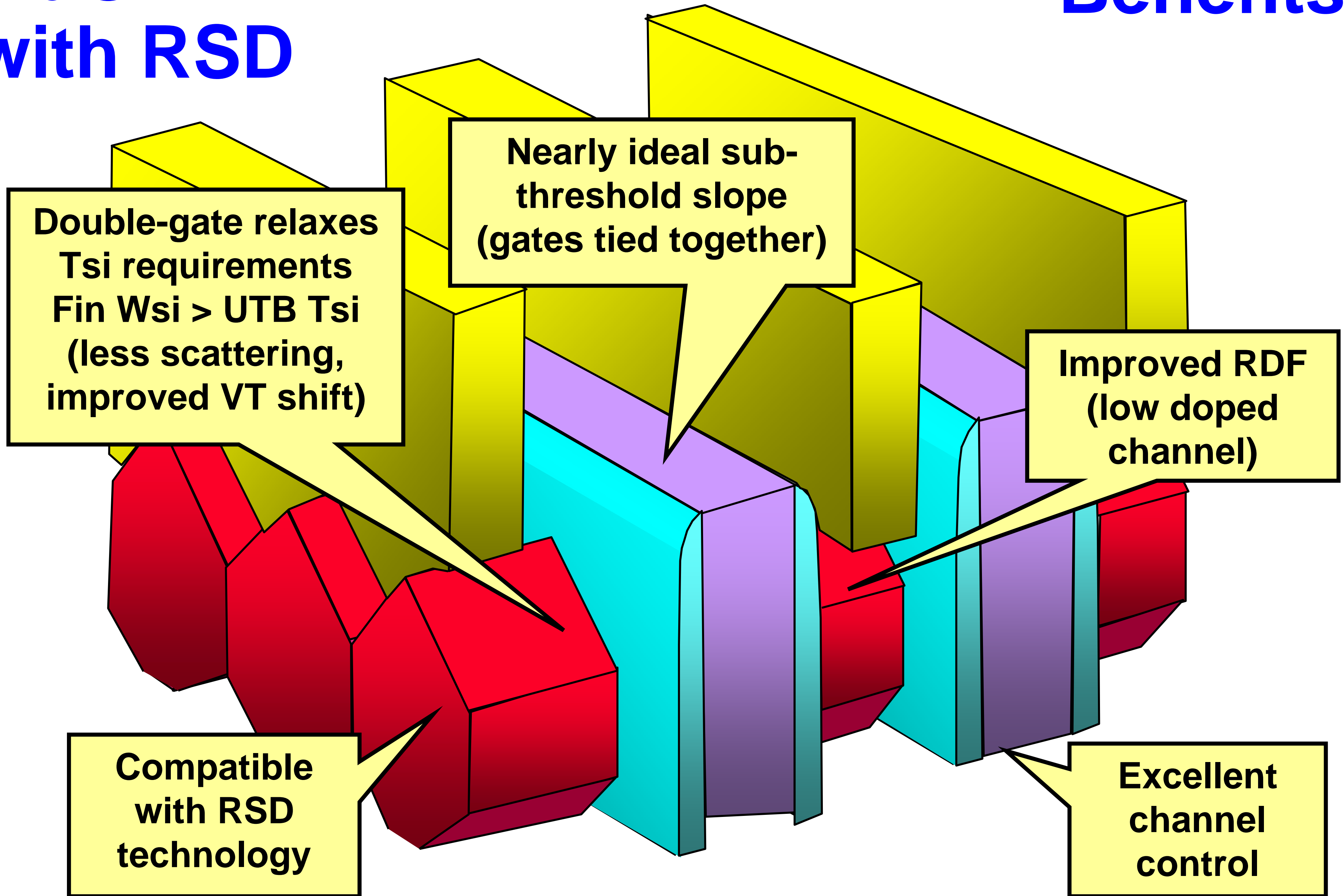
MuGFET

Benefits

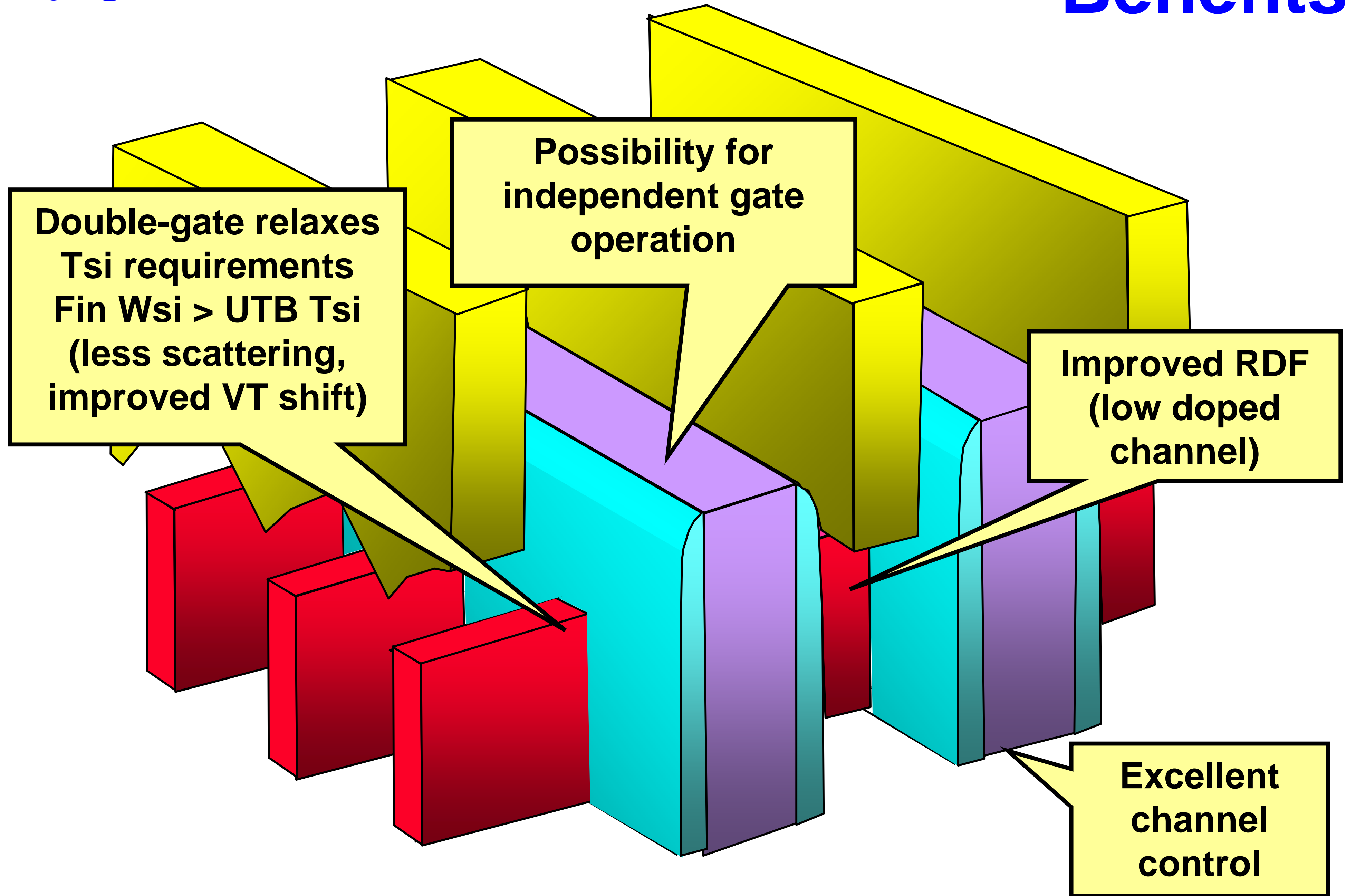


MuGFET with RSD

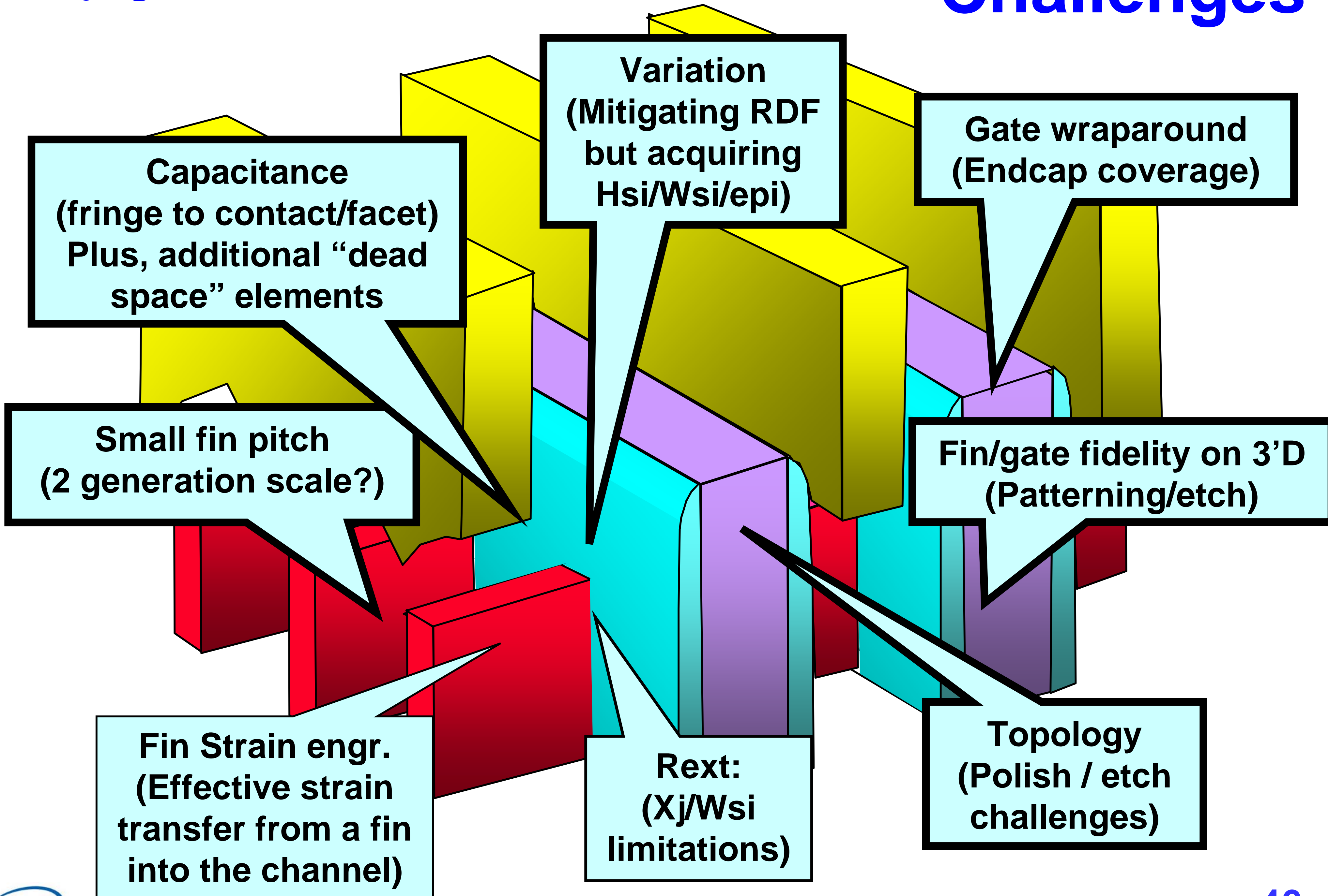
Benefits



MuGFET Benefits



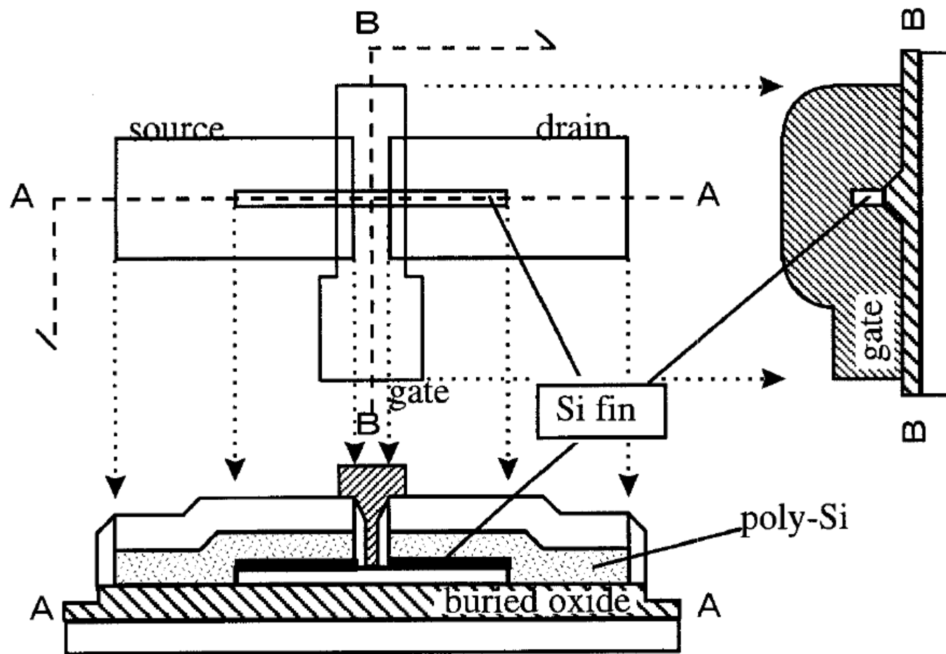
MuGFET Challenges



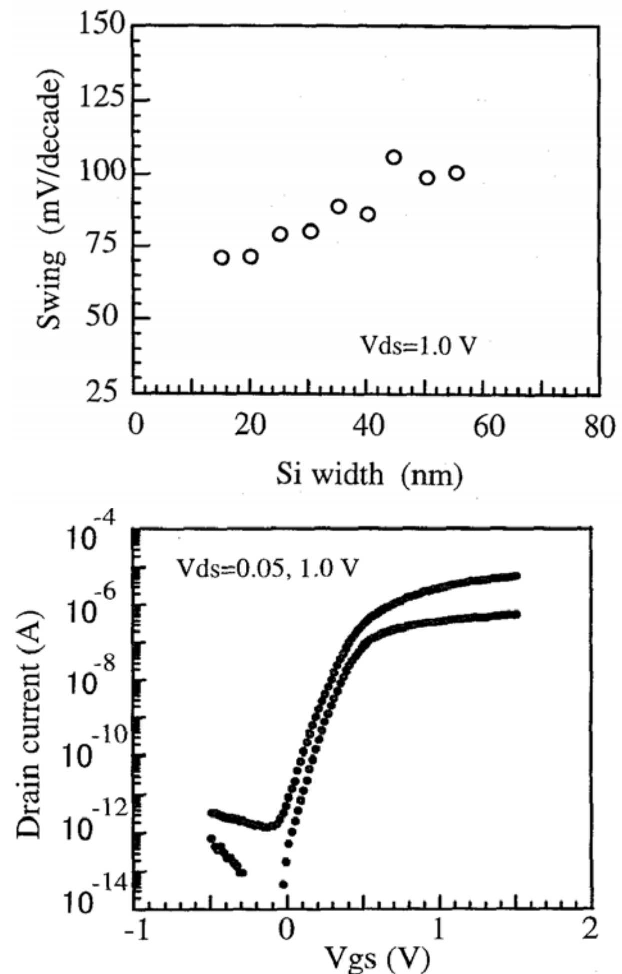
Hisamoto – Hitachi / Berkeley– IEDM 1998 [3]

A Folded-channel MOSFET for Deep-sub-tenth Micron Era

Digh Hisamoto, Wen-Chin Lee*, Jakub Kedzierski*, Erik Anderson**, Hideki Takeuchi+, Kazuya Asano++, Tsu-Jae King*, Jeffrey Bokor*, and Chenming Hu*
Central Research Laboratory, Hitachi Ltd., *) EECS, UC Berkeley,
**) Lawrence Berkeley Laboratory, +) Nippon Steel Corp., ++) NKK Corp.

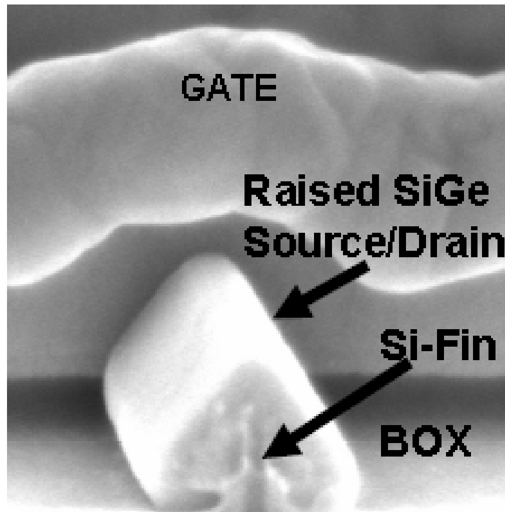


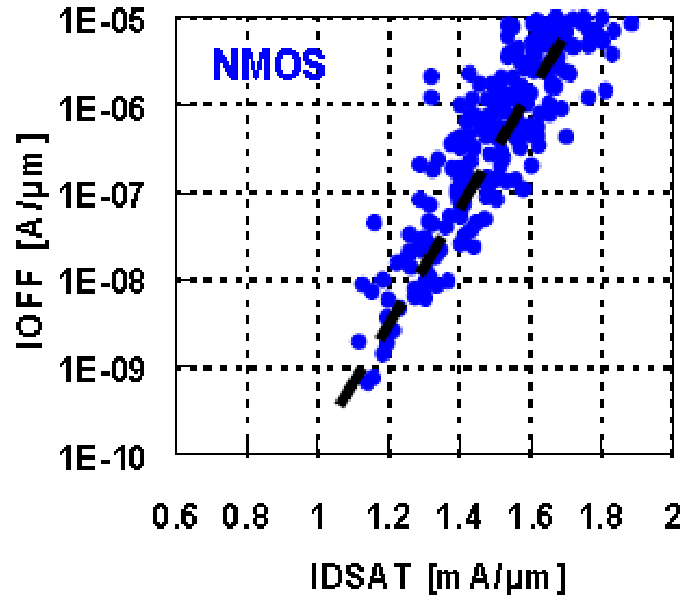
. 1 Folded channel MOSFET layout design and device structure.
: bottom is A-A cross section, and the right is B-B cross section

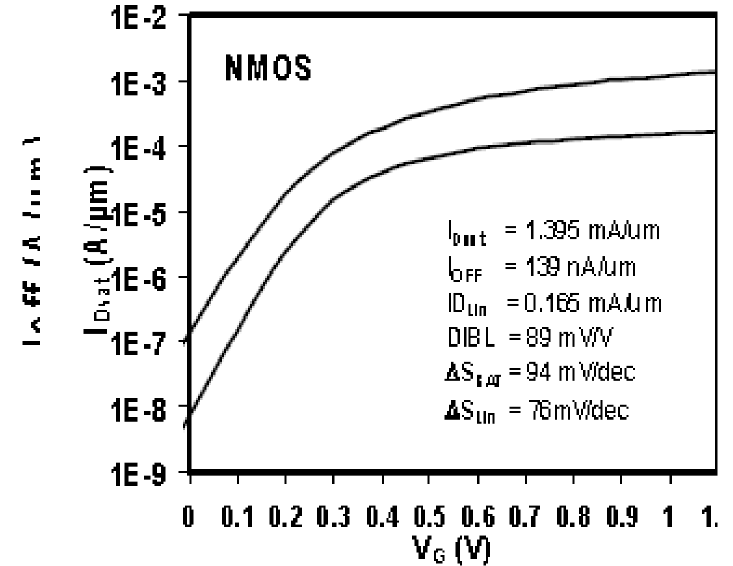


MuGFET

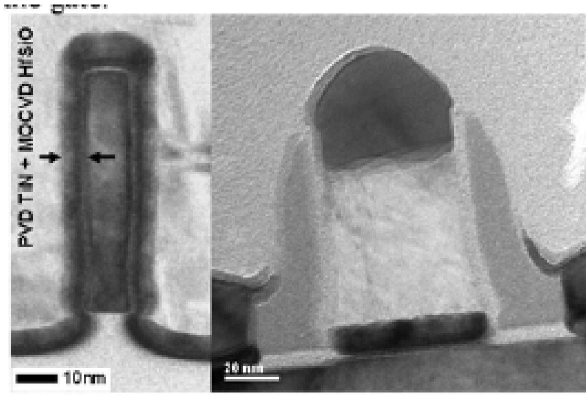
Kavalieros – Intel – IEDM 2006

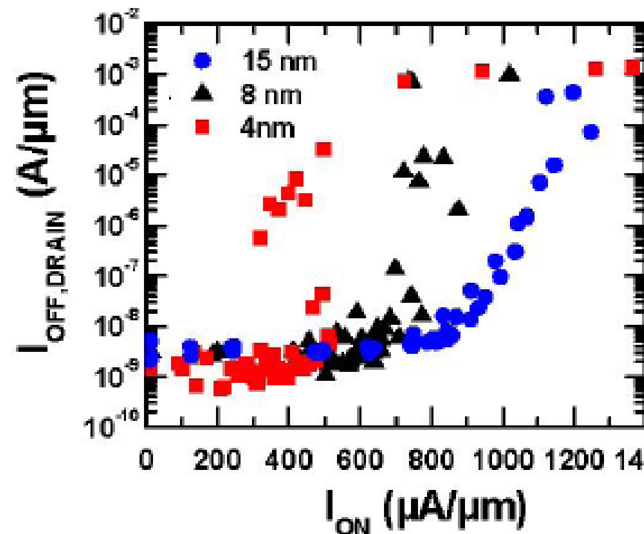


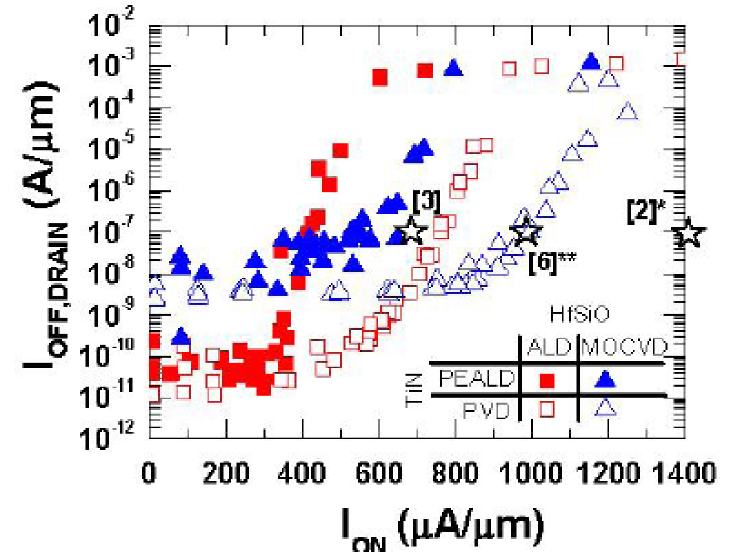




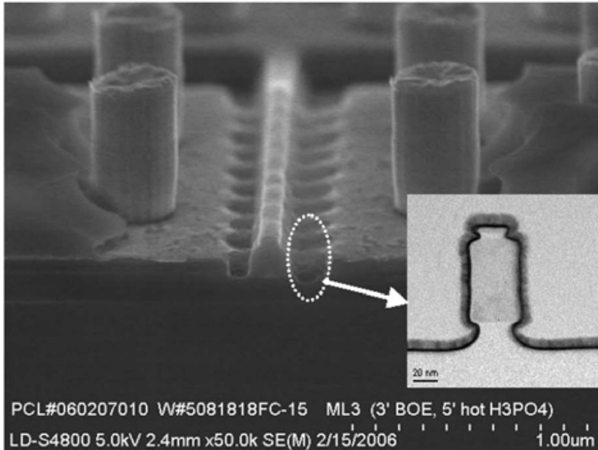
Vellianitis – NXP-TSMC – IEDM 2007

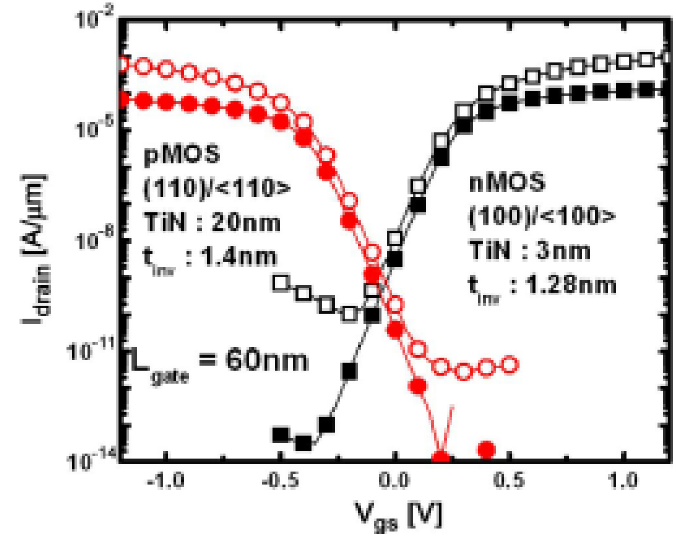


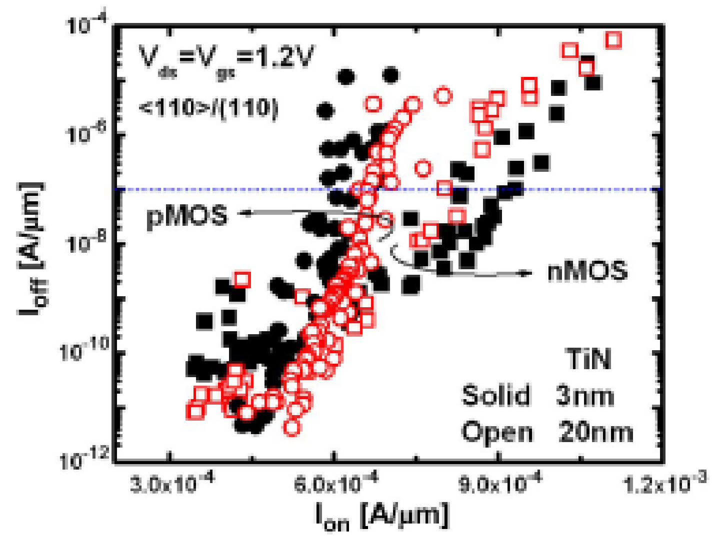




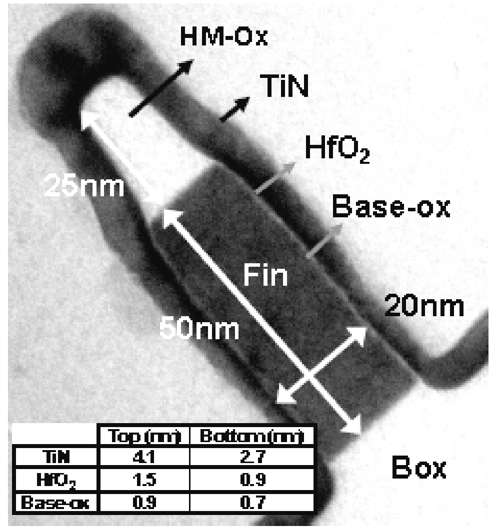
Kang – Sematech – VLSI 2008



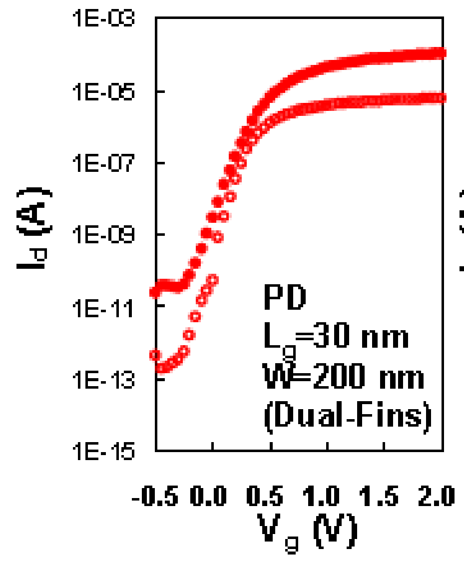


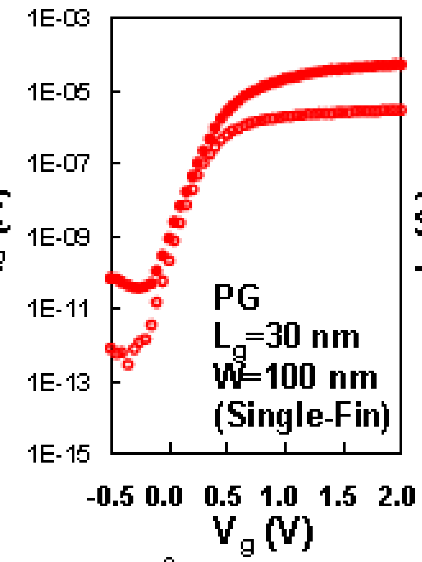


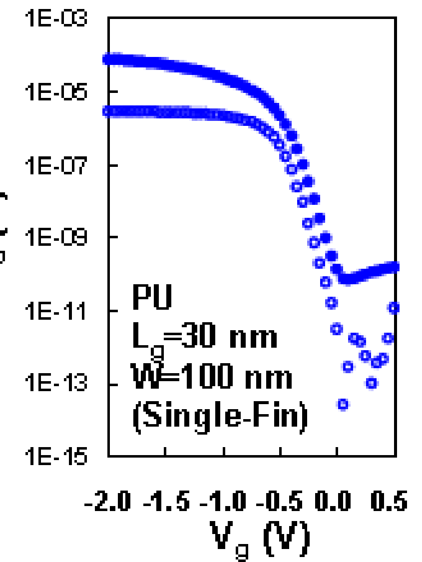
Kawasaki – Toshiba (IBM Alliance) – IEDM 2009



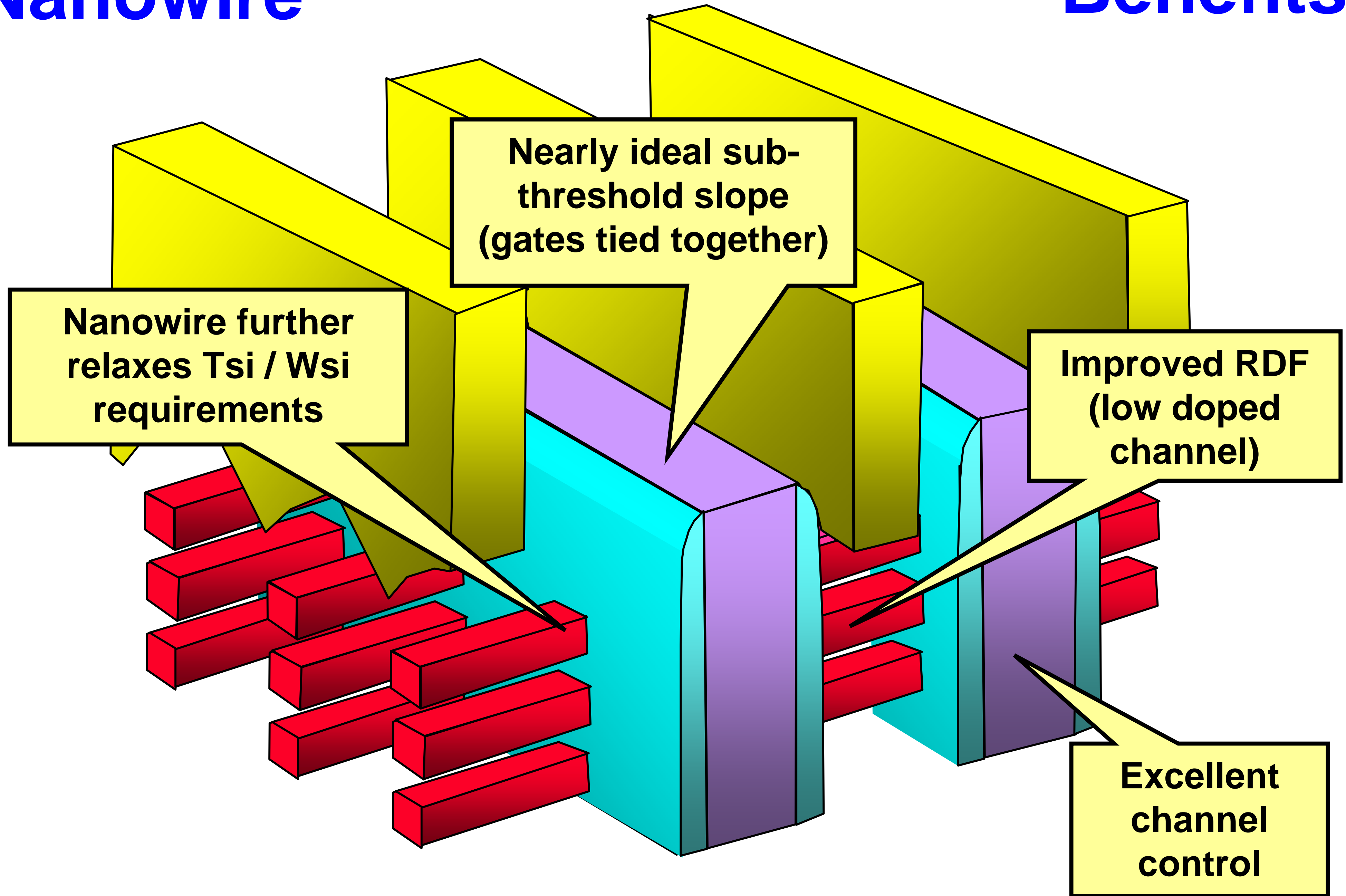
	Top (nm)	Bottom (nm)
TiN	4.1	2.7
HfO_2	1.5	0.9
Base-ox	0.9	0.7



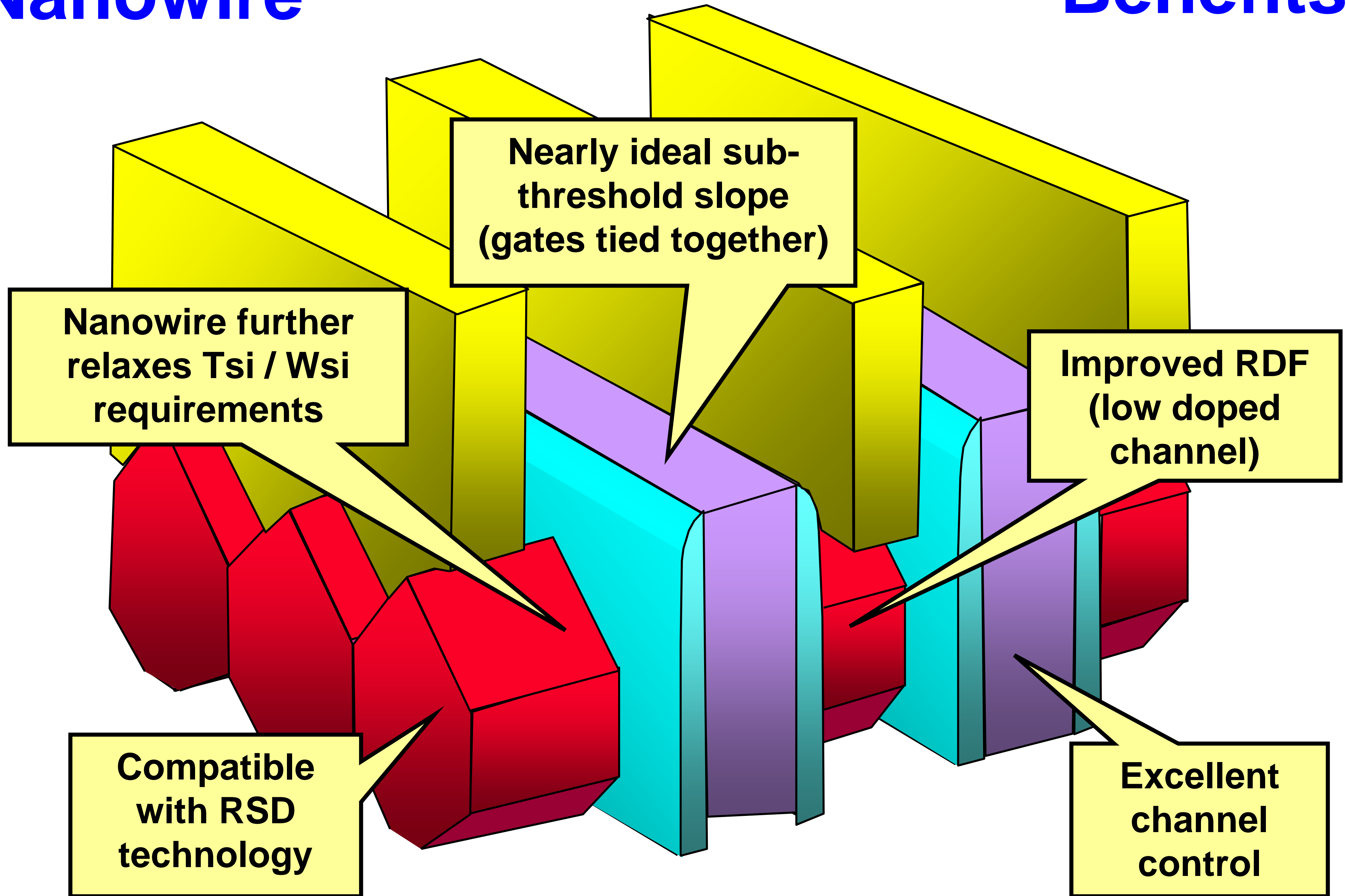




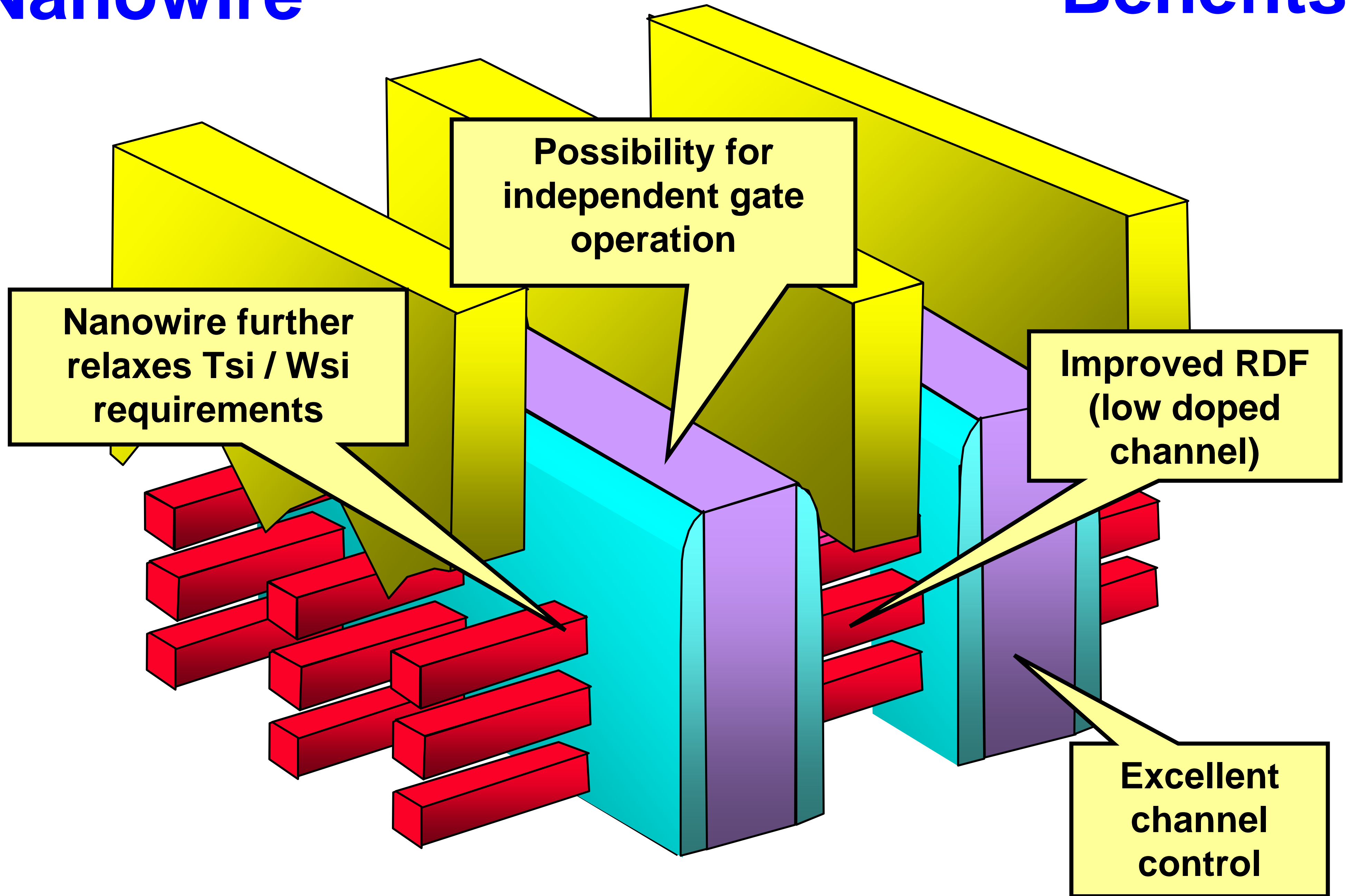
Nanowire Benefits



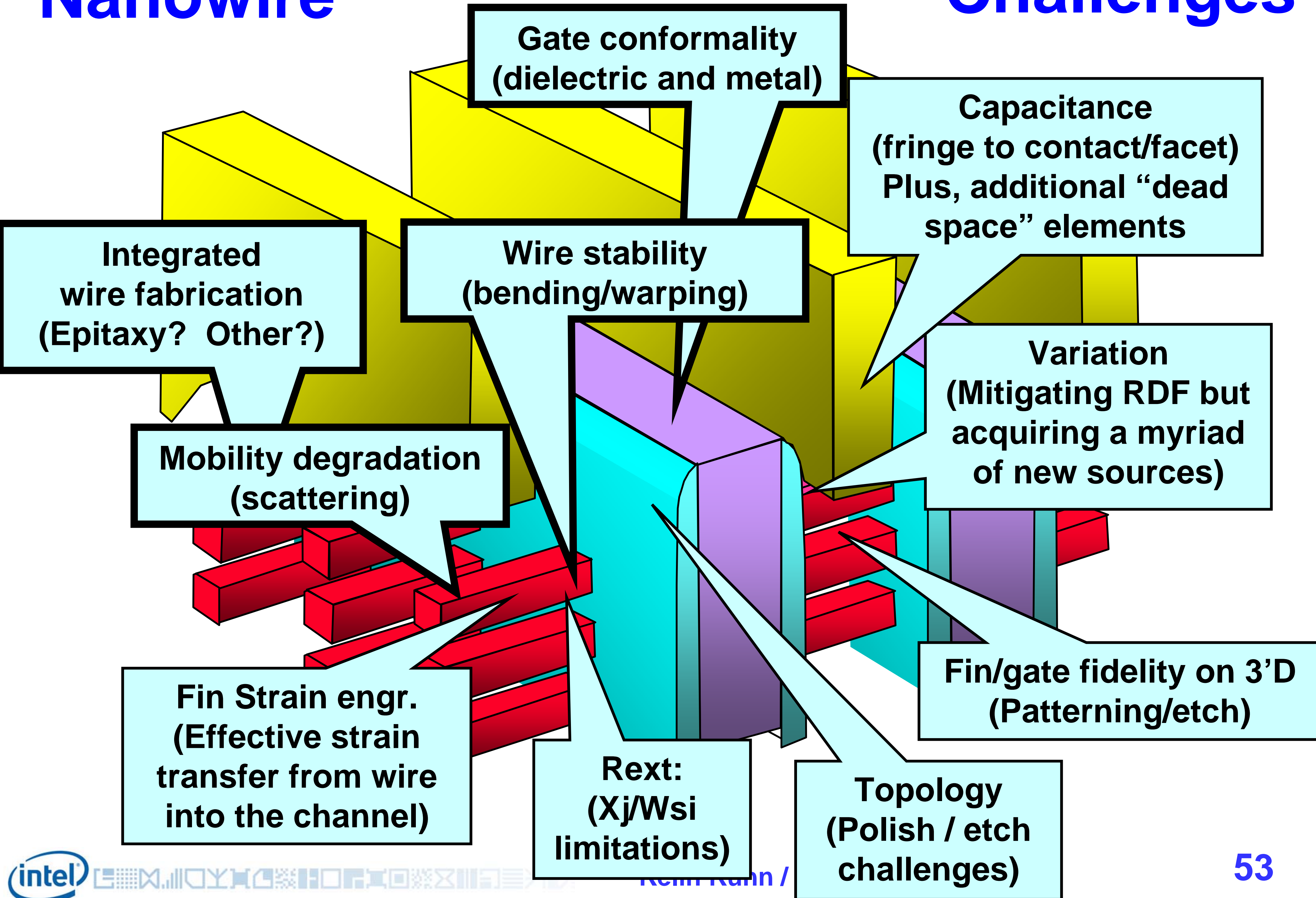
Nanowire Benefits



Nanowire Benefits

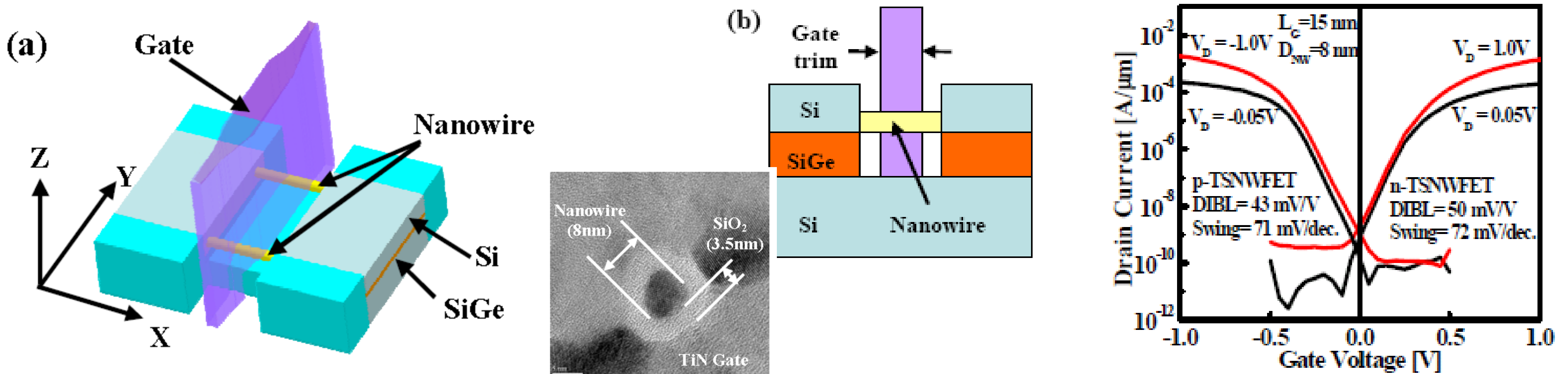


Nanowire Challenges



Nanowire FETs

Yeo – Samsung – IEDM 2006



Dupre – CEA-LETI – IEDM 2008

(a)
Gate
A'
Source
(Cyclic SEG)
A
Gate
Drain
(Cyclic SEG)

(a) 3D-NWFET
w_{Si}=14nm
Poly Si
Si
Si
G
Si
HfO_2+TiN
BOX

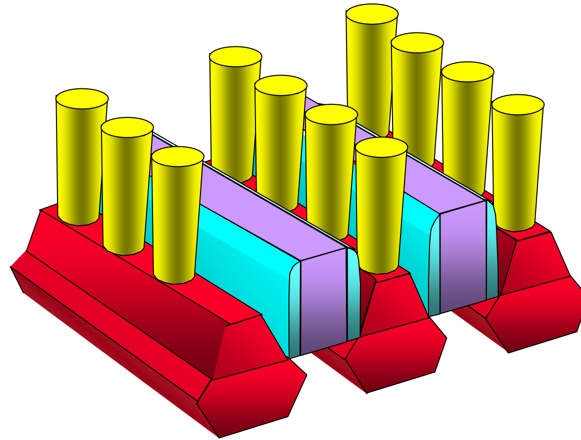
(b) ΦFET
16nm
Si
HTO
SiN
Si
G1
G2
Si
28nm
Si
PolySi
HfO_2+TiN

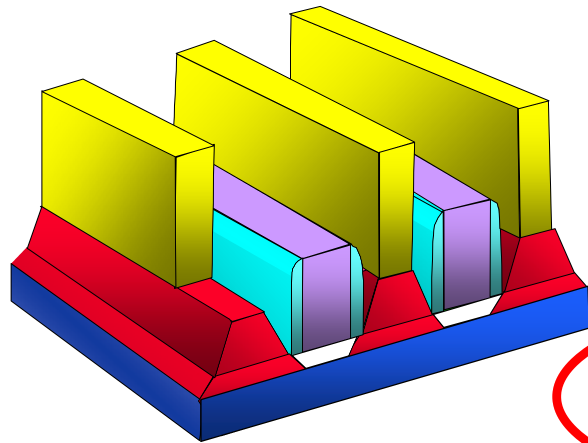
DIBL (mV/V)
FinFET w_{Si}=20nm
FinFET w_{Si}=6nm
3D-NWFET 15nm
Gate length L (μm)

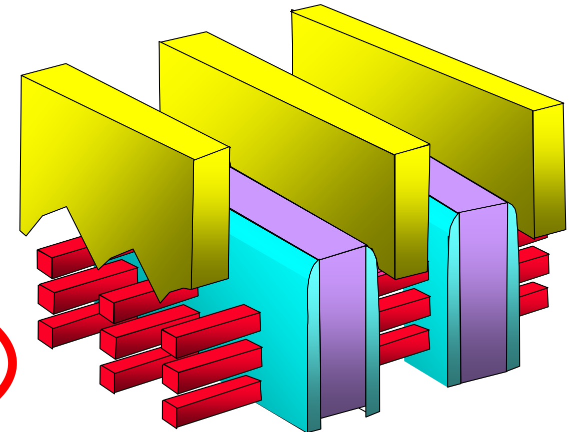
Electron μ_{eff} (cm²/V/s)
FinFET w_{Si}=20nm
ΦFET w_{Si}=15nm
3D-NWFET w_{Si}=15nm
FinFET w_{Si}=6nm
N_{inv} (x10^{12}cm^{-2})

AGENDA

- Scaling history
- Gate control
  - High-k metal-gate
  - Structural enhancements
- Resistance
- Capacitance
- Mobility
  - Strain
  - Orientation
  - Advanced channel materials
- Summary



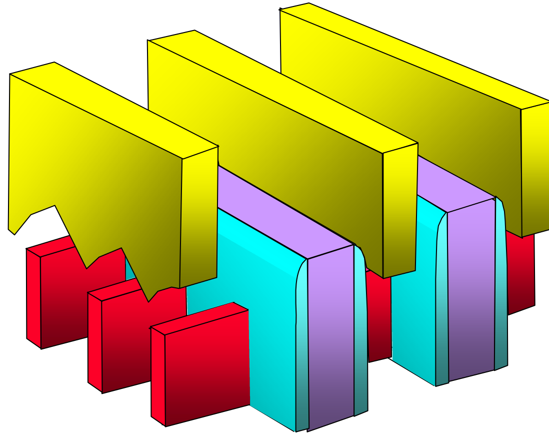


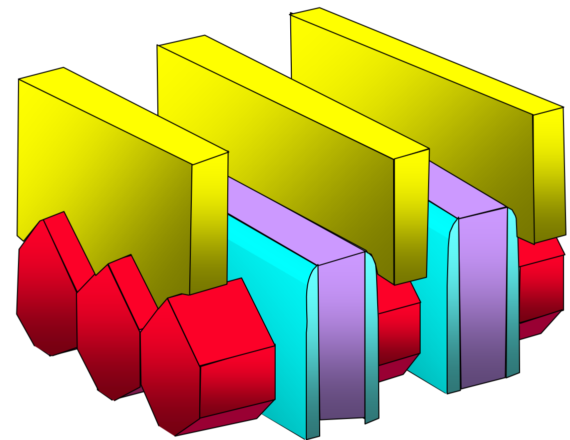


Resistance

Capacitance

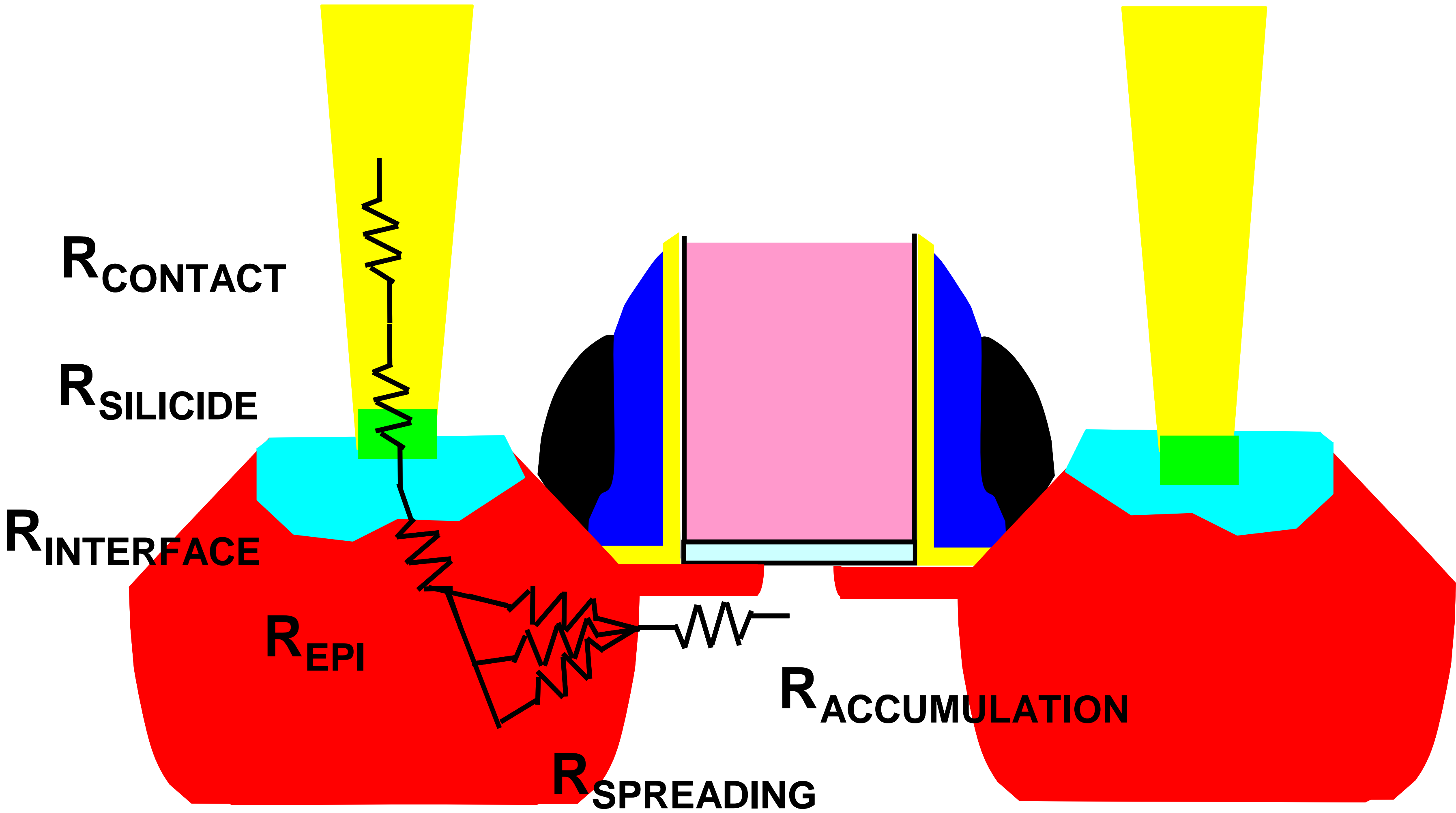
Mobility



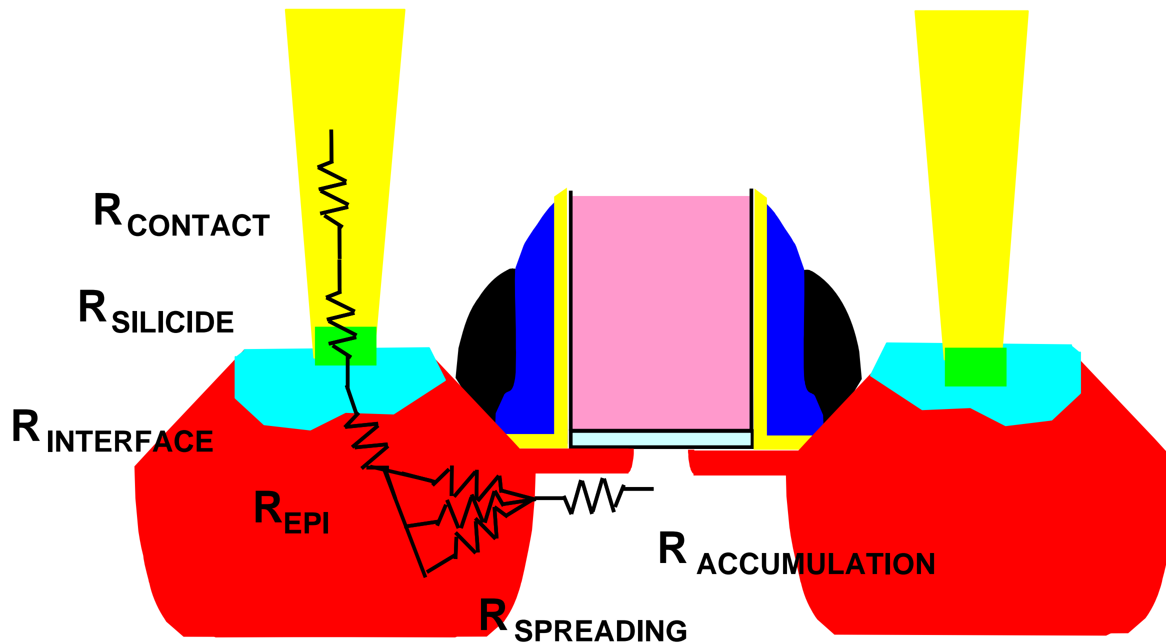


Challenges for ALL Architectures

Planar Resistive Elements



Improvement in Planar Elements



$$R_{\text{interface}} \propto \exp\left(\frac{q\phi_B}{\sqrt{N_D}}\right)$$

$$R_{\text{interface}} \propto \frac{1}{A}$$

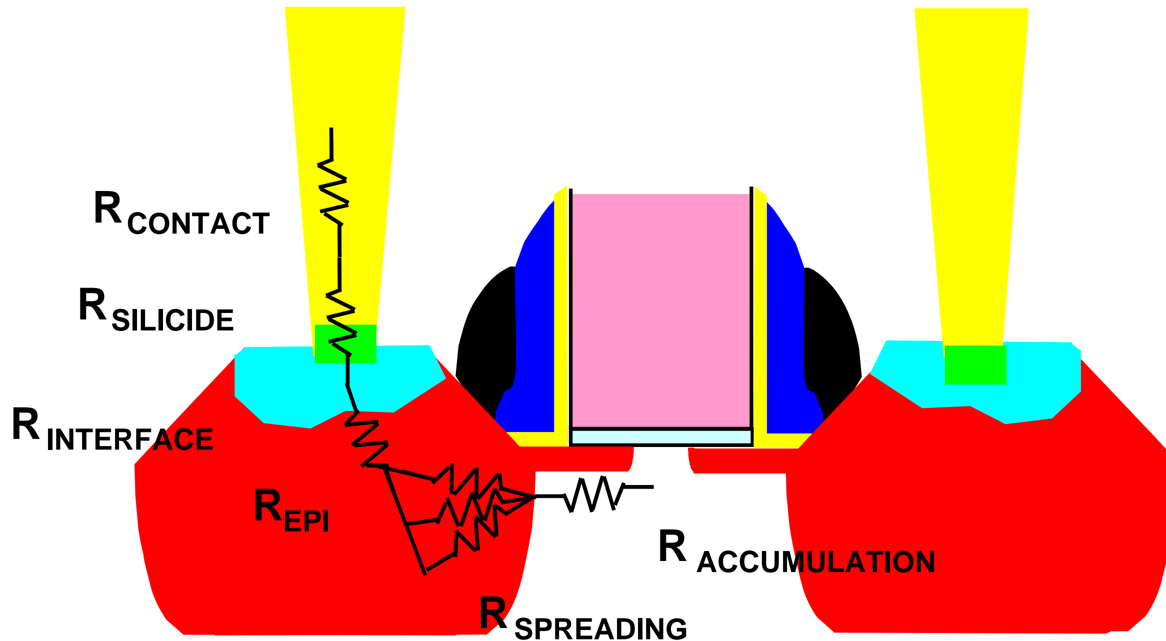
$q\phi_B$ – *Schottky Barrier Height (SBH)*

N_D – *Substrate doping conc.*

A – *Contact area*

- Evolutionary R_{acc} improvement through X_j scaling (anneal/implant) until the end of the planar roadmap (thereafter Tsi/Wsi limited)
- R_{epi} / $R_{spreading}$ improvement from raised source/drain (RSD)
- Limited $R_{silicide}$ improvement (NiSi has the lowest known resistivity)
- Significant possibility for $R_{interface}$ improvement, particularly through SBH optimization ($R_{interface}$).
- $R_{contact}$ improvement from high conductivity metals (copper?)

Improvement in Planar Elements



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- $R_{contact}$ improvement from high conductivity metals (copper?)

Schottky theory vs. experimental SBHs for metals on nSi
Mukherjee – Intel

Schottky theory
Experiment

ϕ_{nSi} (e.v.)

1.3
1.1
0.9
0.7
0.5
0.3
0.1
0.1

4th period transition metals

5th period transition metals

6th period transition metals

Lanthanides

Ti 22;4
V 23;4
Cr 24;4
Mn 25;4
Fe 26;4
Co 27;4
Ni 28;4
Y 39;5
Zr 40;5
Nb 41;5
Mo 42;5
Ru 44;5
Rh 45;5
Pd 46;5
Gd 64;6
Dy 66;6
Er 68;6
Yb 70;6
Hf 72;6
Ta 73;6
W 74;6
Re 75;6
Os 76;4
Ir 77;6
Pt 78;6

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

Desired for PMOS

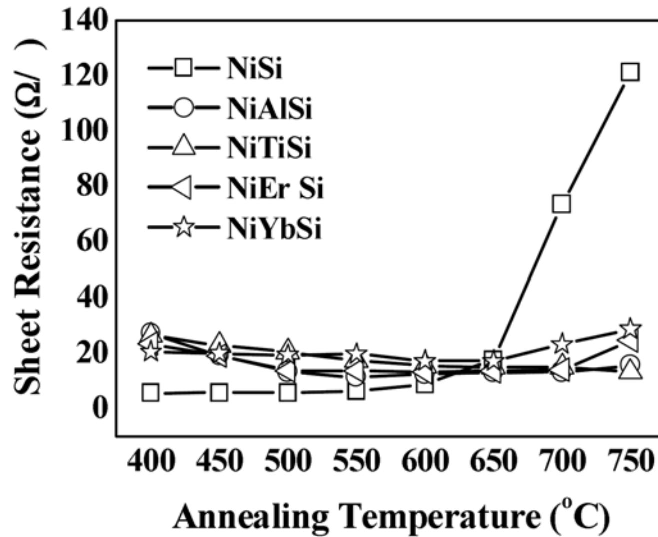
Si Mid-Gap

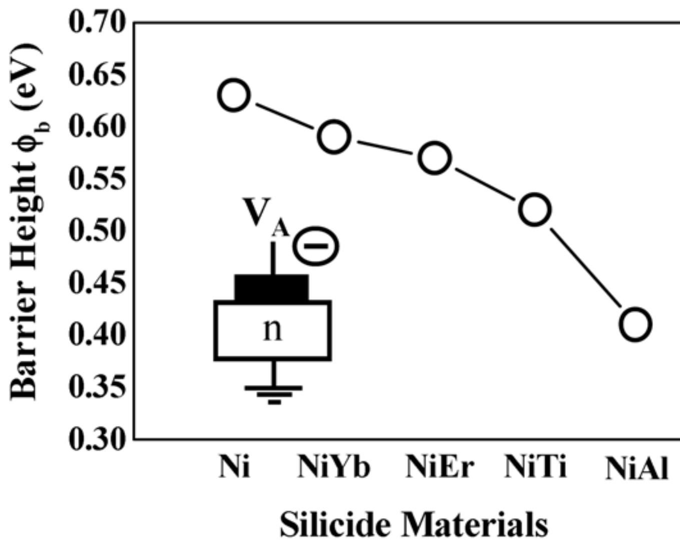
Desired for NMOS

Fermi level pinned to mid-gap for most metals on Si

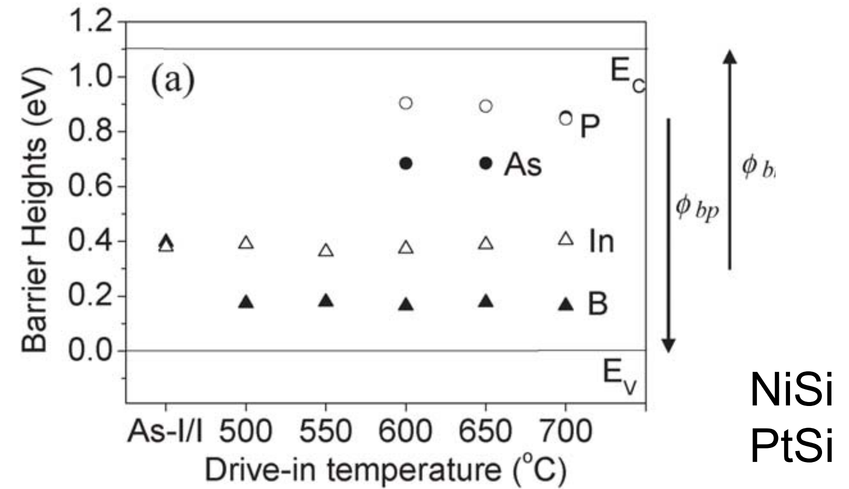
K. Kuhn – IEDM SC 2008

Alloy and Implant Modifications to Silicides

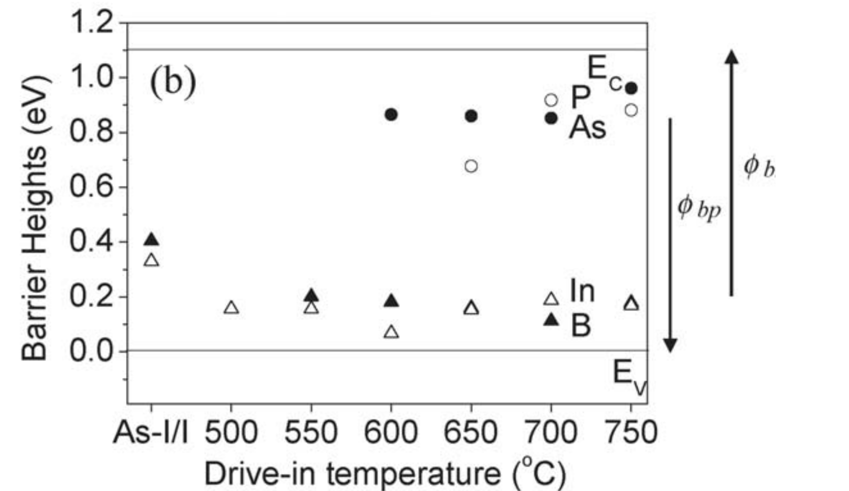




Lee –NUS-Singapore
IEDM 2006
Ni-alloy silicides

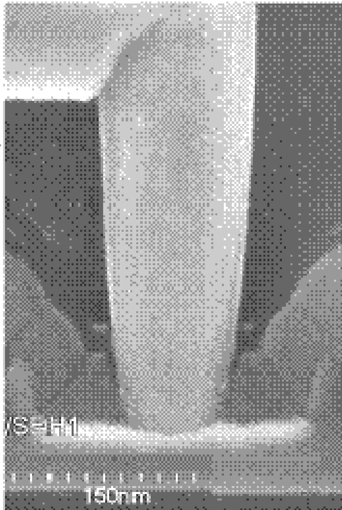


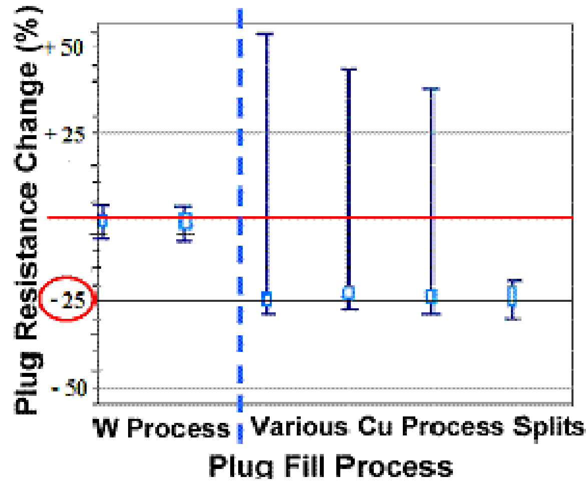
NiSi
PtSi

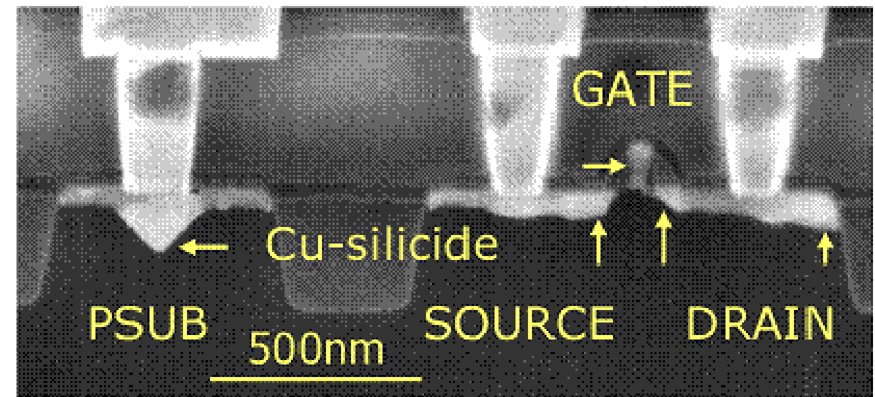


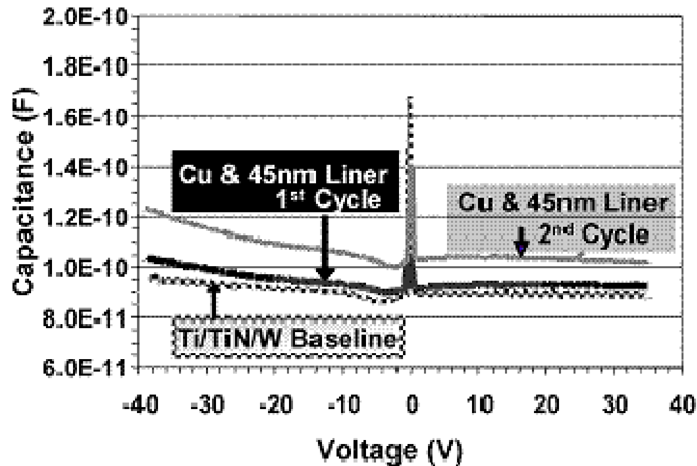
Zhang – KTH Sweden
EDL 2007
Implant modification of SBH
(SB FET paper)

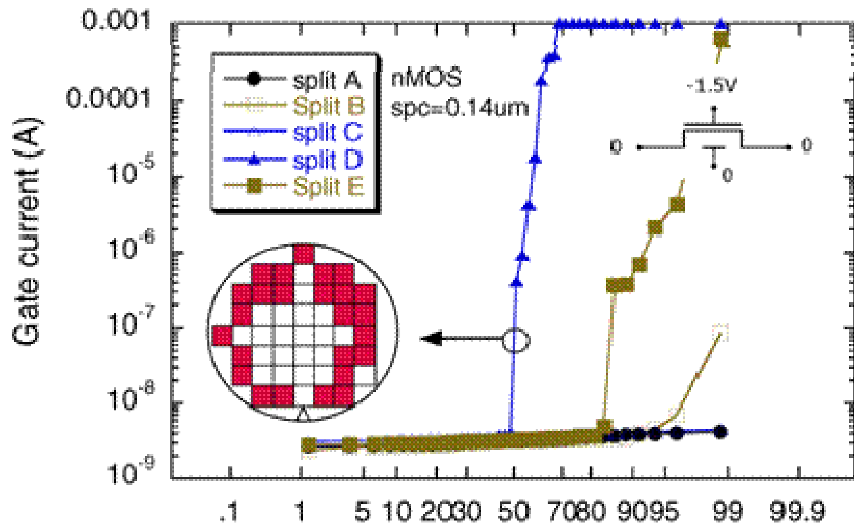
Copper Contacts





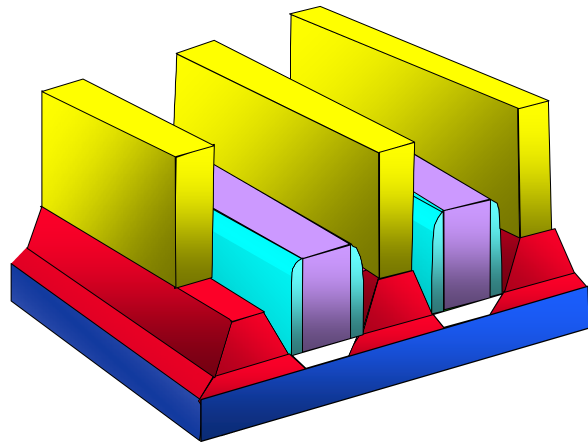


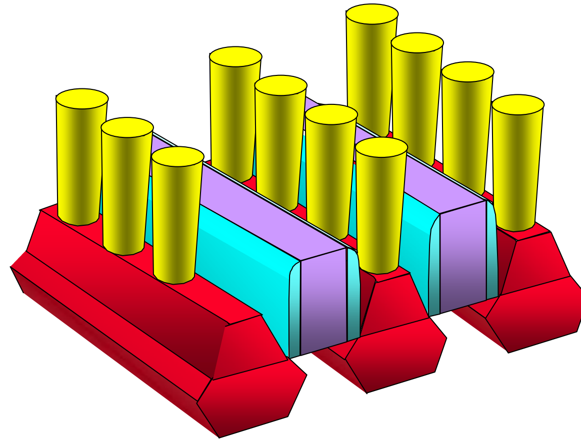


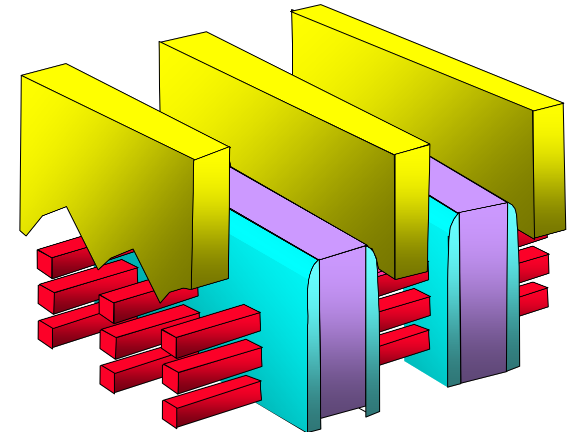


Topol – IBM
VLSI 2006
Fabrication of Cu contacts

Van den Bosch – IMEC
IEDM 2006
Challenges of Cu contacts



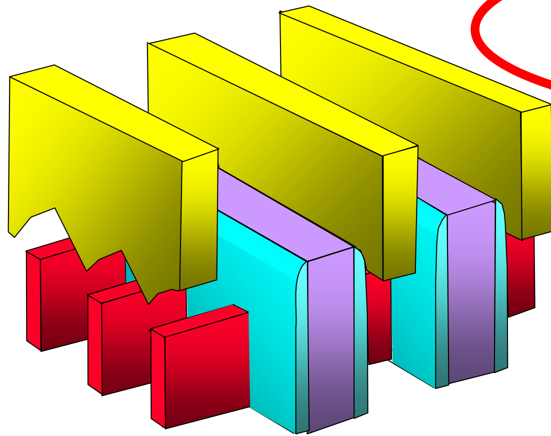


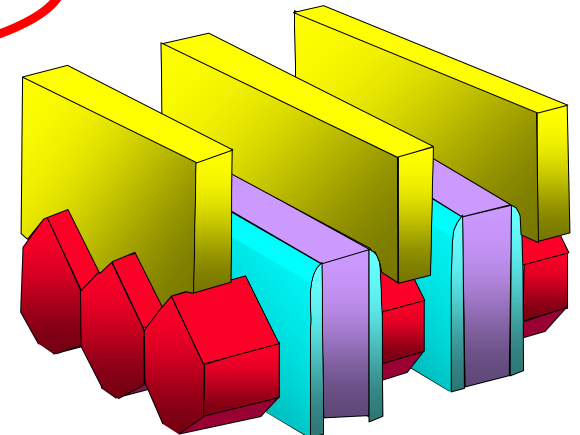


Resistance

Capacitance

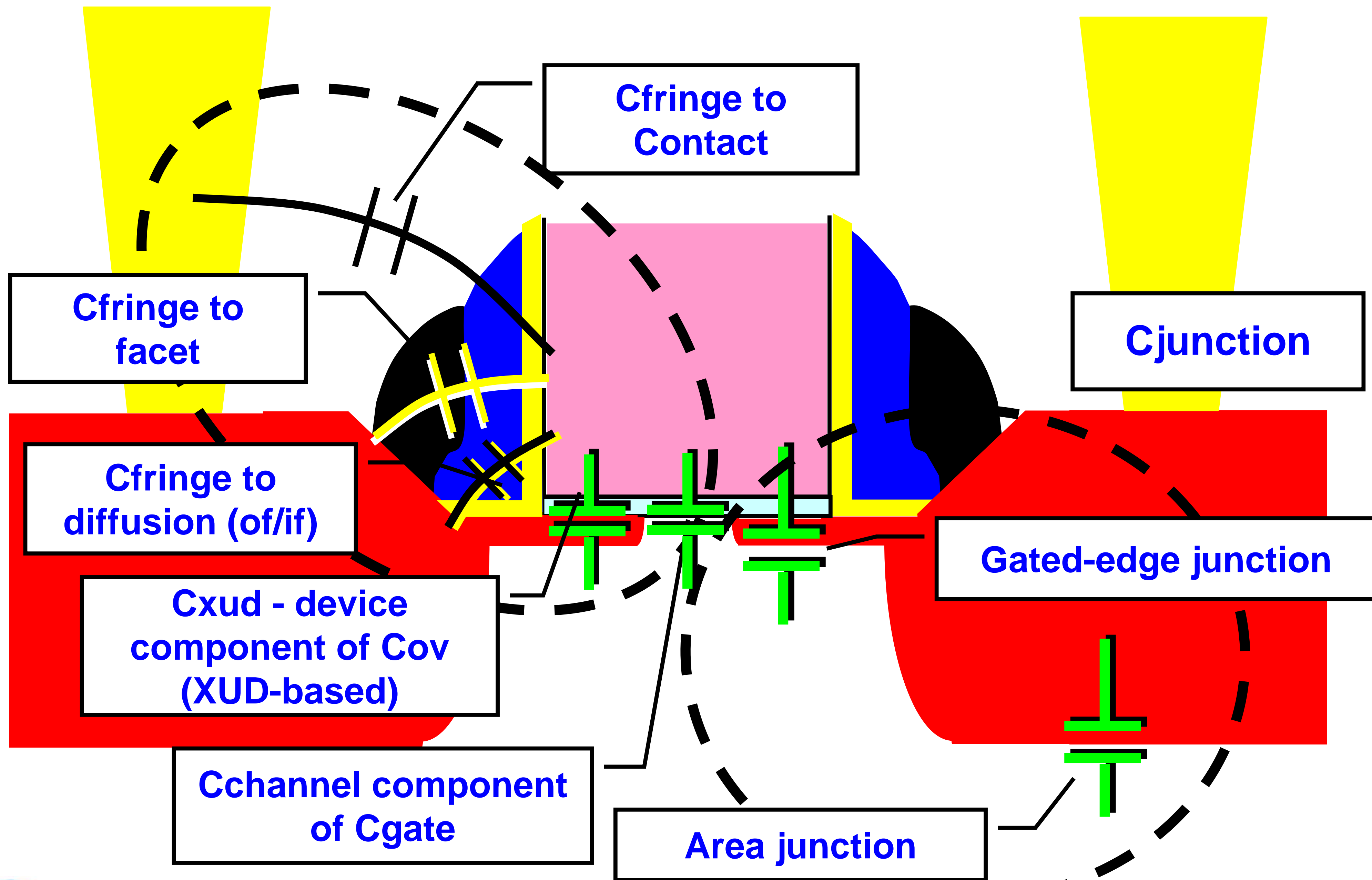
Mobility



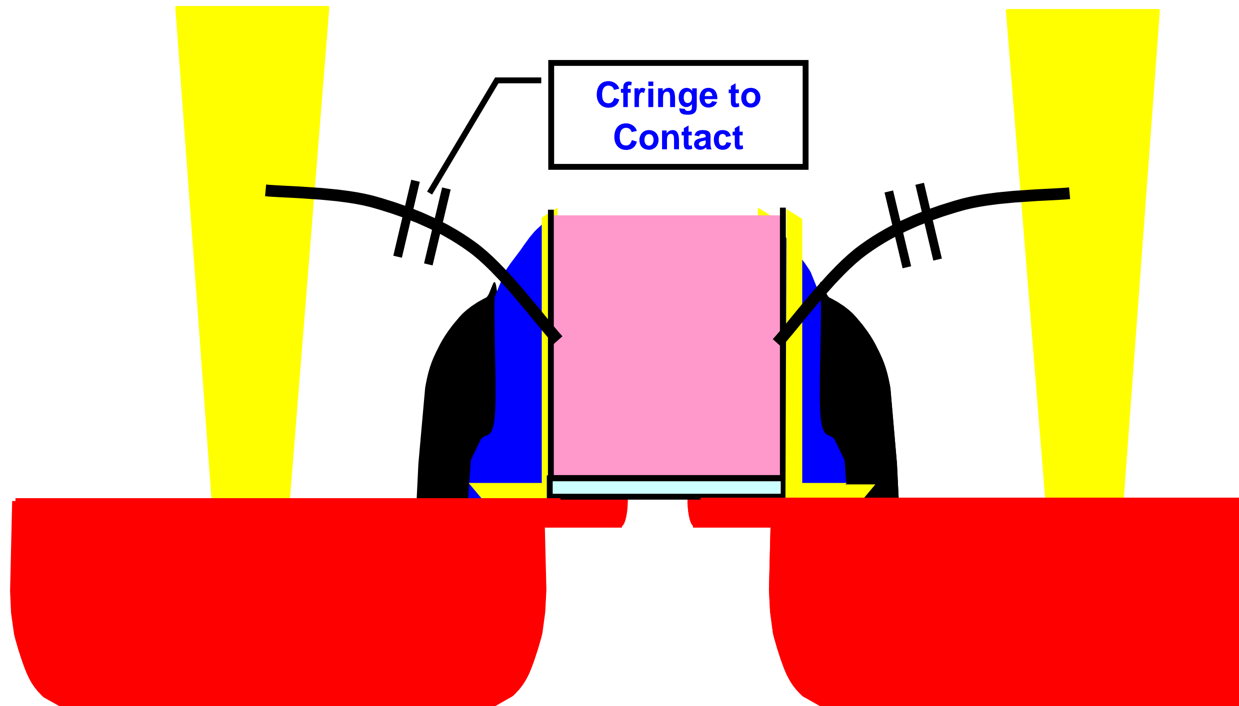


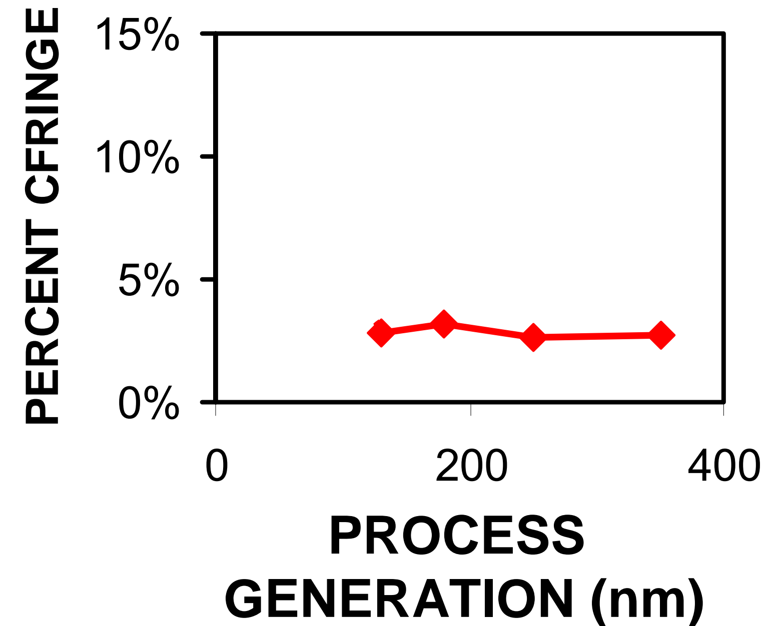
Challenges for ALL Architectures

Planar Capacitive Elements



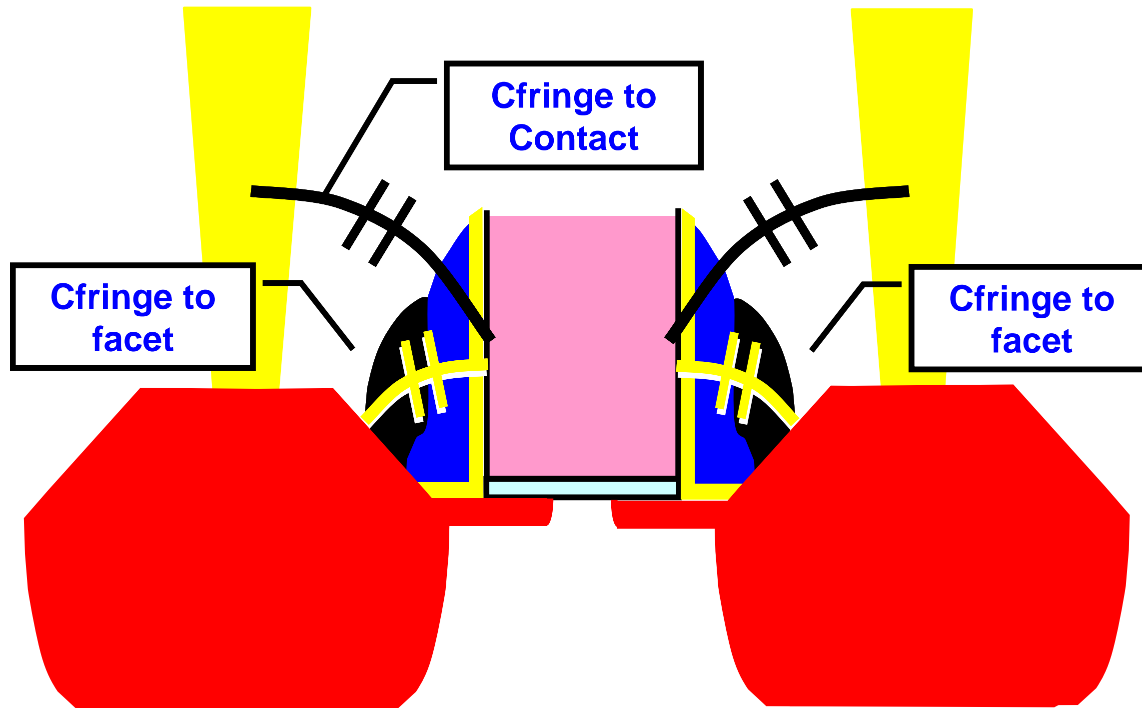
Planar Capacitive Elements

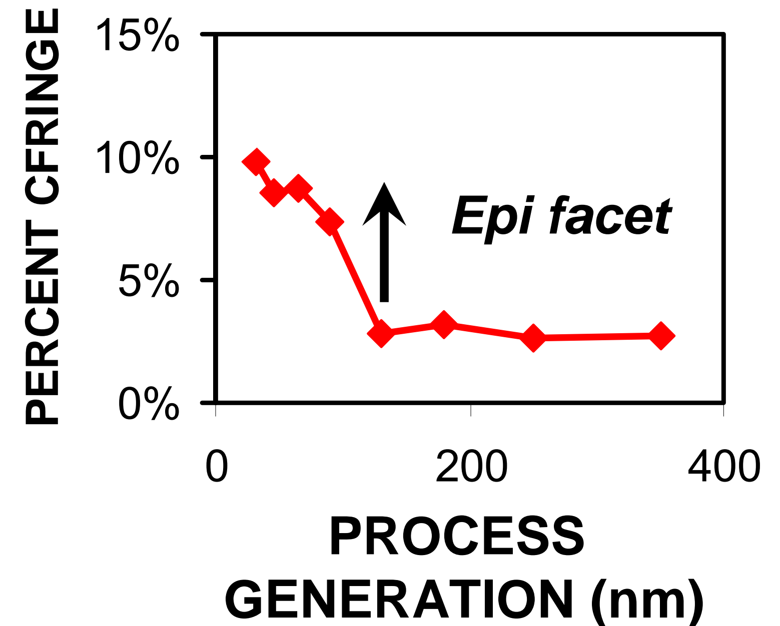




“Golden” days of scaling:
Who worried about Cfringe?

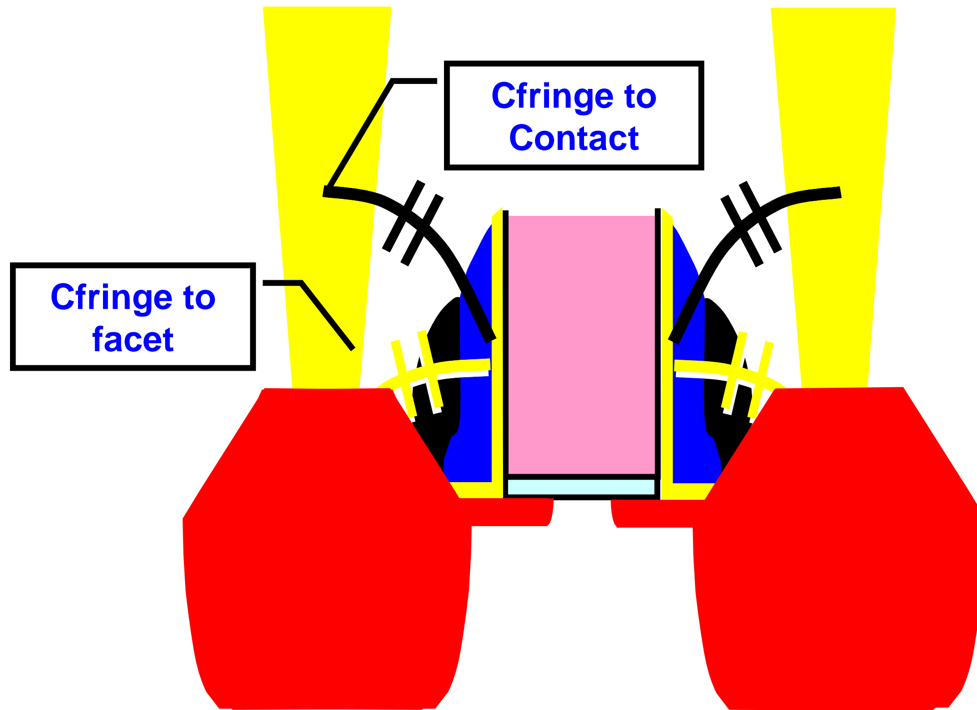
Planar Capacitive Elements

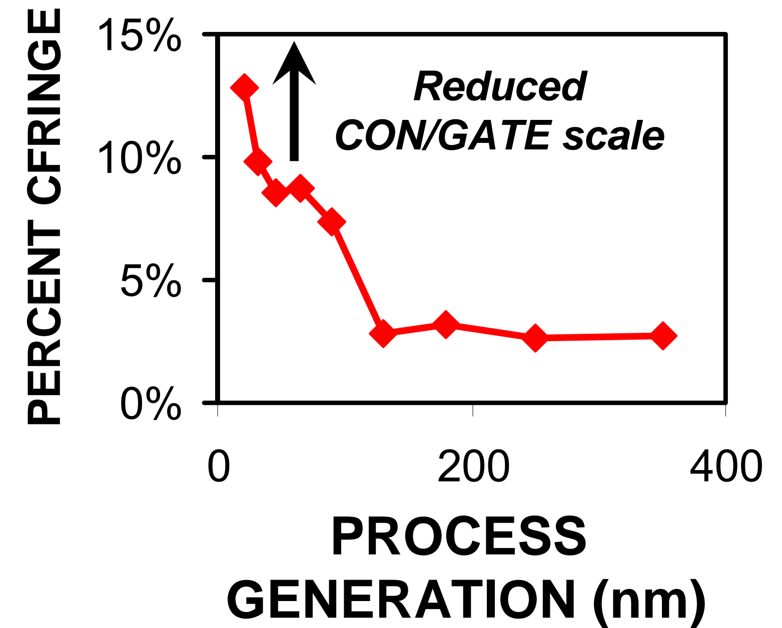




"Silver" days of scaling: Introduction of epi: Increased fringe due to facet

Planar Capacitive Elements

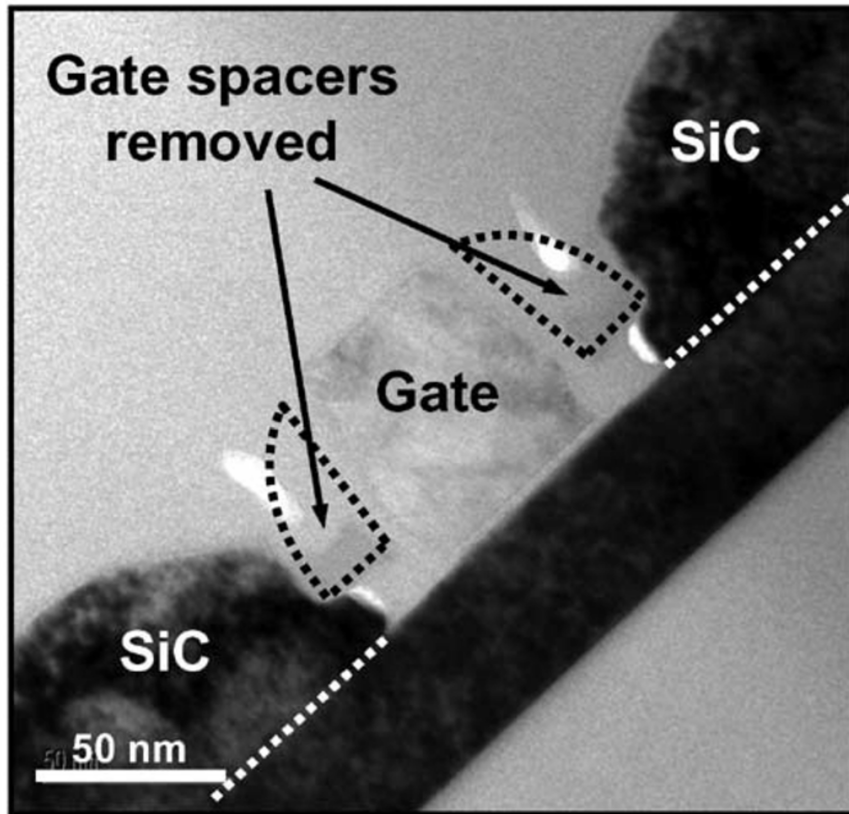




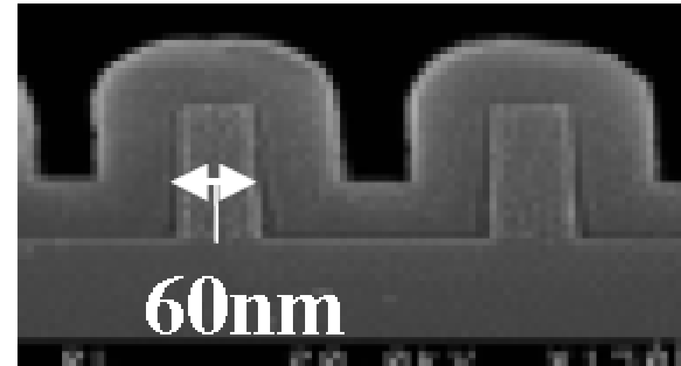
“Bronze” days of scaling

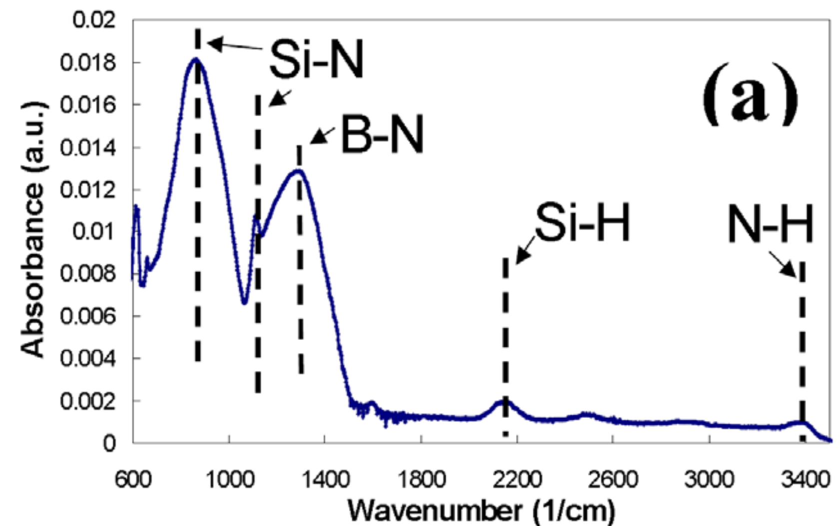
Gate and contact CD dimensions scaling slower than contacted gate pitch – fringe matters

Innovative Spacer Technologies

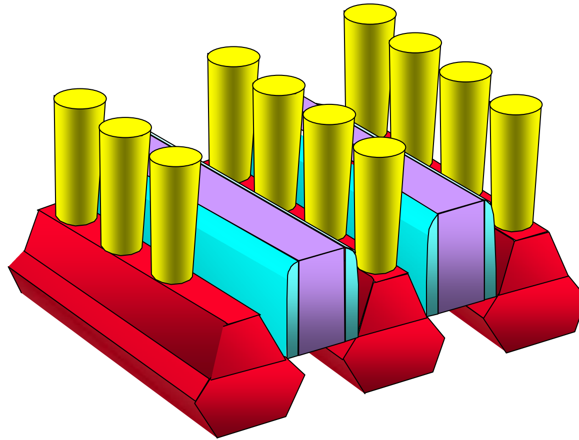


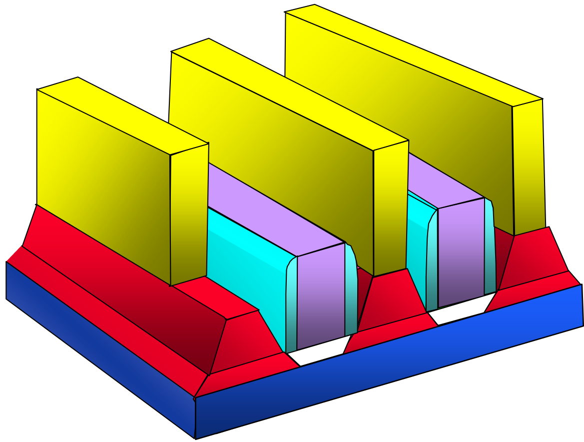
SPACER REMOVAL
Liow – NUS Singapore
EDL 2008

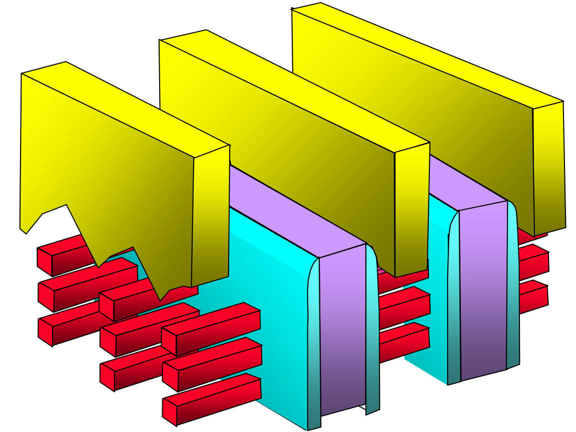




SiBCN (Low-K) SPACER
Ko –TSMC
VLSI 2008



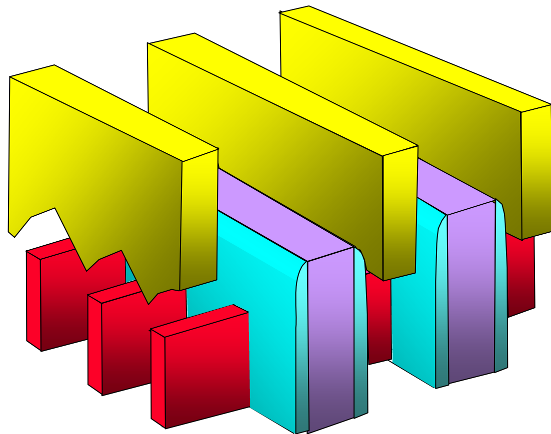


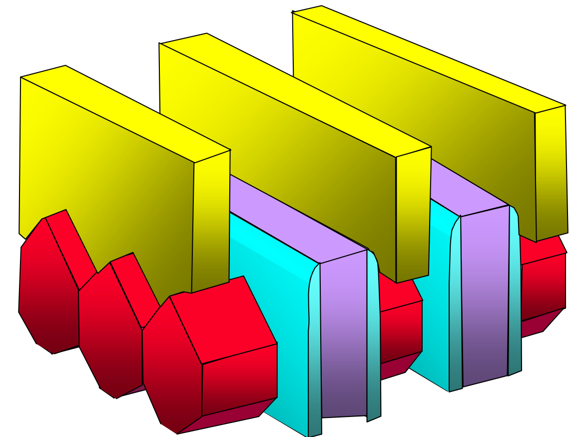


Resistance

Capacitance

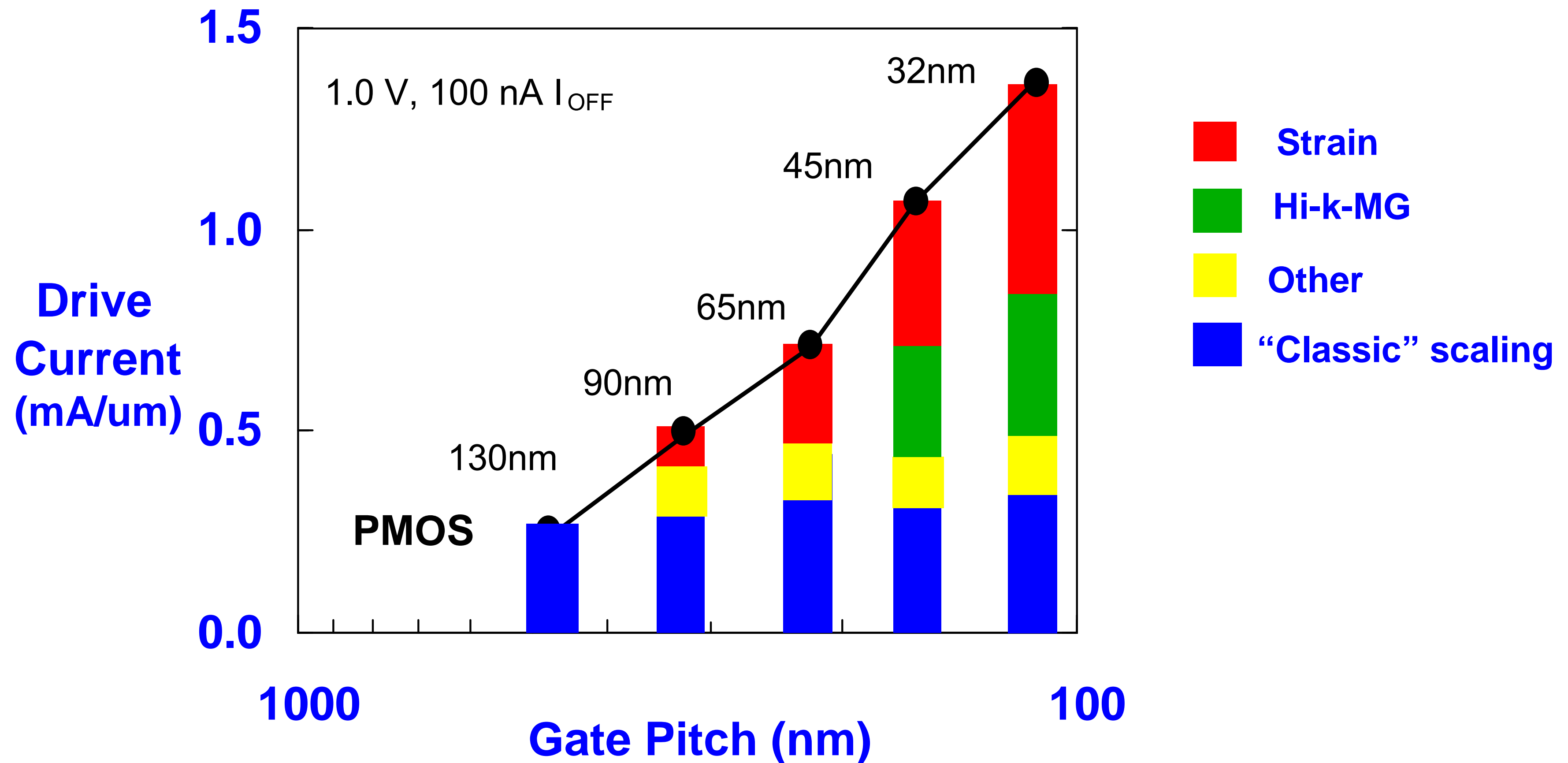
Mobility





Challenges for ALL Architectures

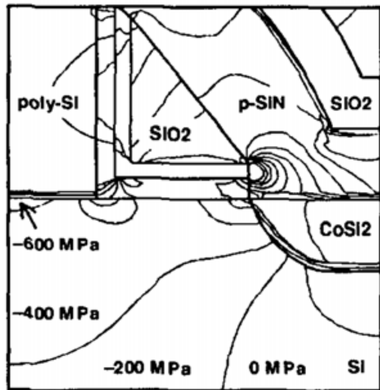
Transistor Performance Trend

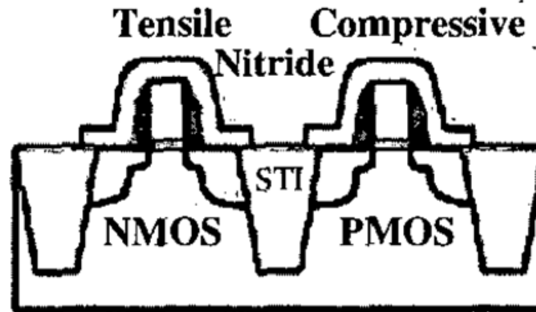


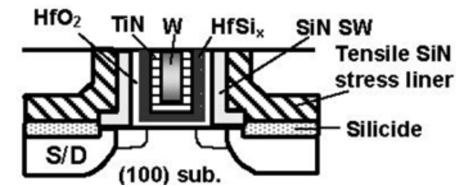
Strain is a critical ingredient in modern transistor scaling

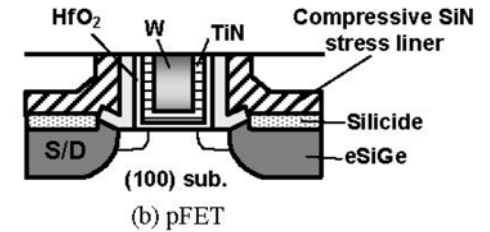
Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation

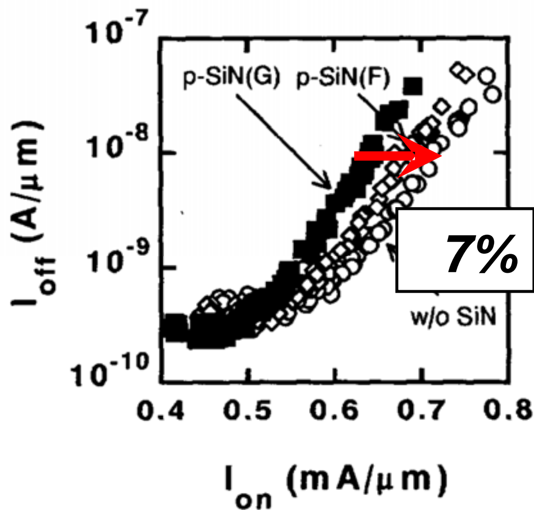
Etch-stop nitride (CESL)

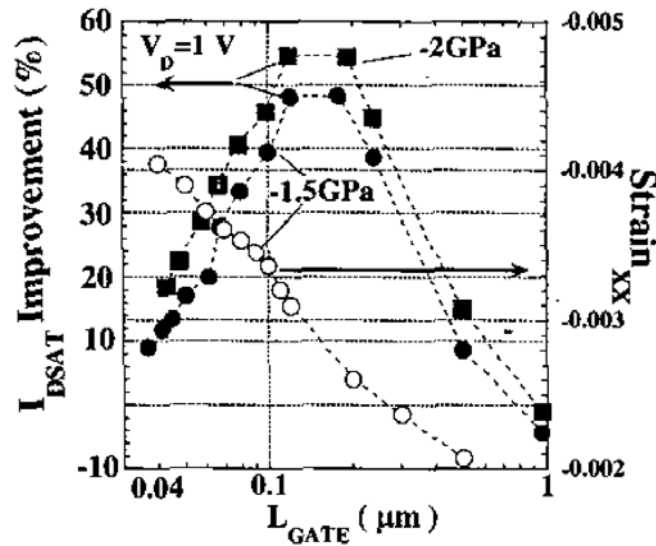


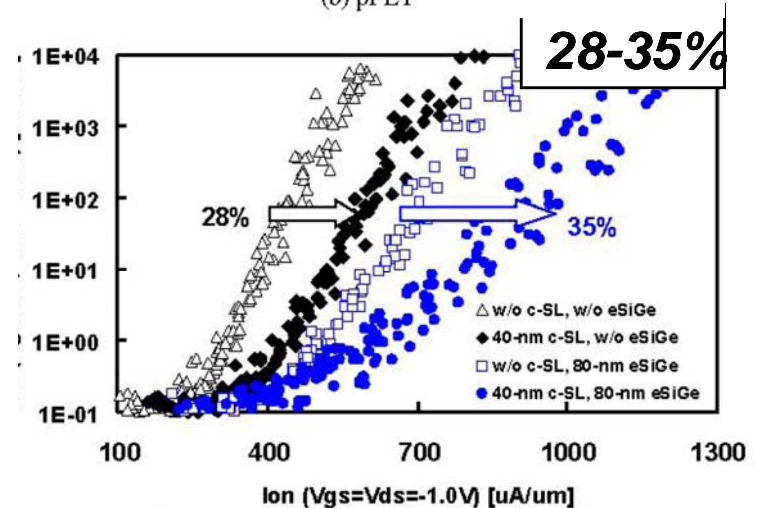










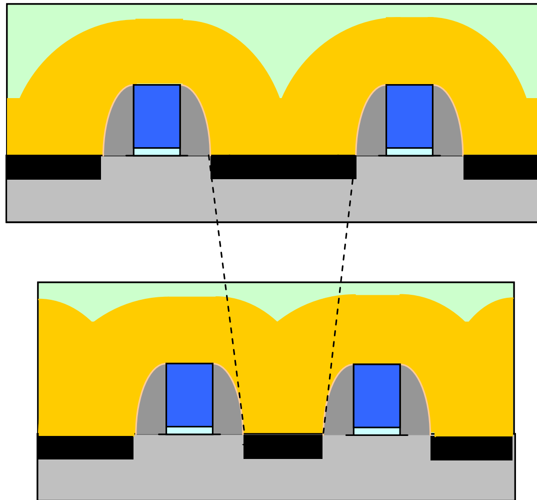


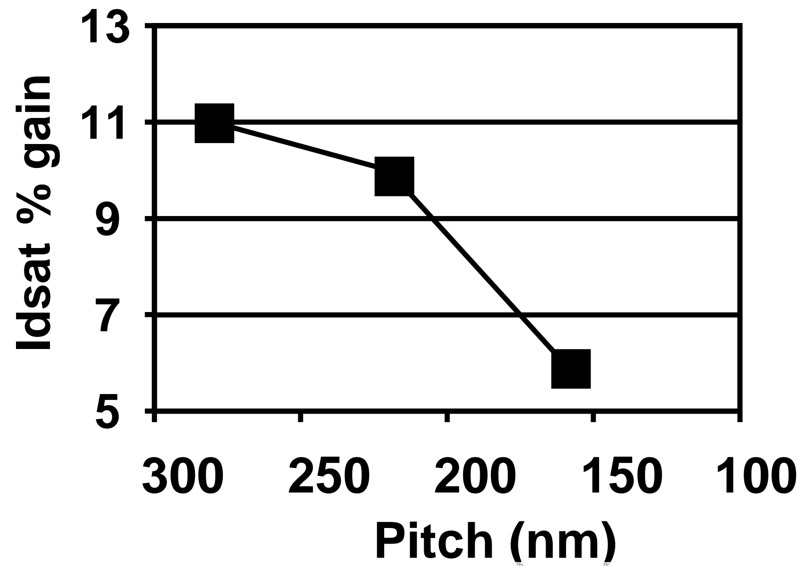
Ito – NEC
IEDM 2000
NMOS SiN strain

Pidin – Fujitsu
IEDM 2004
N and PMOS

Mayuzumi – Sony
IEDM 2007
Dual-cut stress liners (MG process)

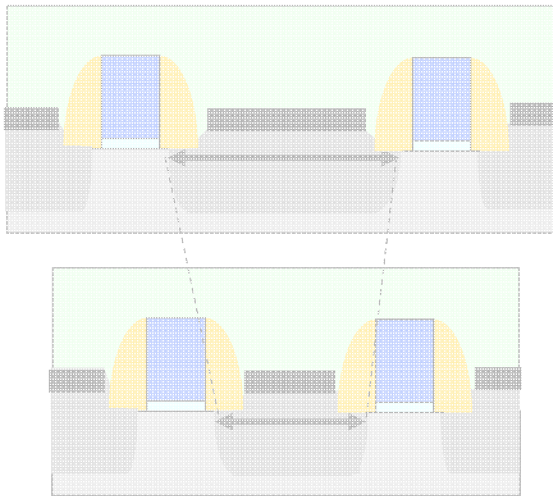
Strain: Pitch dependence

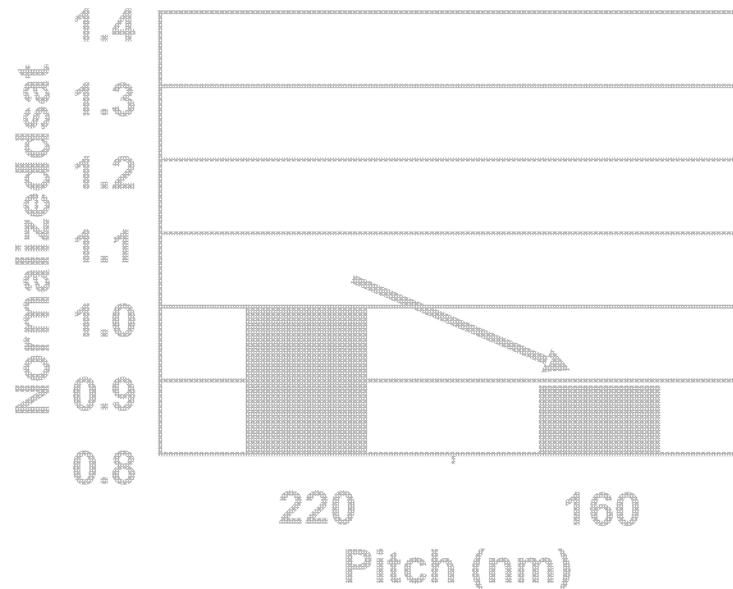




NMOS

Pitch degradation increases with film pinchoff, requires higher stress, thinner films



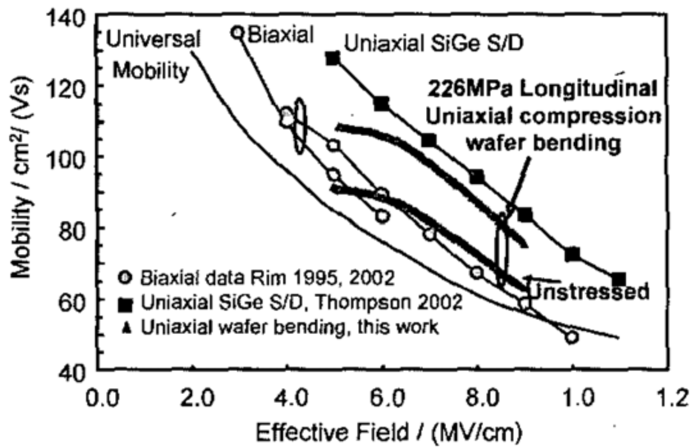


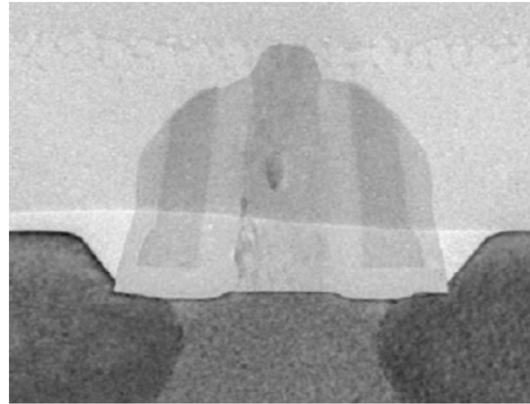
PMOS

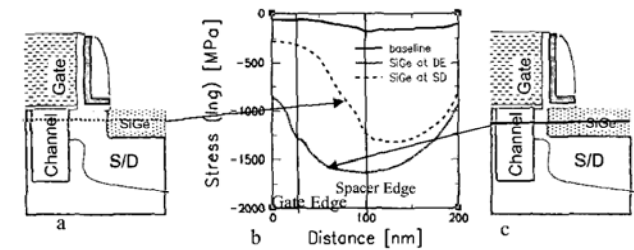
eSiGe S/D mobility strongly dependent on pitch

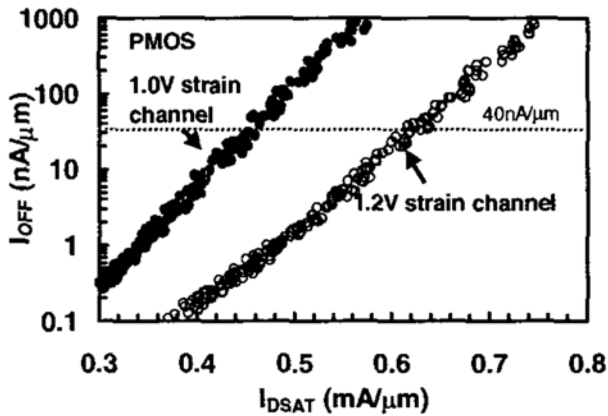
Auth, Intel, VLSI 2008

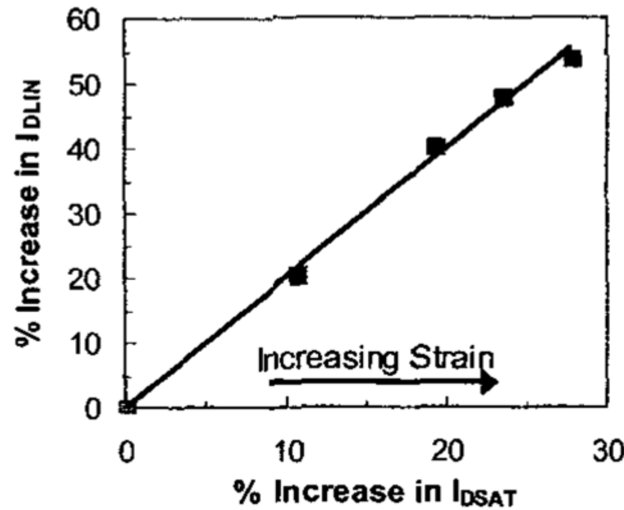
Embedded SiGe (PMOS)

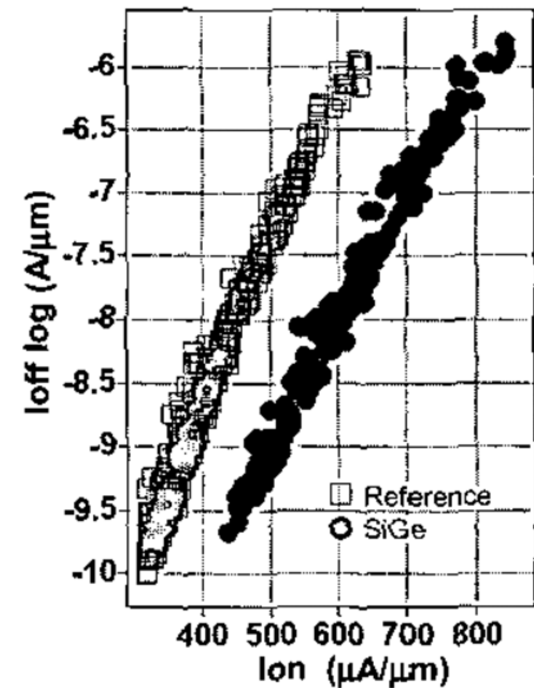










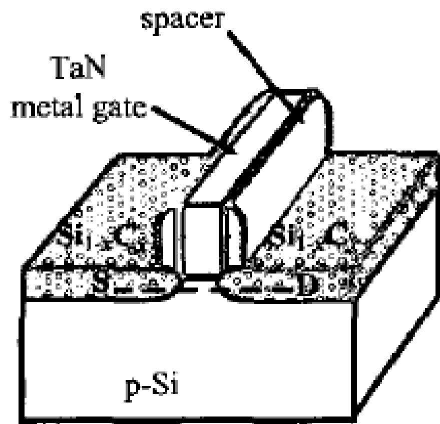


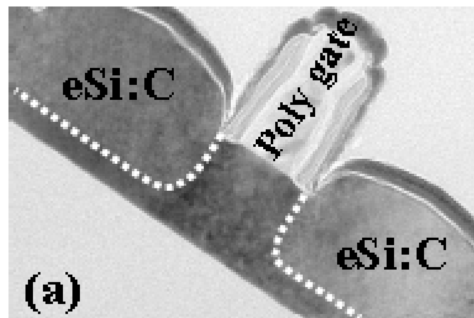
Thompson – Intel
IEDM 2002 / 2004

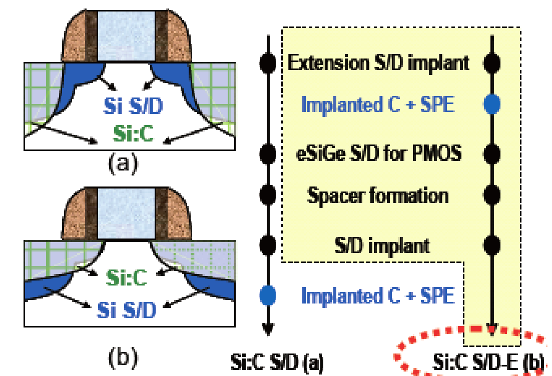
Ghani – Intel
IEDM 2003

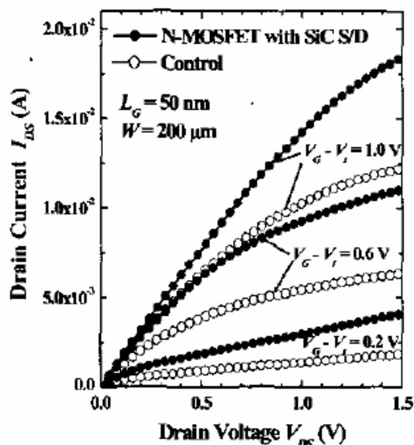
Chidambaram
TI / Applied Materials
VLSI - 2004

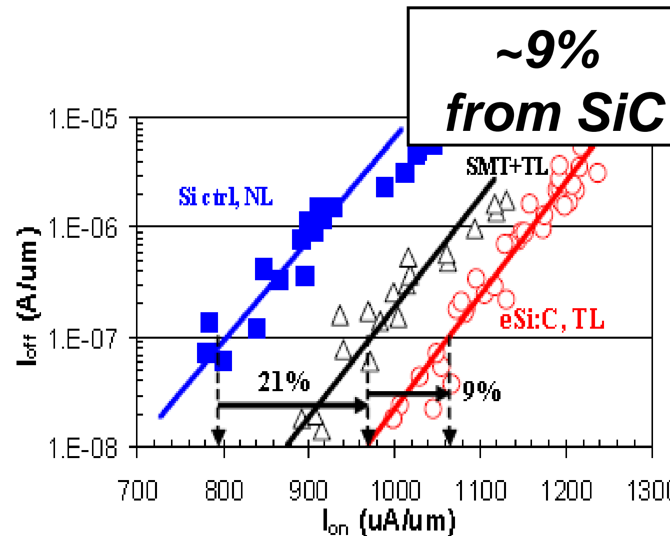
Embedded Si:C (NMOS)

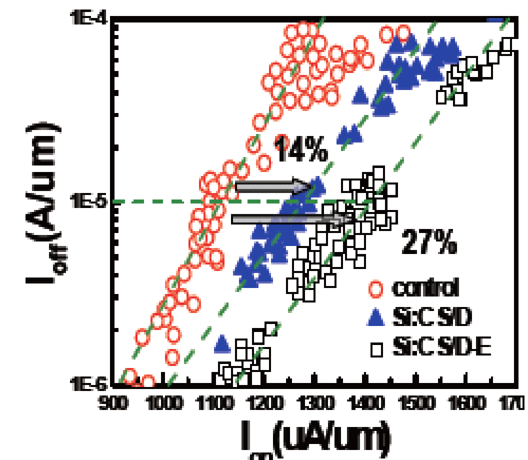










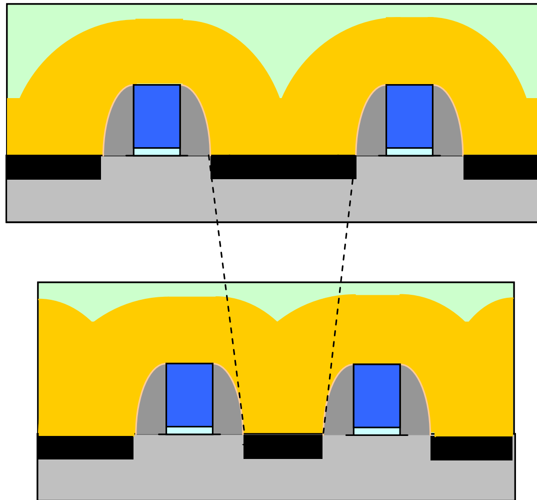


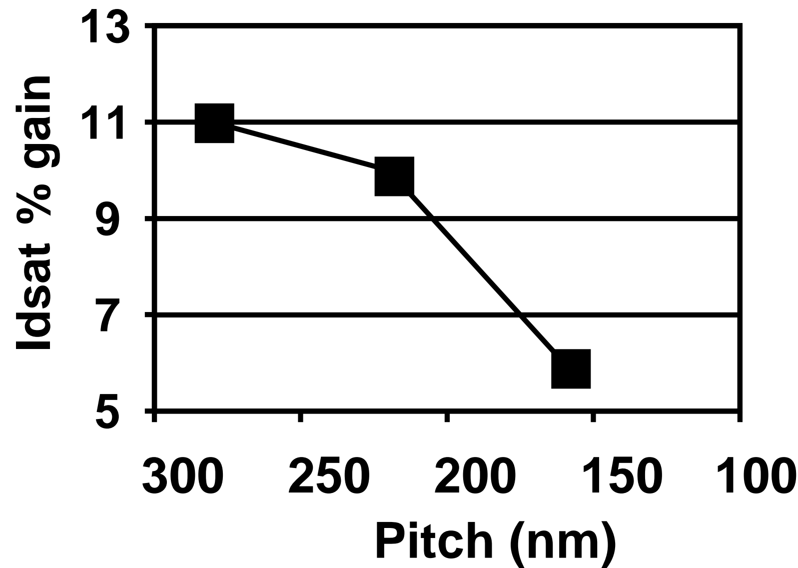
Ang – NUS-Singapore
IEDM 2004
Selective epi SiC (undoped)

Yang – IBM
IEDM 2008
In-situ epi P-SiC

Chung – Nat'l Chiao Tung U.
VLSI 2009
Implanted C + SPE

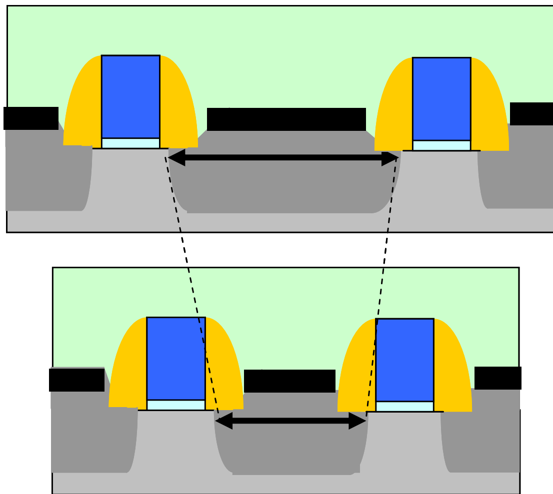
Strain: Pitch dependence

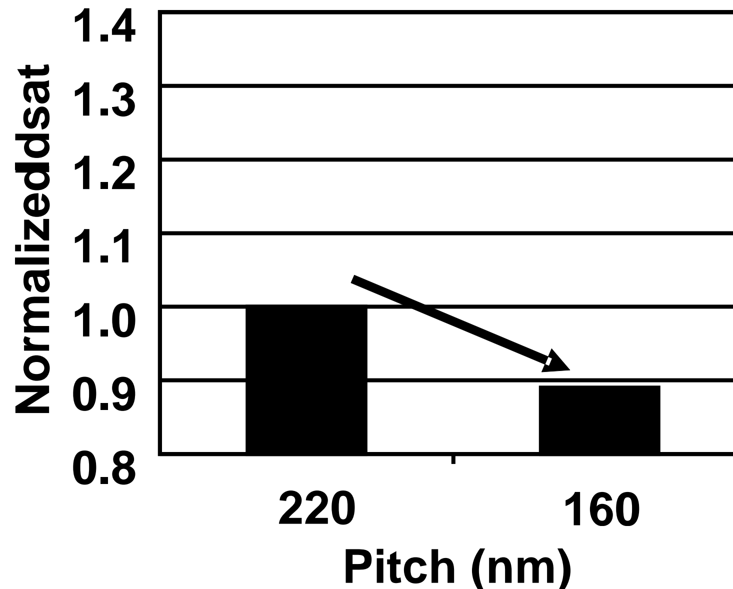




NMOS

Pitch degradation increases with film pinchoff, requires higher stress, thinner films





PMOS

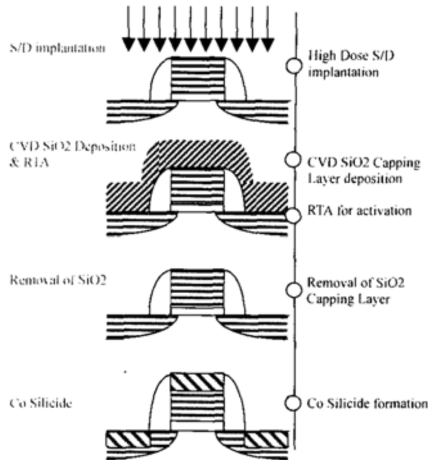
eSiGe S/D mobility strongly dependent on pitch

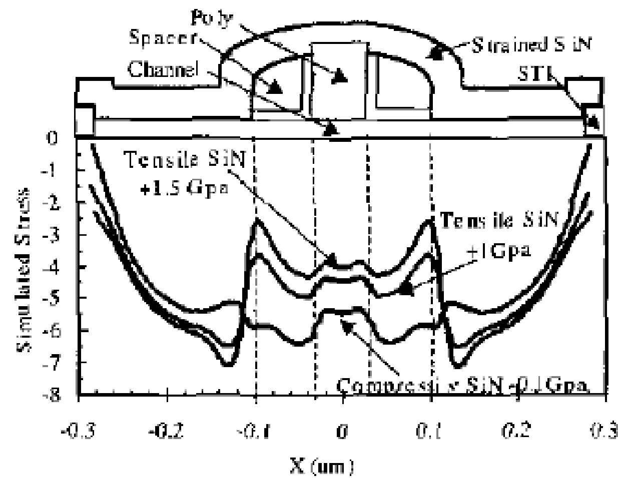
Auth, Intel, VLSI 2008

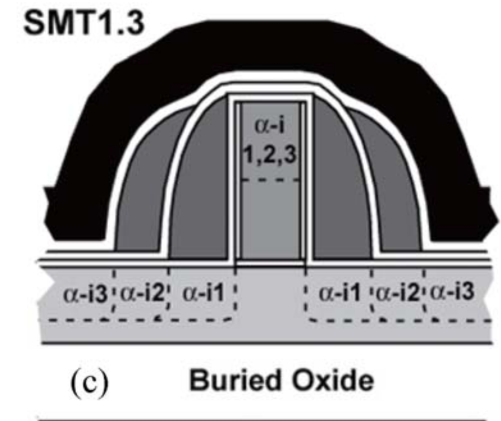
Strain: Pitch dependence

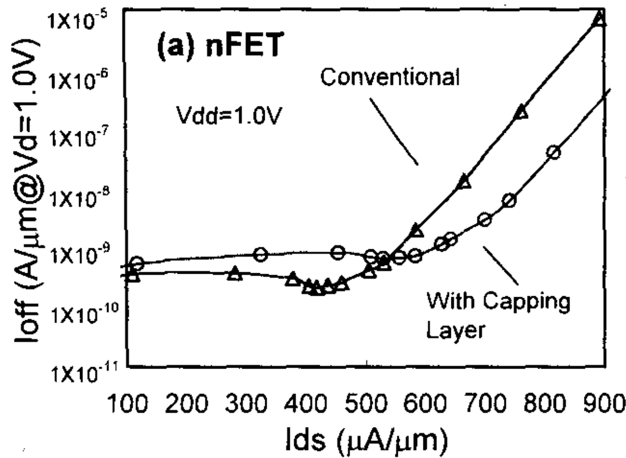
What about strain options less sensitive to pitch?

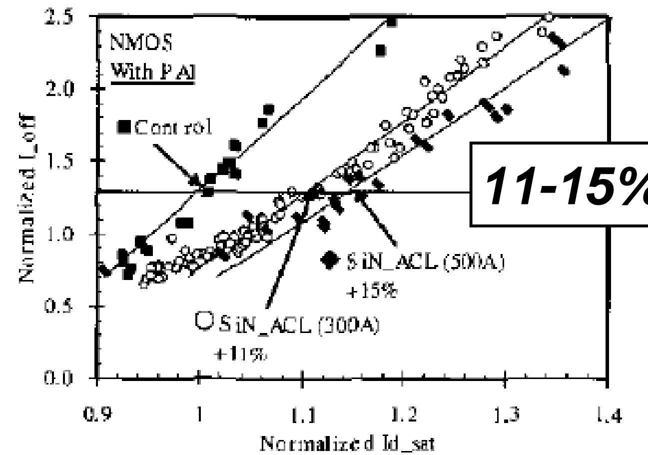
Stress Memorization (SMT)

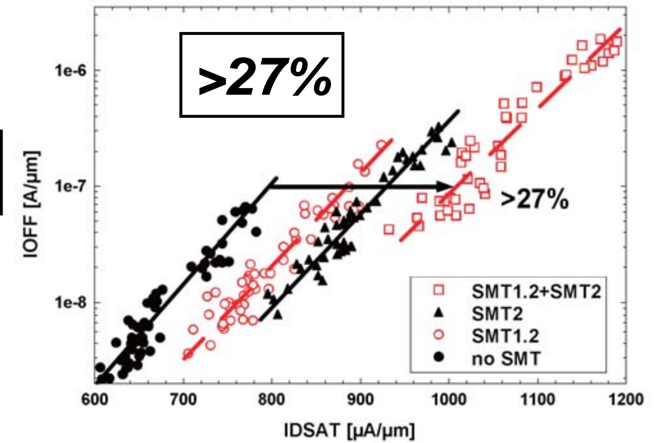










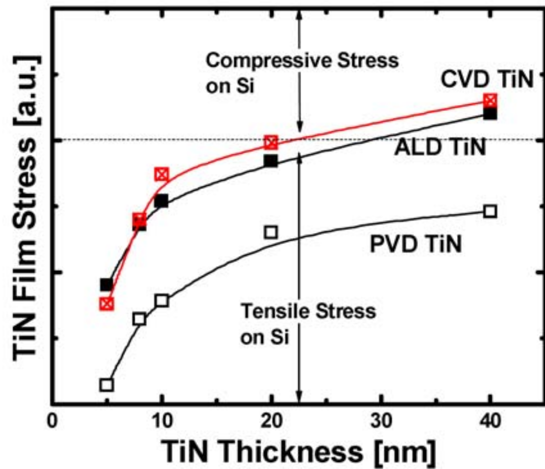


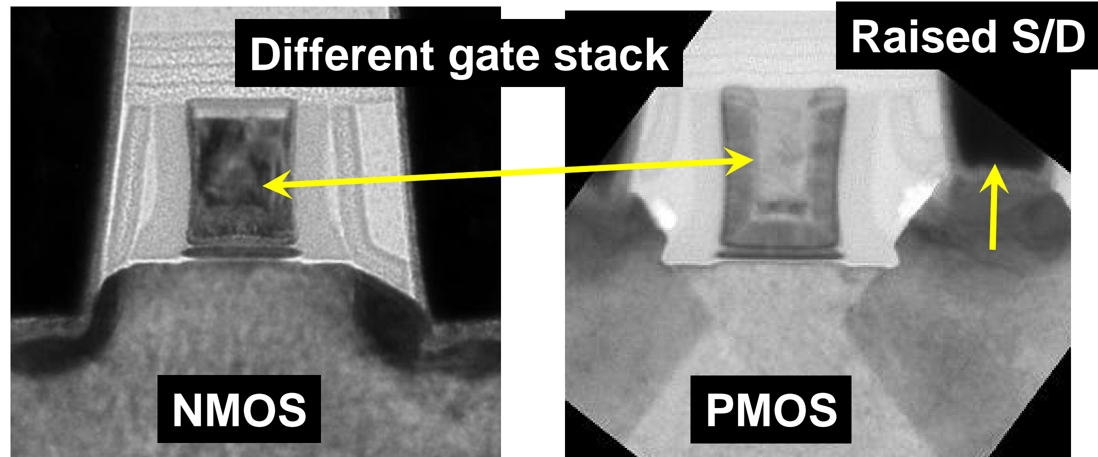
Ota – Mitsubishi
IEDM 2002
NMOS SMT

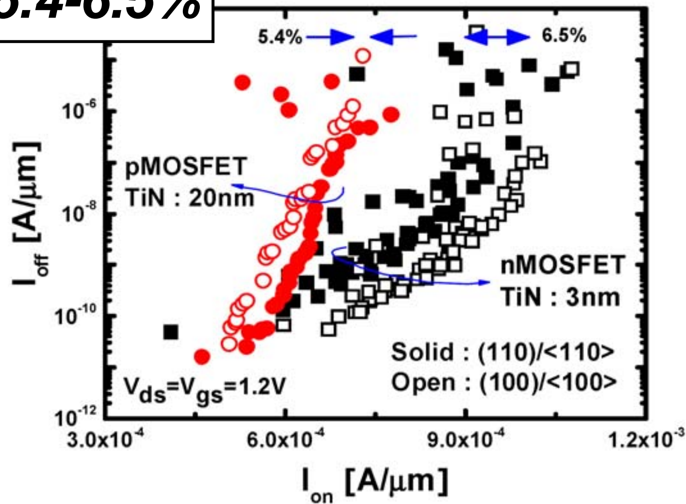
Chen – TSMC
VLSI 2004
NMOS SMT

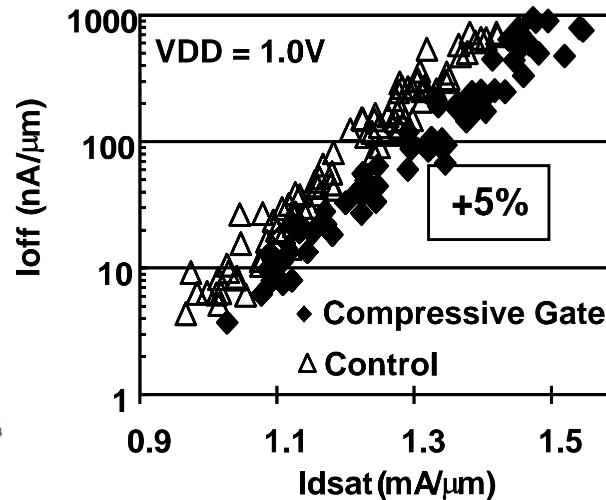
Wei – AMD
VLSI 2007
Multiple liners

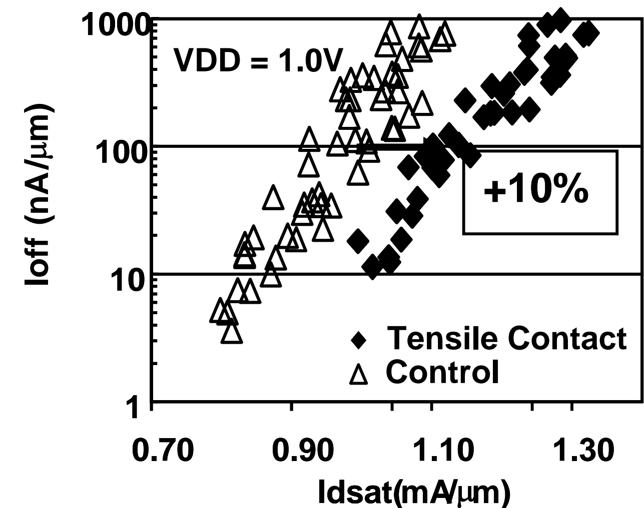
Metal stress (gate and contact)







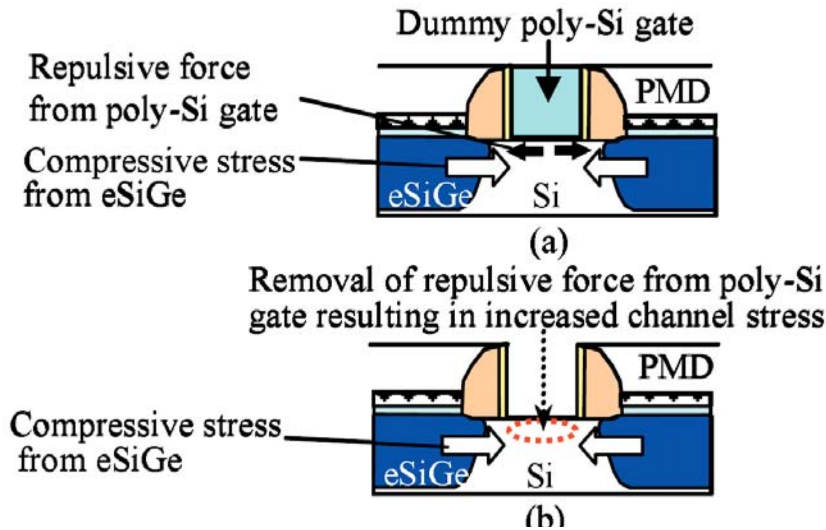




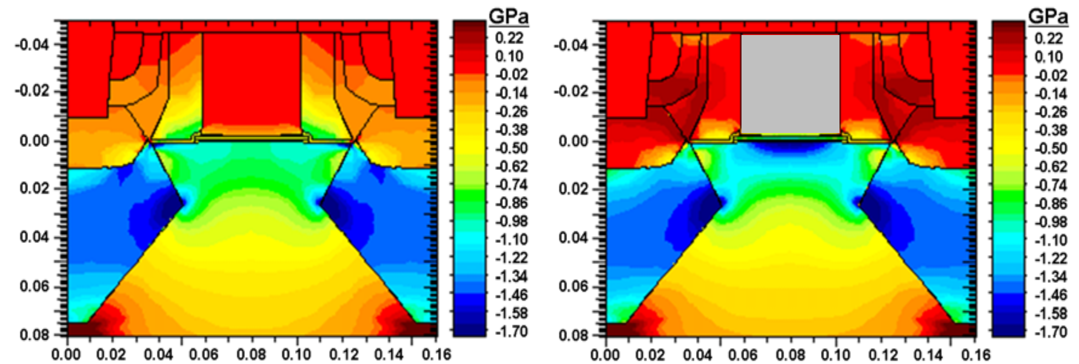
Kang – Sematech
IEDM 2006

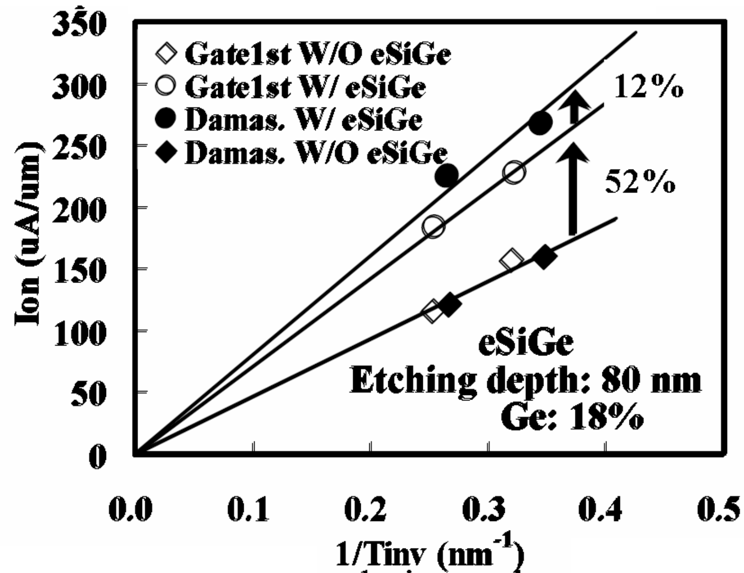
Auth – Intel
VLSI 2008

Enhanced PMOS strain: Gate last HiK-MG

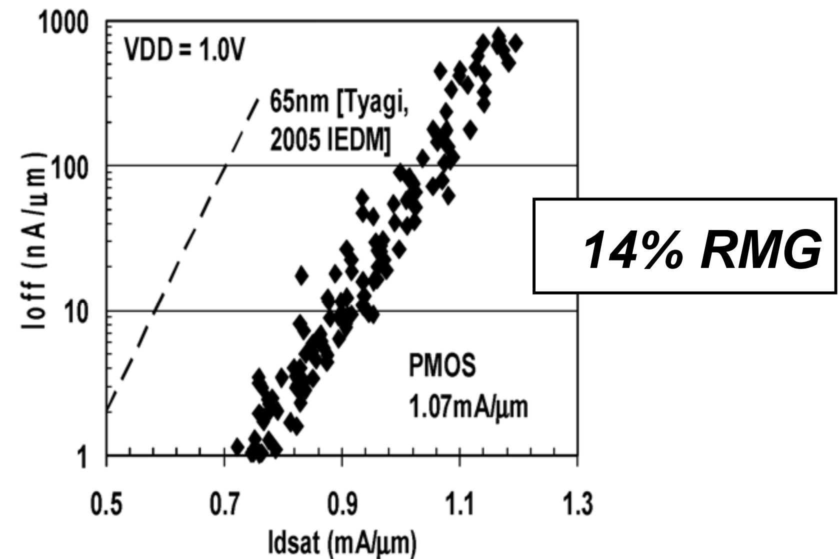


Before gate removal After gate removal





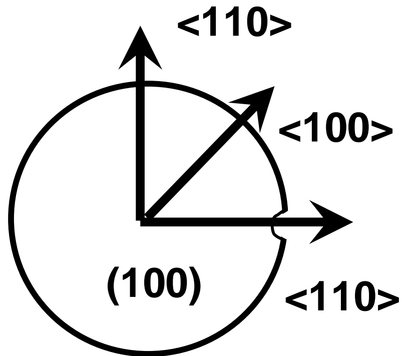
Wang – Sony
VLSI 2007



Auth – Intel
VLSI 2008

ORIENTATION

(100) surface – top down

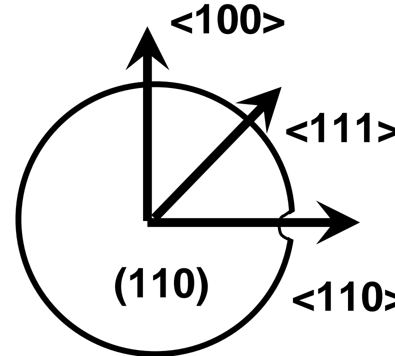


Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a "45 degree" wafer)

Both <110> directions are the same.

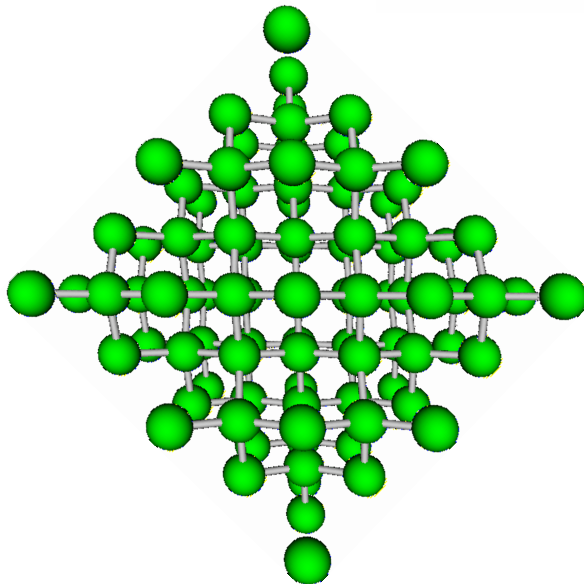
(110) surface – top down

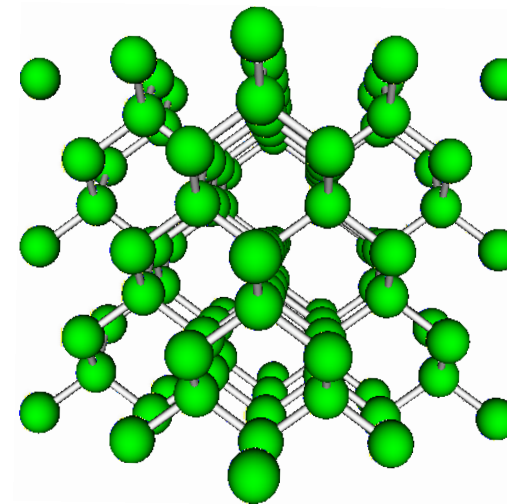


Non-standard

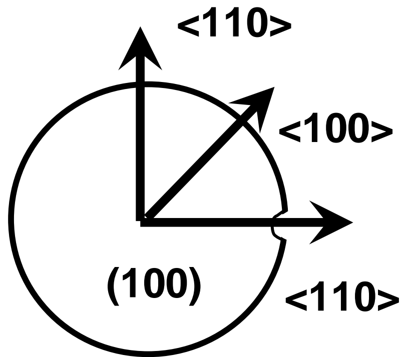
(110) Surface

Three possible channel directions
<110> <111> and <100>





(100) surface – top down

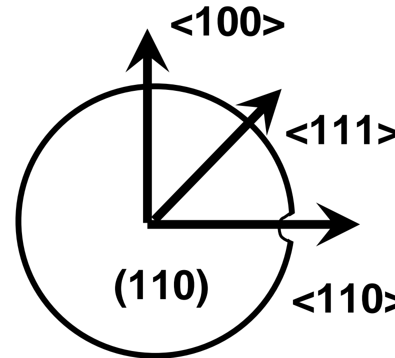


Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a "45 degree" wafer)

Both <110> directions are the same.

(110) surface – top down

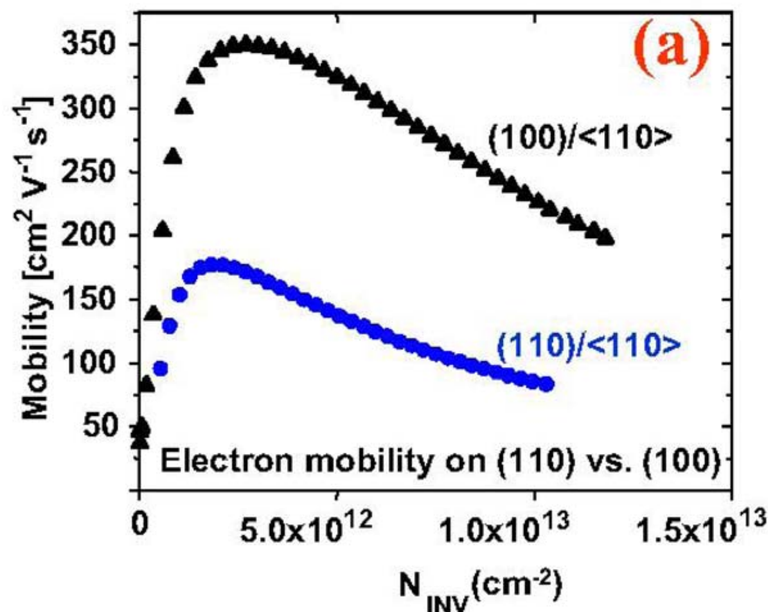


Non-standard

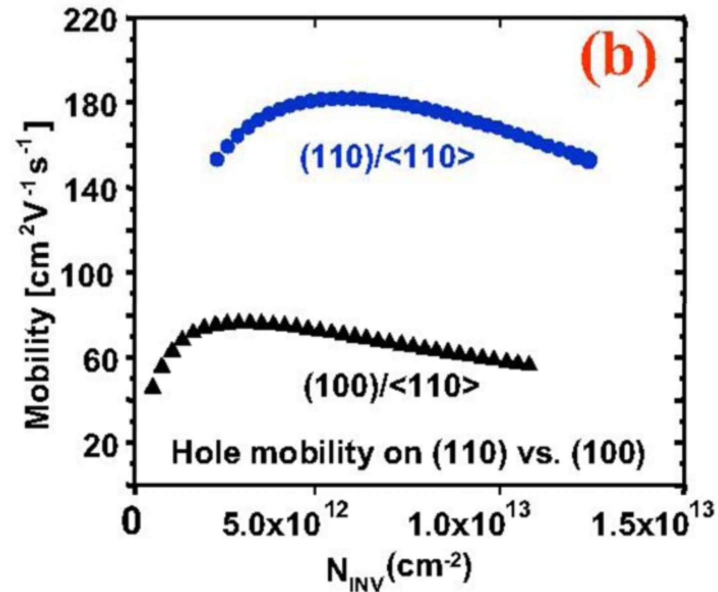
(110) Surface

Three possible channel directions
<110> <111> and <100>

(100) BEST NMOS

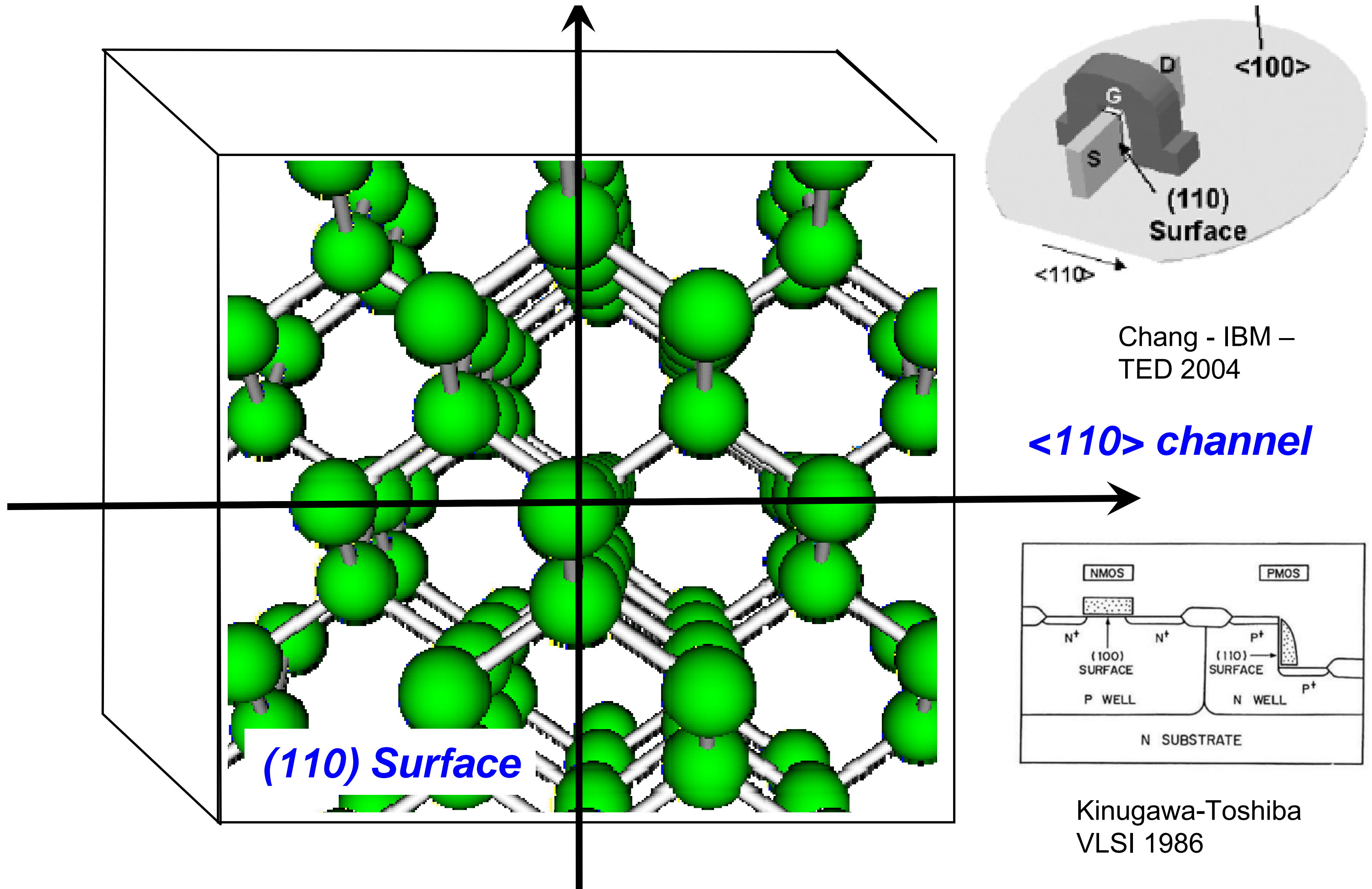


(110) <110> BEST PMOS



Yang
AMD/IBM
EDST 2007

PMOS Vertical Devices on (100)



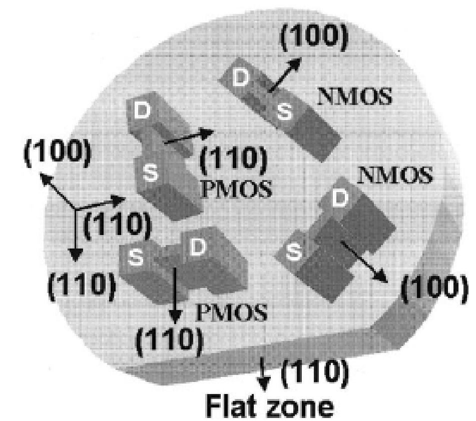
(110) surface <110> channel results when a VFET is fabricated on typical (100) Si - good for PMOS, not for NMOS

NMOS Vertical Devices on (100)

Put NMOS at 45degrees to PMOS?

(100) Surface

<100> channel

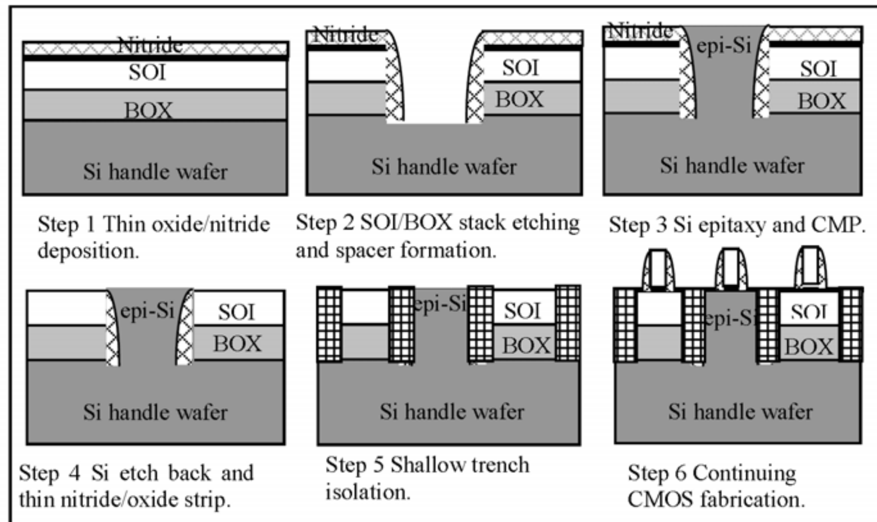


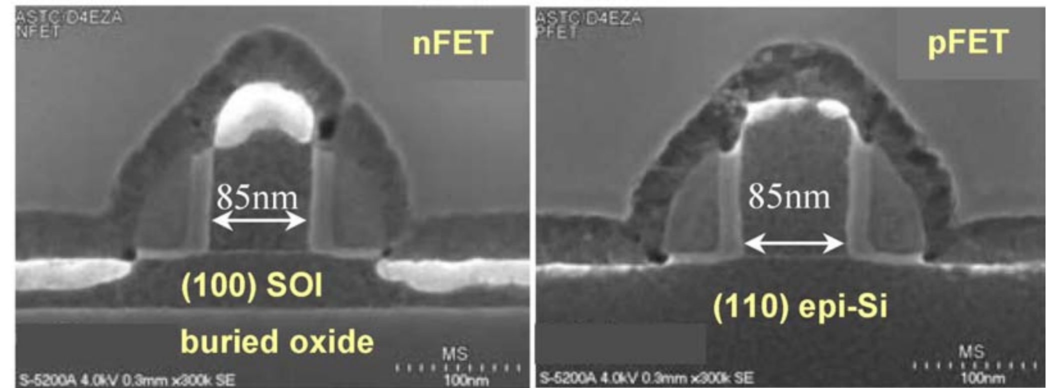
Chang - Berkeley
Proc. IEEE 2003

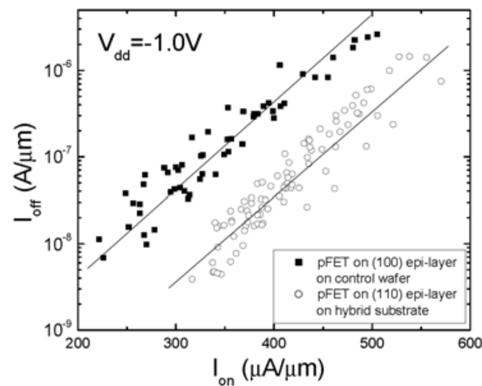
(100) surface <100> channel for a VFET fabricated at 45 degrees typical (100) Si – very challenging for lithography

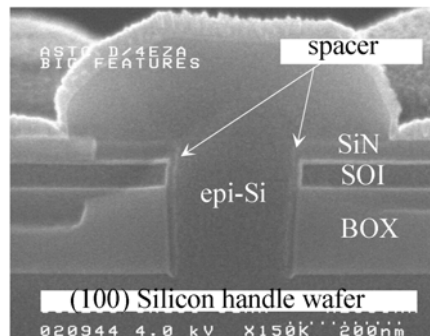
Early HOT

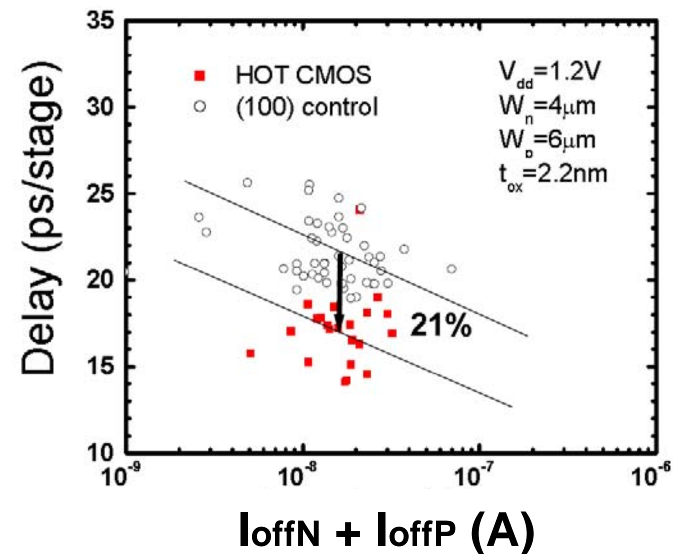
Elegant solution!











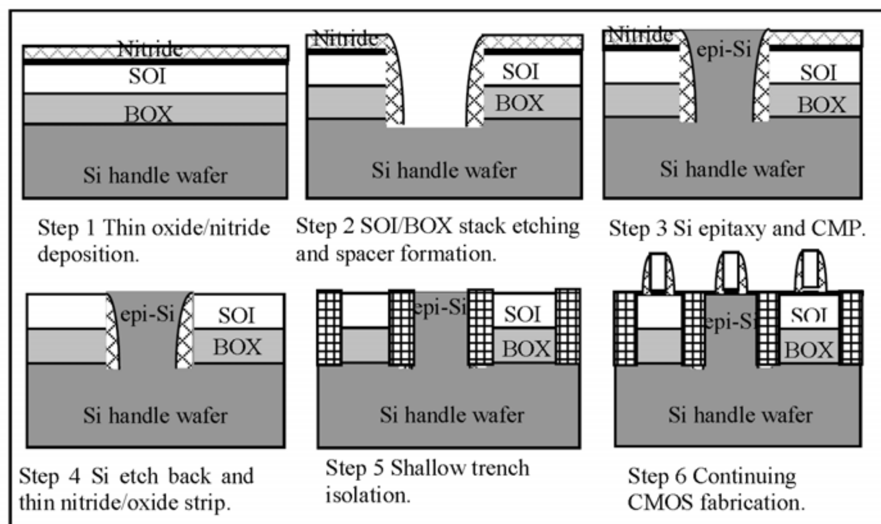
Yang – IBM
IEDM 2003 [28]
First HOT

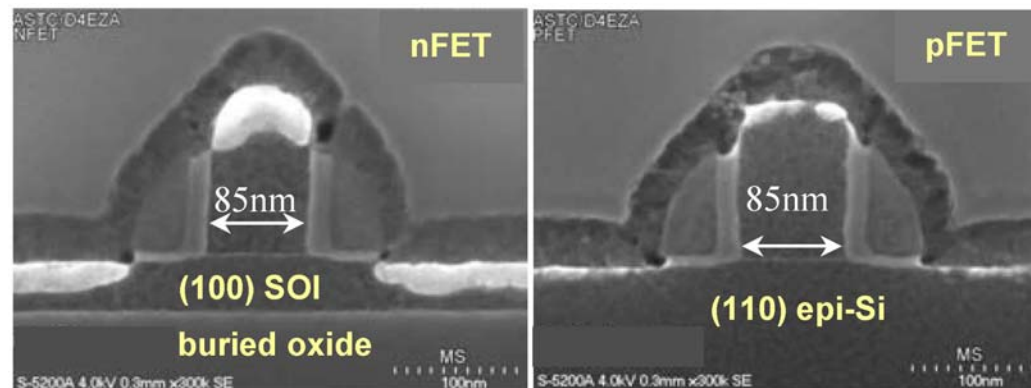
Yang – AMD/IBM
VLSI 2004
HOT RO

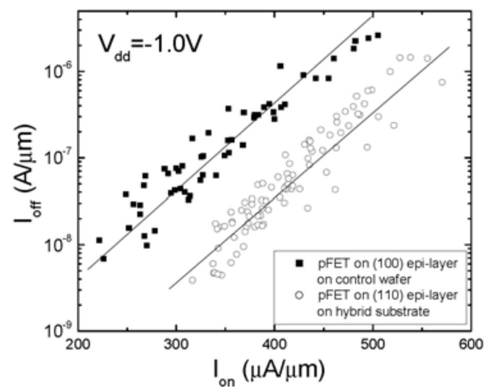
Wafer bonding; SOI of opposite type of handle wafer; both options (N and PMOS SOI explored)

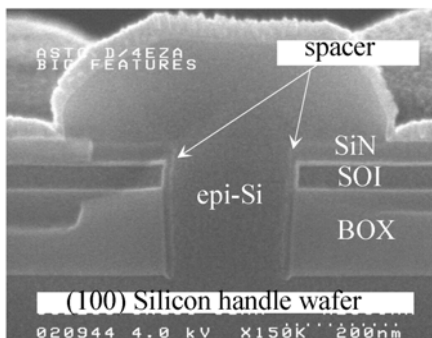
Early HOT

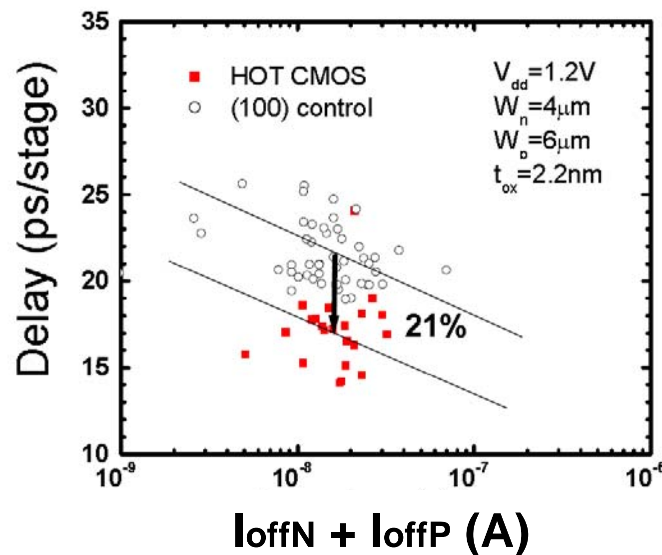
Elegant solution!







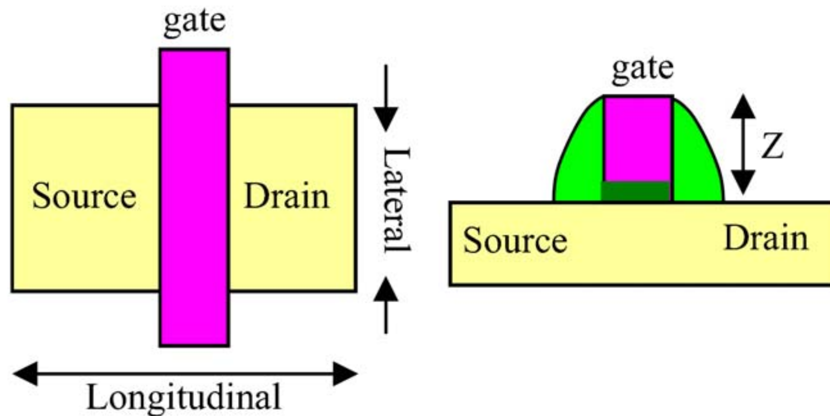




Yang – IBM
IEDM 2003 [28]
First HOT

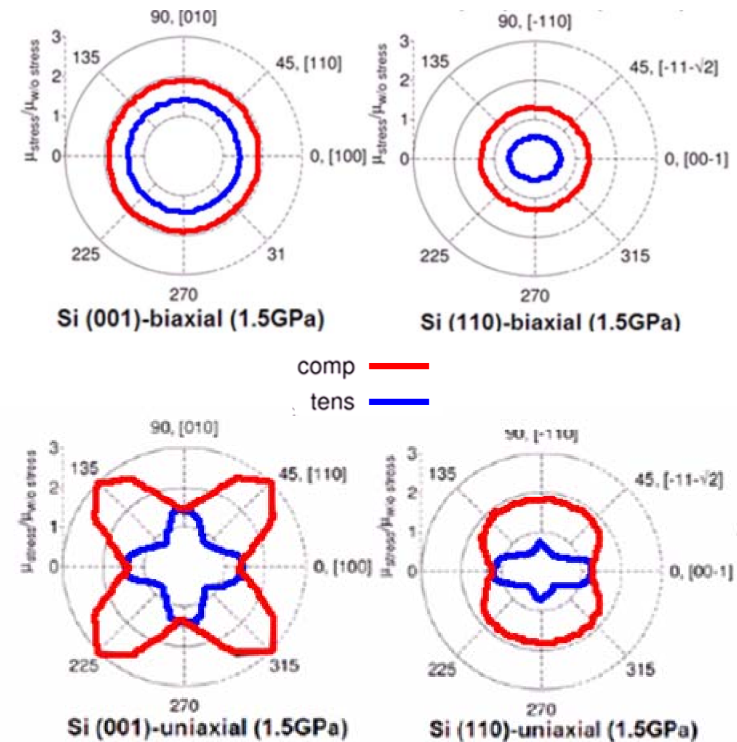
Yang – AMD/IBM
VLSI 2004
HOT RO

Strain AND orientation optimization



		NMOS	PMOS
Longitudinal	X	Tensile	Compressive
Lateral	Y	Tensile	Tensile
Si Depth	Z	Compressive	Tensile

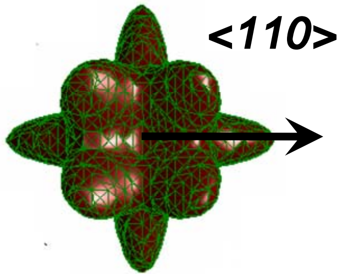
Chan – IBM
CICC 2005



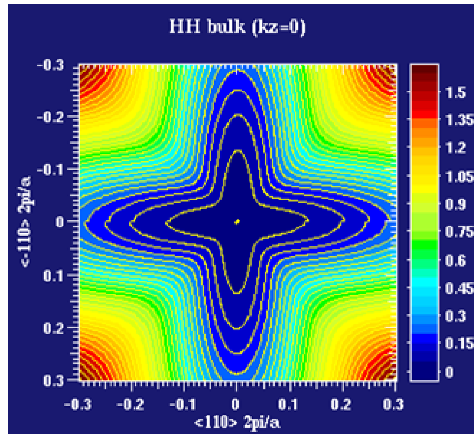
Krishnamohan – Stanford
IEDM 2008

More complex for non-(100) orientations

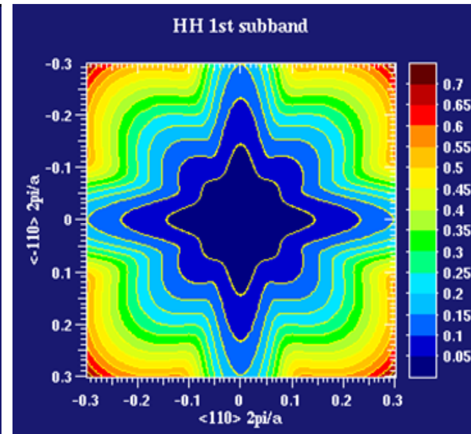
(100)



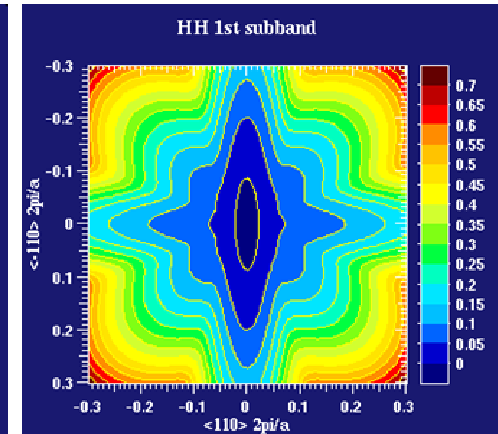
(001) Surface (k⊥=0)



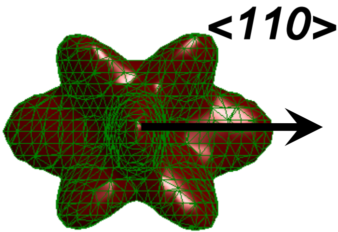
(001) Surface Vg=-1V



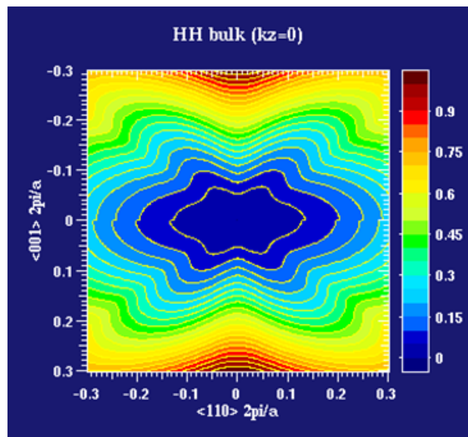
(001) Surface Vg=-1V, Sxx=-1GPa



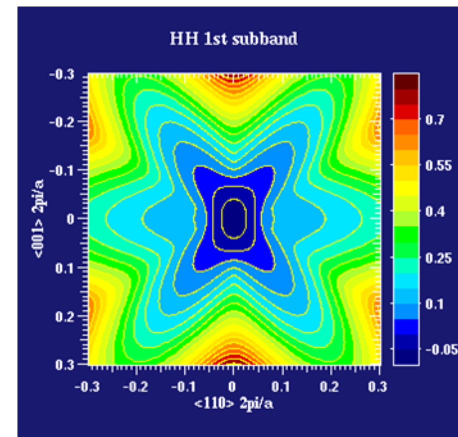
(110)



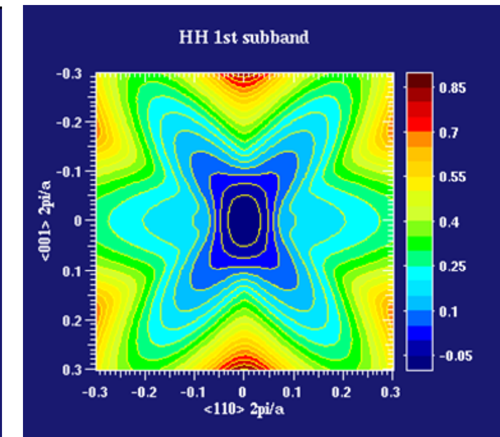
(110) Surface (k⊥=0)



(110) Surface Vg=-1V



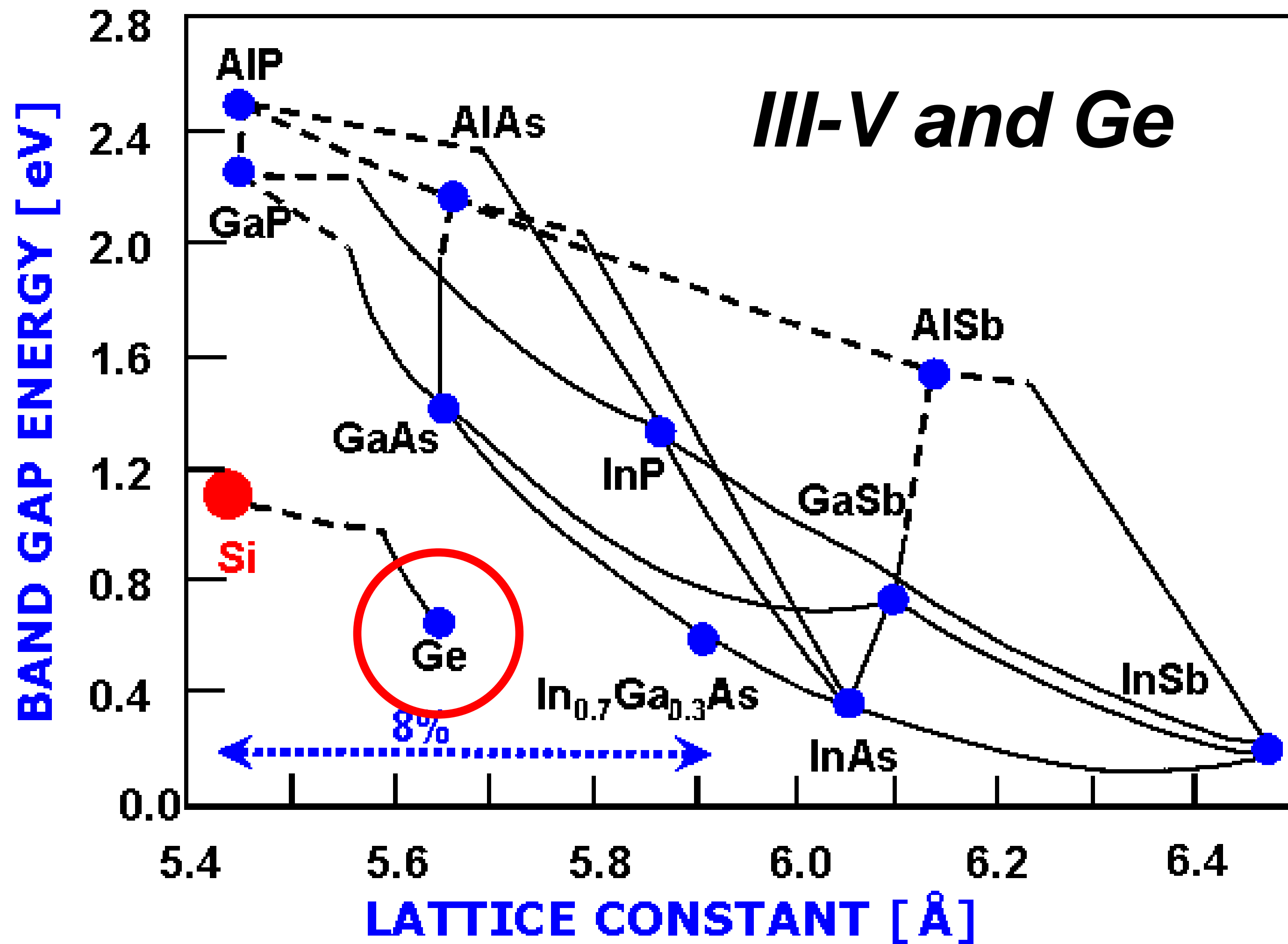
(110) Surface Vg=-1V, Sxx=-1GPa



BULK | **1'D CONFINED** | **1'D CONFINED STRAINED**

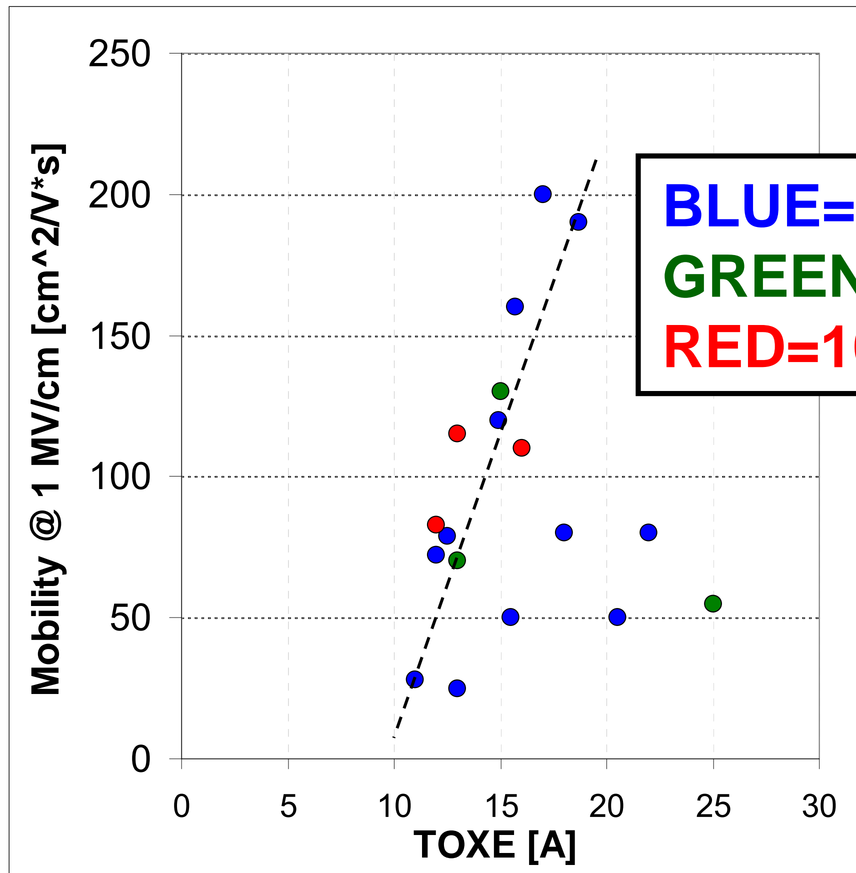
Kuhn/Packan, Intel, IEDM 2008

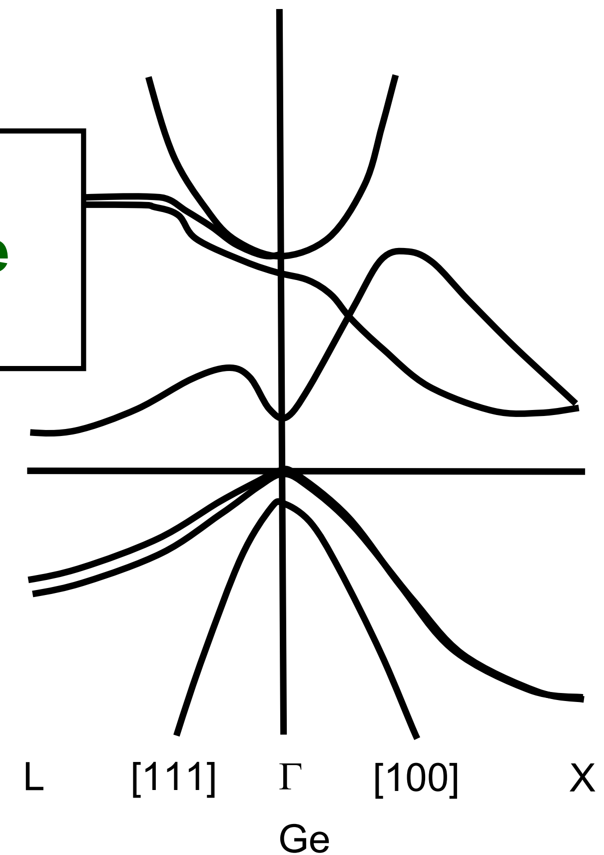
Interesting Alternative Materials



Adapted from Kavalieros – Intel - VLSI SC 2007

Challenges of TOXE scaling in Ge and SiGe



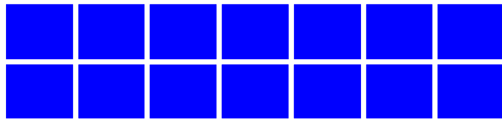


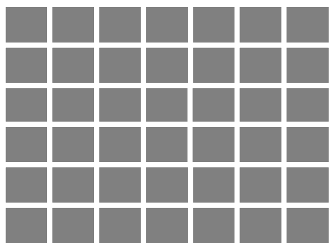
R. Chau, Intel, ESSDERC 2008

At thin electrical oxide thickness (TOXE), all industry/university data show degraded mobility

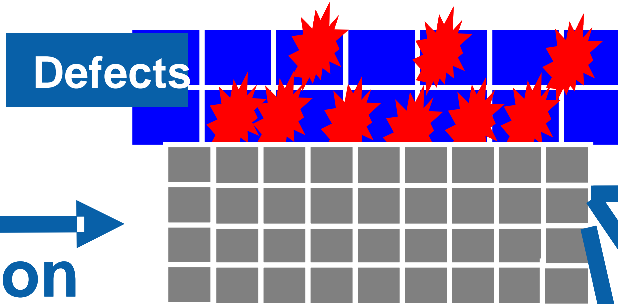
New oxide invention required to enable a Ge/SiGe channel for future technology nodes

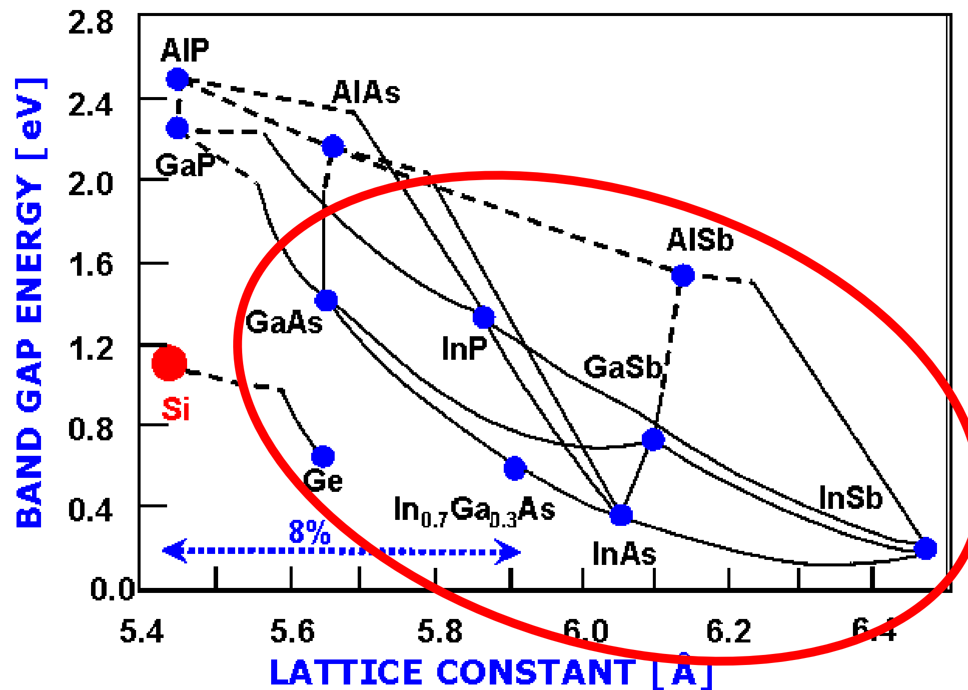
Challenge of Lattice Mismatch Issues

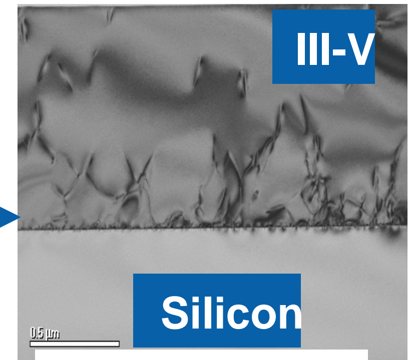




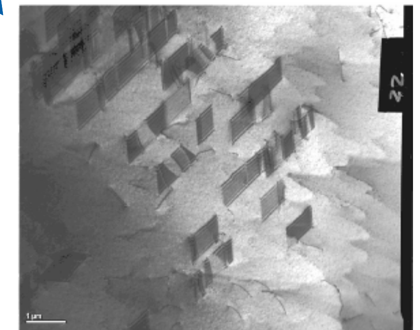
Direct Deposition



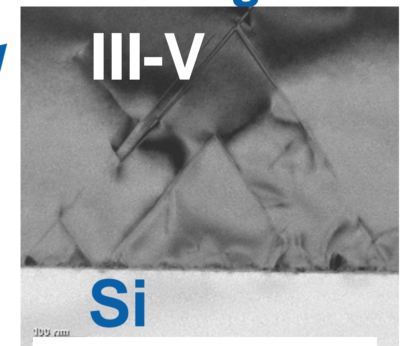




Dislocations



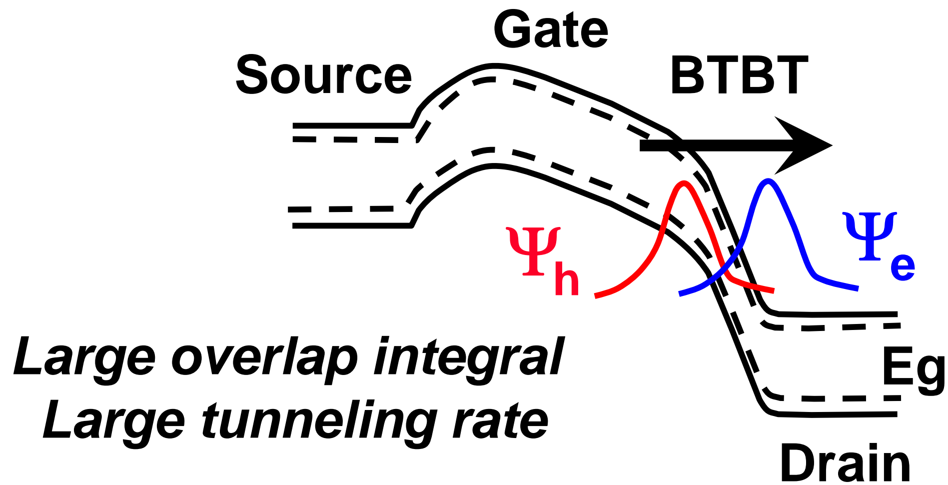
Stacking faults



Twin Defects

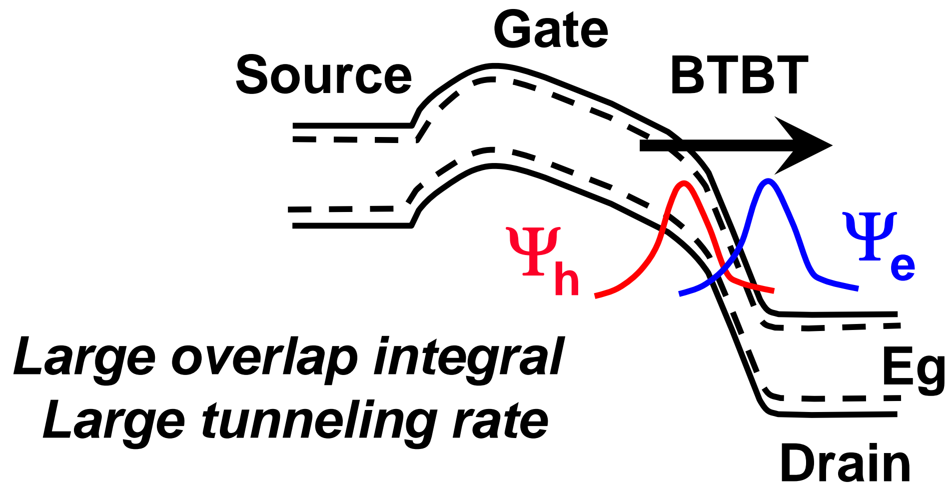
Adapted from Kavalieros – Intel - VLSI SC 2007

Challenges of Alternative N-Channel Materials

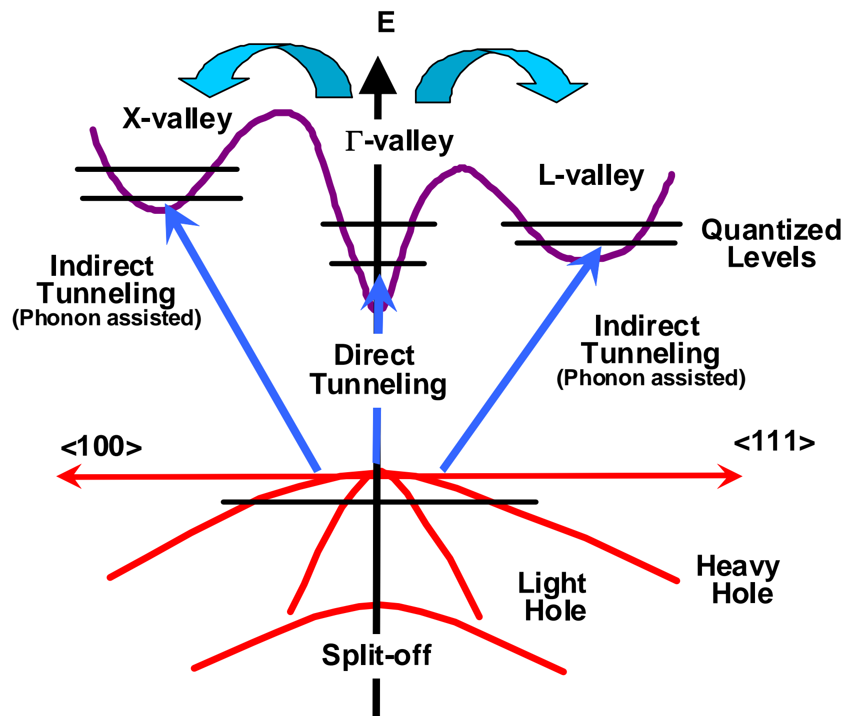


- Low Eg III-V materials (InAs, InSb, Ge) are subject to Ioff increases due to band-to-band tunneling (and the effect worsens with strain).

Challenges of Alternative N-Channel Materials



Large overlap integral
Large tunneling rate



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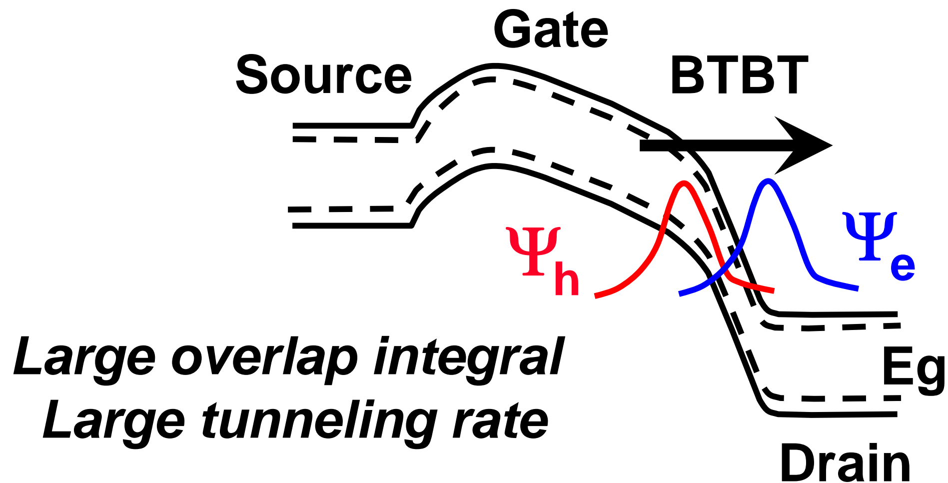
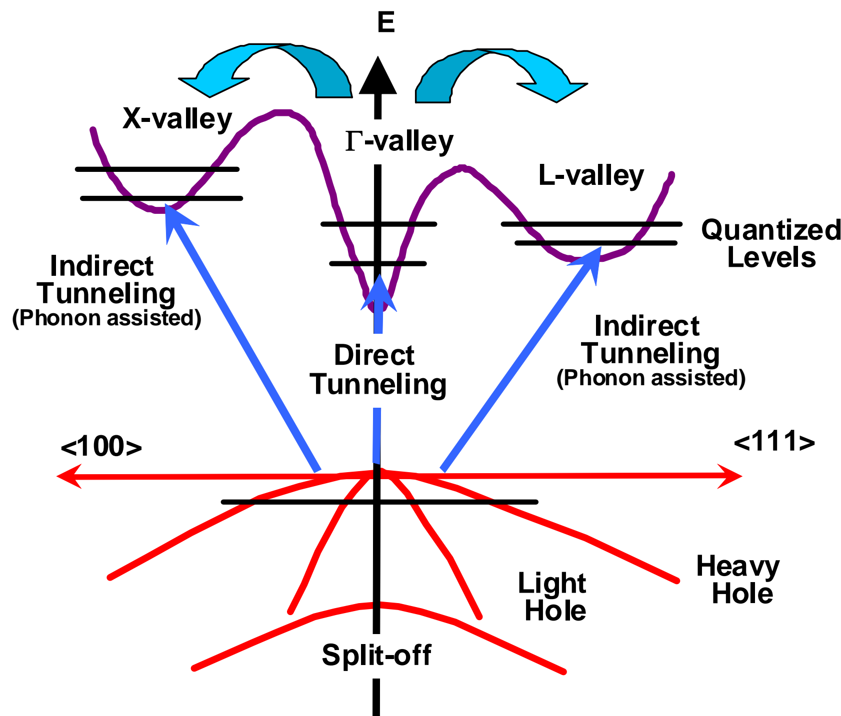
- Very high mobility materials (ex: InAs, InSb) have low density of states in the Γ-valley, resulting in reduced Ion.

Saraswat – Stanford – IEDM 2006

Challenges of Alternative N-Channel Materials





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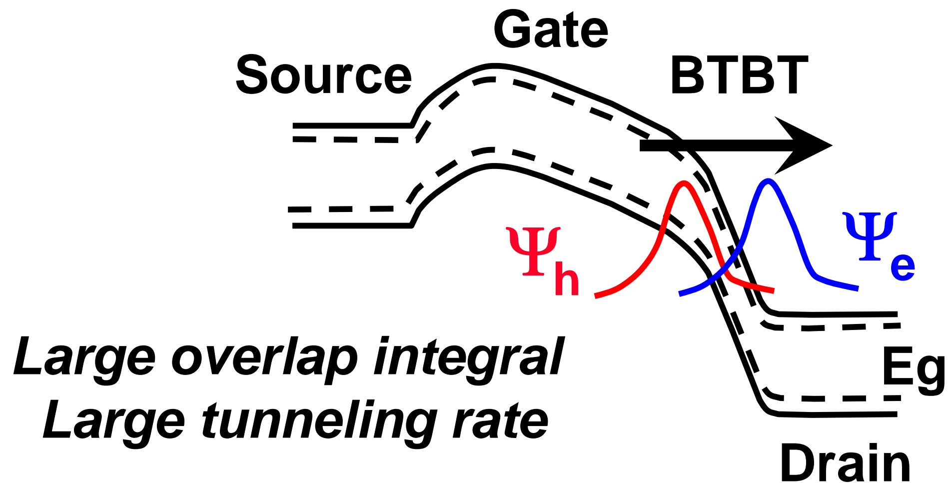
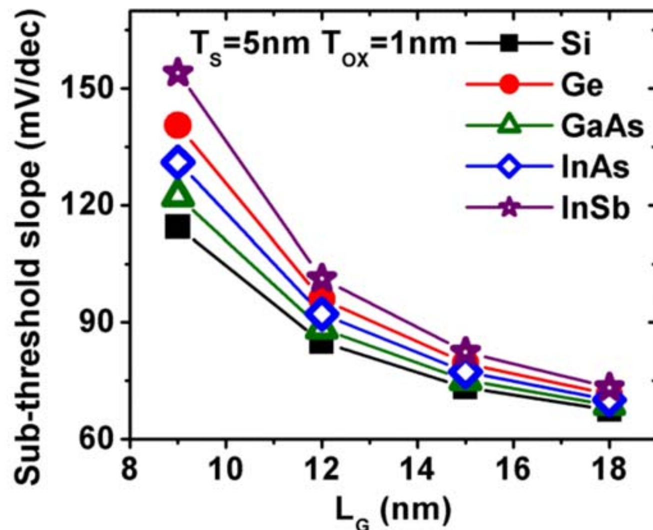
Saraswat – Stanford – IEDM 2006

Challenges of Alternative N-Channel Materials





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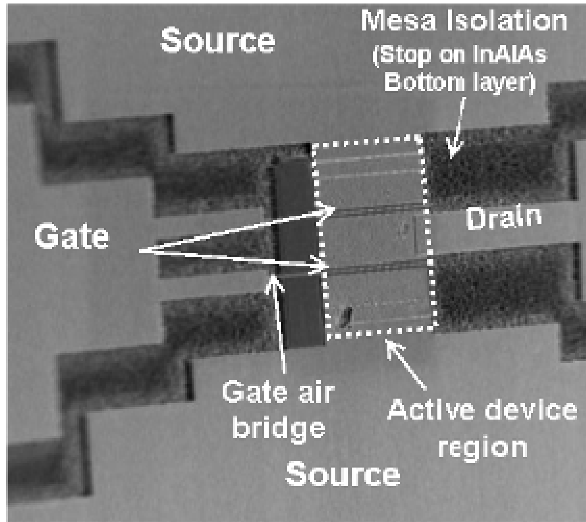
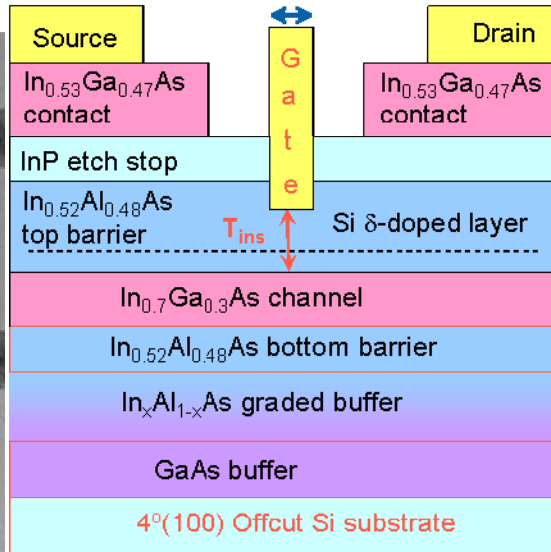
- At high fields, the quantized energy levels in the Γ-valley rise faster than in the L and X valleys, and thus the current is largely carried in the lower mobility L and X-valleys.
- Higher k materials (InAs, InSb) have increased subthreshold slope.

Saraswat – Stanford – IEDM 2006

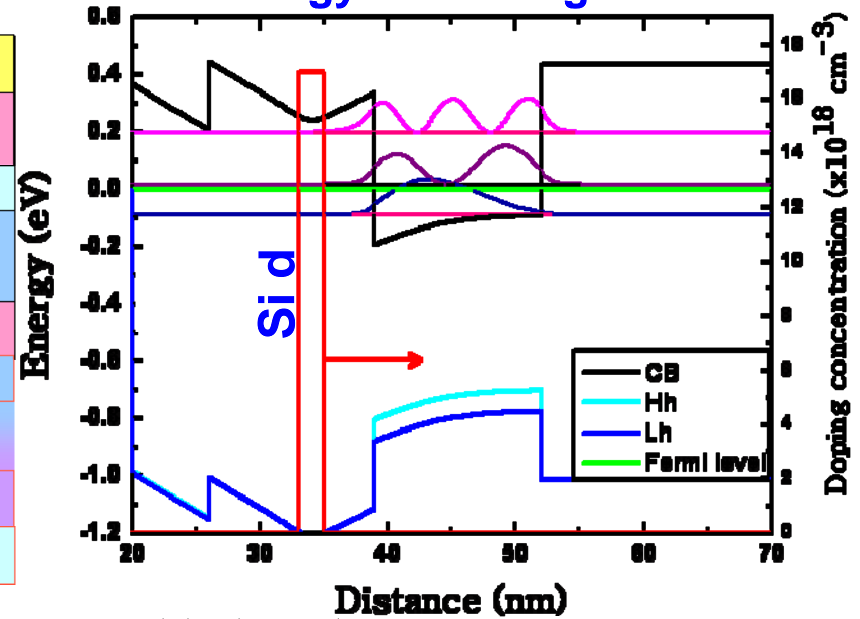
III-V Materials as Transistor Channels

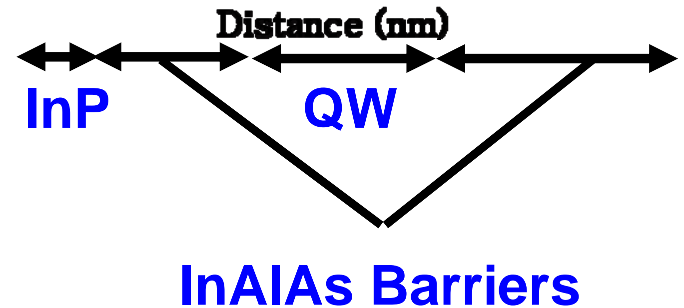
SEM Micrograph

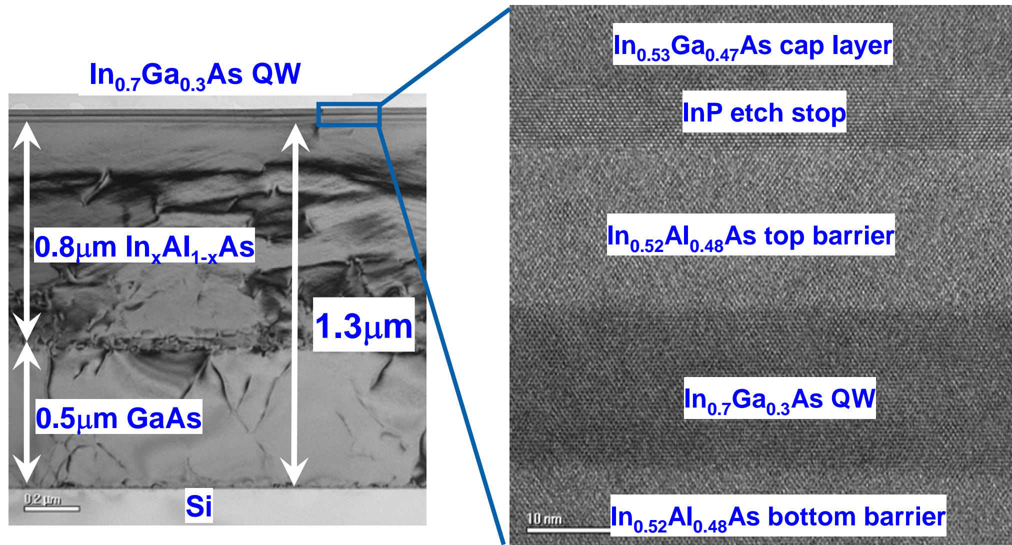




Energy Band Diagram



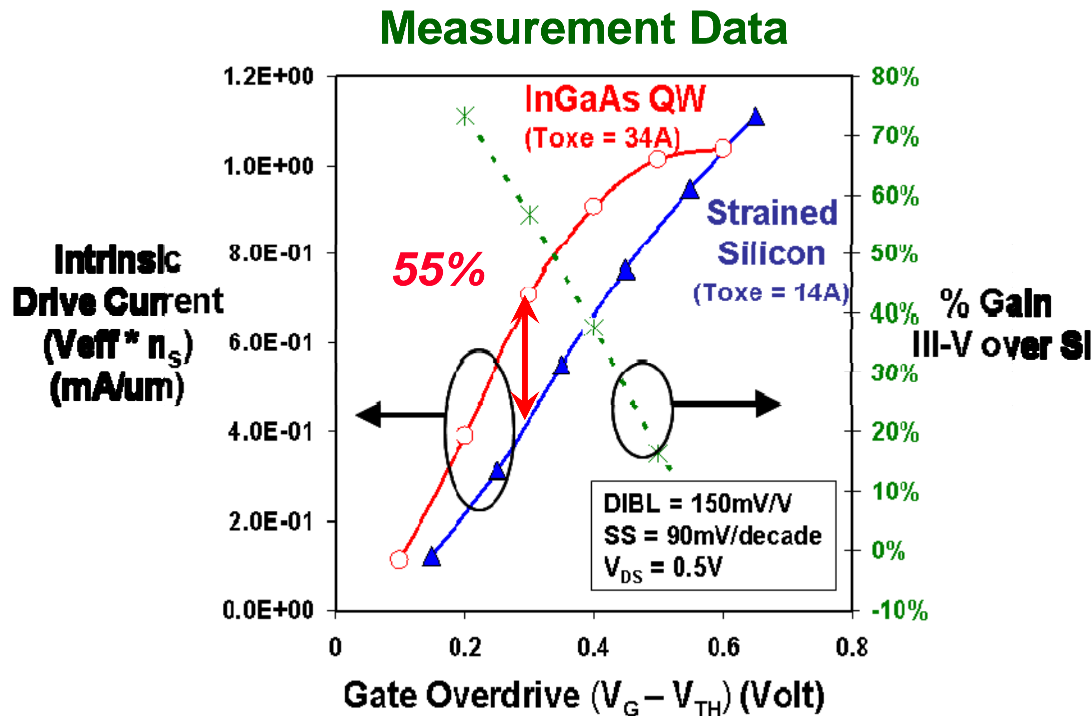


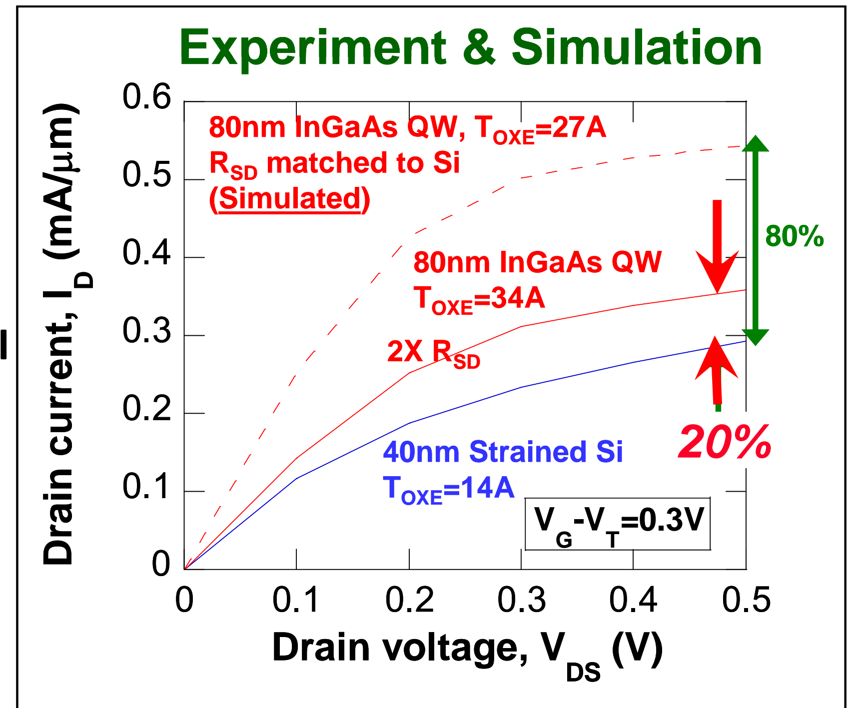


$In_{0.7}Ga_{0.3}As$ QW stack is virtually defect-free

R. Chau, ESSDERC 2008
J. Kavalieros, VLSI SC, 2008

Success of III-V Materials as Transistor Channel (Vcc = 0.5V)





R. Chau, ESSDERC 2008

At a gate overdrive = 0.3V, III-V QWFET shows 55% intrinsic drive current gain over strained Si

At a drain voltage of 0.5V, III-V QWFET shows >20% I_{DSAT} gain over strained Si (despite thicker Toxe and higher R_{SD})

AGENDA

- Scaling history
- Gate control
  - High-k metal-gate
  - Structural enhancements
- Resistance
- Capacitance
- Mobility
  - Strain
  - Orientation
  - Advanced channel materials
- **Summary**

Looking Forward Past 32nm

Low risk
Further enhancements in strain technology Further enhancements in HiK-MG technology
Medium Risk
Optimized substrate and channel orientation Reduction in MOS parasitic resistance Reduction in MOS parasitic capacitance
High risk
UTB devices MuGFETS Advanced materials (Ge, III-V) Nanowires

Questions???