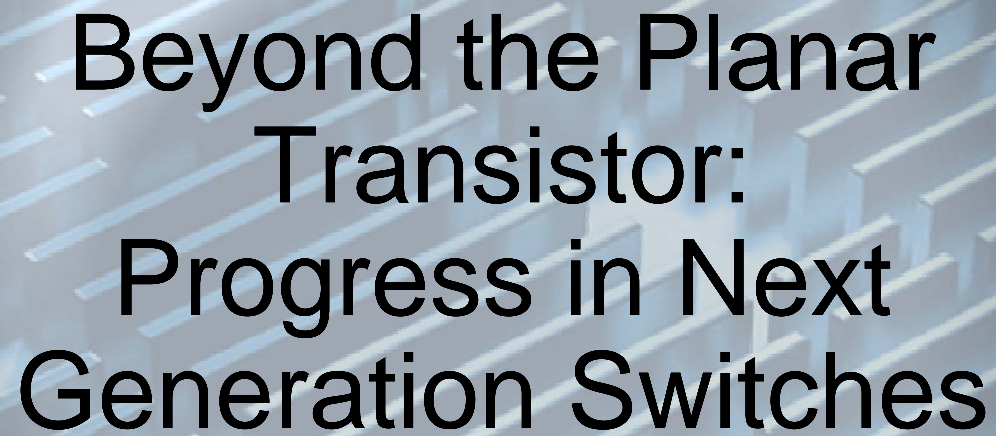
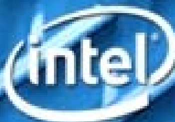


Beyond the Planar Transistor: Progress in Next Generation Switches

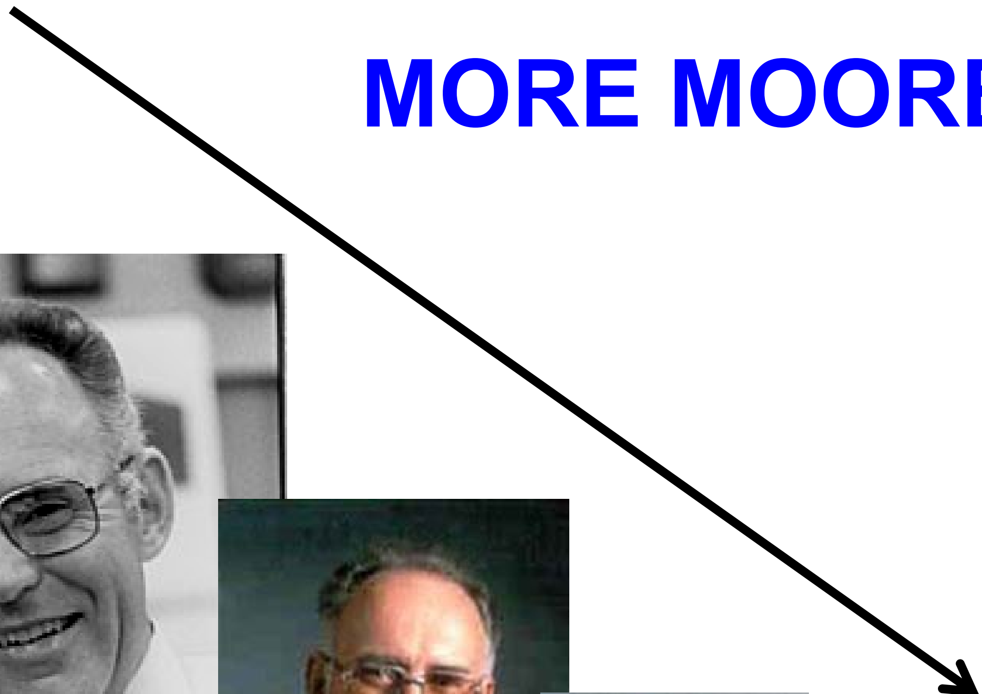
Kelin J. Kuhn
Intel Fellow
Director of Advanced
Device Technology

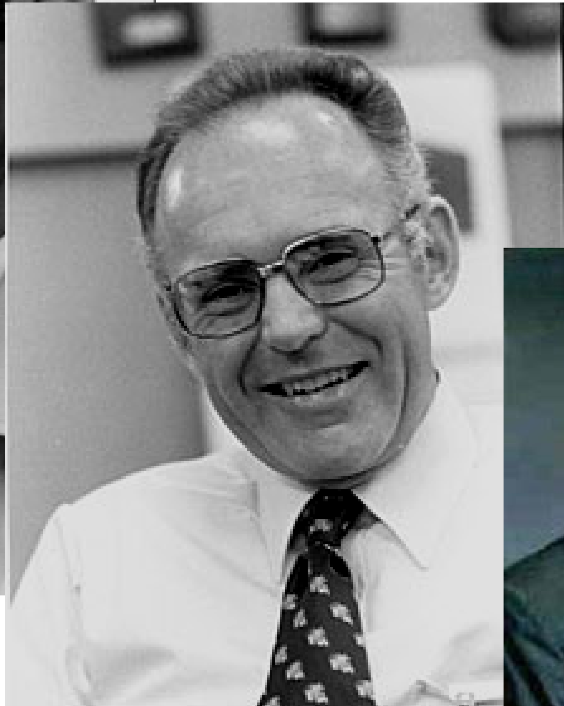


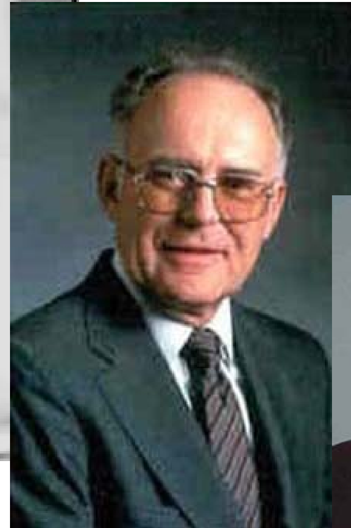
MORE MOORE

MORE THAN MOORE

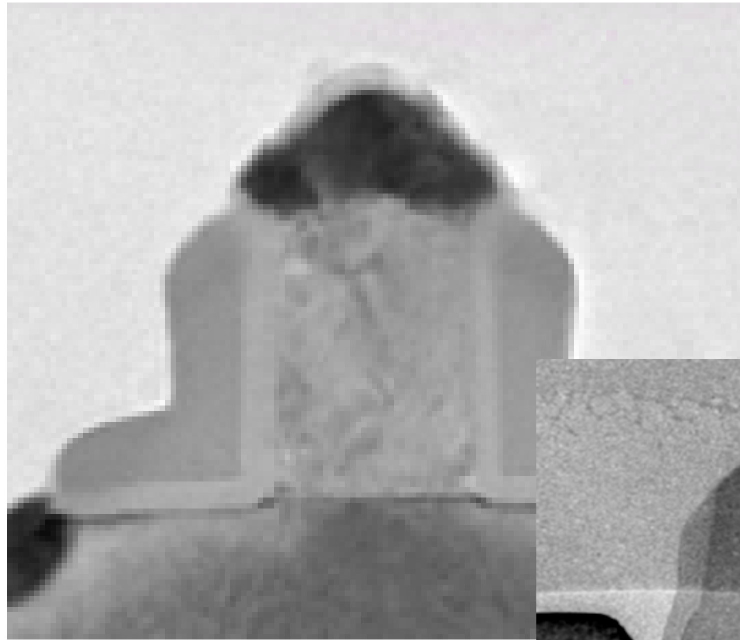
MORE MOORE

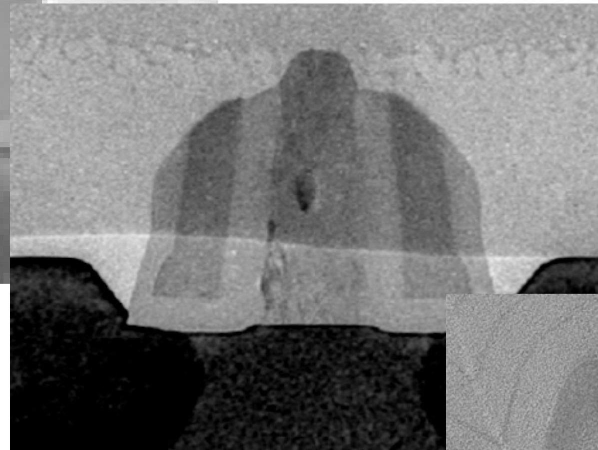


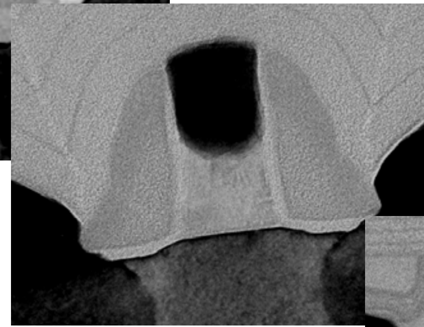


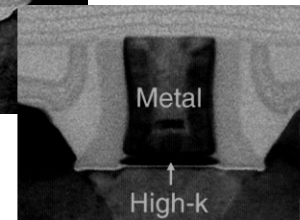


MORE MOORE

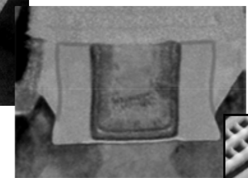

130nm

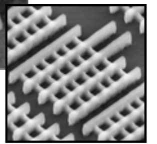

90nm


65nm

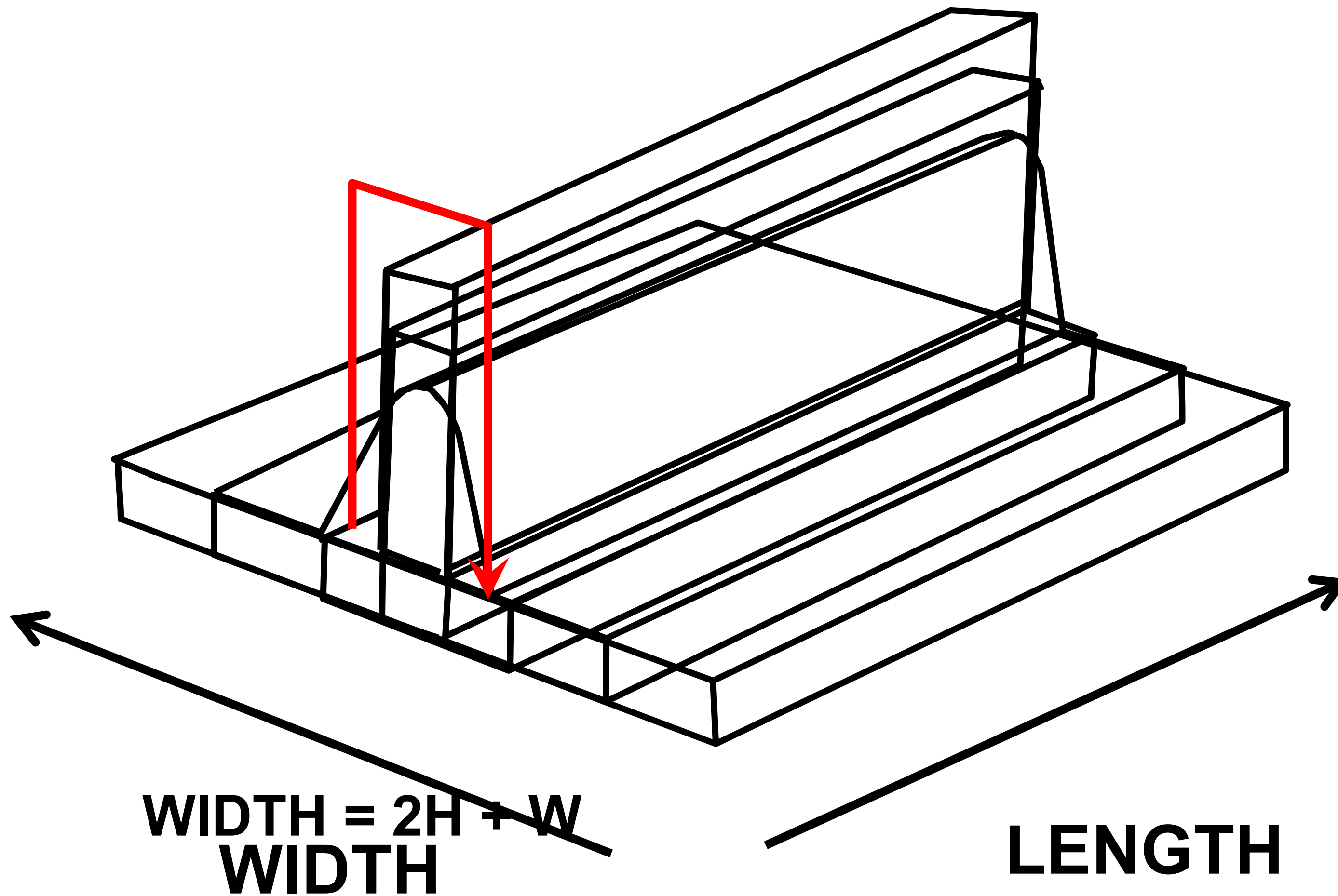


45nm

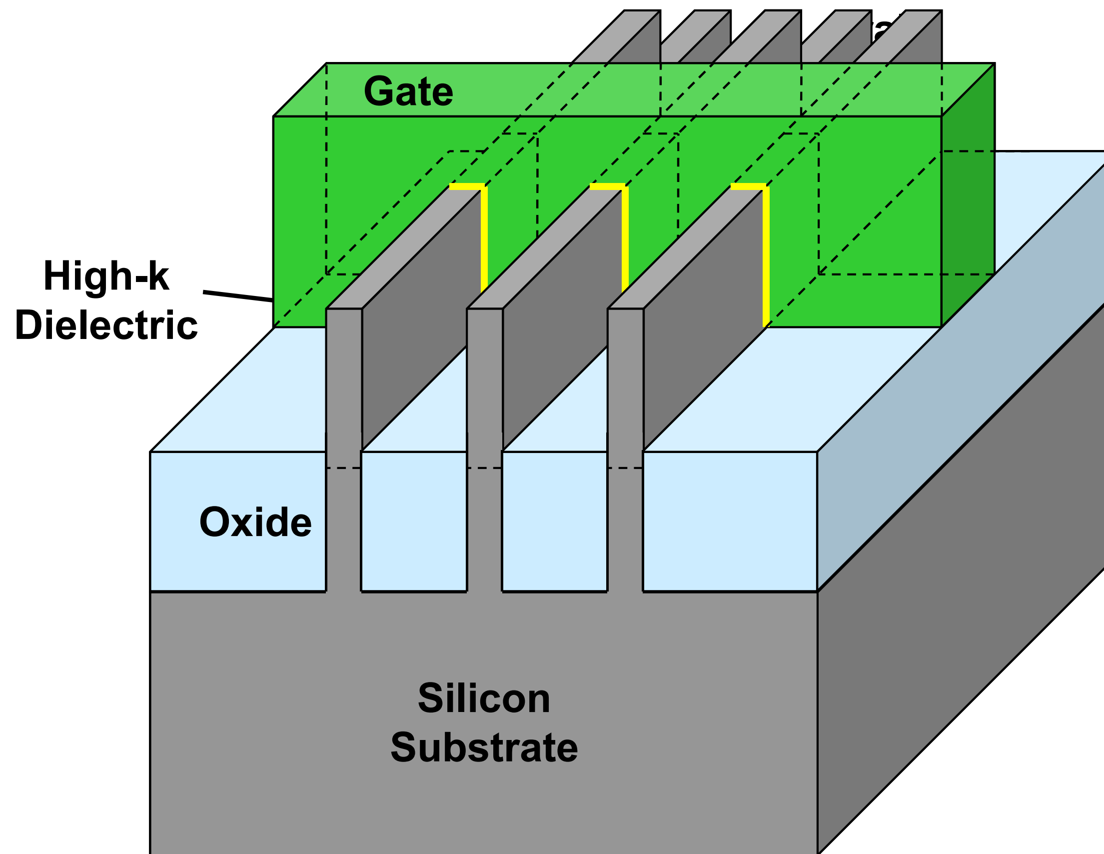

32nm


22nm

TriGate

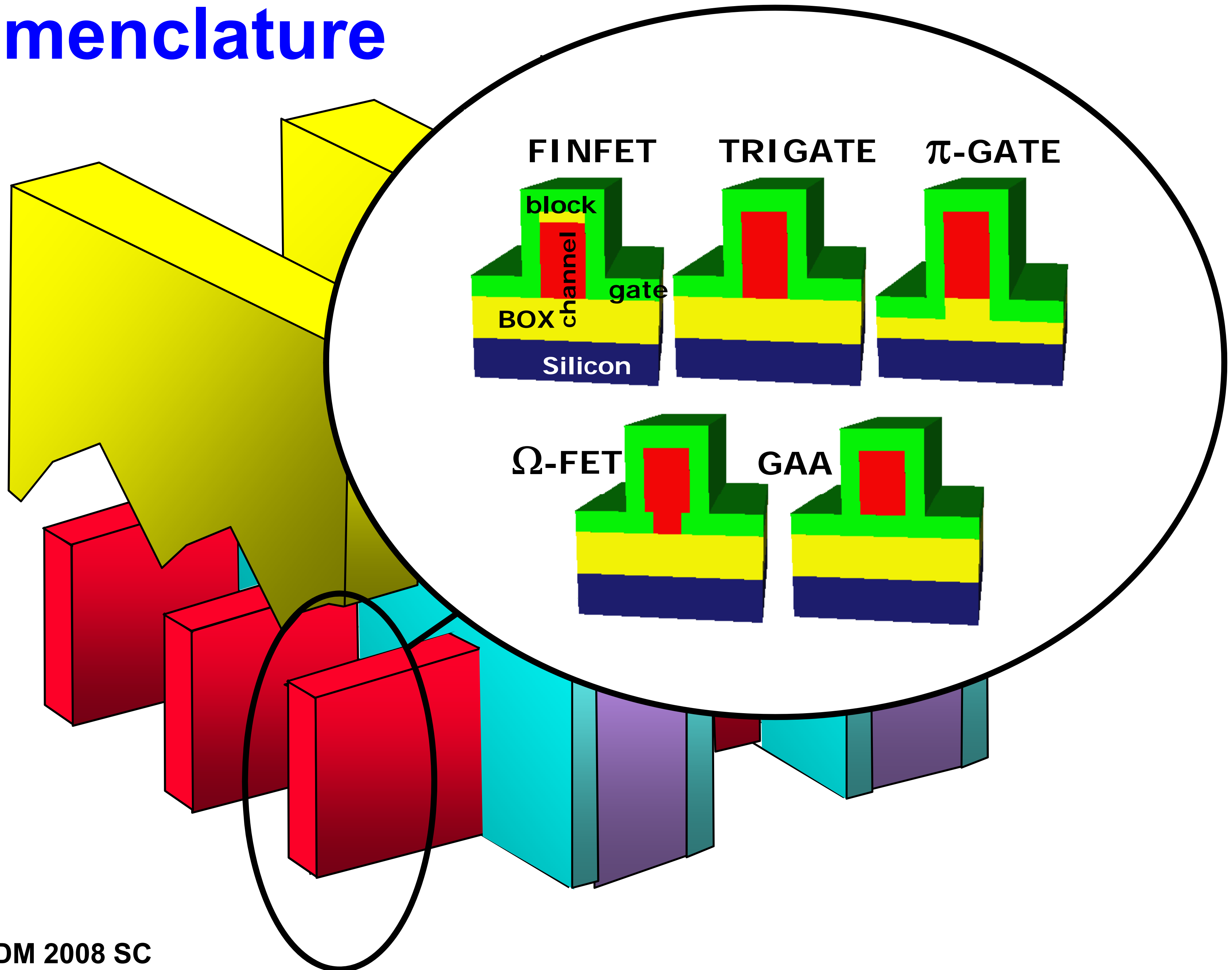


TriGate



Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

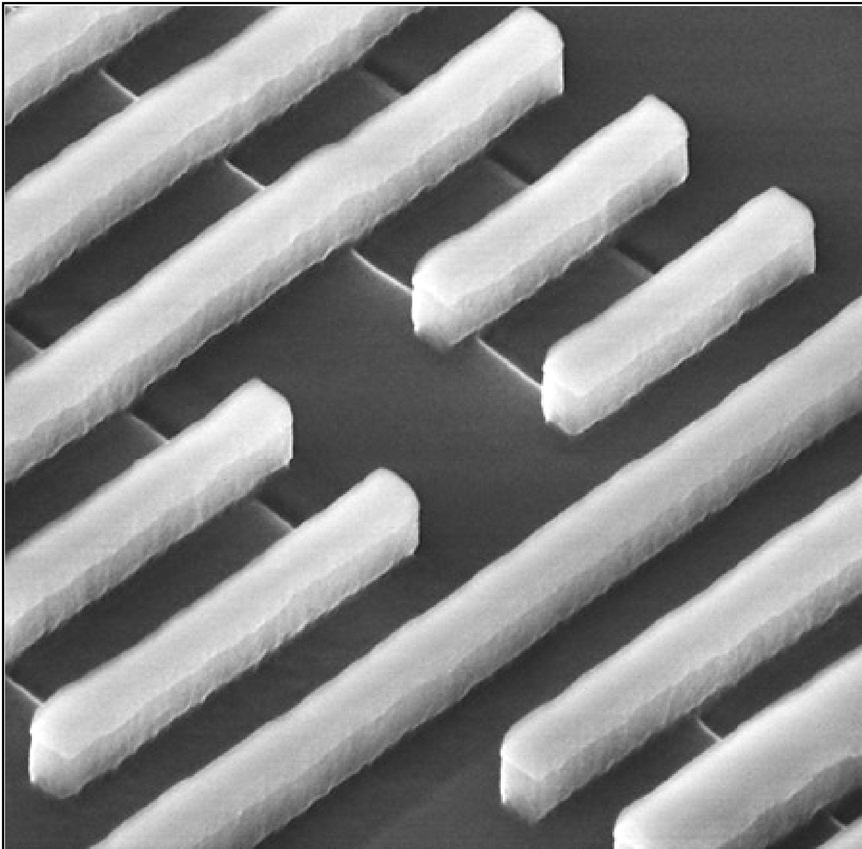
Nomenclature



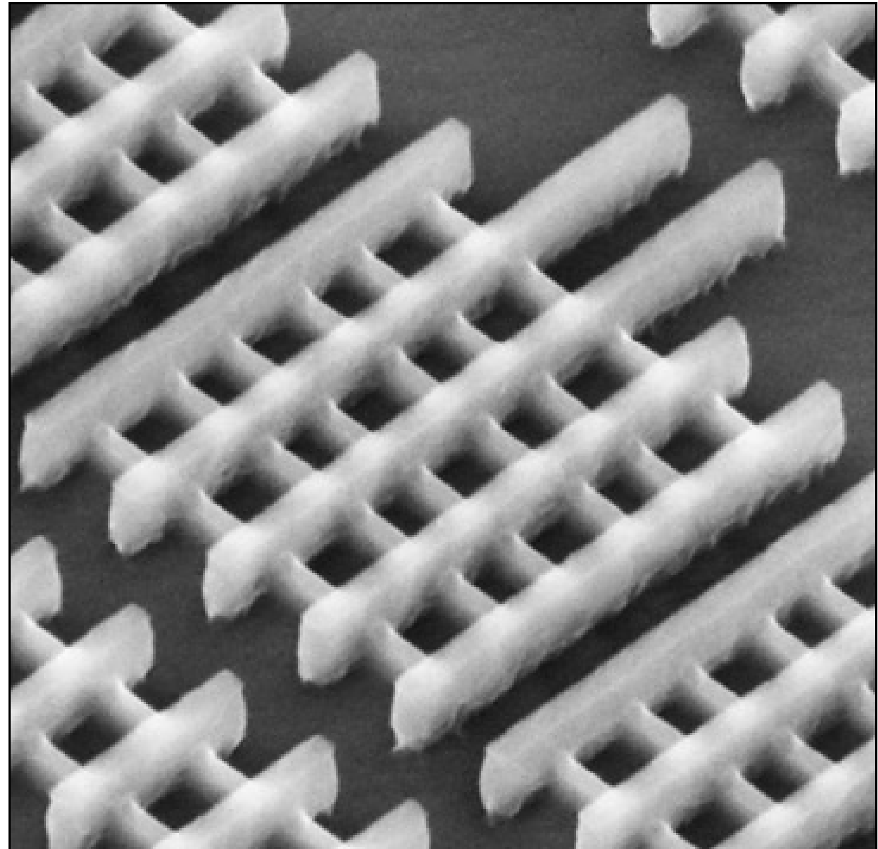
Kuhn IEDM 2008 SC

April 25th 2011: Intel announces 22nm production TriGate process

32 nm Planar Transistors

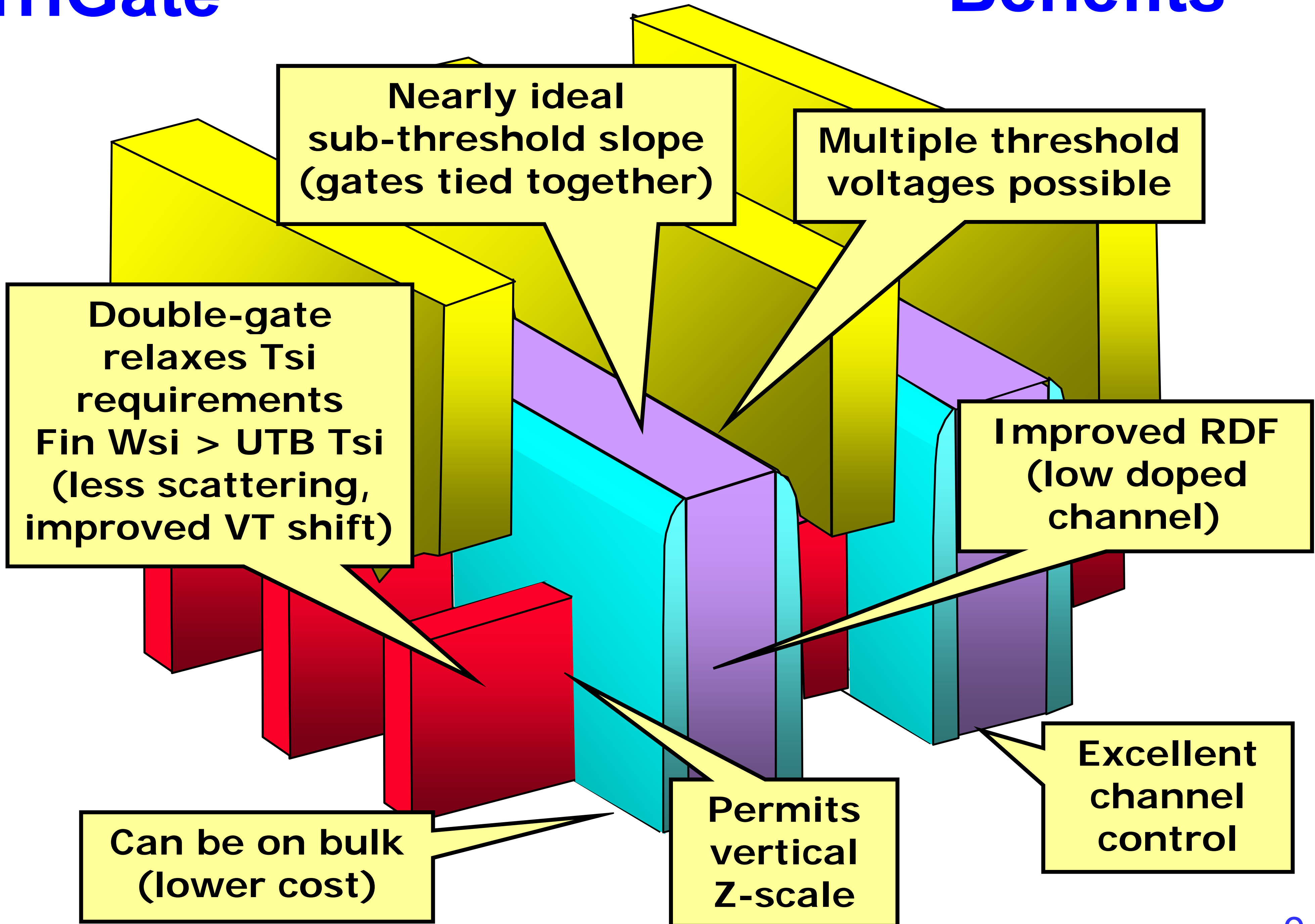


22 nm Tri-Gate Transistors

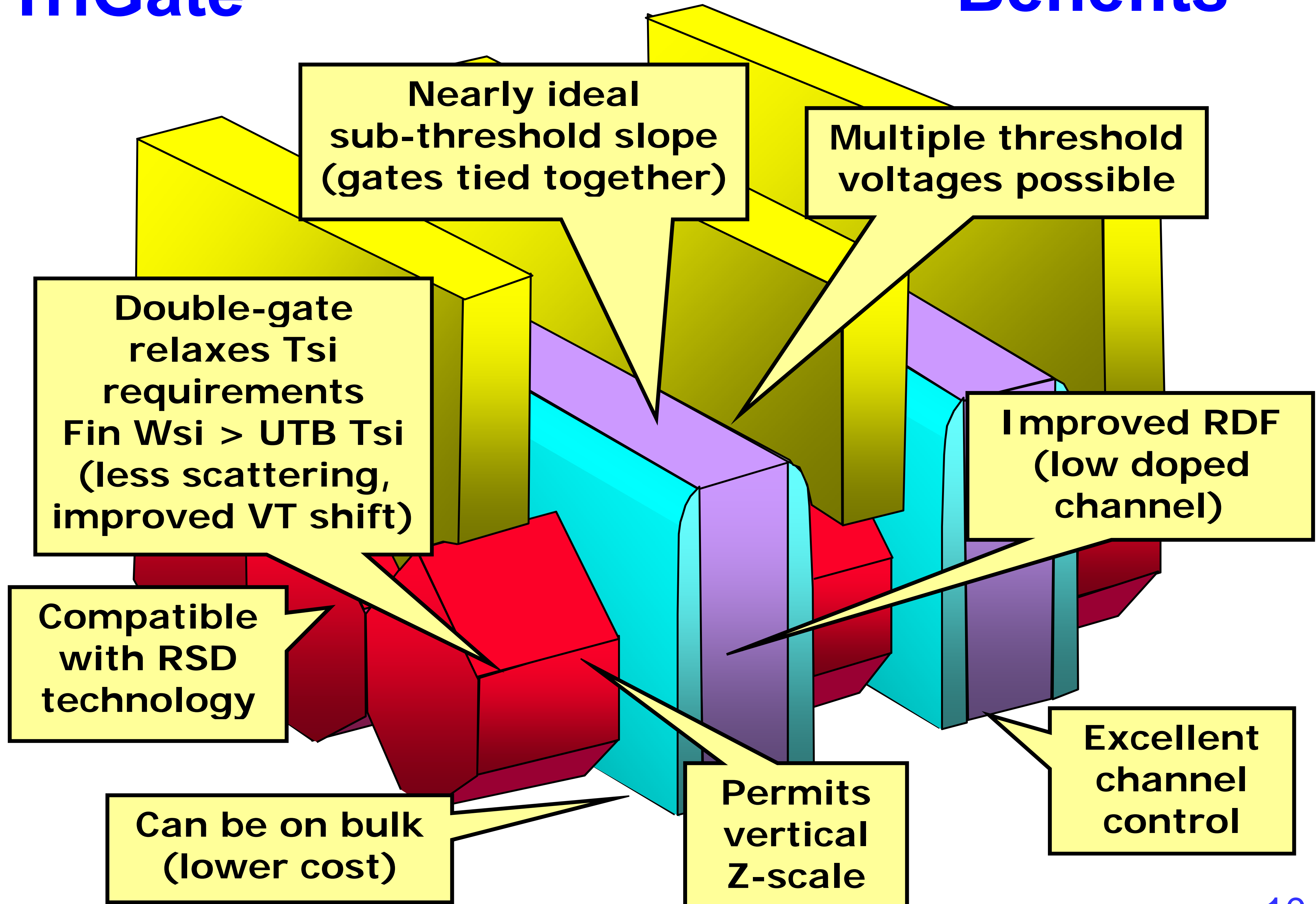


Mark Bohr, Kaizad Mistry: Intel, April 25th, press release

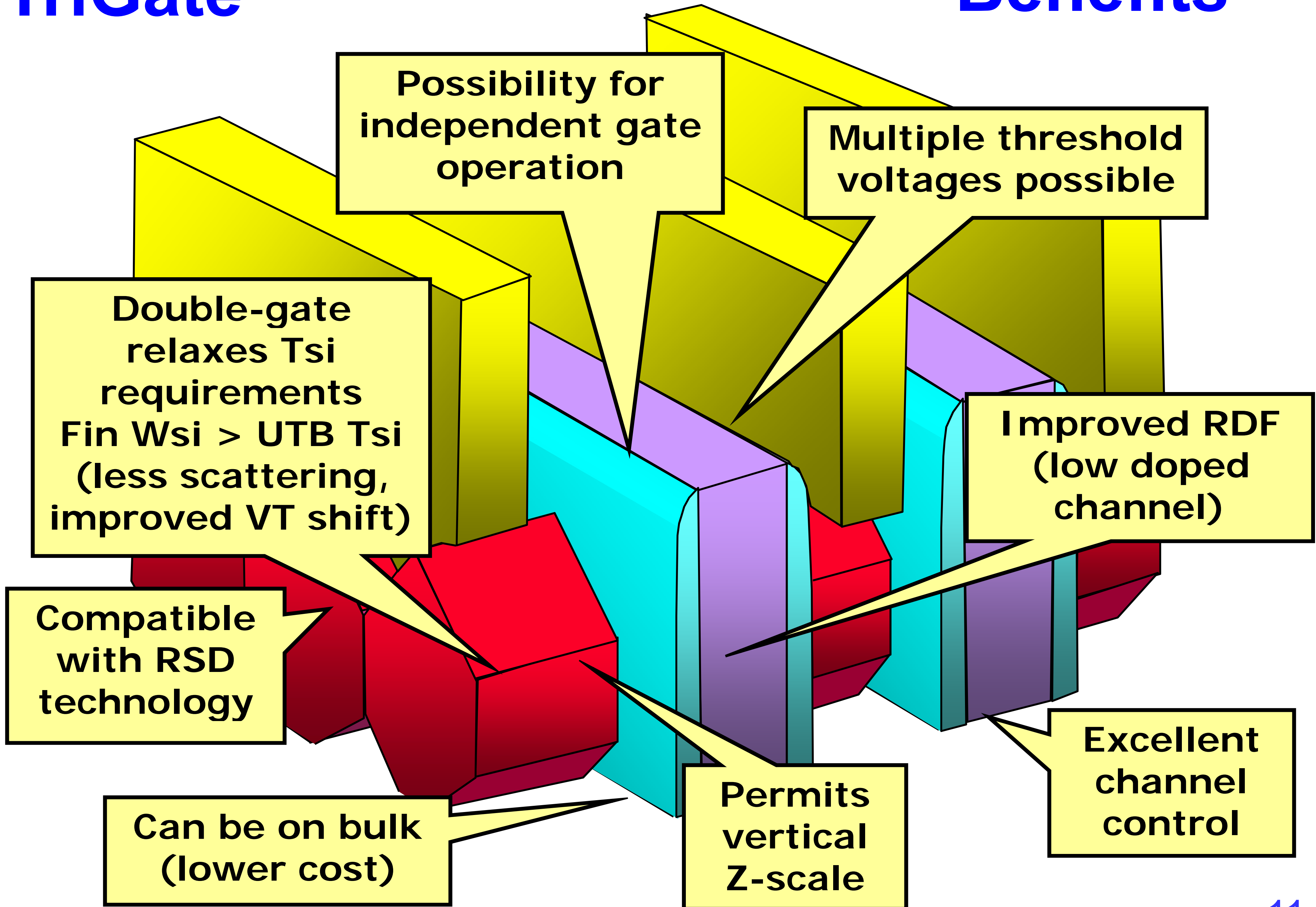
TriGate Benefits



TriGate Benefits

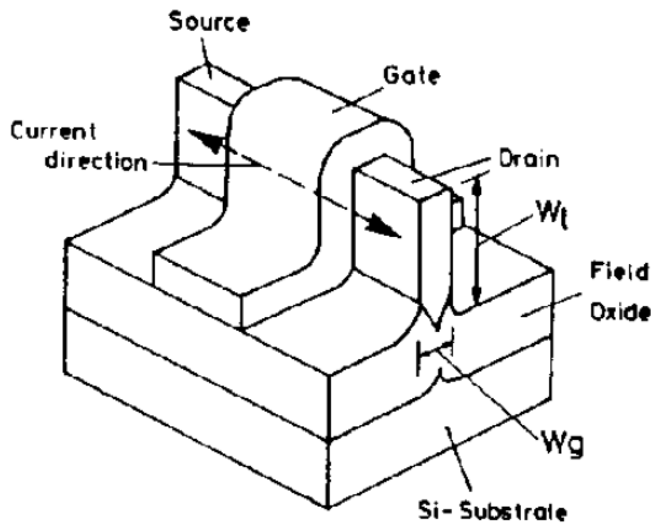


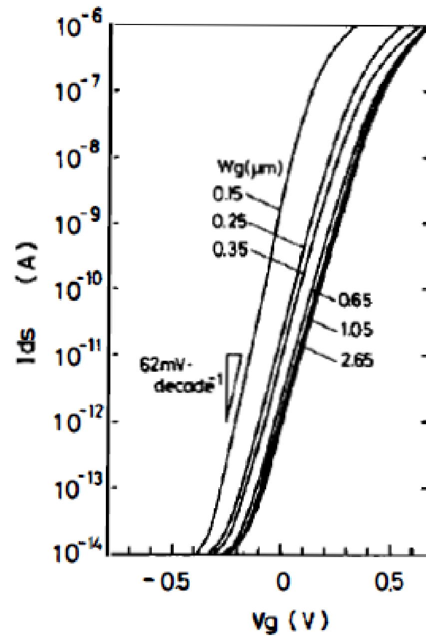
TriGate Benefits

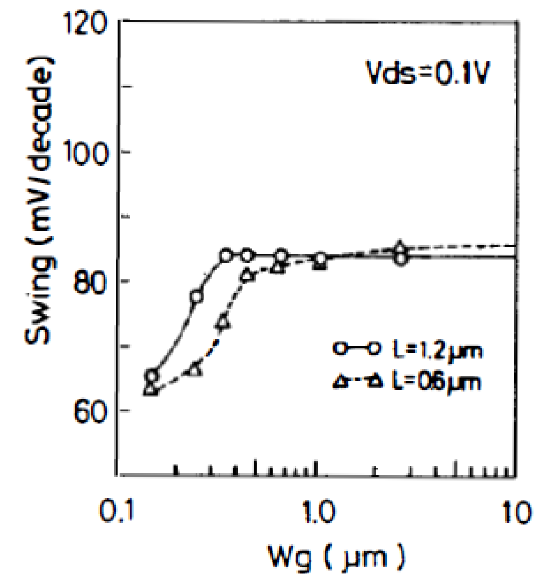


MuGFET

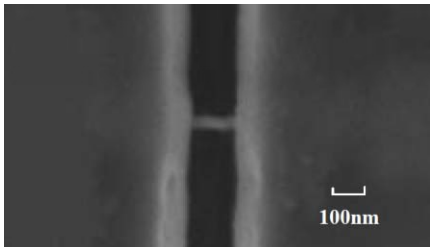
Hisamoto – IEDM 1989

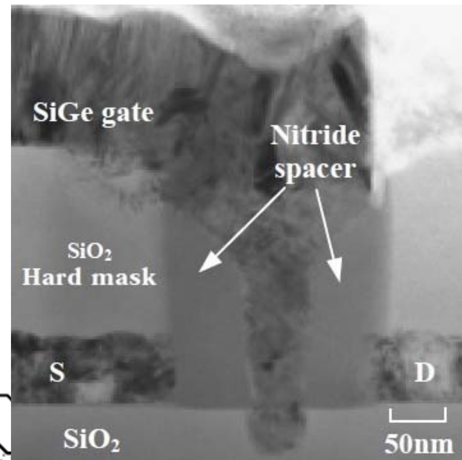


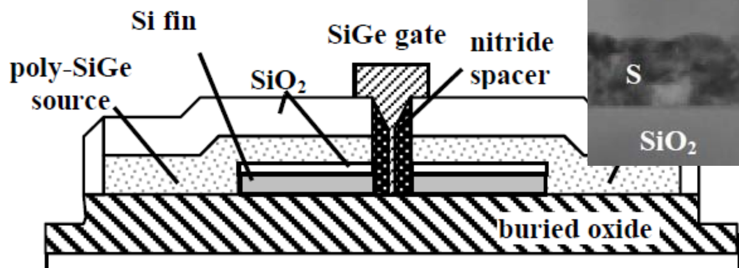


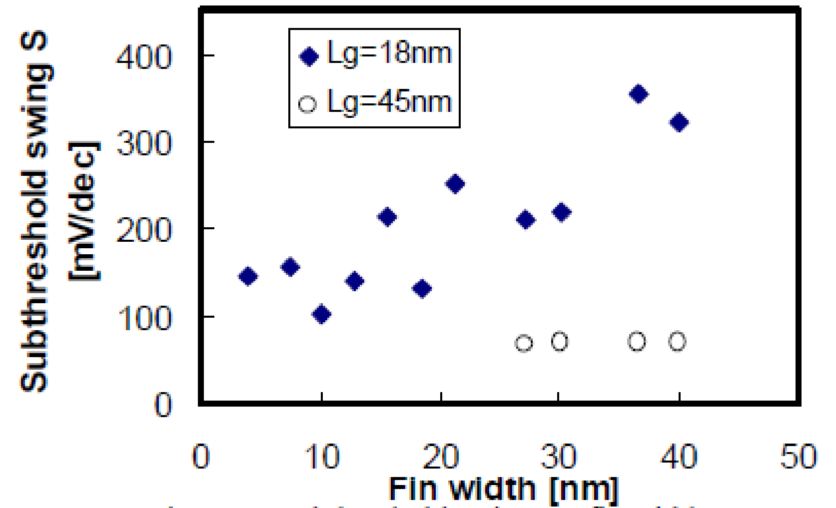


Huang (Hu) – IEDM 1999



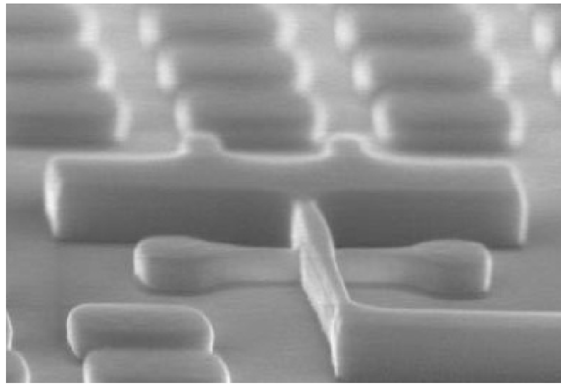


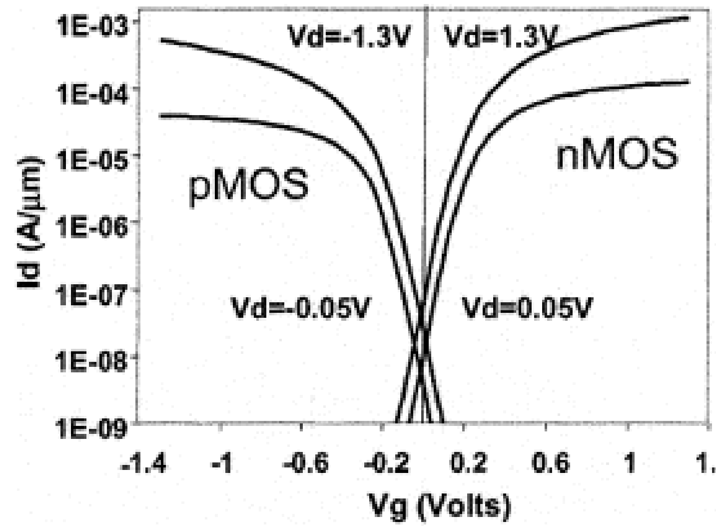


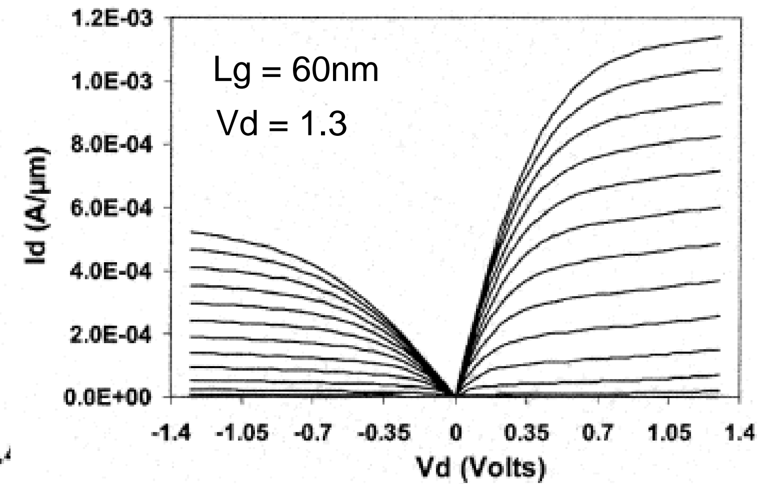


TriGate

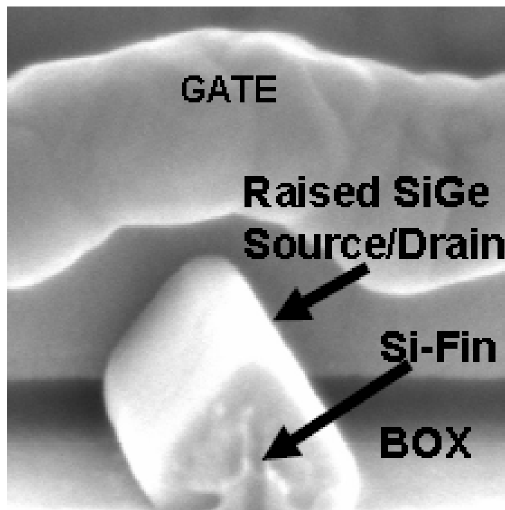
Chau – ISSDM 2002

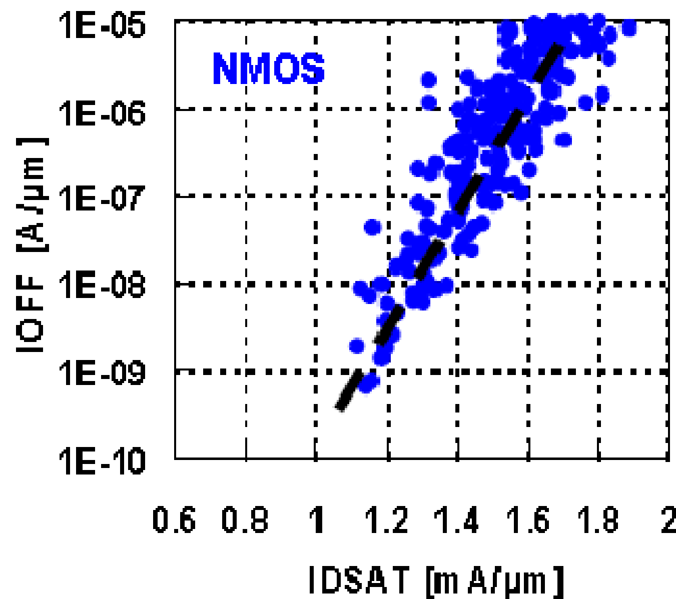


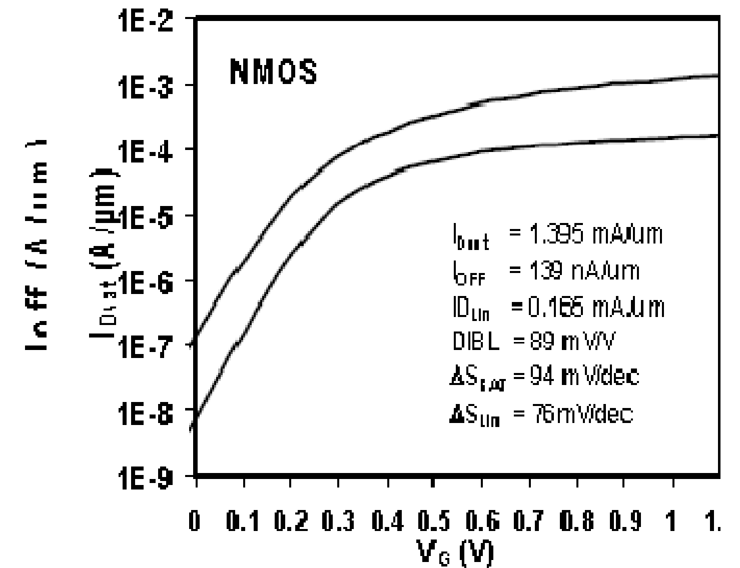




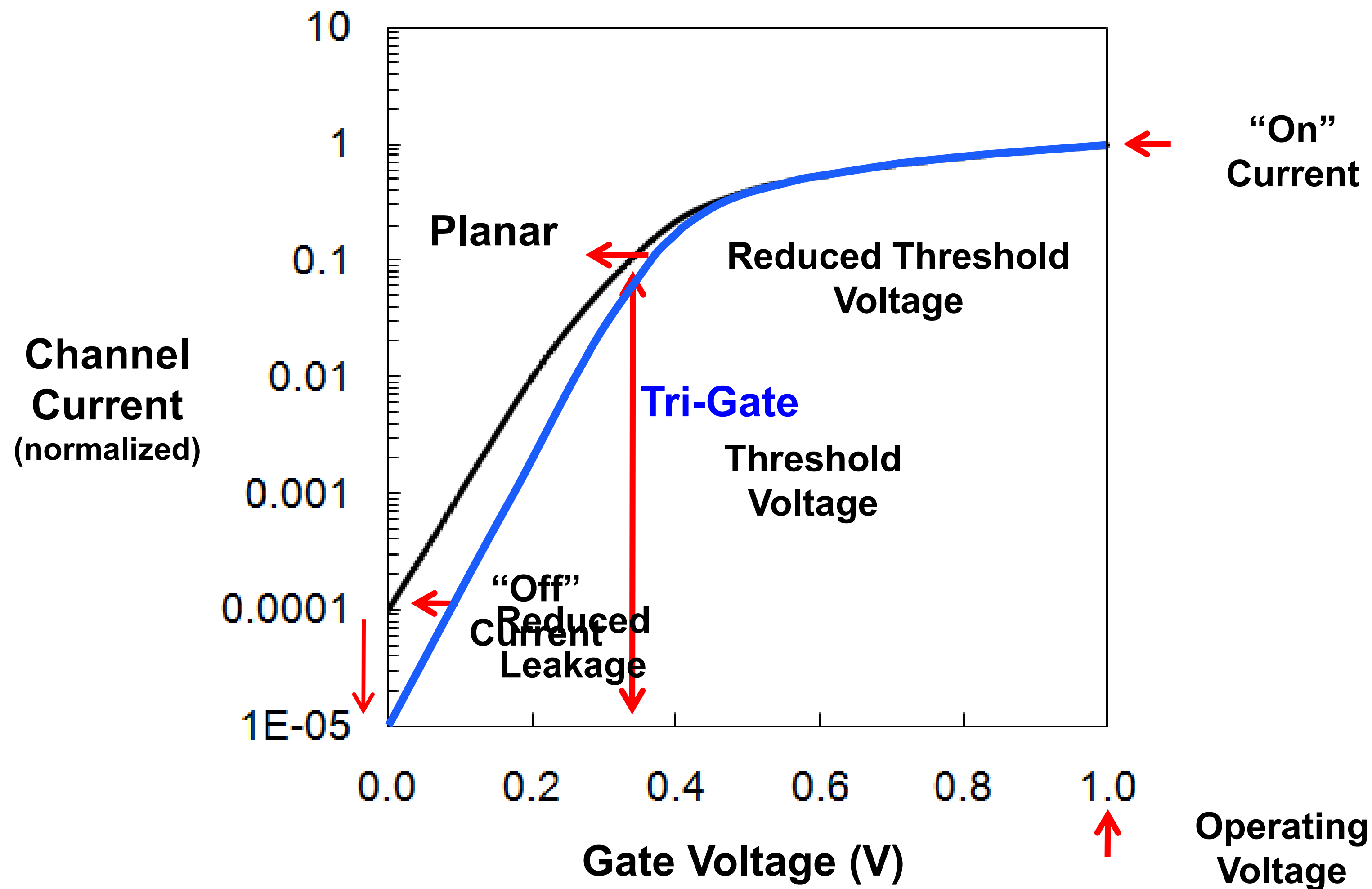
Kavalieros - IEDM 2006





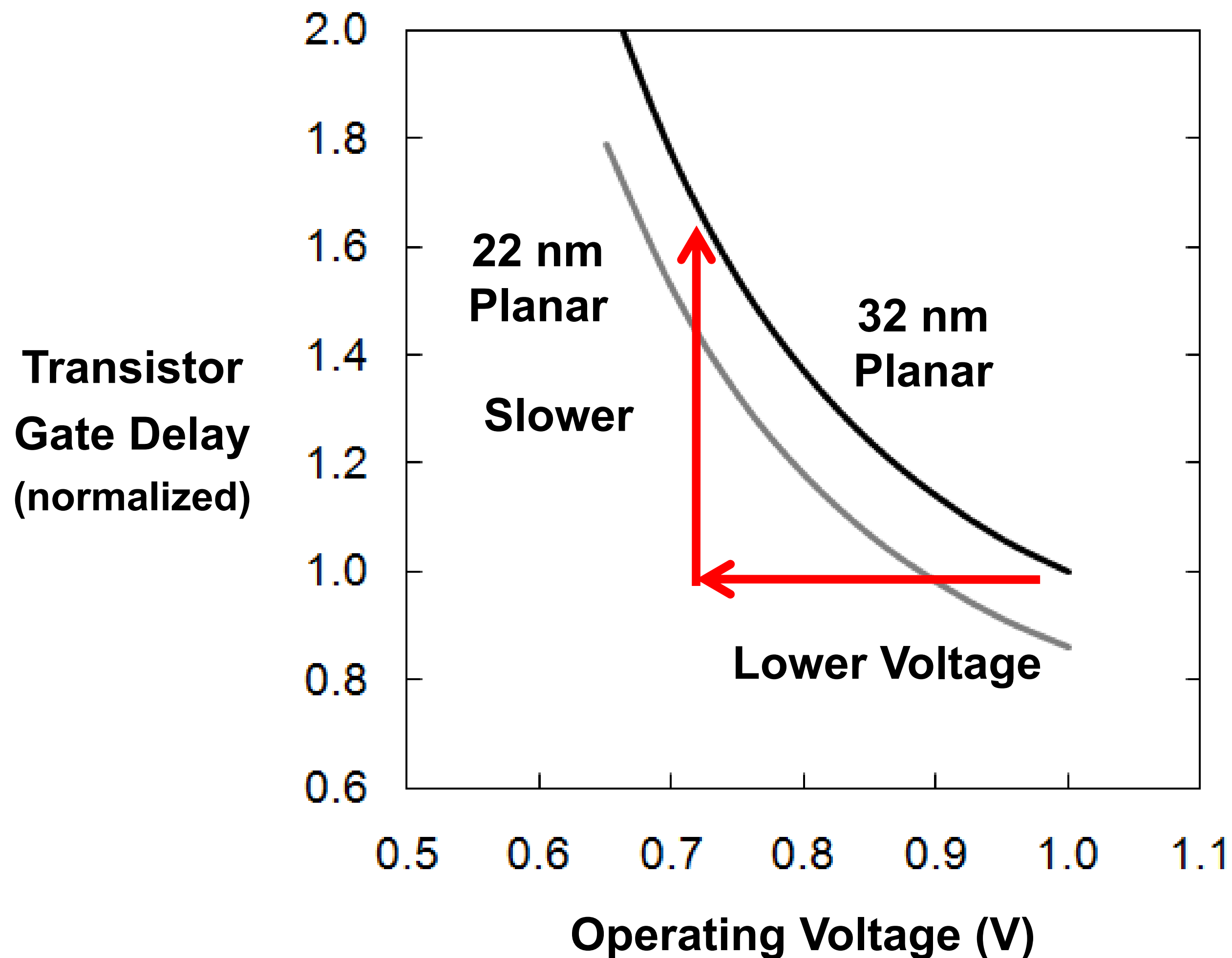


Electrostatics Benefits



Basic ID-VG

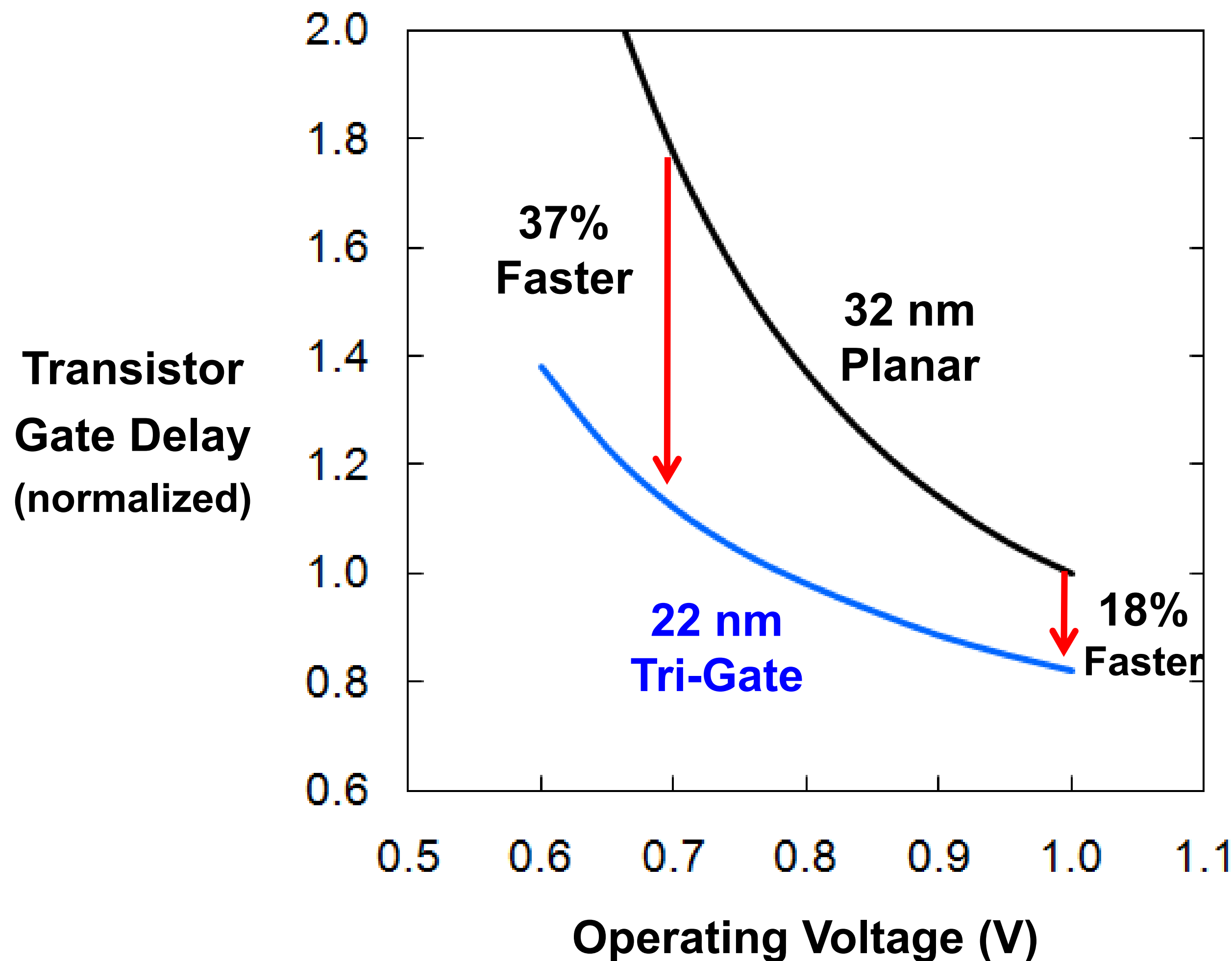
Electrostatics Benefits



22nm extension → similar ID-VG shape

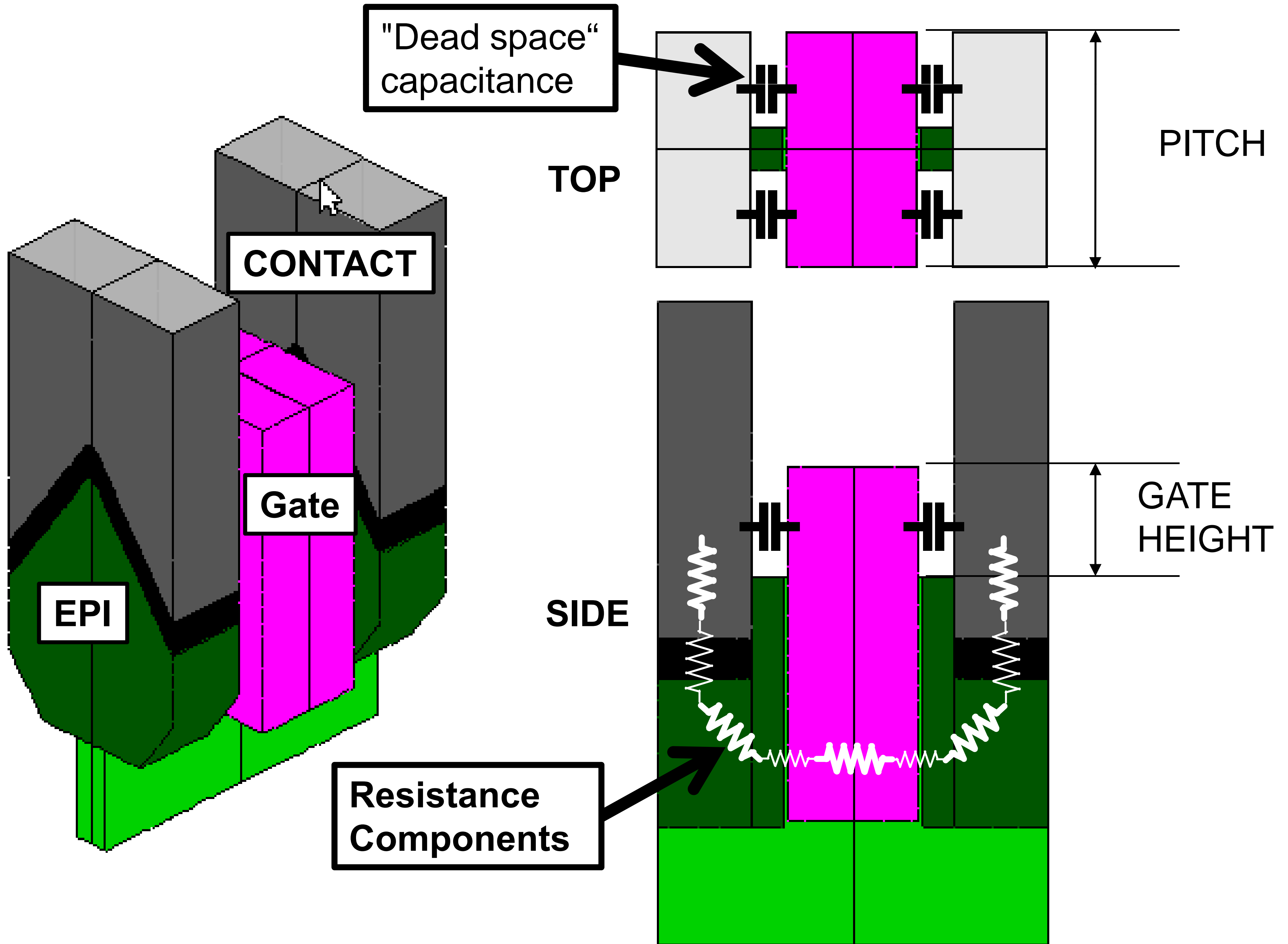
Kelin Kuhn SEMATECH 8th Int'l Sym. on Adv. Gate Stack Tech. 2011

Electrostatics Benefits

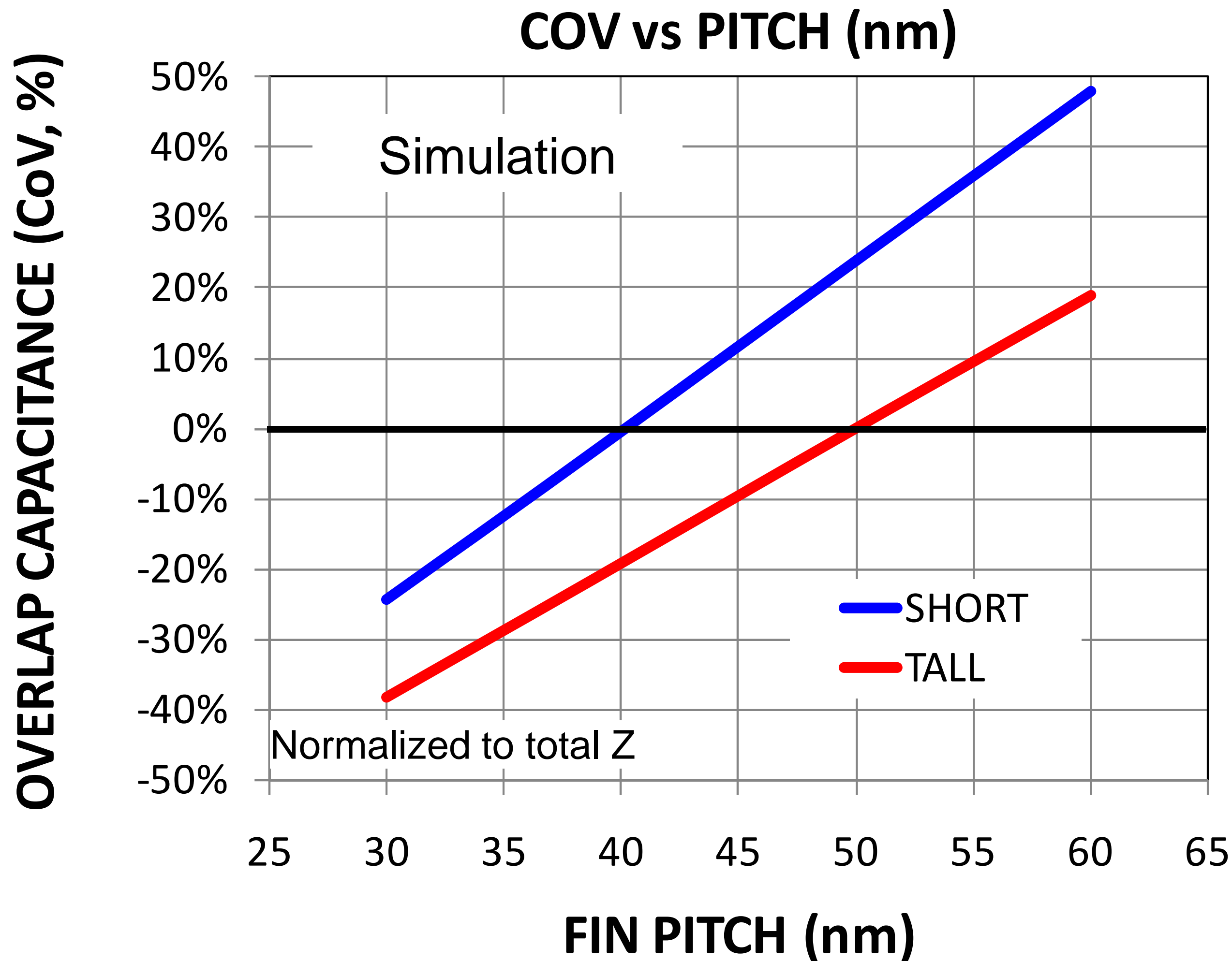


22 nm transistors provide improved performance at high voltage and an unprecedented performance gain at low voltage

Kelin Kuhn SEMATECH 8th Int'l Sym. on Adv. Gate Stack Tech. 2011

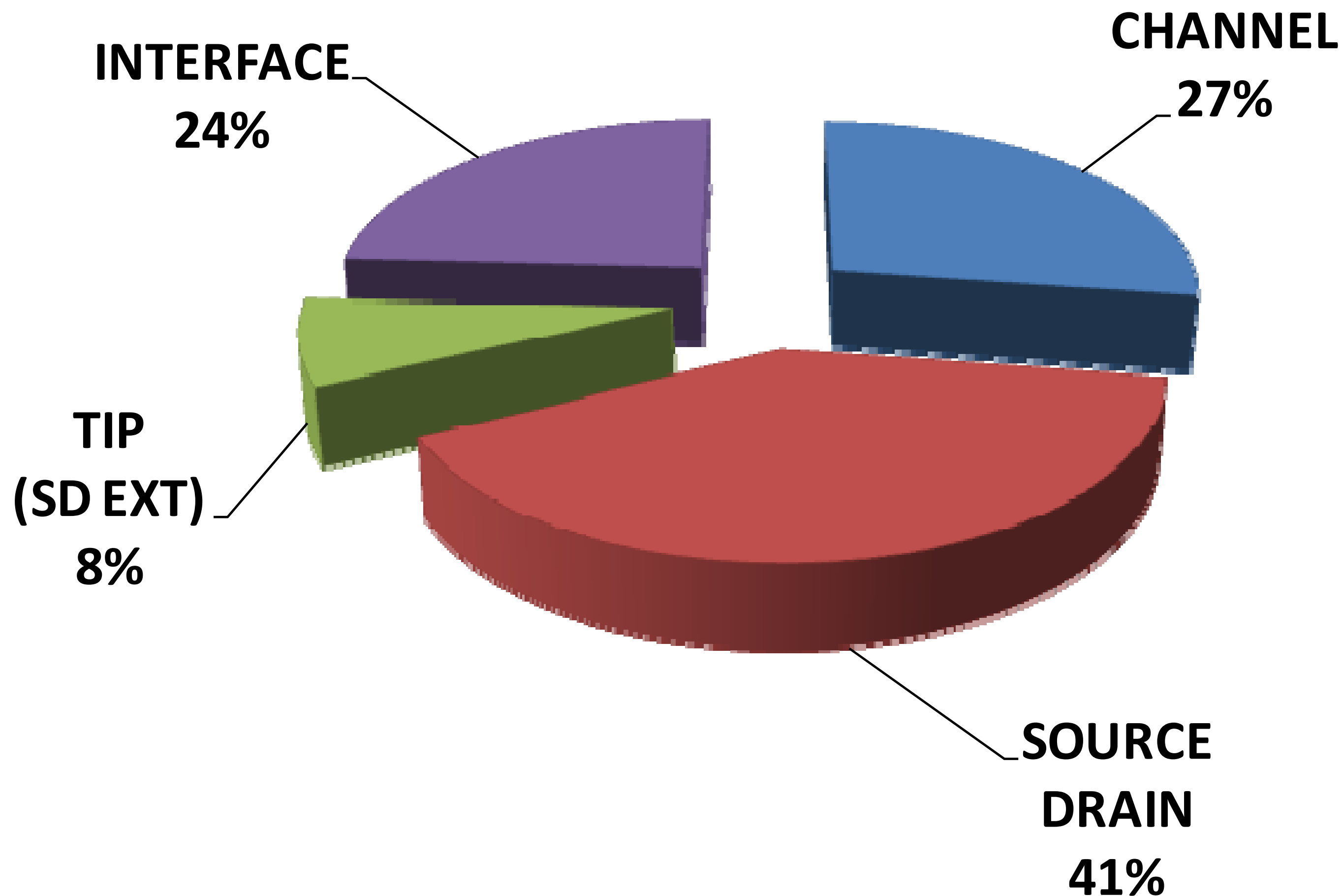

"Dead space"
capacitance
TOP
PITCH
CONTACT
Gate
EPI
SIDE
GATE
HEIGHT
Resistance
Components

Overlap Capacitance (Cov) vs Pitch



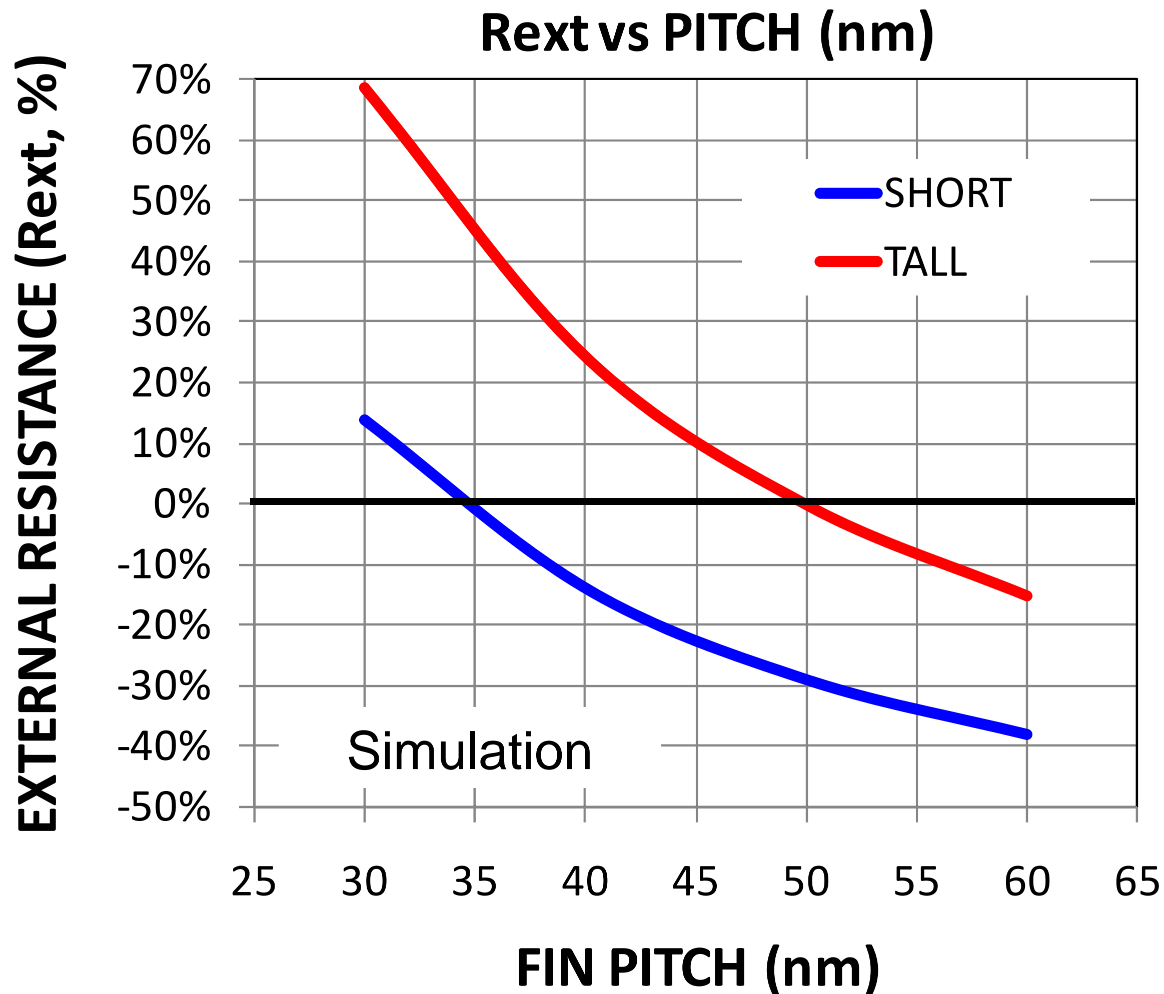
Taller fins and tighter pitches improve overlap capacitance

External Resistance Segmentation



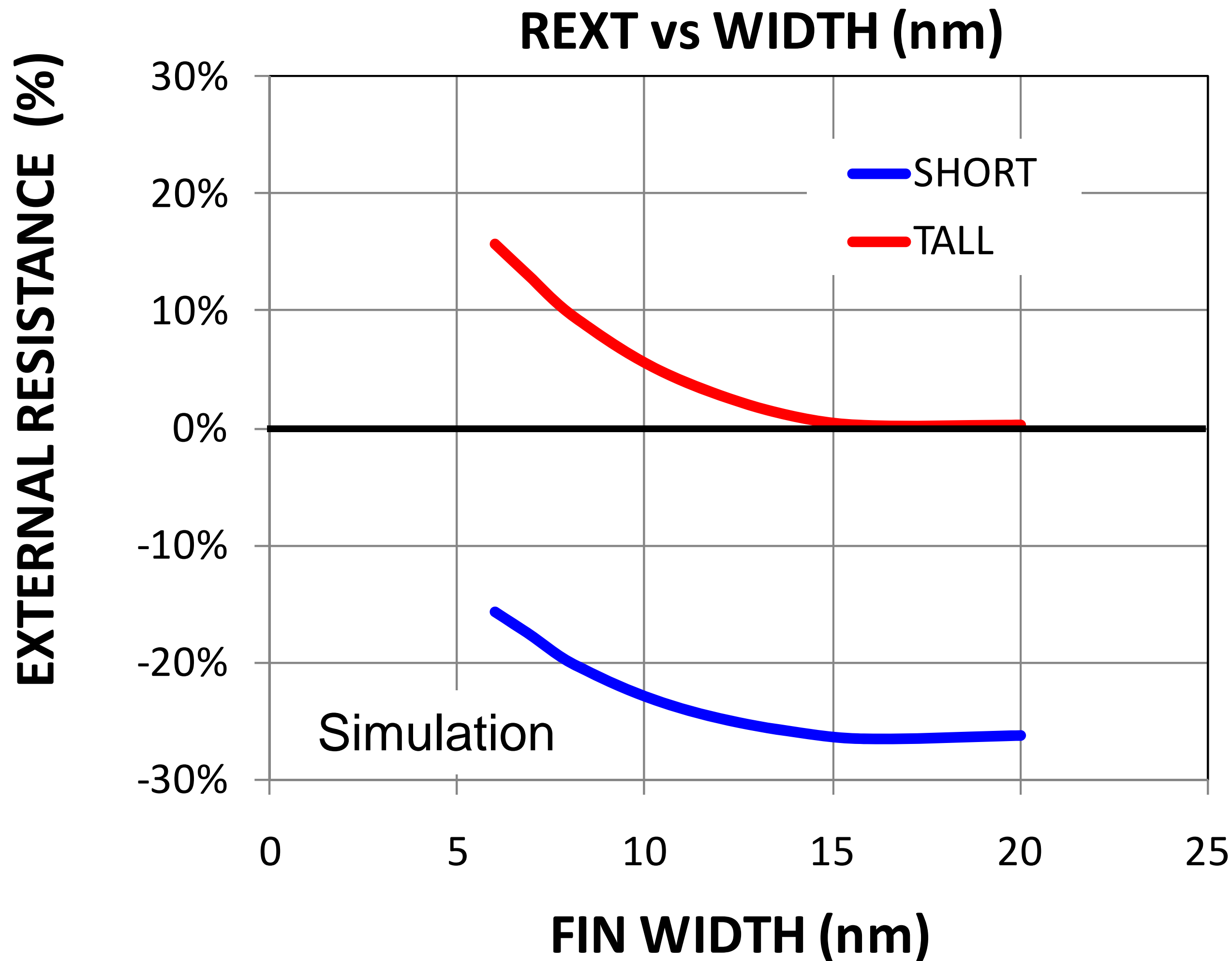
Rext = S/D resistance + Tip resistance
Greater than channel resistance!

External Resistance (Rext) vs Pitch



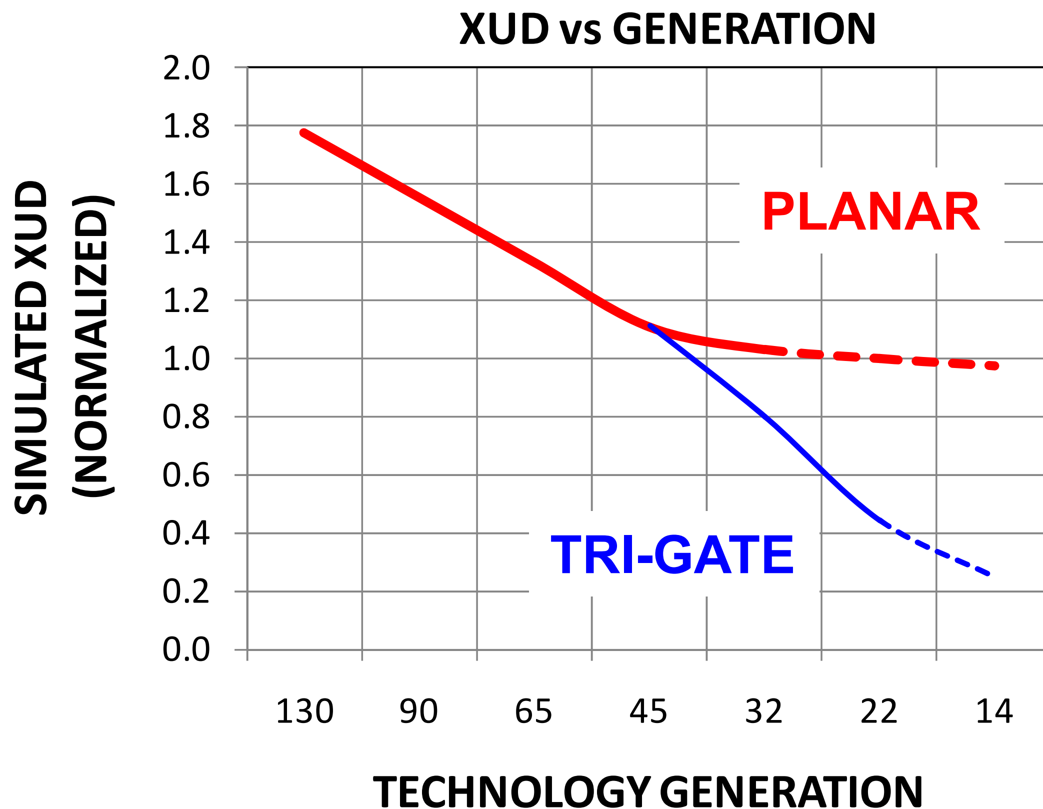
Taller fins and tighter pitches degrade external resistance

External Resistance (Rext) vs Width



Taller fins and smaller widths degrade external resistance

Xud Improvement with Tri-Gate



Planar:

- Needs high doping to control SCE →
- Tip is depleted near the channel →

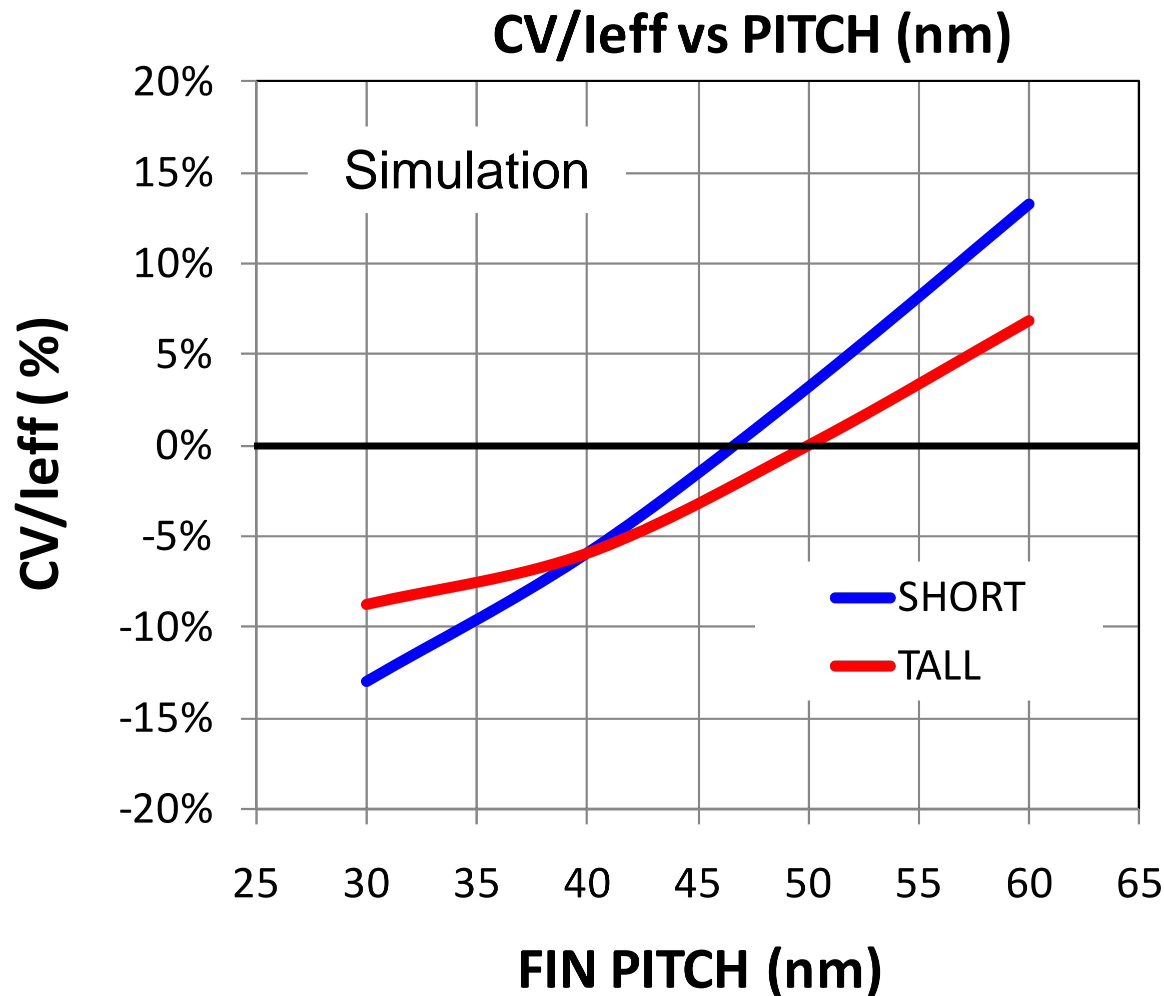
∴ Requires gate overlap to neutralize depletion

TG (or UTB):

- Has good SCE (if TSi is small enough) →
- Low or no doping to control SCE →
- Small or no tip depletion →

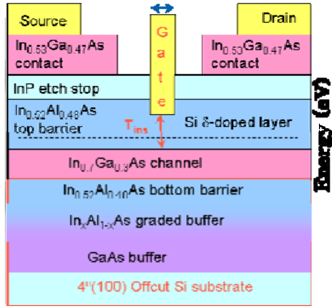
∴ Xud can be smaller

CV/Ieff vs Pitch

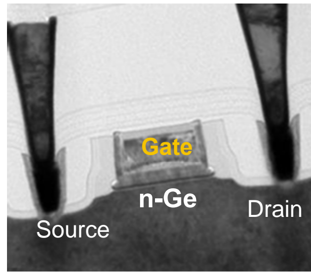


Optimal performance is a trade-off between R and C and requires optimizing height, width and pitch

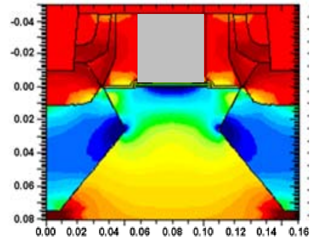
MORE THAN MOORE

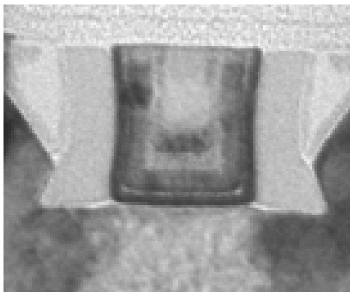


III-V



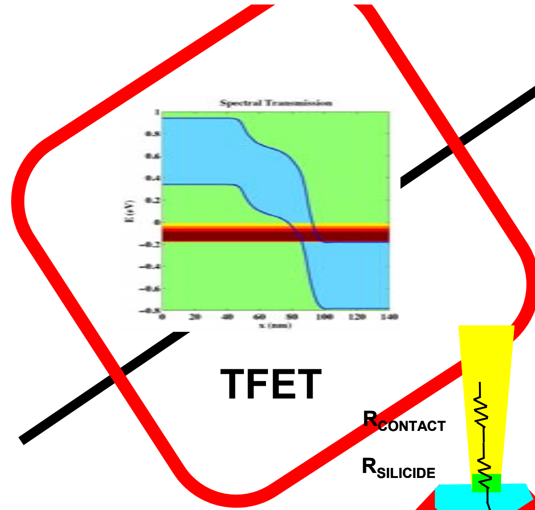
Ge


Strain

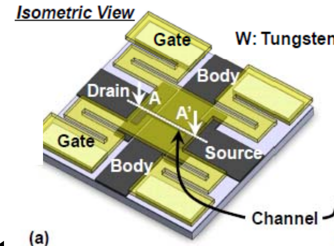

32nm

MOBILITY

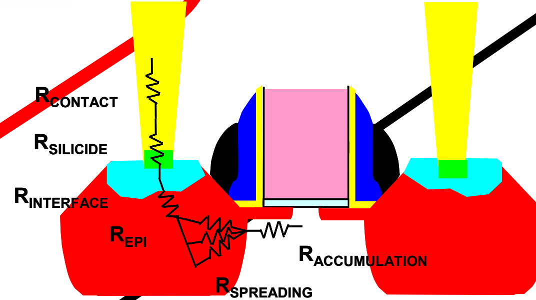
STRUCTURE



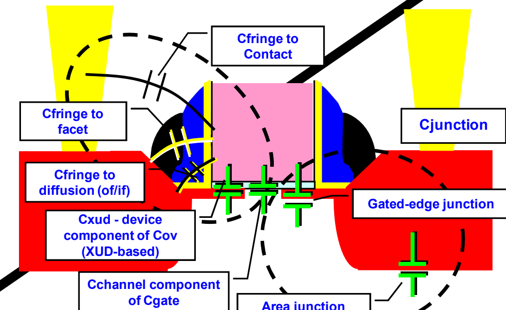
TFET



RELAY

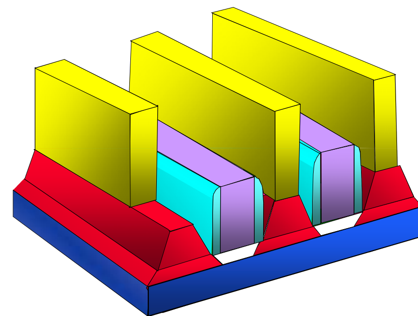


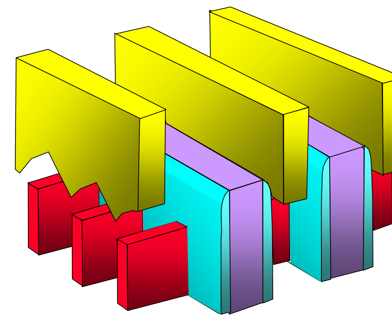
Resistance

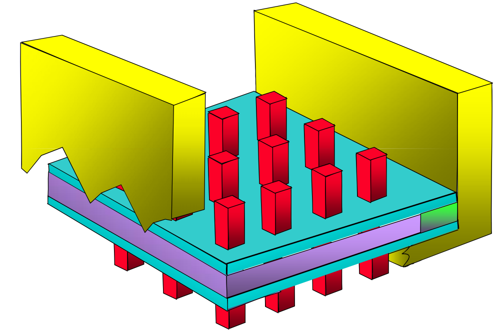


Capacitance

PARASITICS

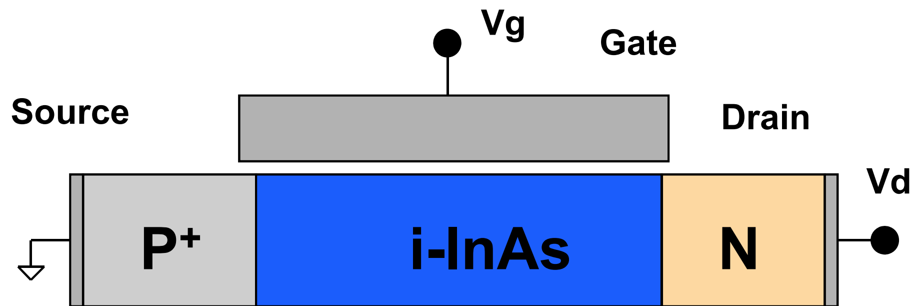

UTB SOI

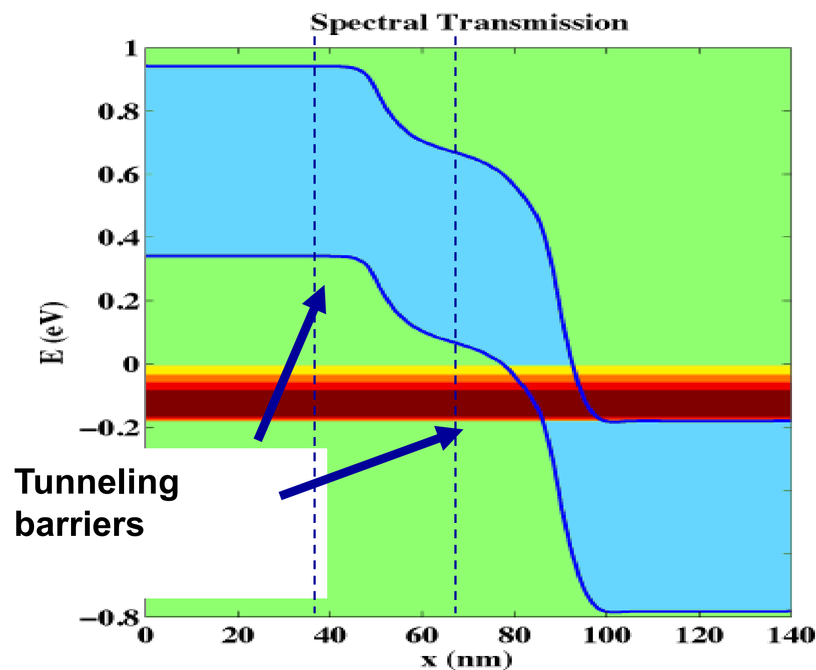

Fins


Wires/Dots

ELECTROSTATIC CONFINEMENT

TFET (Tunneling Field-Effect Transistor)





Courtsey M. Luisier (Purdue)
M. Luisier and G. Klimeck, EDL, 2009

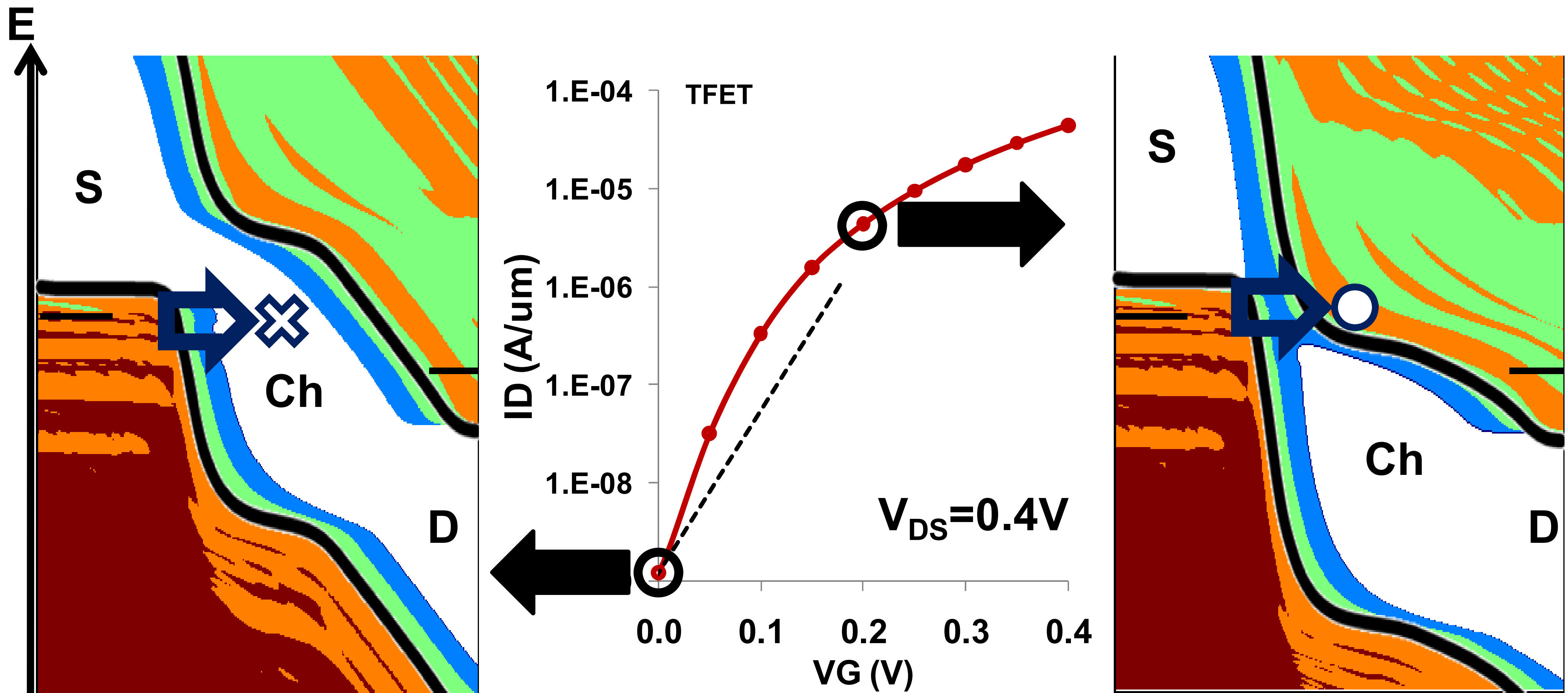
Tunnel FETs operate by tunneling through the S/D barrier rather than diffusion over the barrier

Two required conditions:

- Thin enough barrier over a large enough area for effective (high current) tunneling.
- Sufficient density of states on both the transmission and receiving sides to provide energetic locations for the carriers.

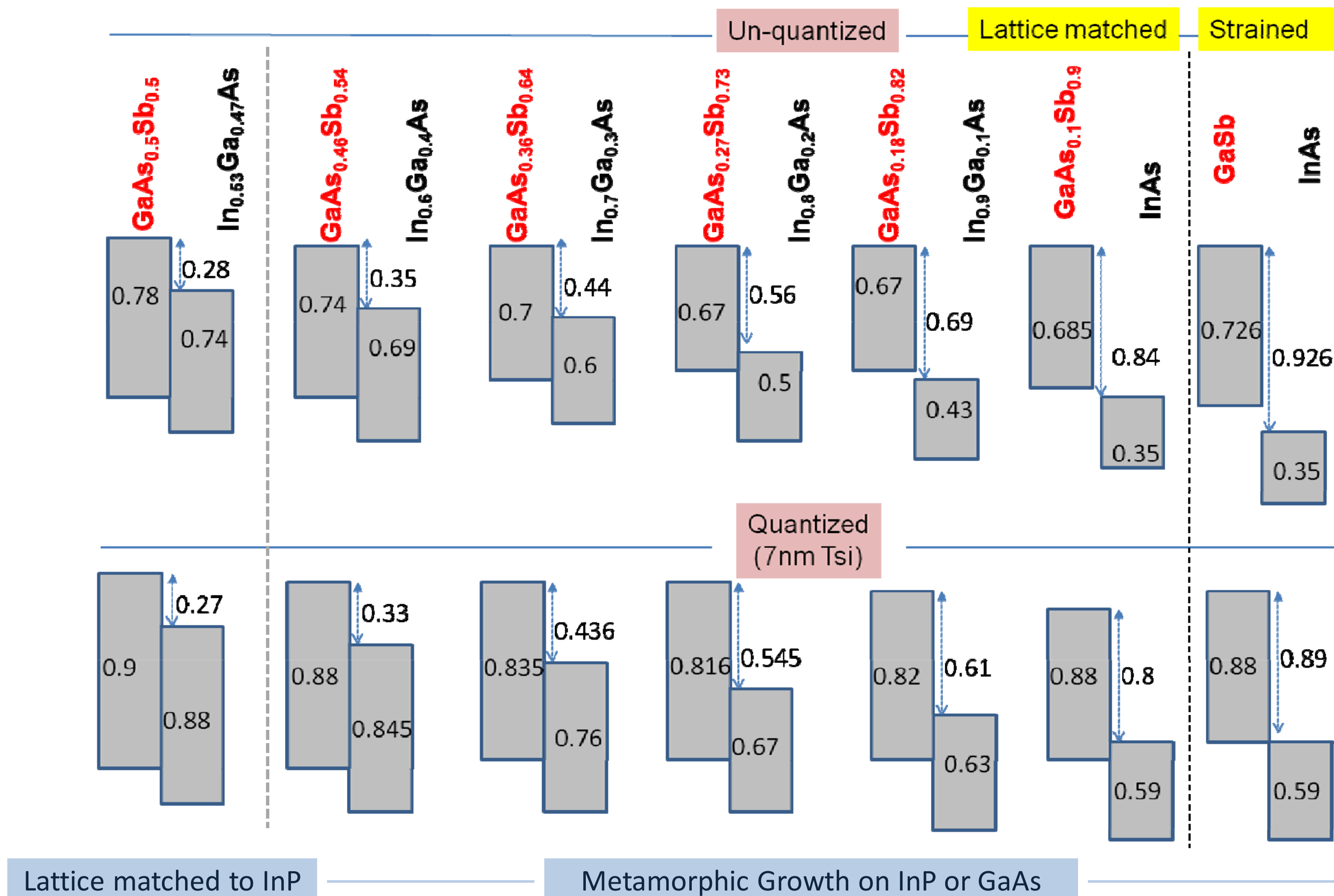
TFET Sub-threshold Slope

- **Tunneling probability increases sharply at the onset of *Source Valence Band* and *Channel Conduction Band* overlap**



Avci, Intel, VLSI 2011

HTFET Material Considerations



Staggered and broken gap systems have higher tunneling probability.

11

Theresa Mayer and Suman Datta, Penn State, SRC review 2011

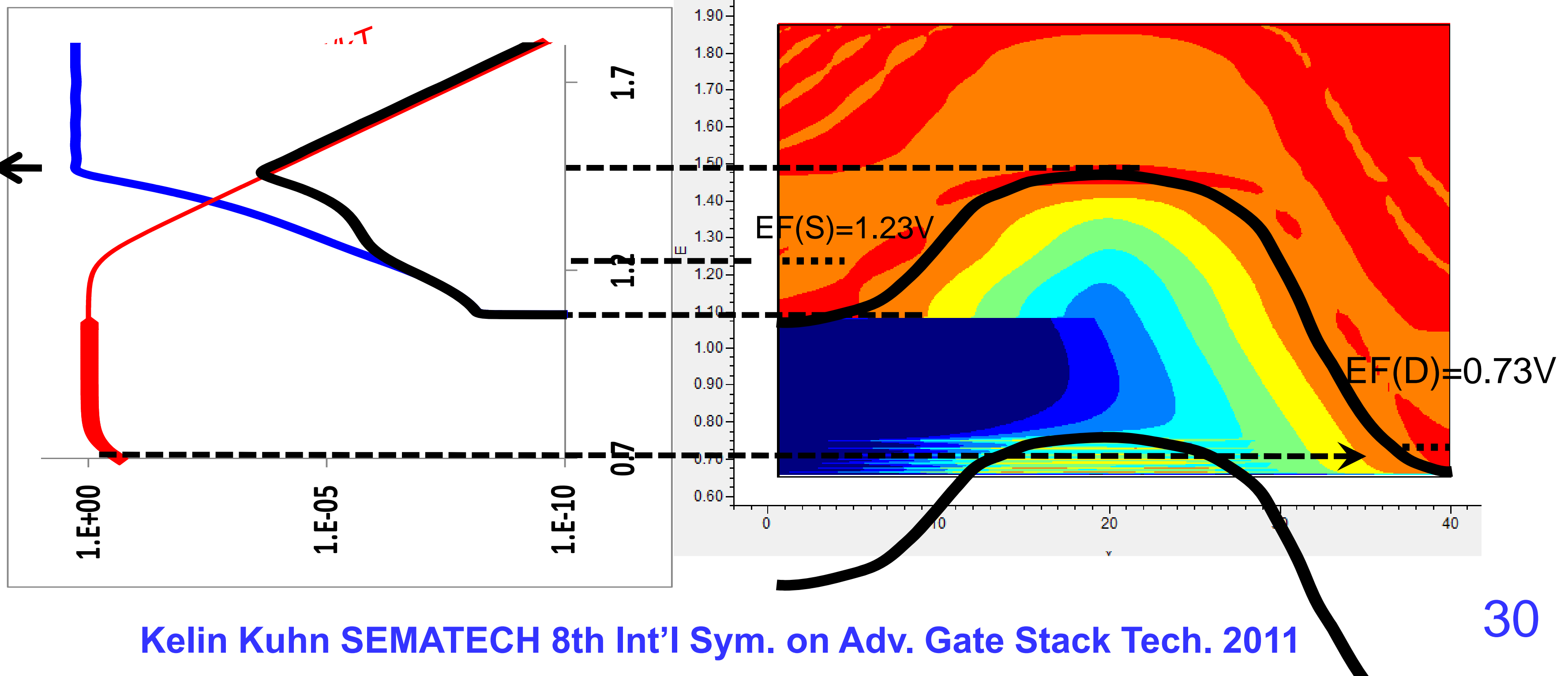
MOSFET Sub-threshold Slope = 60 mV/dec

MOSFET SS = 60 mV/dec, because the current increase is driven by Fermi distribution tail over the barrier.

- J(E): Current density = f(E)*T(E)
- f(E): Electron occupancy difference b/w S and D
- T(E): Transmission rate including # of modes

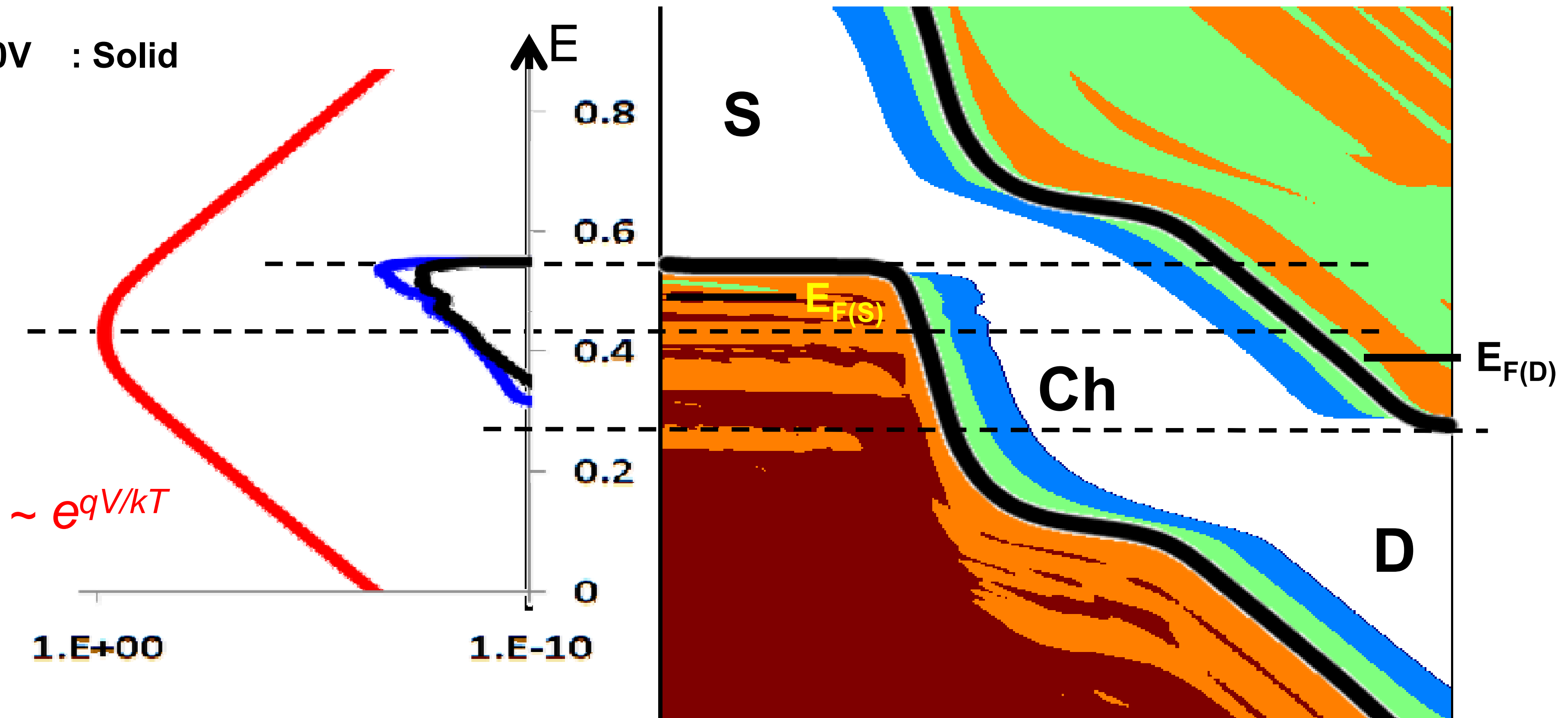
f(E) peak is between Fermi levels
T(E) edge is at conduction band

5nm-thick $In_{0.7}Ga_{0.3}As$ MOSFET at sub-threshold using OMEN



N-TFET Sub-threshold Slope < 60 mV/dec

In N-TFET, sub-threshold current is controlled by the change in tunneling probability at the onset of Valence band and Conduction band overlap.



- J(E): Current density = f(E)*T(E)
- f(E): Electron occupancy difference b/w S and D
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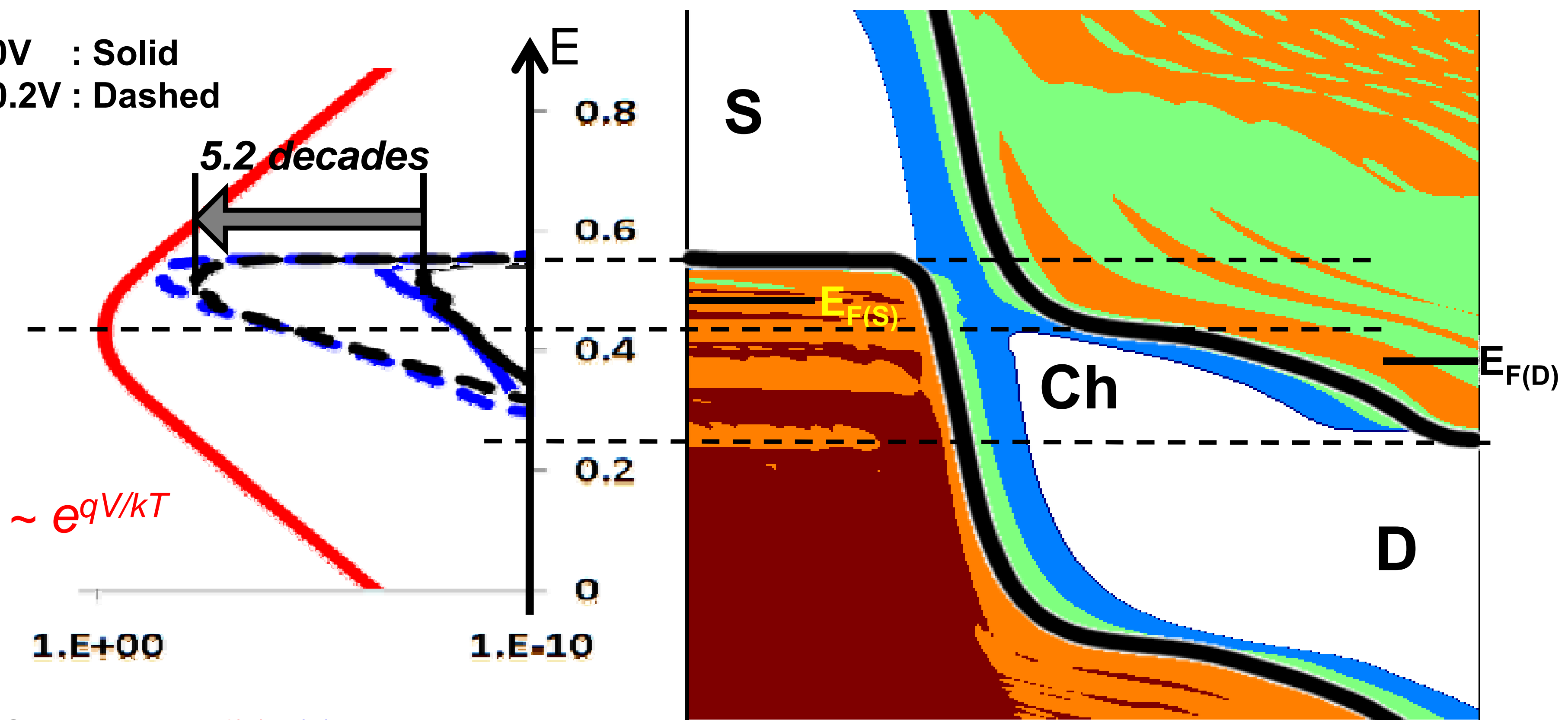
N-TFET Sub-threshold Slope < 60 mV/dec

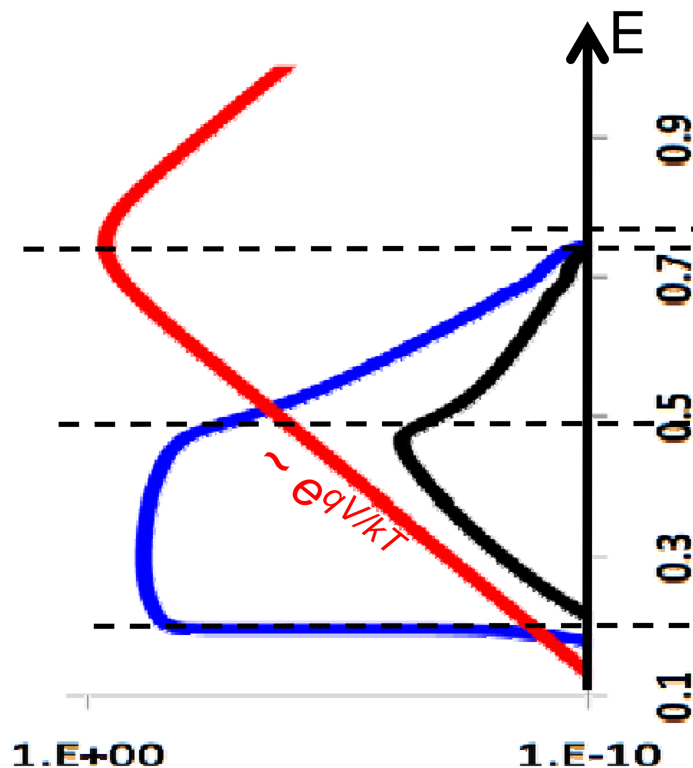
In N-TFET, sub-threshold current is controlled by the change in tunneling probability at the onset of Valence band and Conduction band overlap.

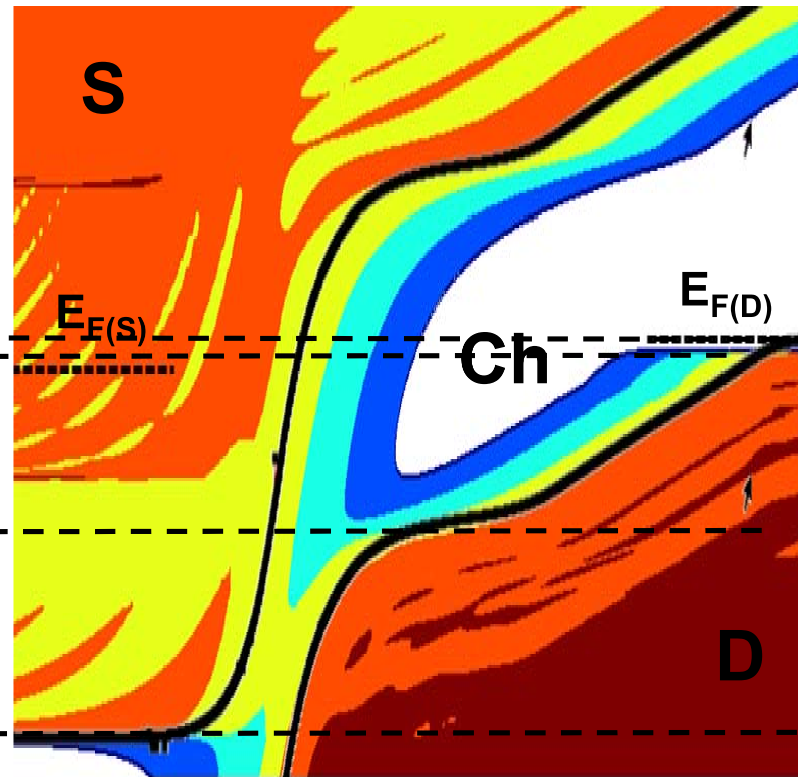


- J(E): Current density = f(E)*T(E)
- f(E): Electron occupancy difference b/w S and D
- T(E): Transmission rate including # of modes

P-TFET Sub-threshold Slope ~ 60 mV/dec

In P-TFET, sub-threshold current is controlled by the change in Fermi distribution difference when EC(S)< EV(Channel) <EF(S).

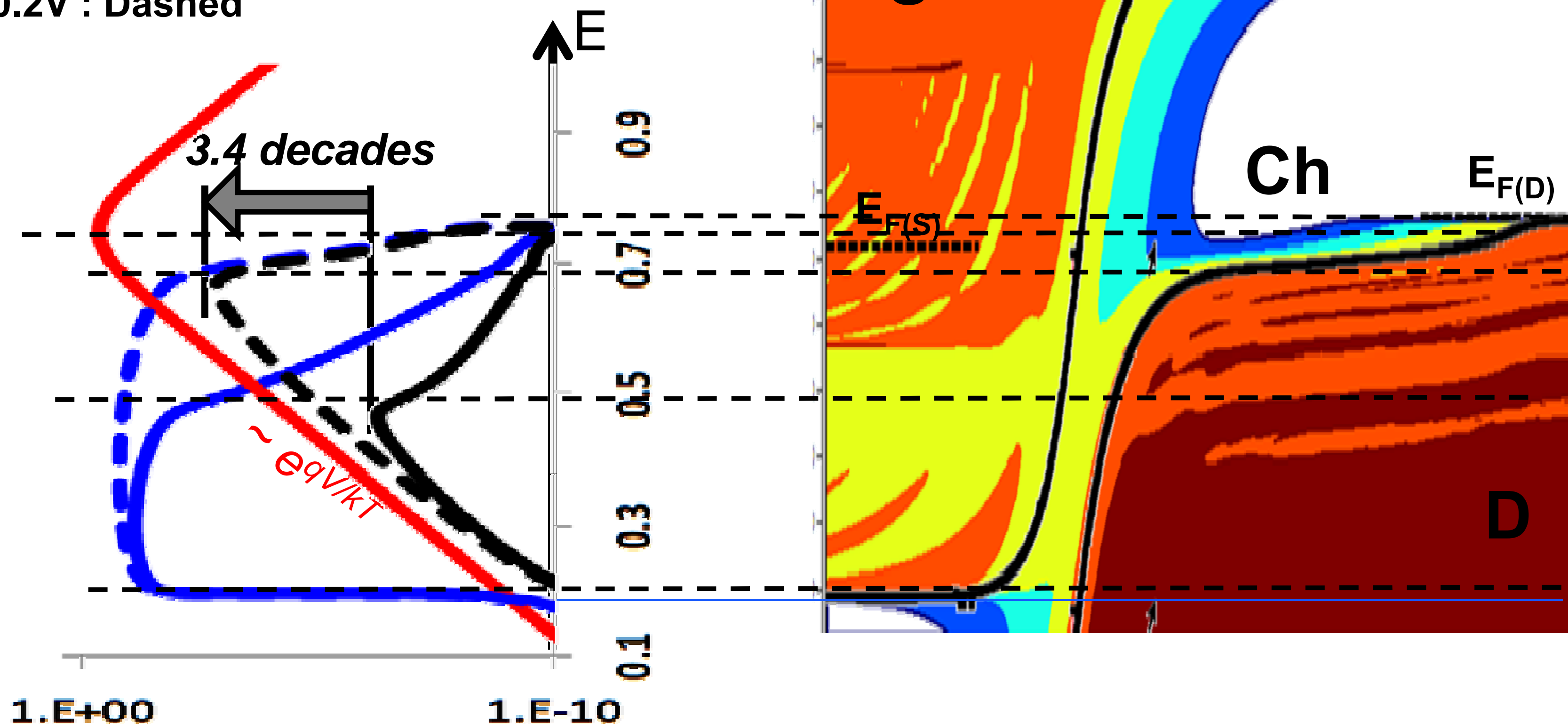




- J(E): Current density = f(E)*T(E)
- f(E): Electron occupancy difference b/w S and D
- T(E): Transmission rate including # of modes

P-TFET Sub-threshold Slope ~ 60 mV/dec

In P-TFET, sub-threshold current is controlled by the change in Fermi distribution difference when EC(S)< EV(Channel) <EF(S).

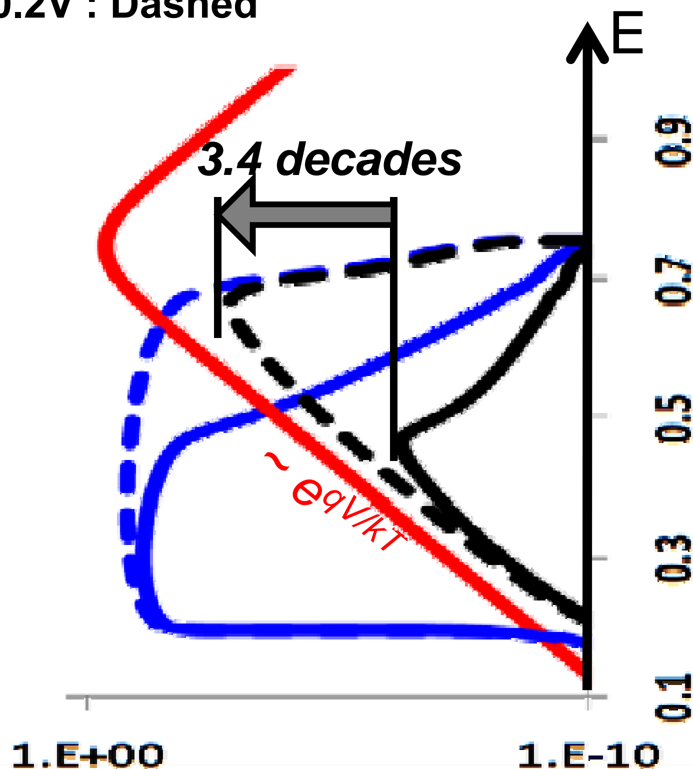


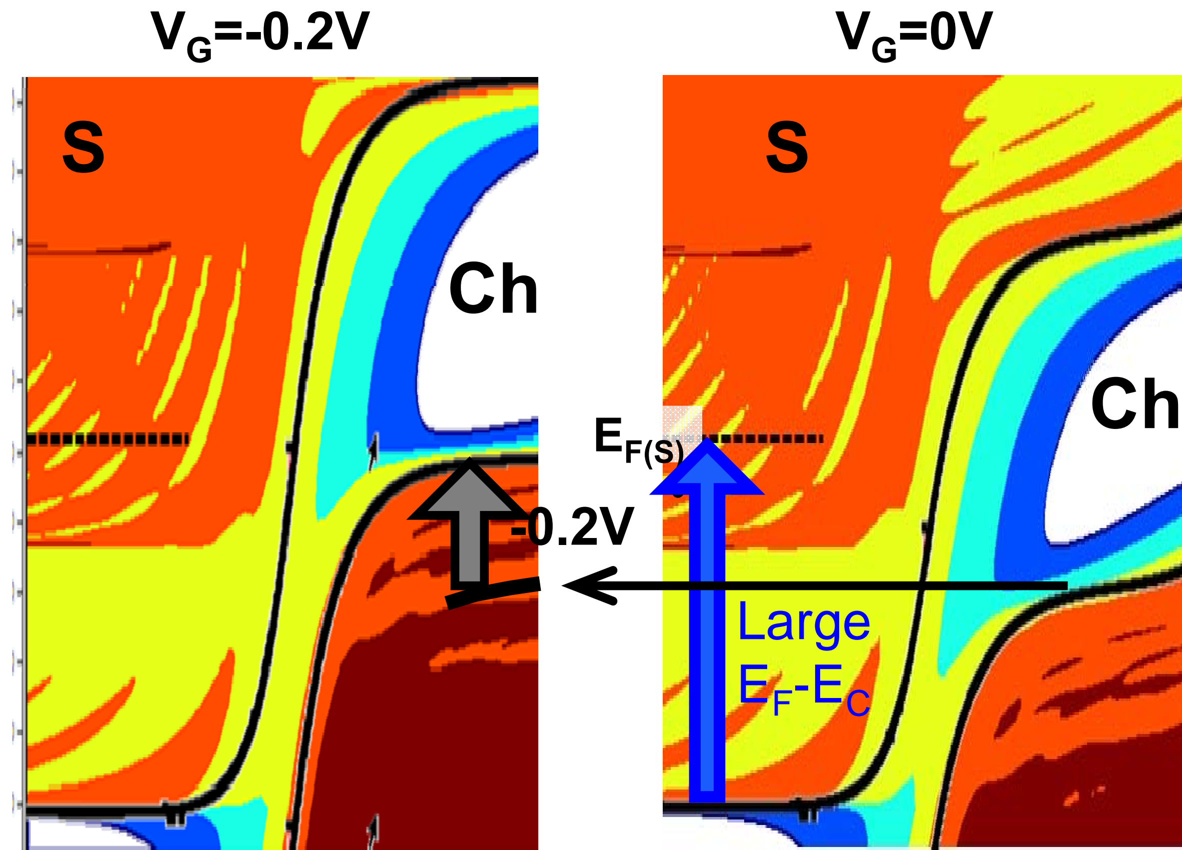
- J(E): Current density = f(E)*T(E)
- f(E): Electron occupancy difference b/w S and D
- T(E): Transmission rate including # of modes

P-TFET Sub-threshold Slope ~ 60 mV/dec

In P-TFET, sub-threshold current is controlled by the change in Fermi distribution difference when EC(S)< EV(Channel) <EF(S).

$J(E) = f(E)^* T(E)$

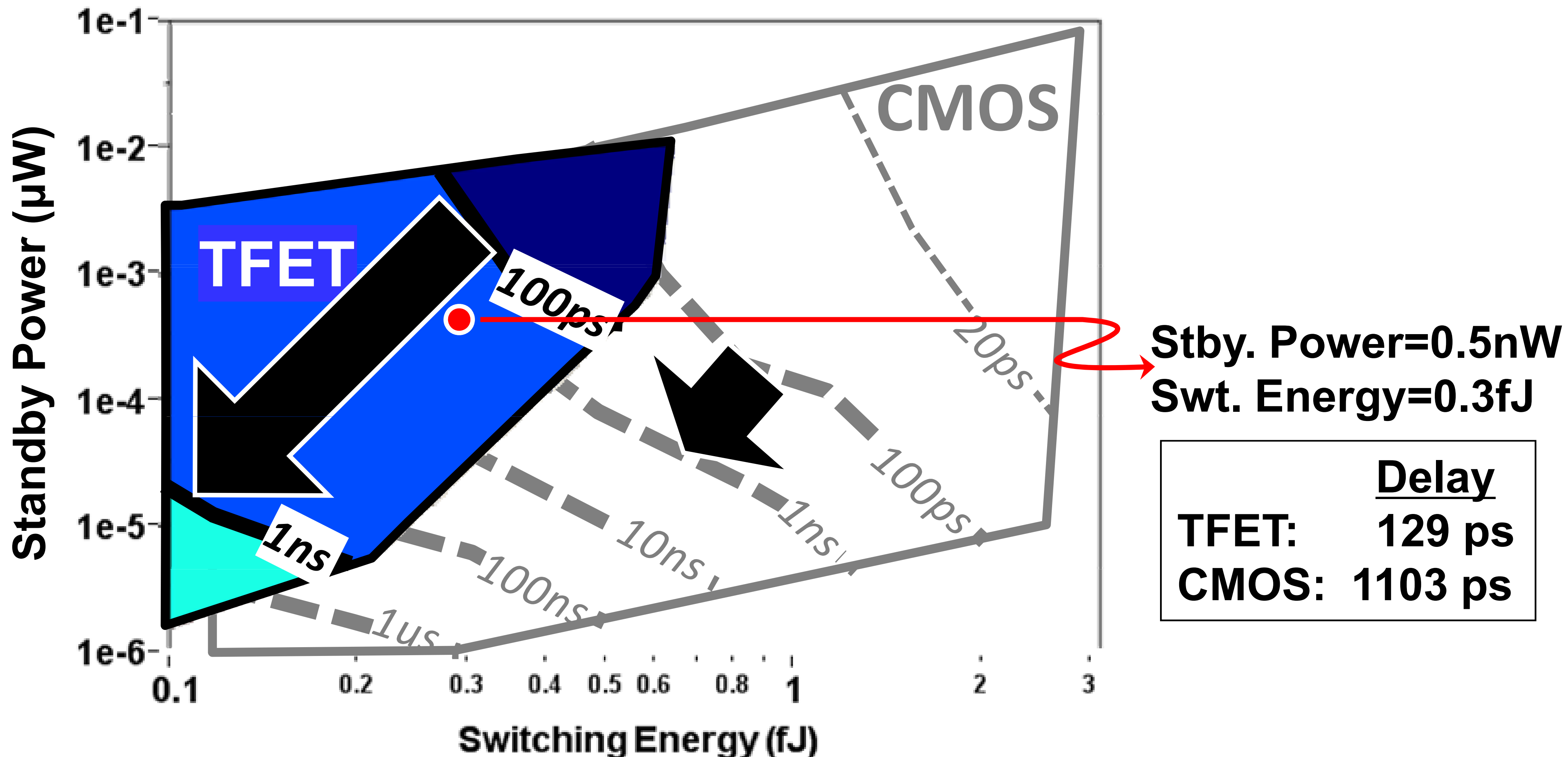




- J(E): Current density = f(E)*T(E)
- f(E): Electron occupancy difference b/w S and D
- T(E): Transmission rate including # of modes

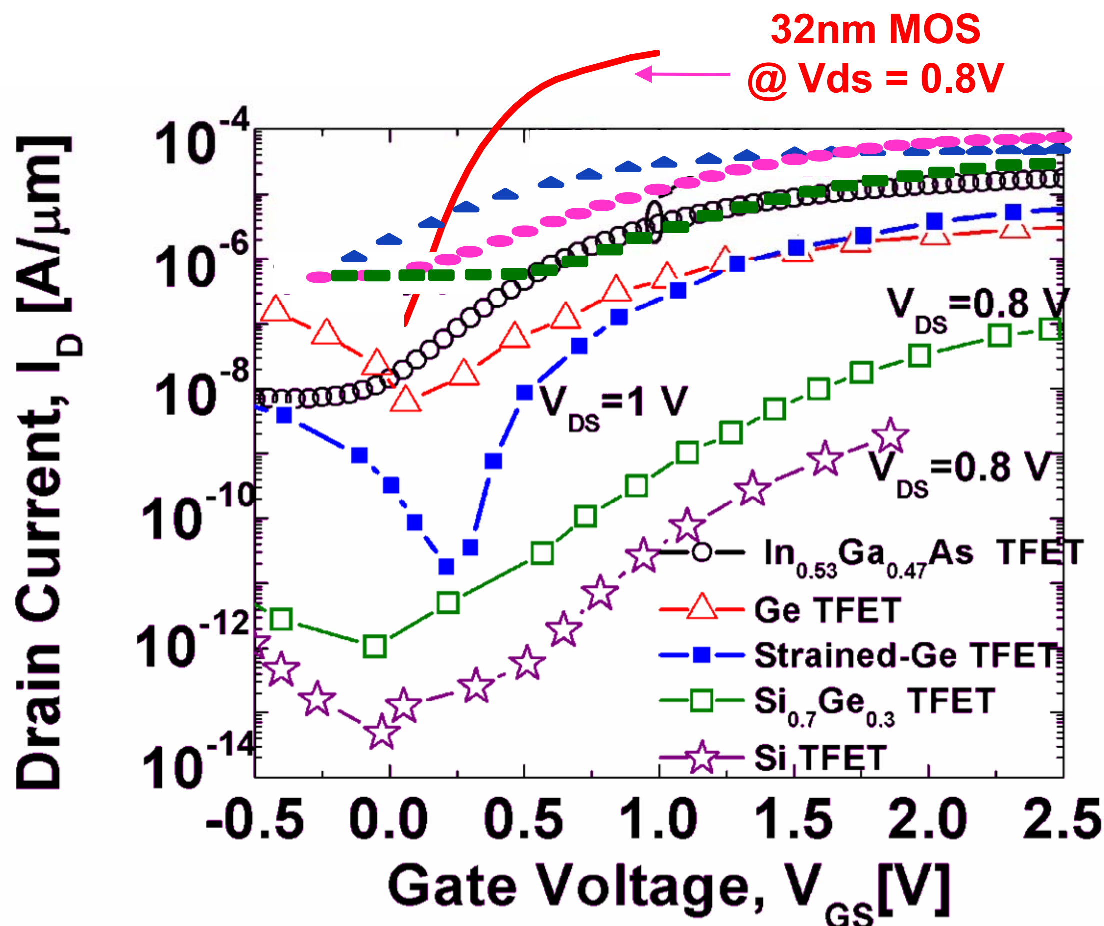
TFET vs. MOSFET

At low switching energy, InAs TFET is theoretically capable of providing more than 8x performance advantage over MOSFET



Avci, Intel, VLSI 2011

Best demonstrated TFETs still have poor drive current



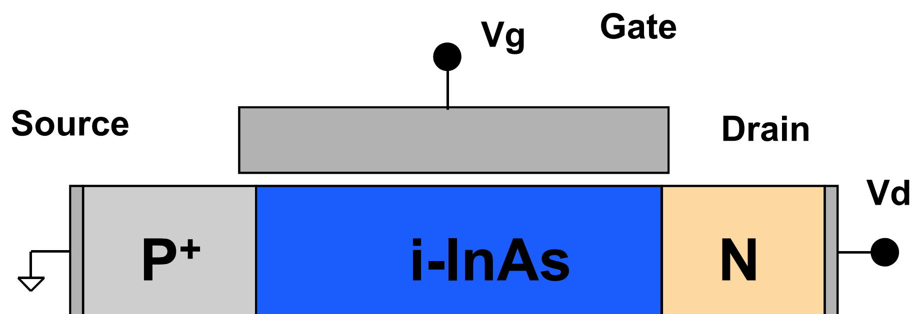
	Ref. [2]	Ref. [3]	Ref. [4]	This Work
SS (mV/dec)	52.8	42	~300	46
I_{ON} (μA/μm)	12.1	0.01	1E-4	1.2
I_{ON}/I_{OFF}	1E4	1E4	1E2	7E7

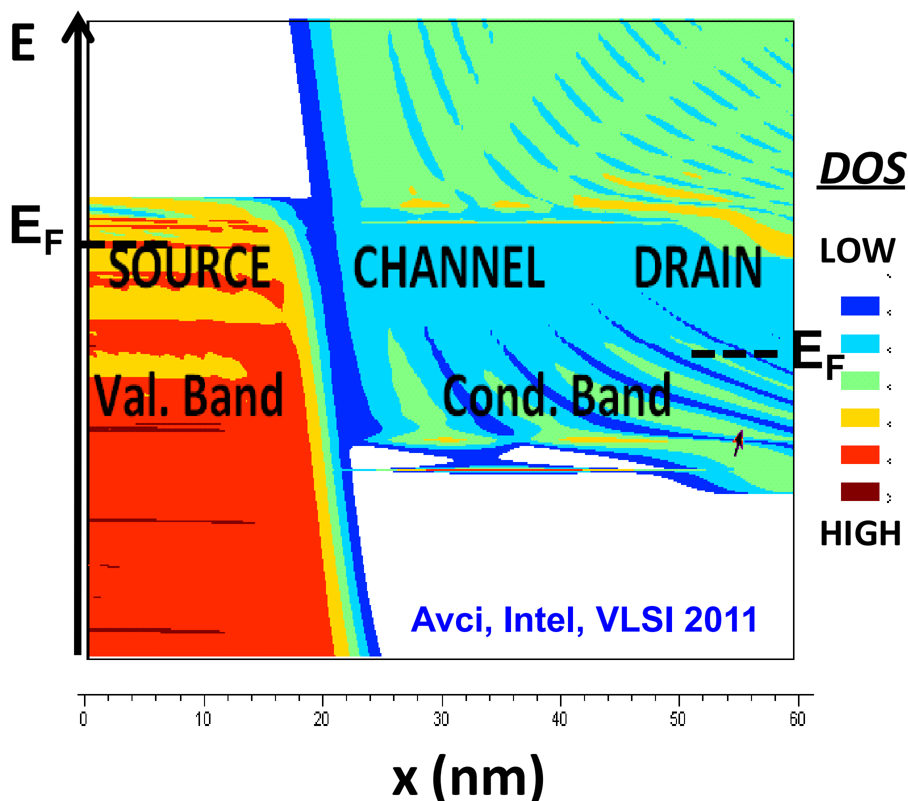
Table. I. Comparison to reported silicon TFETs. ($V_{DS}=V_{GS}-V_{BTBT}=1.0V$)

S. Mookerjea et al., IEDM ’09
D. Mohata, Appl. Phys, Jan ‘11

[1] K. Jeon, et al., VLSI (11.4.1.-1) 2010
[2] W. Choi et al., IEEE-EDL vol.28, no.8, p.743 (2007)
[3] F. Mayer et al., IEDM Tech Dig., p.163 (2008)
[4] T. Krishnamohan et al., IEDM Tech Dig., p.947 (2008)

TFET (Tunneling Field-Effect Transistor)



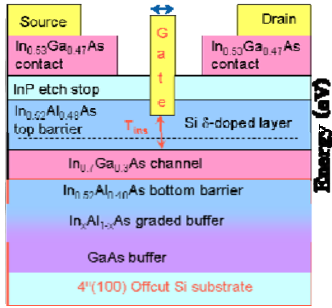


Benefits

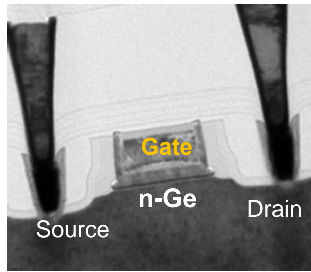
- Steep sub-threshold slope (< 60 mV/dec)
- Large Ion/Ioff ratio
- Geometry scales well
- Some designs are compatible with conventional SiGe/Si CMOS processes

Challenges

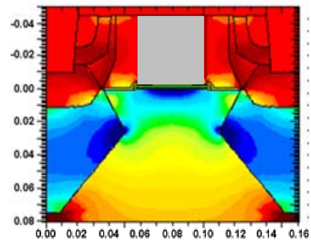
- Poor experimental drive currents
- Ambipolar conduction (high DB leakage for bulk devices)
- No comparable PTFET
- Asymmetric device behavior (issues with SRAM / passgates)
- Most attractive at very low operating voltages (where product frequencies may be disinteresting)



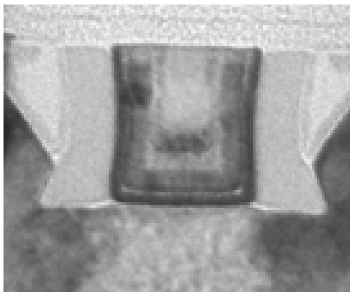
III-V



Ge



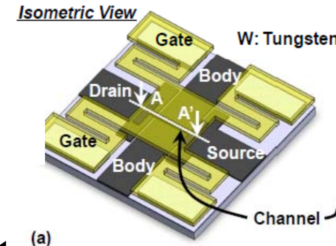
Strain



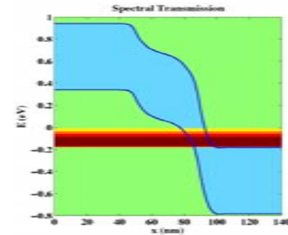
32nm

MOBILITY

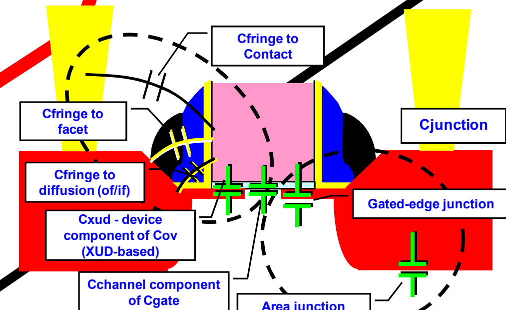
STRUCTURE



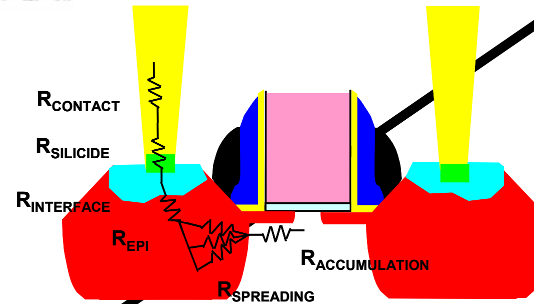
RELAY



TFET

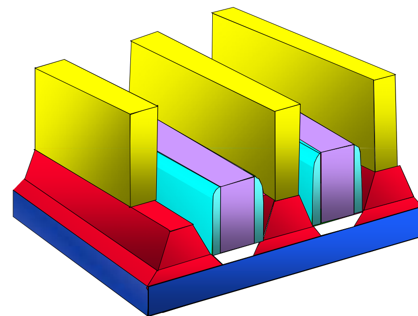


Capacitance

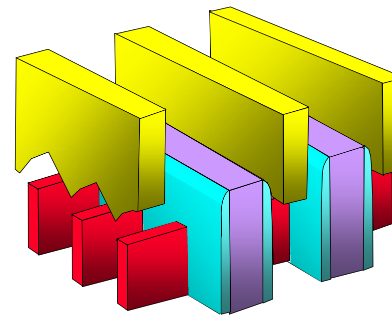


Resistance

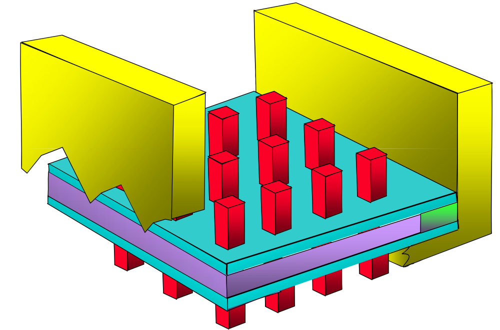
PARASITICS



UTB SOI



Fins

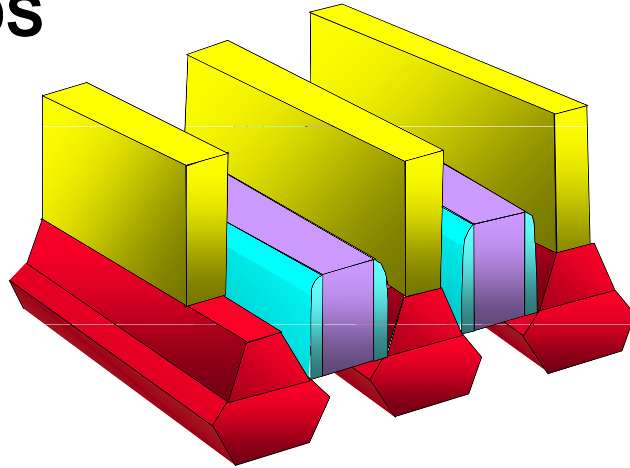


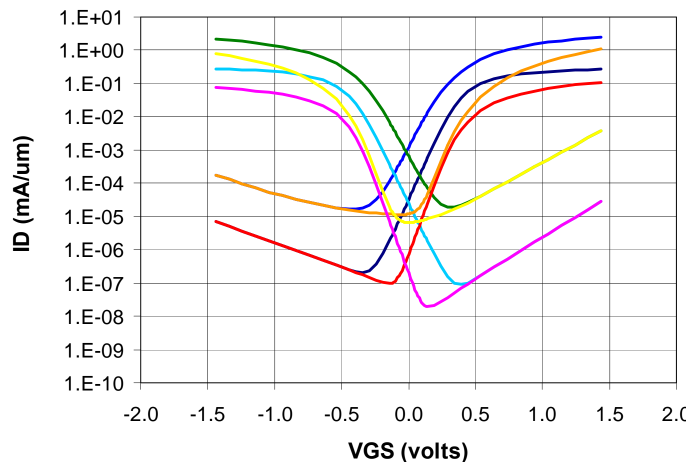
Wires/Dots

ELECTROSTATIC CONFINEMENT

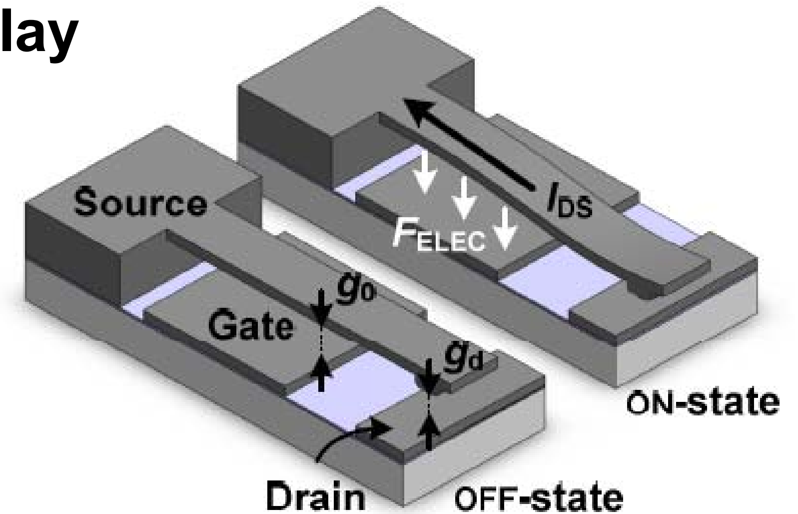
CMOS switch vs Relay switch

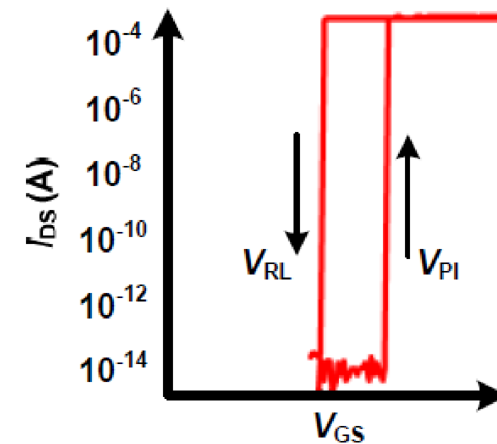
CMOS





3-T Relay

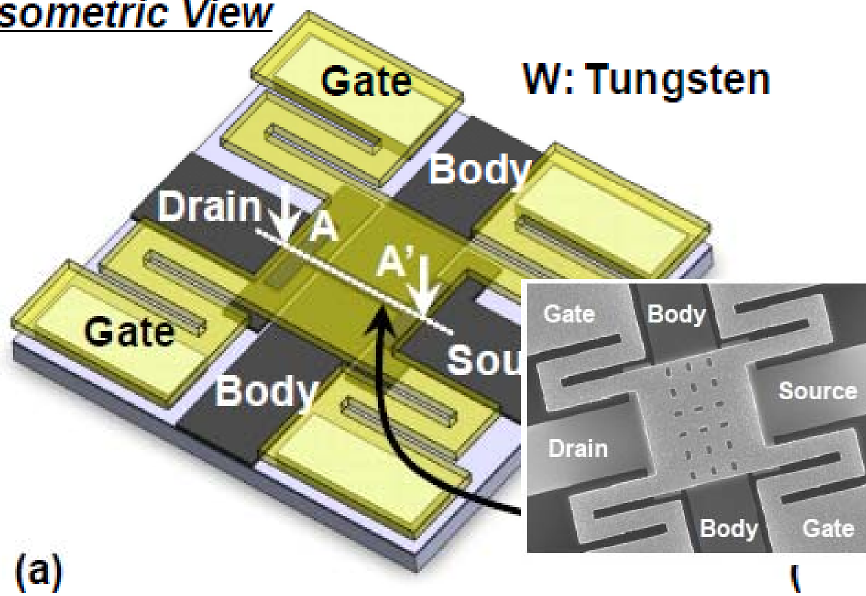


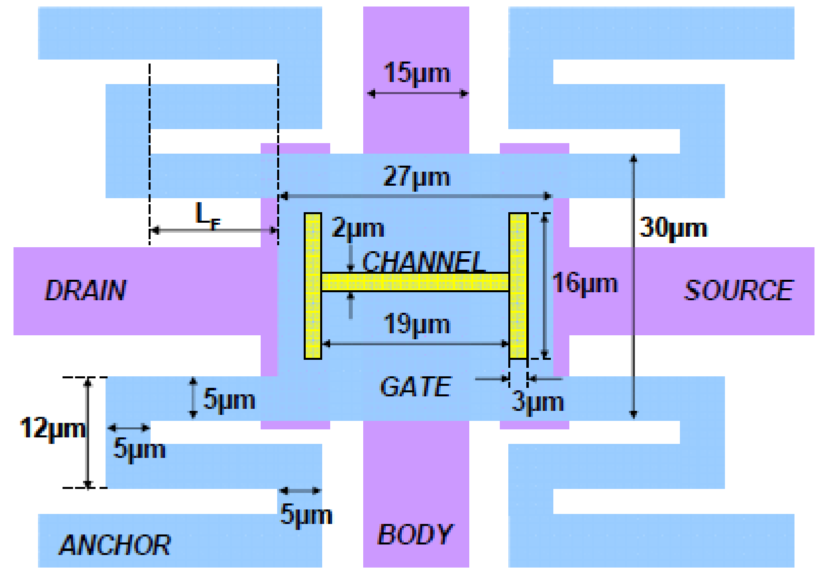


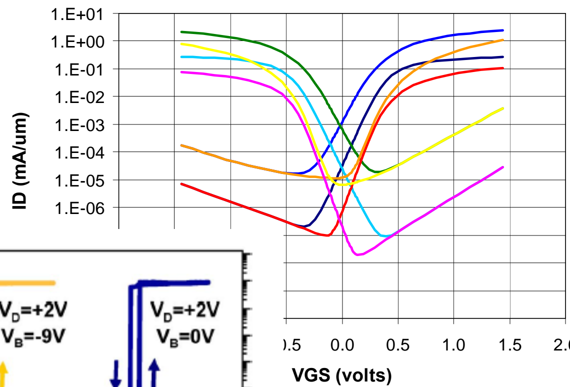
T.J. King-Liu IEDM 2010

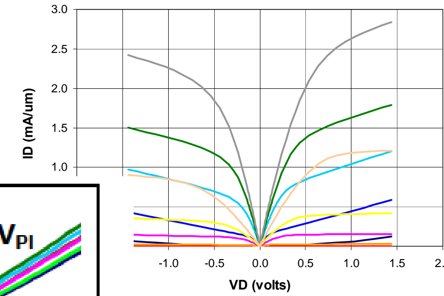
The attraction is infinite sub-threshold slope and zero Ioff

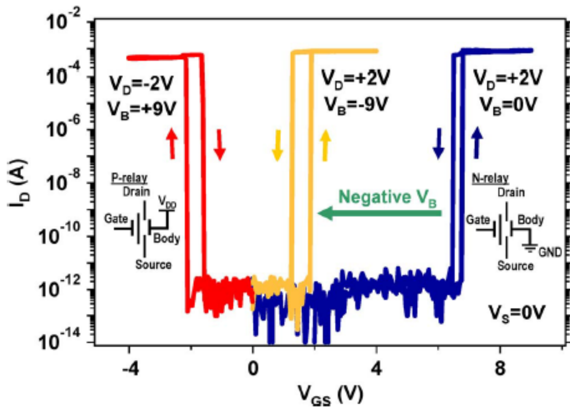
Pseudo-CMOS: 4-Terminal relay



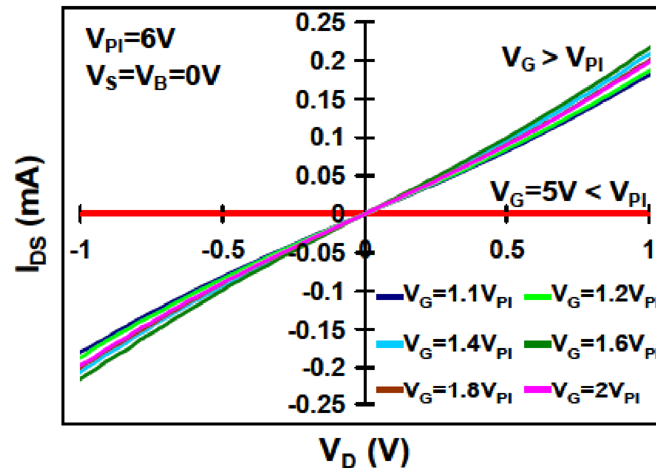








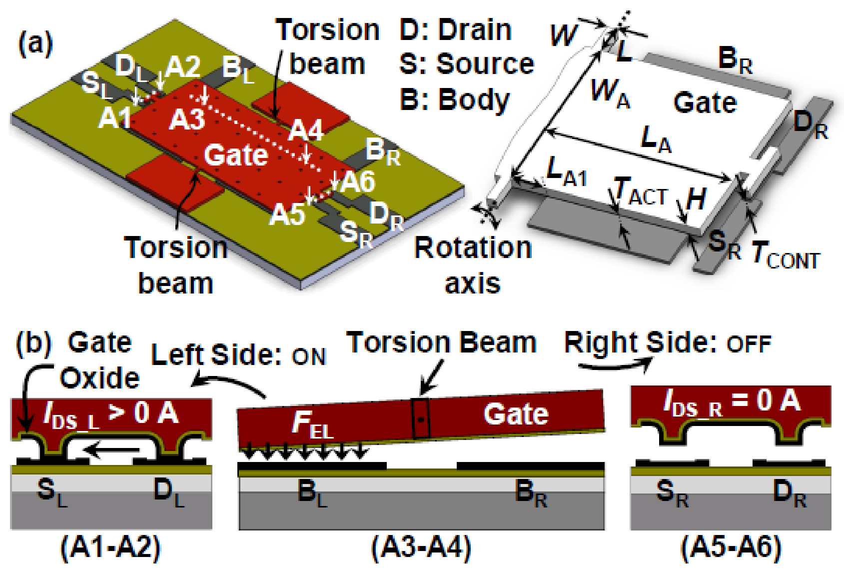
Infinite SS
700 uA/um @1V
Note Hysteresis

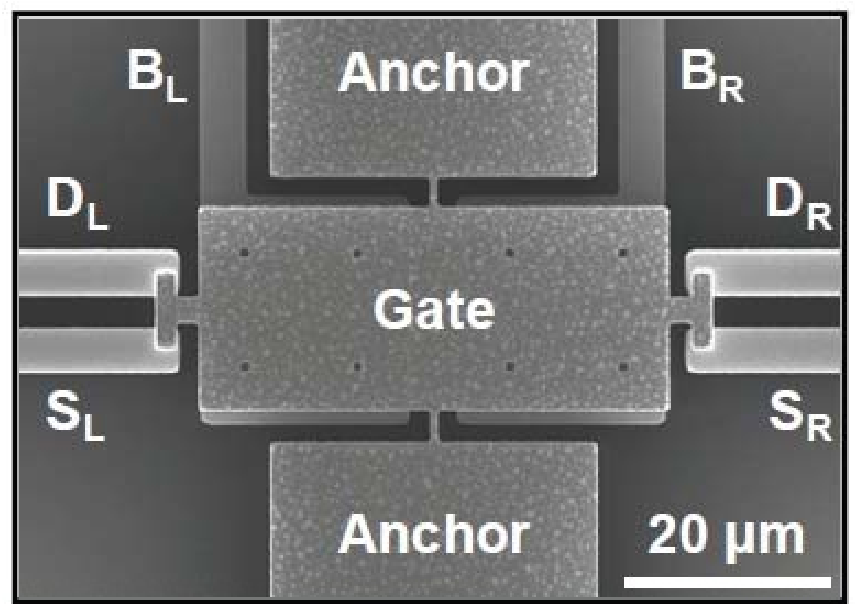


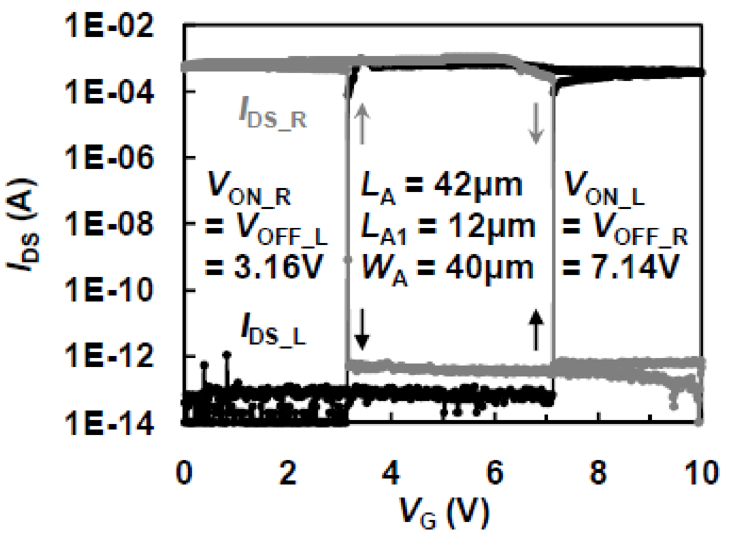
No saturation

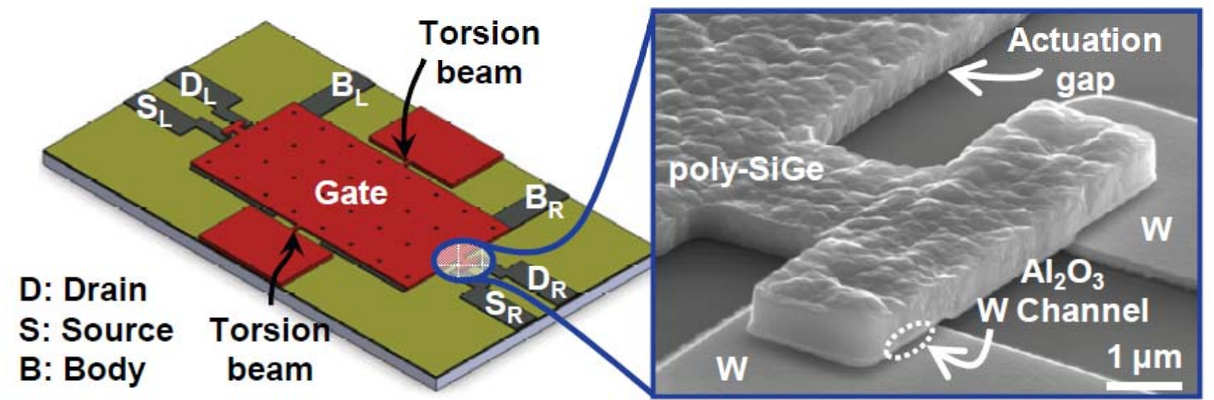
Liu IEDM 2010 / Nathanael IEDM 2009

4 -Terminal Relay vs See-saw Relay



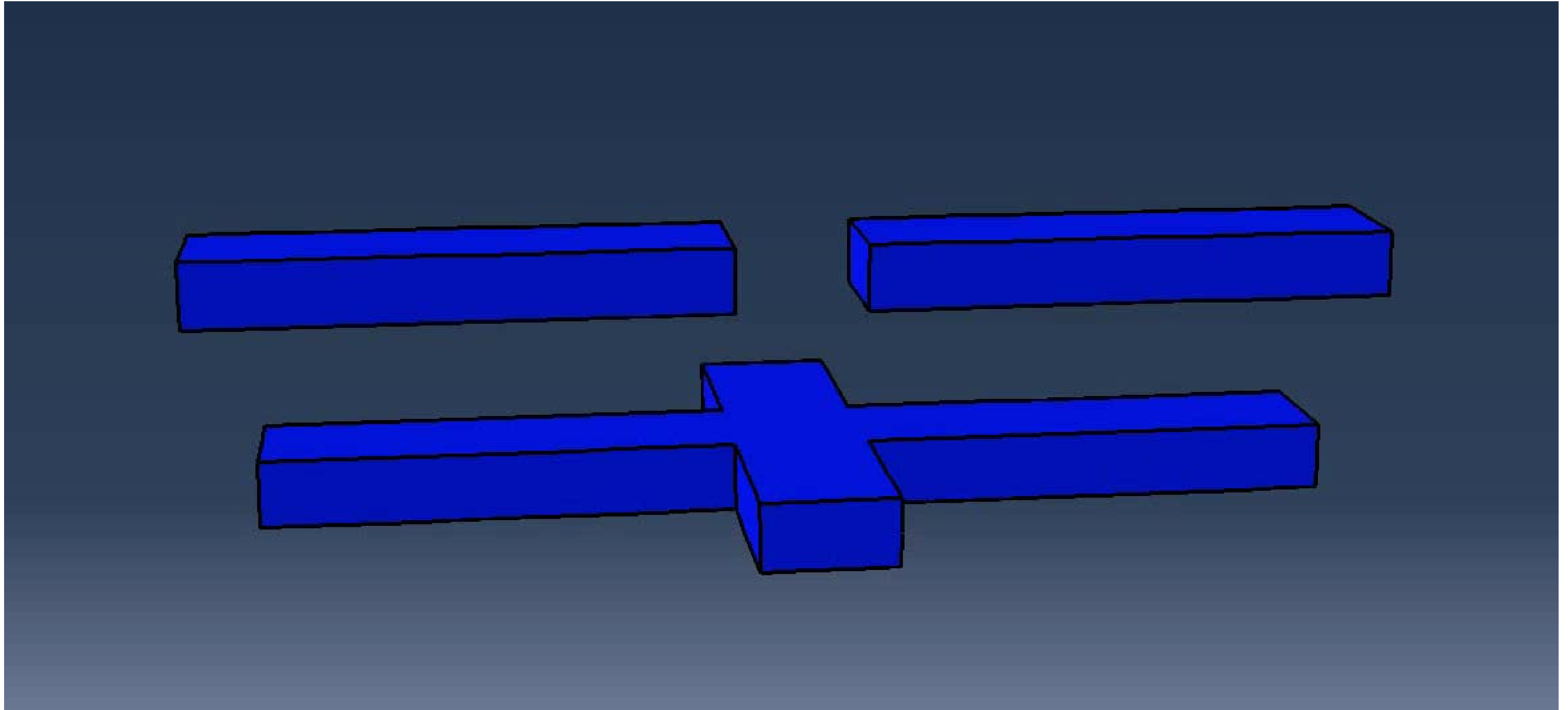




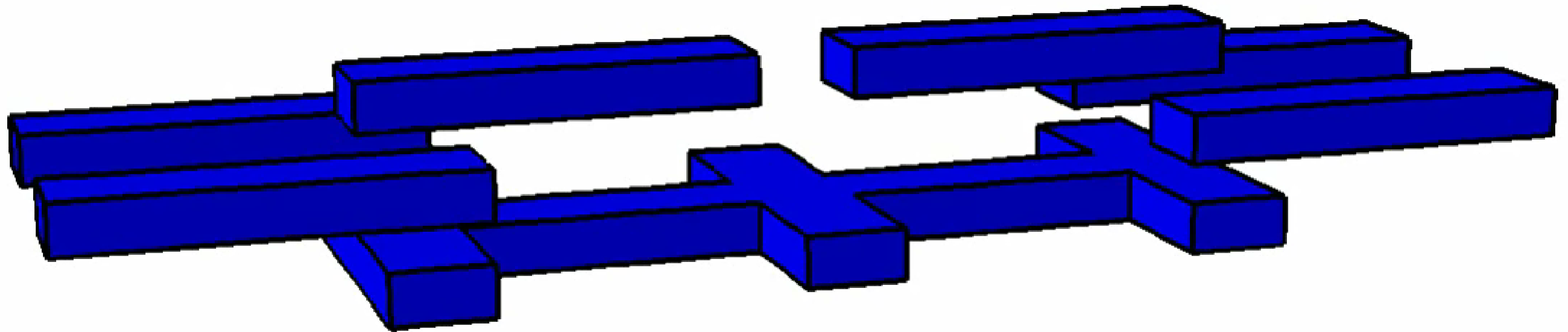


J. Jeon *et al., EDL, vol. 31, no. 4, pp. 371-373, Apr. 2010.*

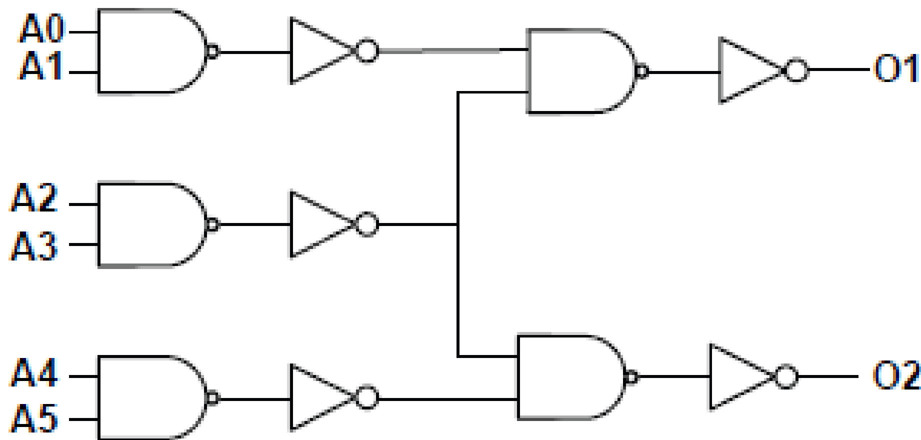
Simple See-saw Relay



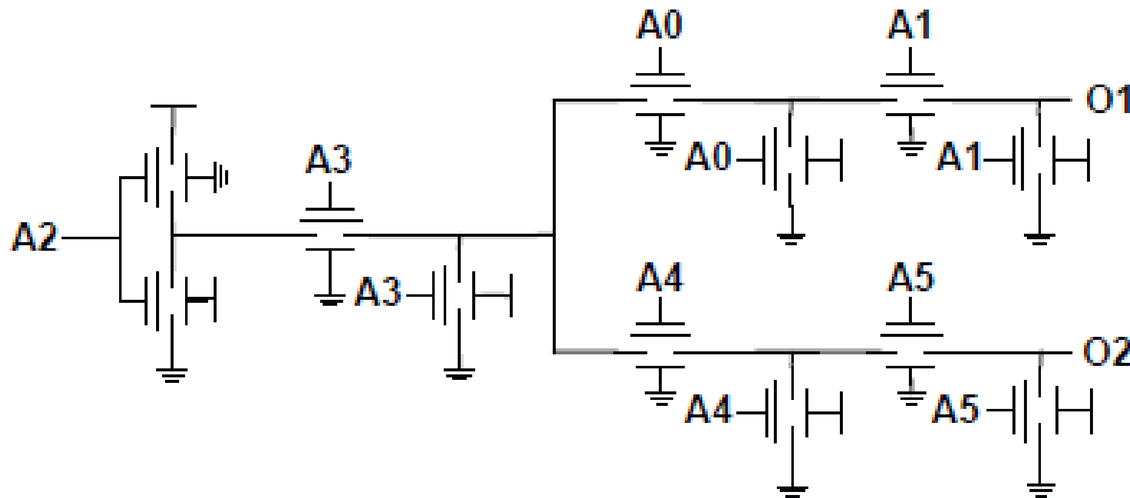
Device-like See-saw Relay



Circuit Design Trade-offs



4 gate delays:
More smaller devices



1 mechanical delay:
Fewer larger devices

Chen et al. ICCAD 2008

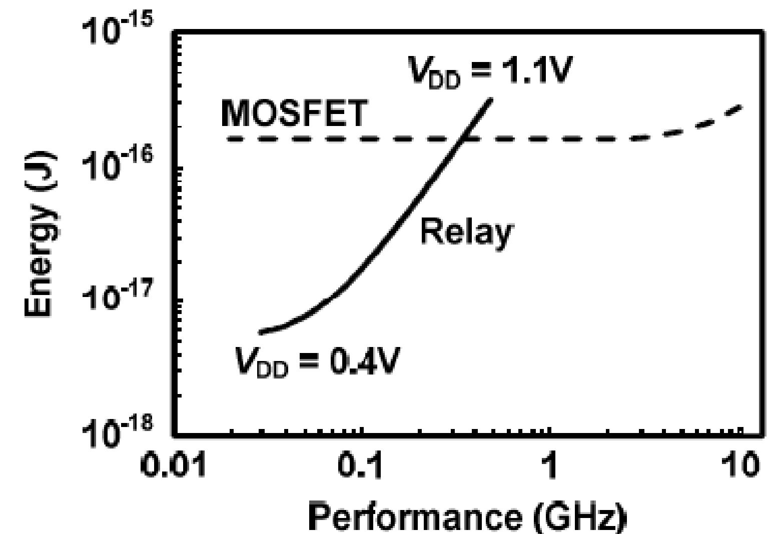
Relay Scaling Laws

TABLE I: ELECTROSTATIC RELAY SCALING THEORY. κ IS A SCALING CONSTANT GREATER THAN 1.

Relay Parameter	Constant Field Scaling
Spring Constant	$1 / \kappa$
Actuation Area	$1 / \kappa^2$
As-Fabricated Gap Thickness	$1 / \kappa$
Mass	$1 / \kappa^3$
Pull-In Voltage	$1 / \kappa$
Pull-In Delay	$1 / \kappa$
Switching Energy	$1 / \kappa^3$
Device Density	κ^2
Power Density	1

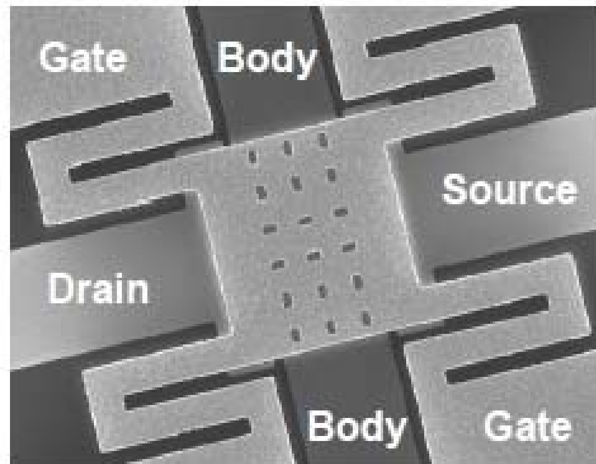
$$V_{\mathrm{PI}} \propto \sqrt{\frac{k g_0^3}{\varepsilon_0 W L}},$$

$$t_{\mathrm{PI}} \propto \sqrt{\frac{m g_{\mathrm{d}}}{k g_0}} \left(\frac{V_{\mathrm{PI}}}{V_{\mathrm{DD}}}\right),$$



Liu IEDM 2010 / Nathanael IEDM 2009

Relay (Liu/Chen – IEDM/ISSCC 2010)



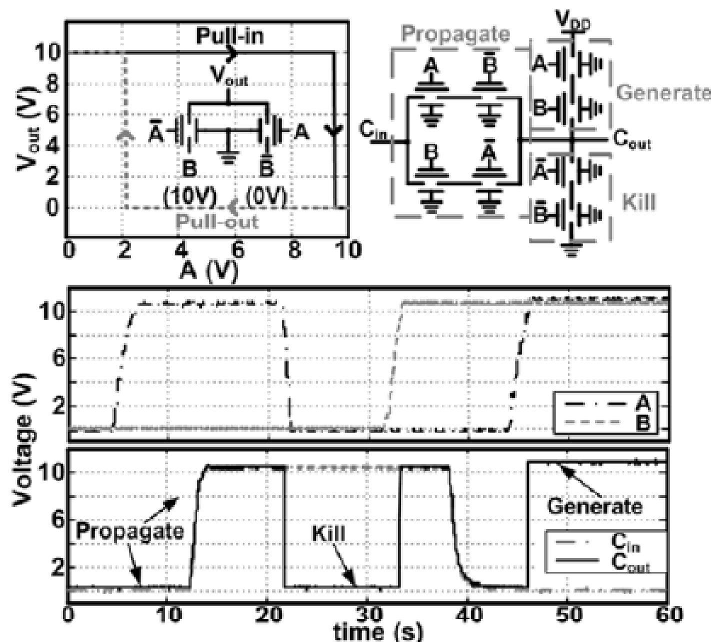


Figure 7.9.2: Schematic and measured VTC/transient waveforms for a MEM-switch based inverter and carry-generation circuit.

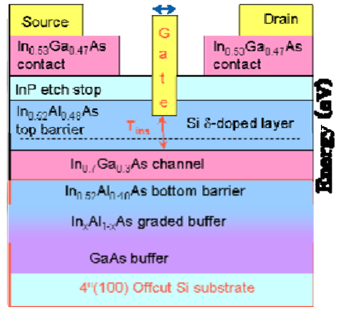
Benefits

- Abrupt / full-rail switching behavior (<< 60 mV/dec)
- Zero Ioff
- Low energy switching
- Compatible with conventional CMOS processes

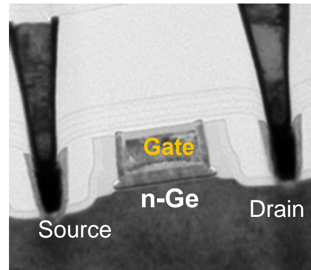
Challenges

- Slower than CMOS
- Reliability and stiction issues
- Hysteresis
- Mechanical delay >> electrical delay, requires change in circuit design (parallel/clocked)

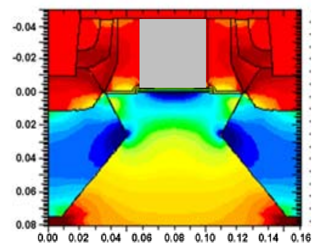
MOBILITY



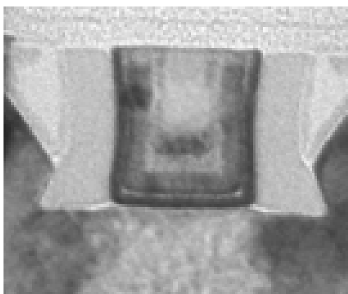
III-V



Ge

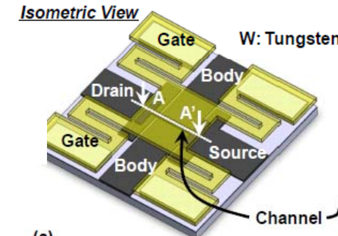


Strain

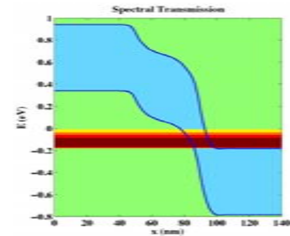


32nm

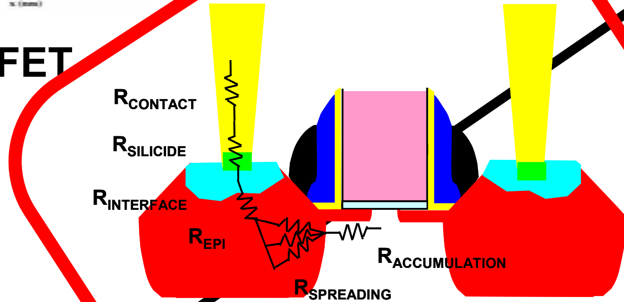
STRUCTURE



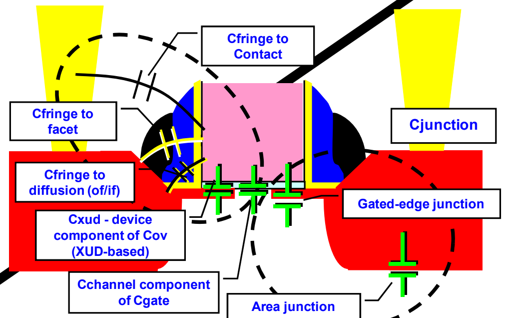
RELAY



TFET

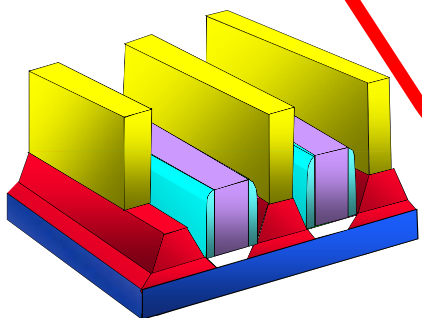


Resistance

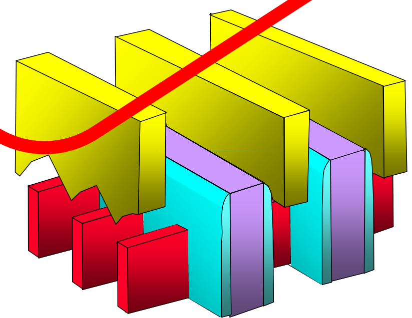


Capacitance

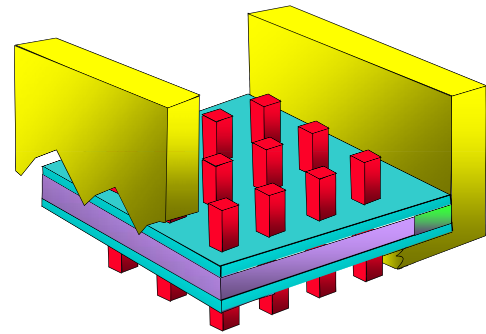
PARASITICS



UTB SOI



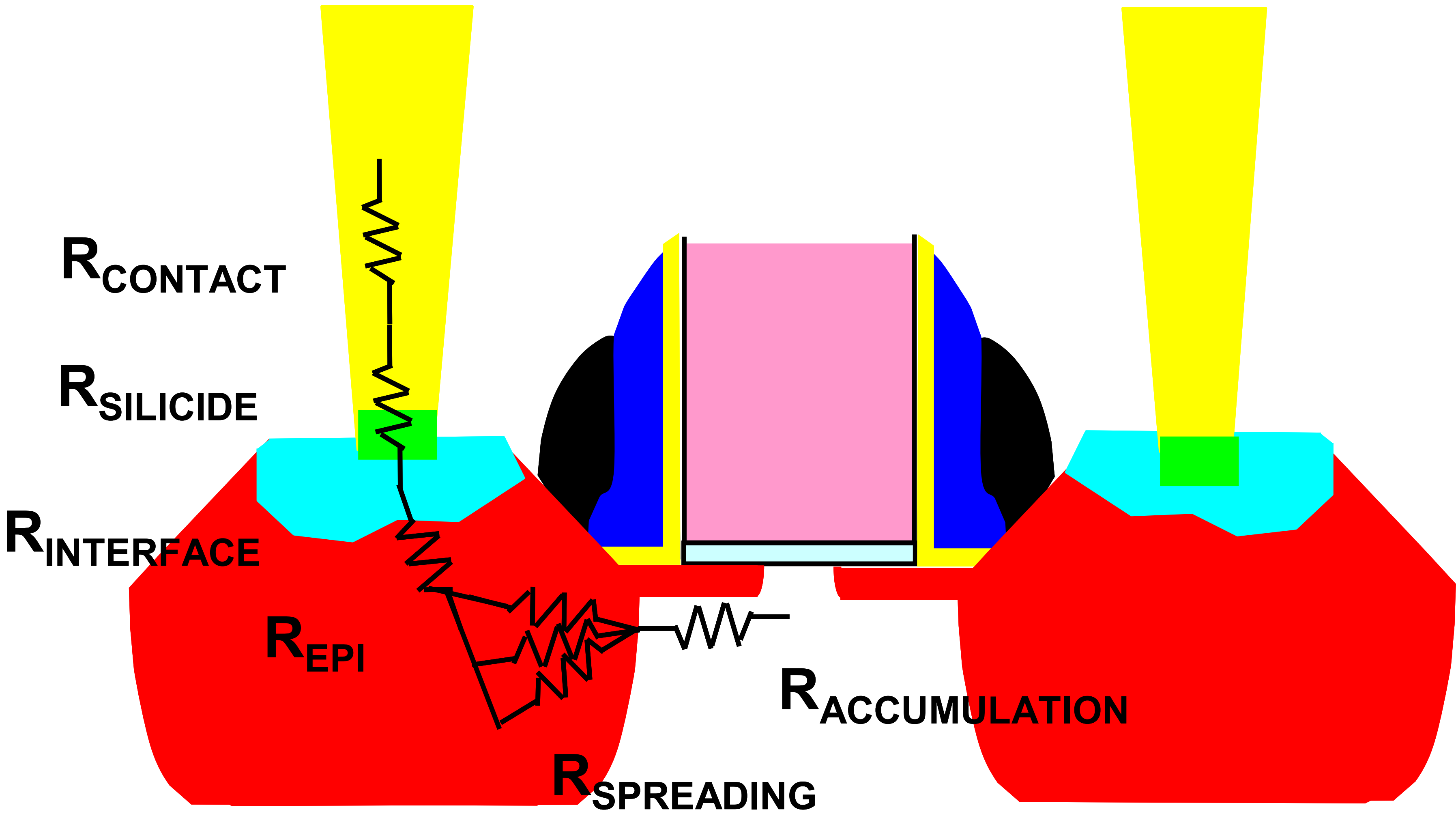
Fins



Wires/Dots

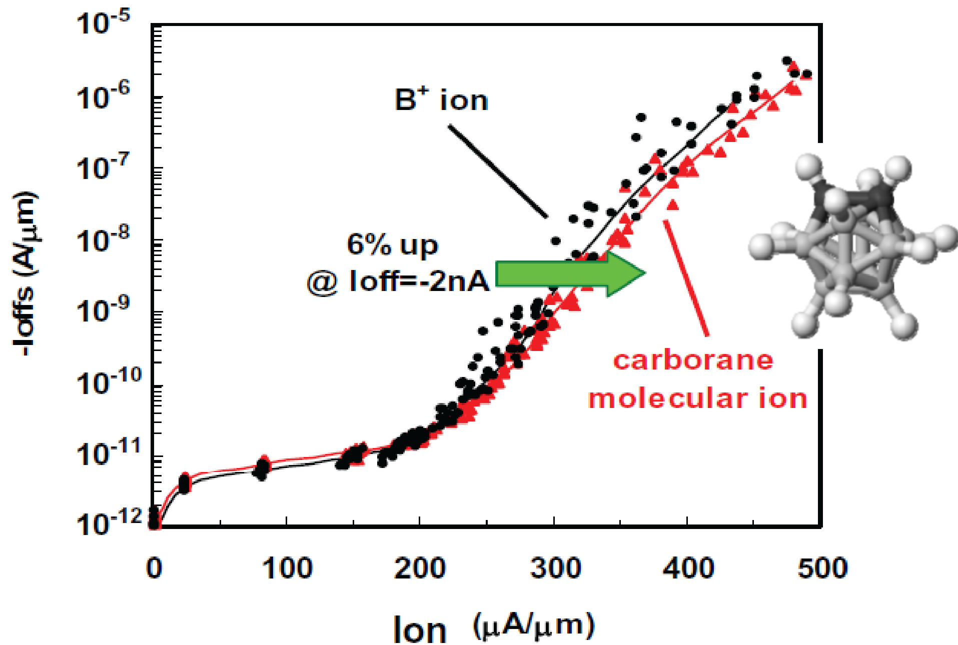
ELECTROSTATIC CONFINEMENT

Planar Resistive Elements

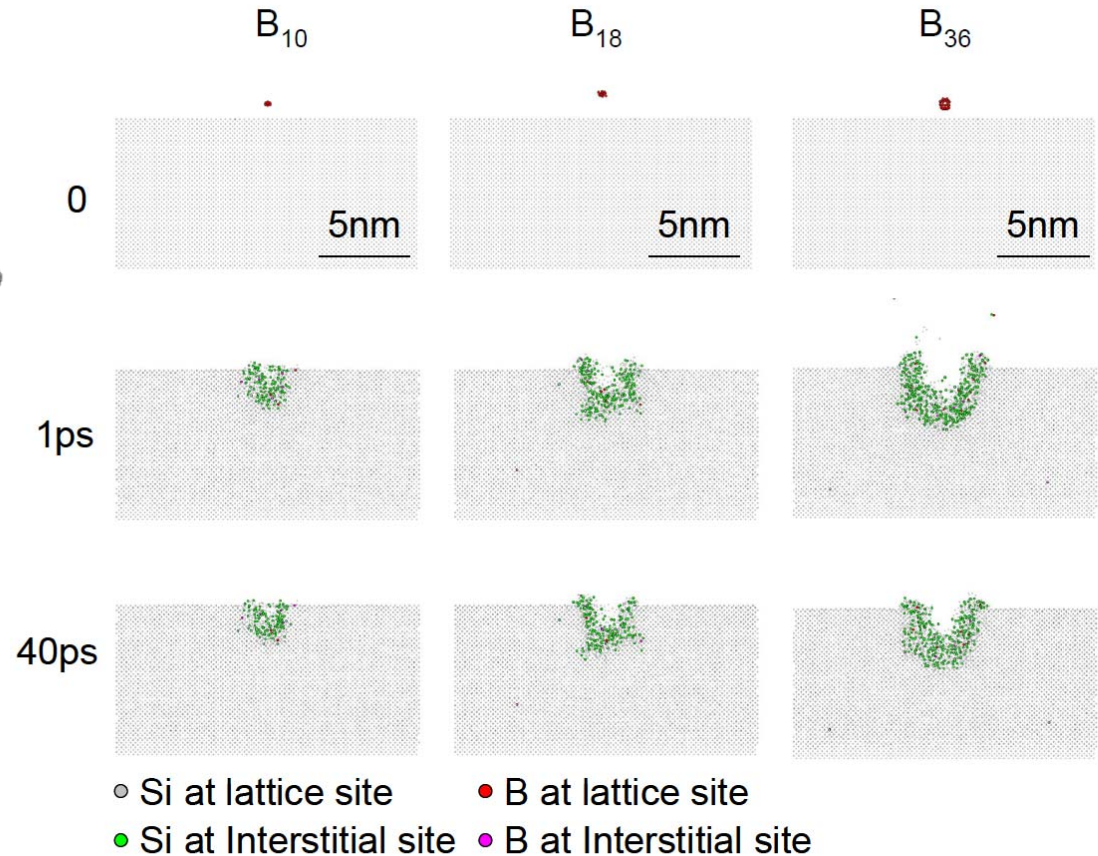


Kuhn, Intel, IEDM SC 2008

Implant goal: ever smaller X_J with improved R_{acc}



Carborane - C2B10H12
(From Renau, IWJT 2010)

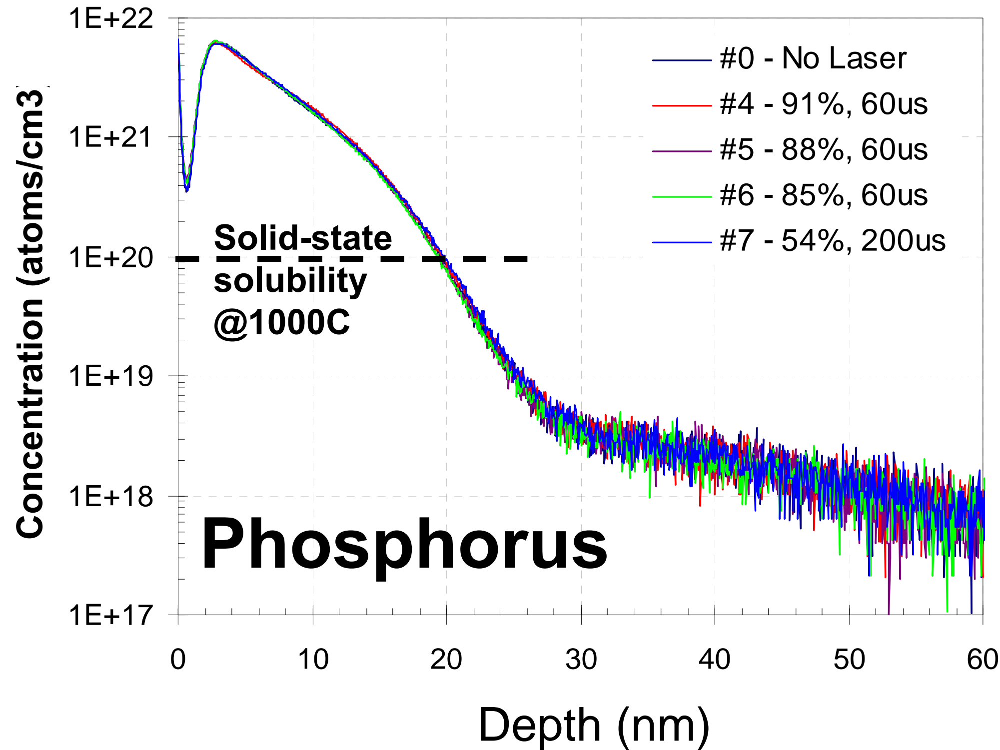


Modeling (Aoki, IWJT 2010)

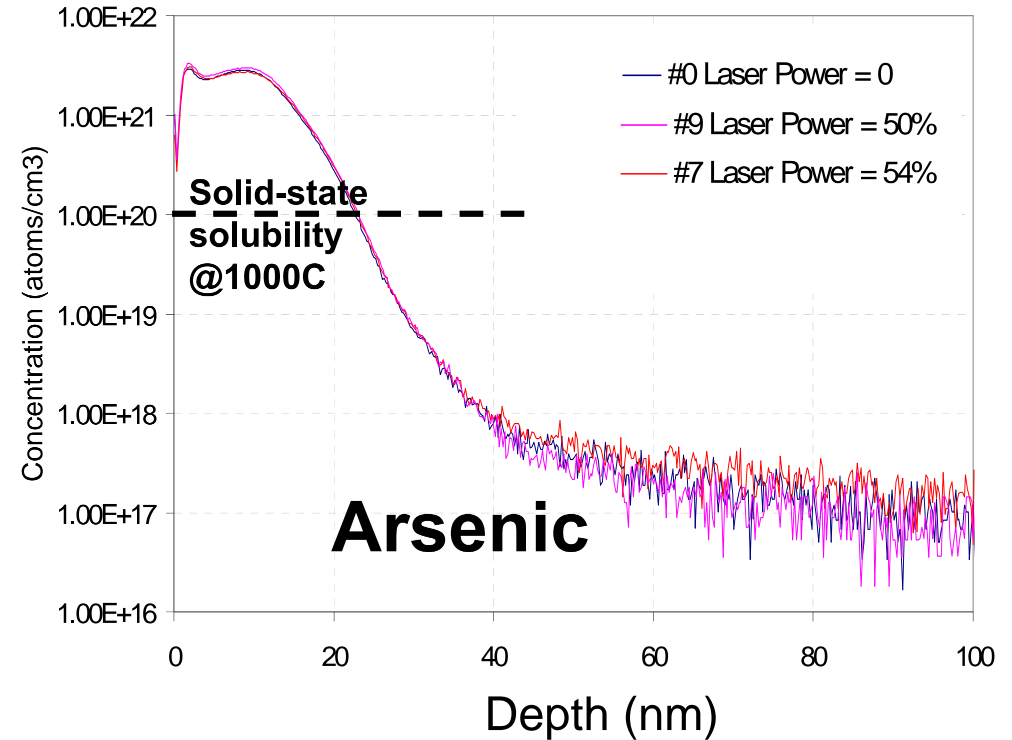
Molecular implants for simultaneous X_J and R_{acc} reduction

Anneal goal: activate and freeze implants in place

Junction depth = 26 nm
Sheet resistance = 150 W/sq



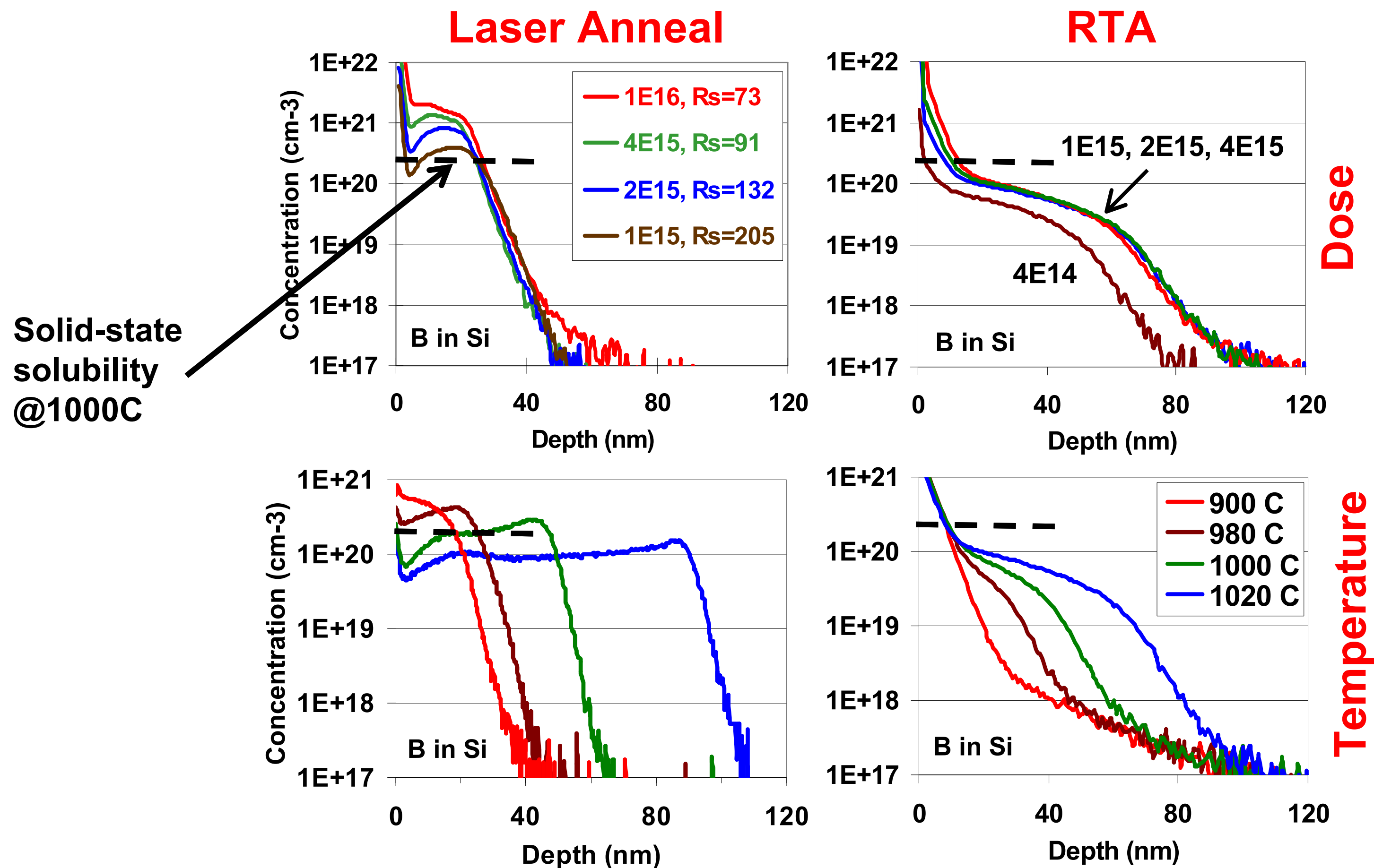
Junction depth = 28 nm,
Sheet resistance = 150 W/sq



Submelt anneal freezes atoms in place for simultaneous X_J and R_{acc} reduction

Kuhn – IWJT 2010

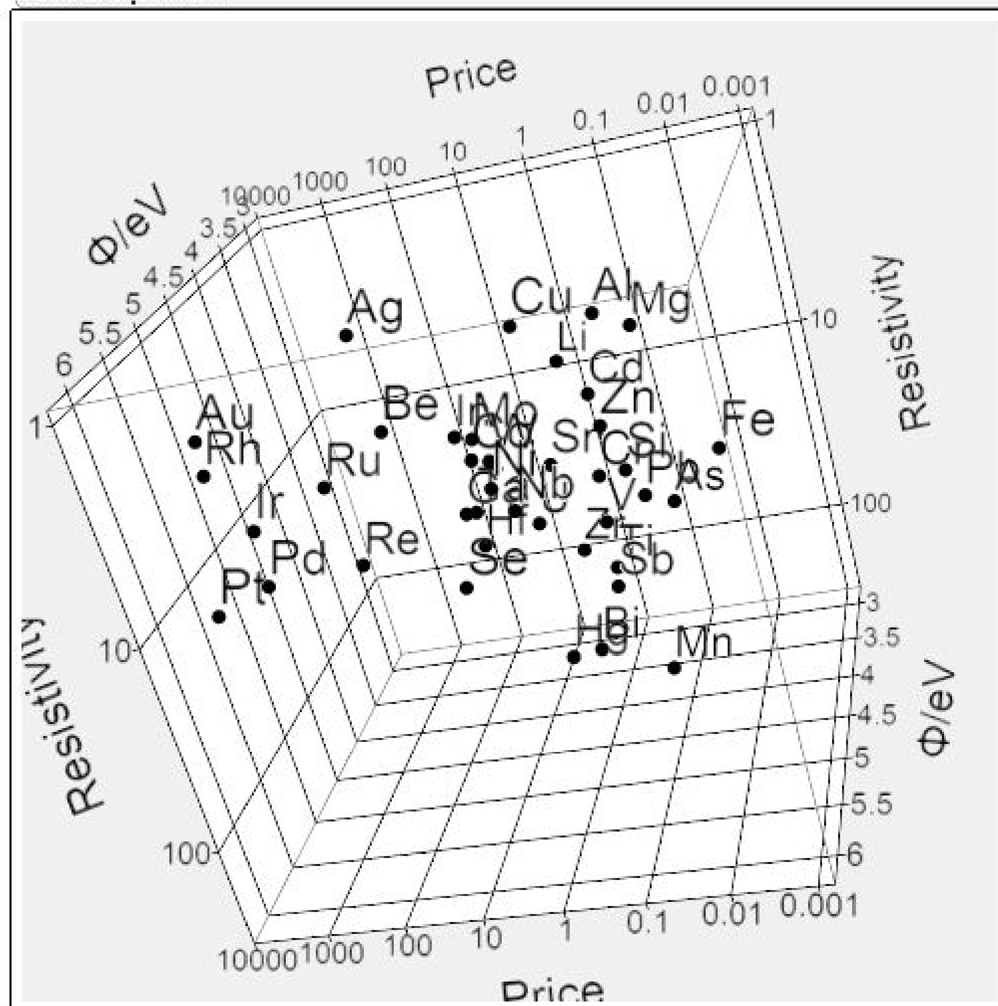
Anneal goal: Superactivation by Solid-phase epitaxial regrowth (SPER)

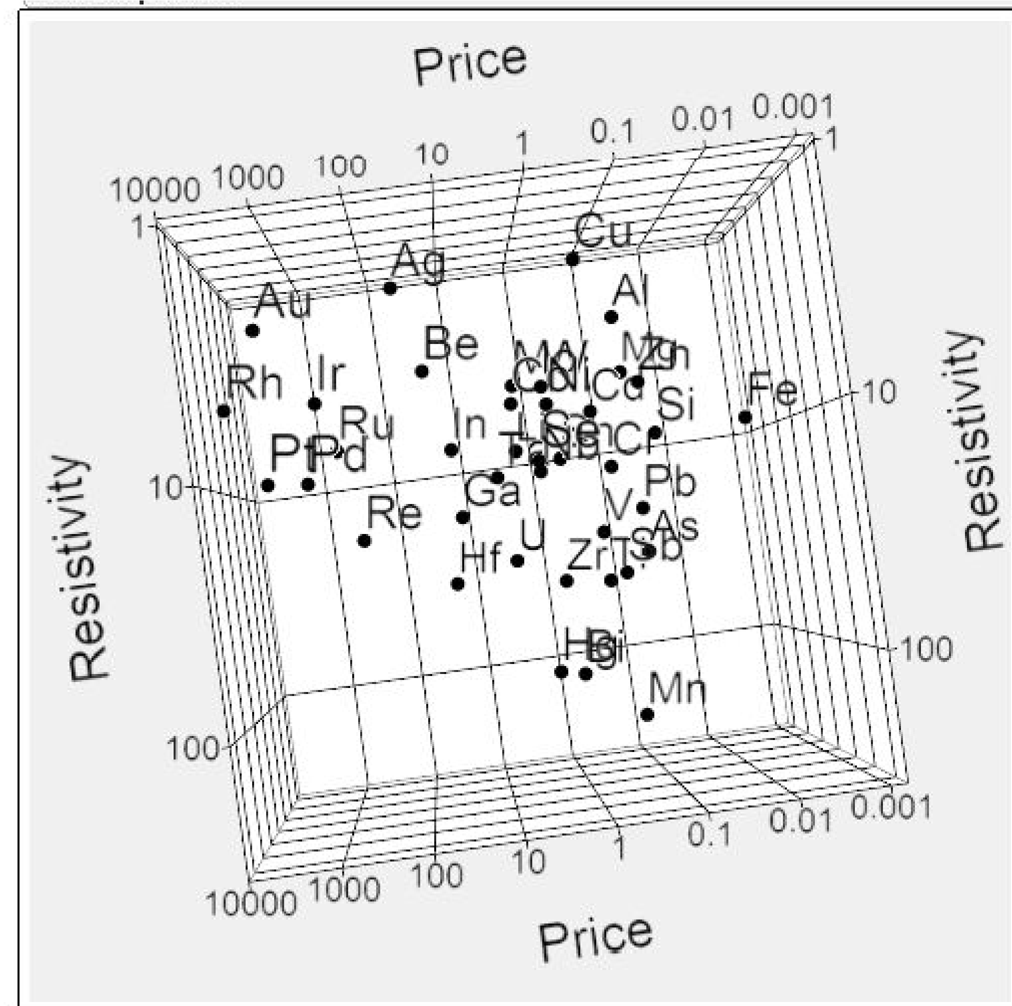


Laser melt anneal vs RTA, showing increased abruptness and non-equilibrium enhanced activation (superactivation)

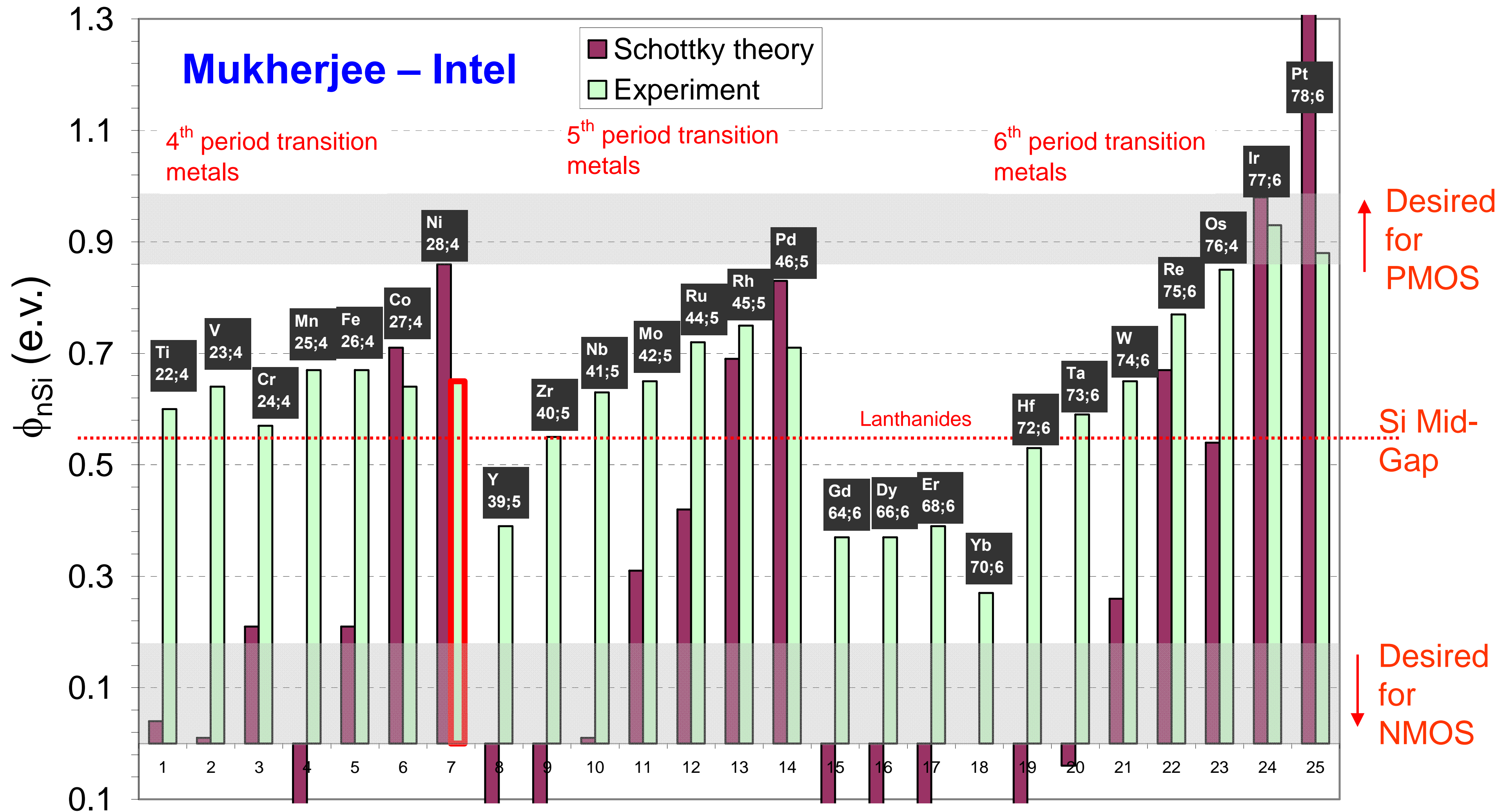
Kuhn – IWJT 2010

Properties of the Elements





Schottky theory vs. experimental SBHs for metals on nSi



Fermi level pinned to mid-gap for most metals on Si

Kelin Kuhn SEMATECH 8th Int'l Sym. on Adv. Gate Stack Tech. 2011

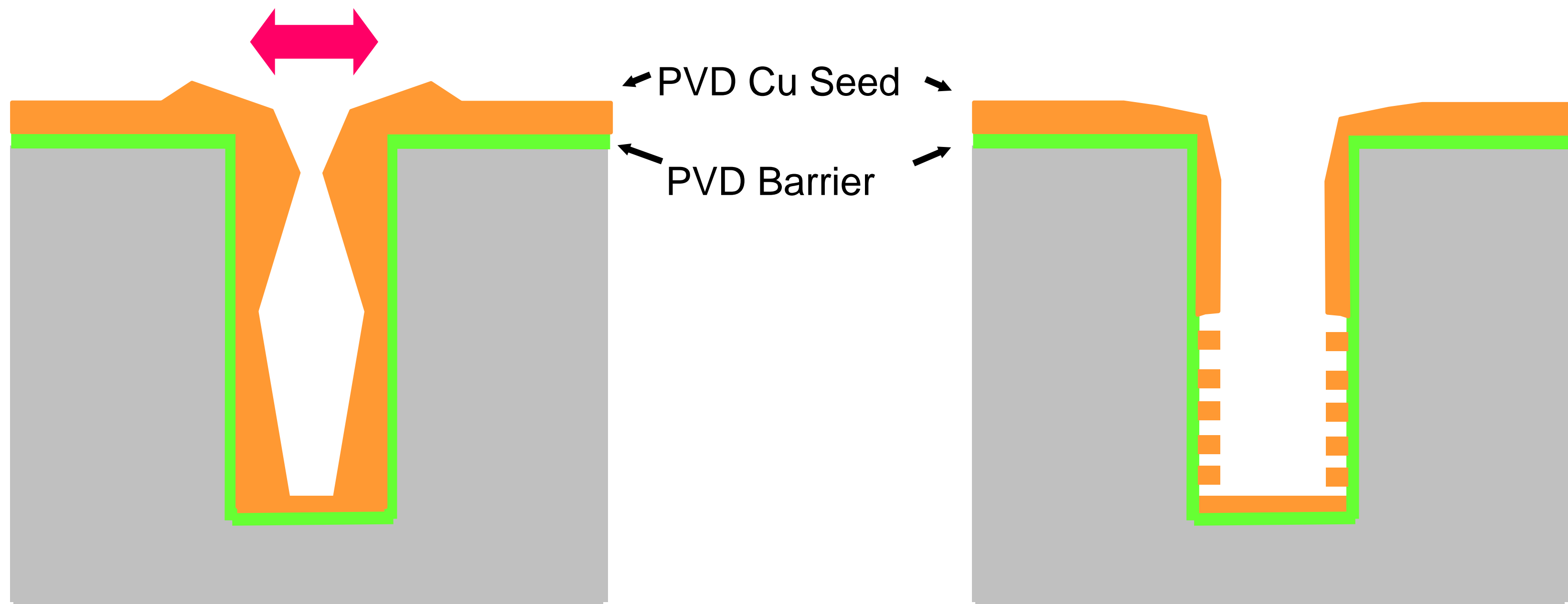
Challenges of PVD

PVD Cu seed lead to overhang and pinch off:

No opening to plate

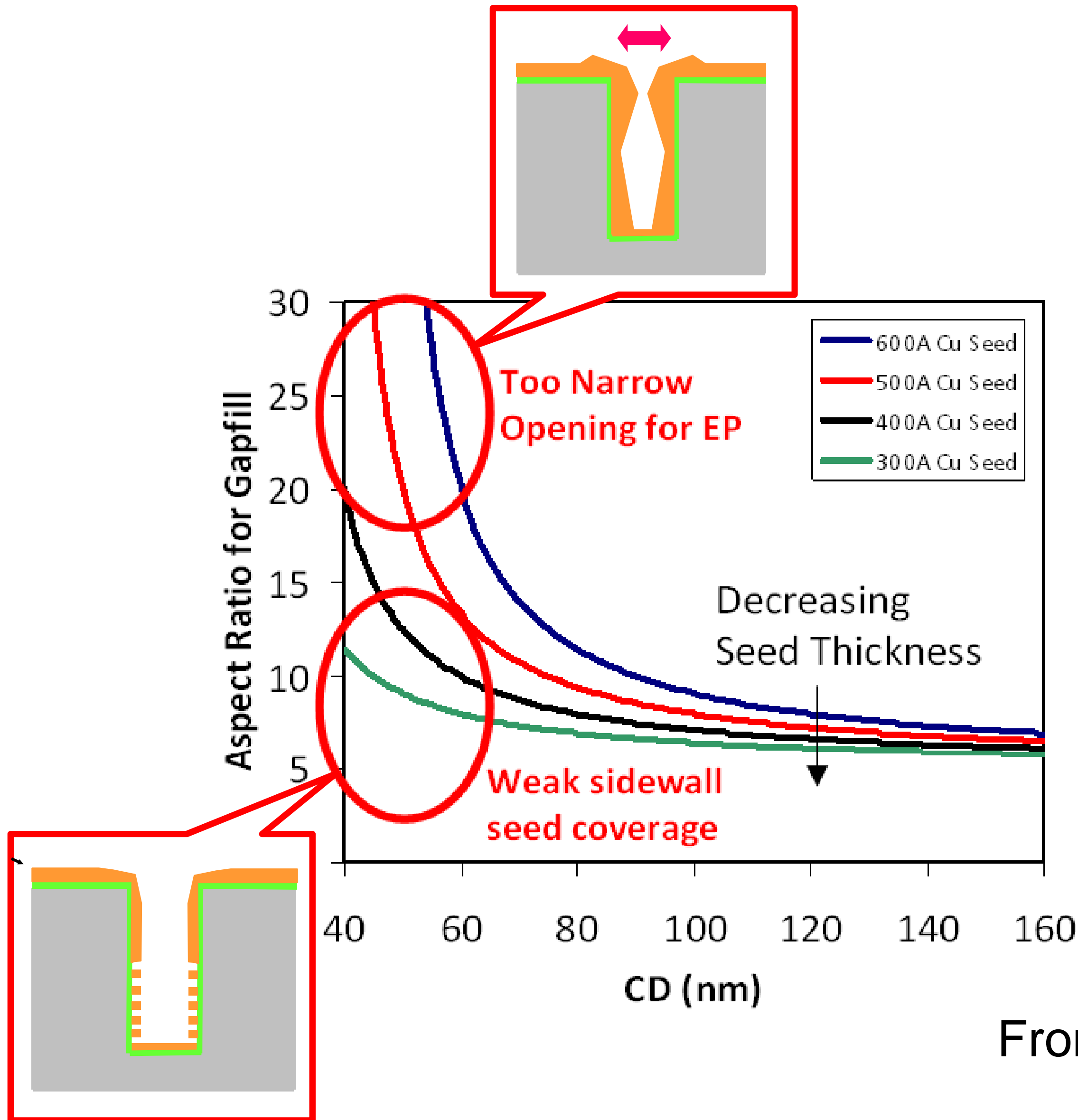
Thin seed leads to discontinuities:

Plating terminal effect and barrier oxidation



From J. Clarke, Intel

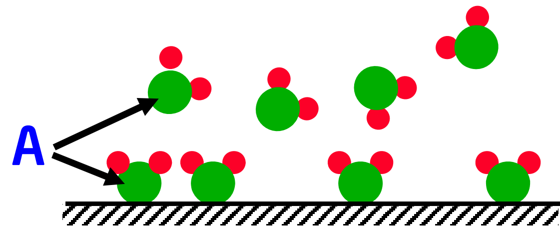
Limitations of PVD

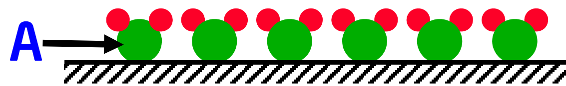


From J. Clarke, Intel

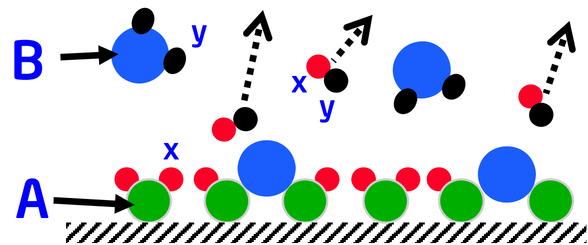
Scalability below 30 nm is challenging

Crafting Films with Atomic Layer Deposition

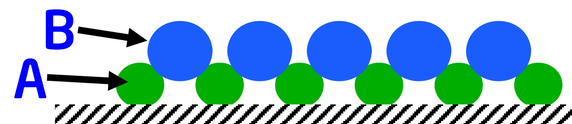




Self-limiting coverage = thickness precision
Potential for high selectivity



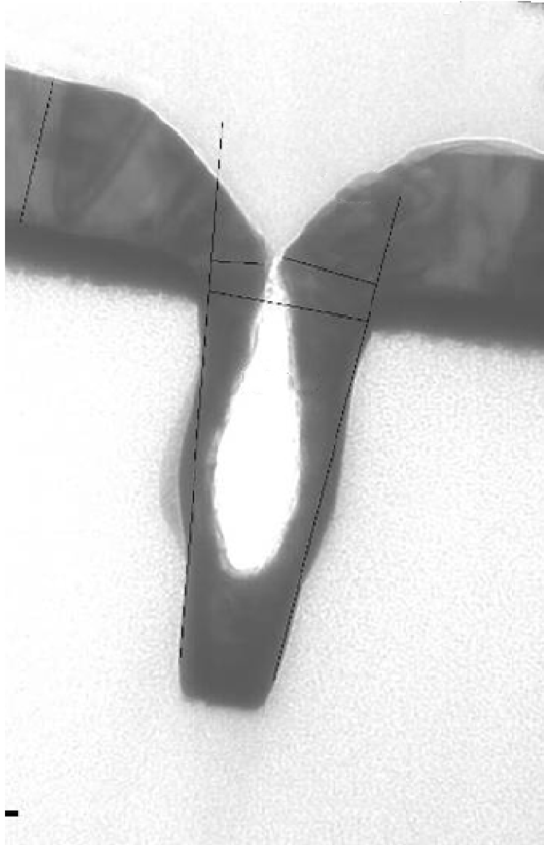
Wide variety of potential co-reactants
Build desired chemical structure in place



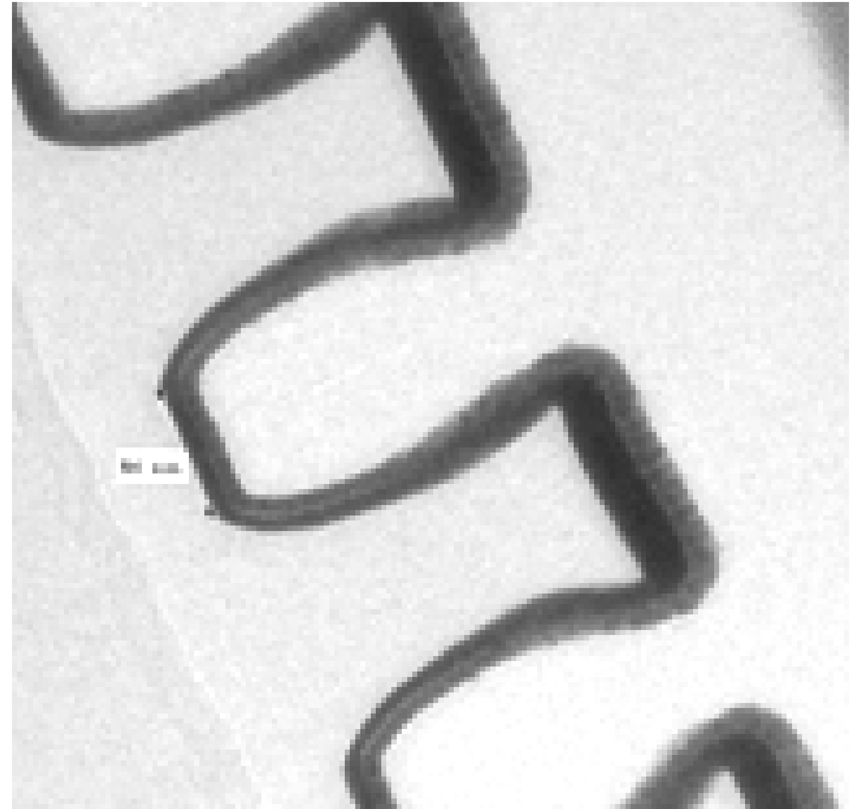
Robust films at much lower thermal budget

Kelin Kuhn SEMATECH 8th Int'l Sym. on Adv. Gate Stack Tech. 2011

PVD versus ALD

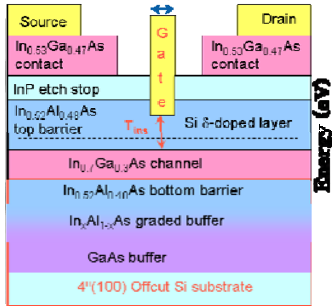


PVD Seed
Overhang

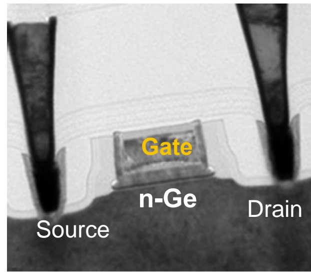


ALD Seed
Conformal

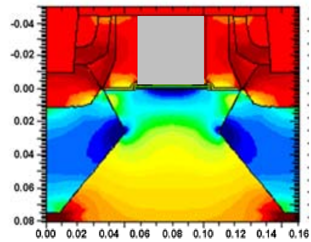
From J. Clarke, Intel

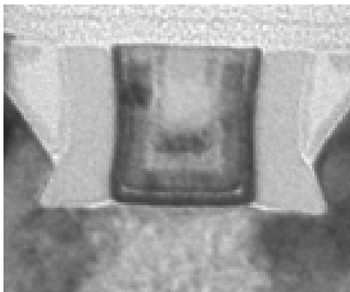


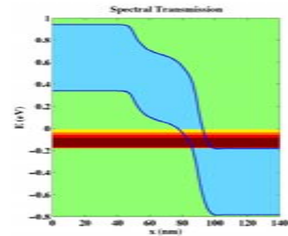
III-V



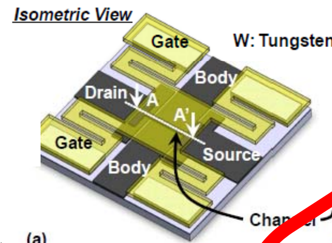
Ge


Strain

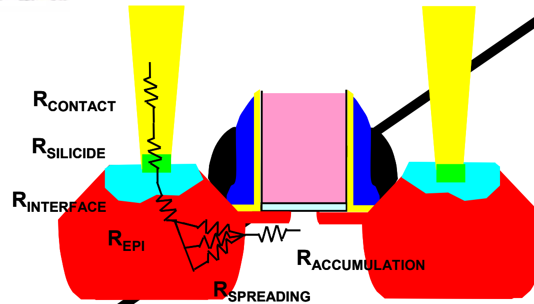

32nm



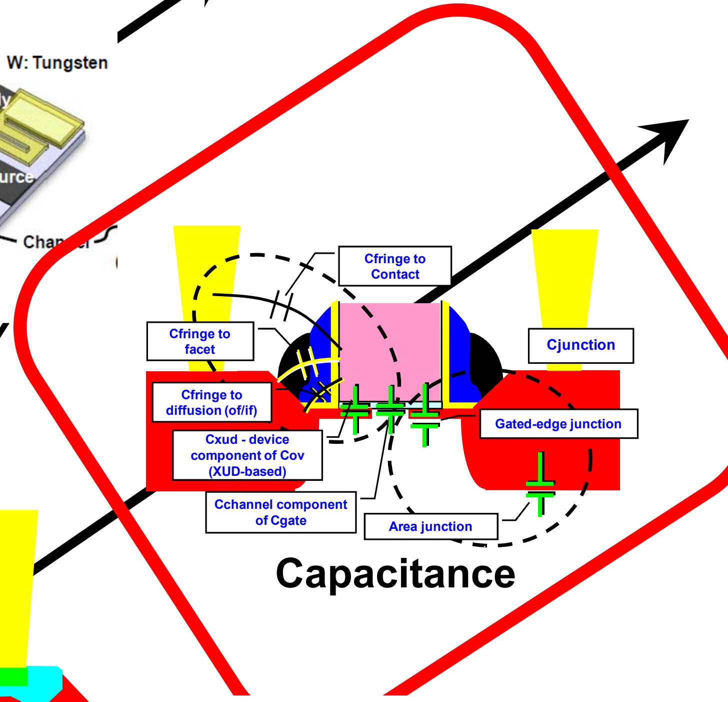
TFET



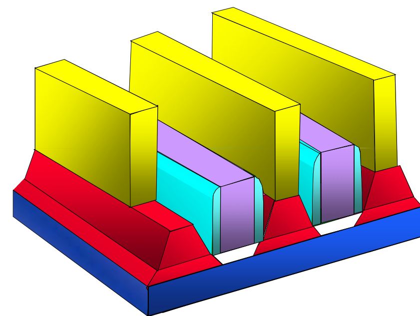
RELAY

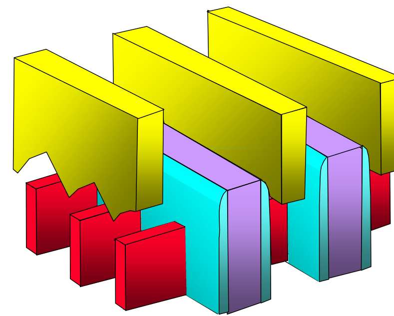


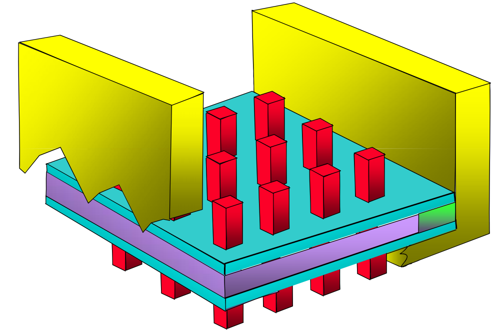
Resistance



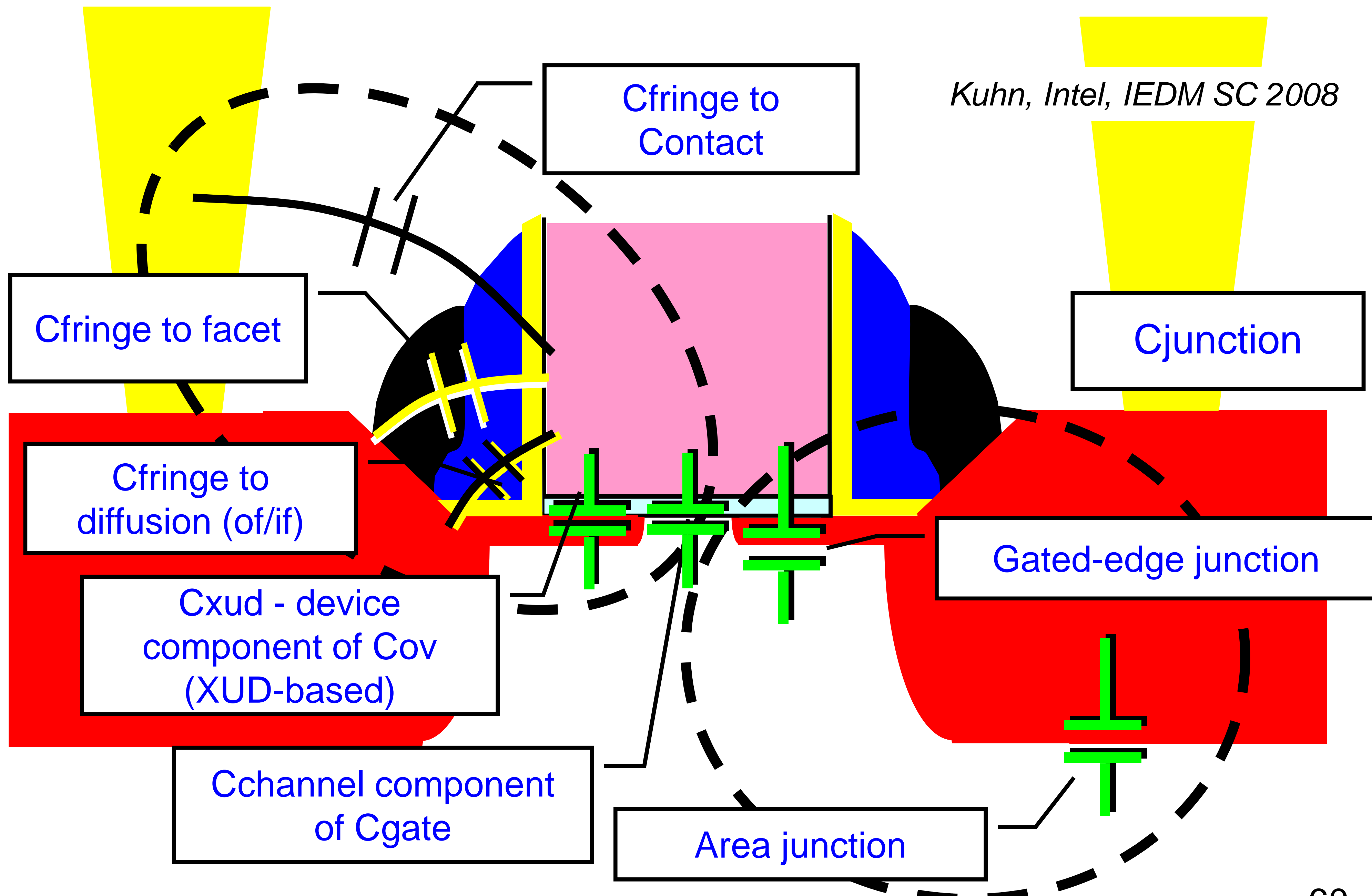
Capacitance


UTB SOI

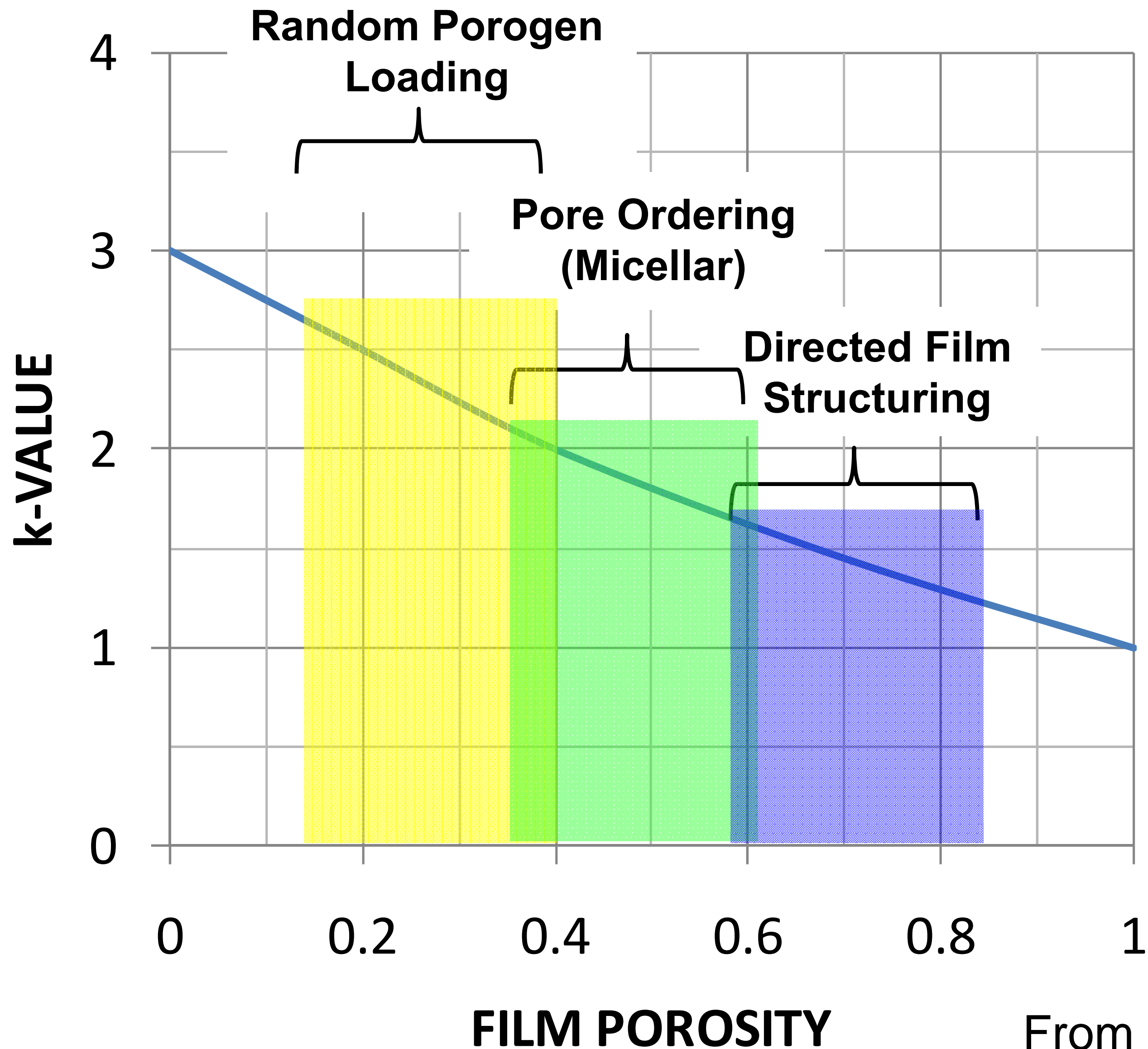

Fins


Wires/Dots

Planar Capacitive Elements

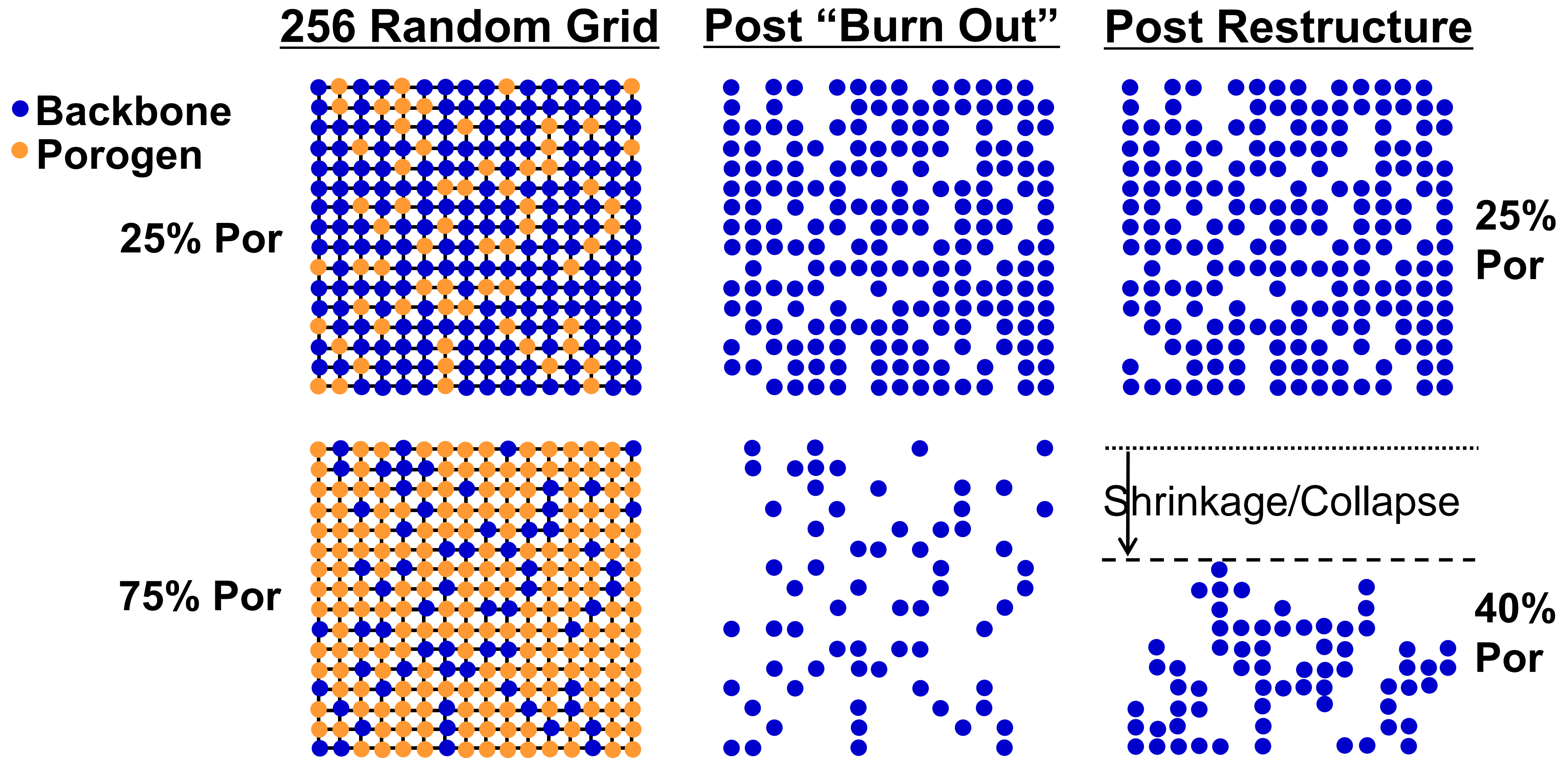


Low-k driven by porosity



From J. Clarke, Intel

Percolation Threshold: 2D Grid Example



Calculations for 3D (4 Coord): Percolation Threshold at 57% Porosity

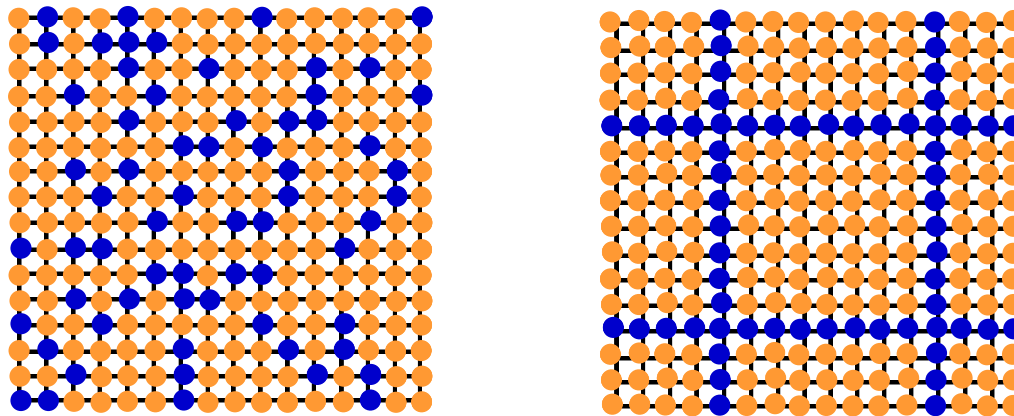
Theoretical Limit Exists For Random Co-Mixing

From J. Clarke, Intel

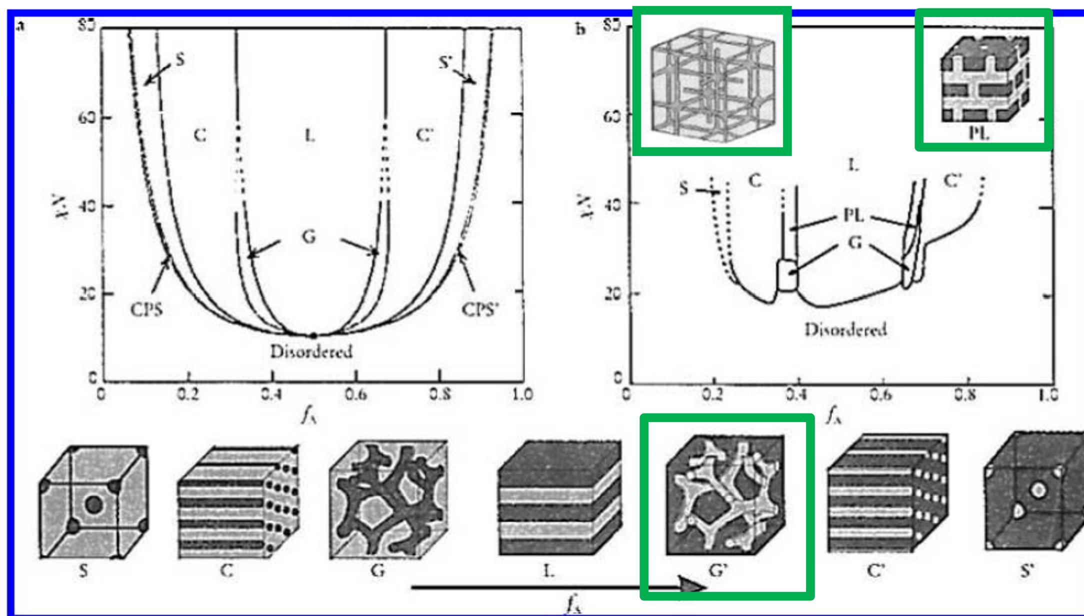
Towards "Directed" Dielectrics

2D

75% Por



3D



Structural Control is Critical

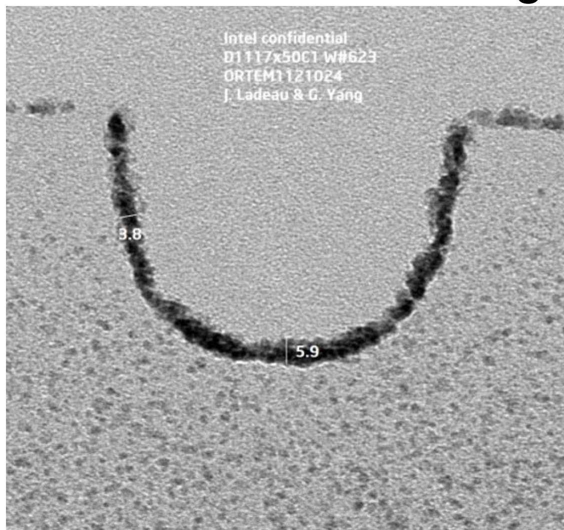
Kim et. al., *Chem. Rev. 2010, 110, 146–177*

From J. Clarke, Intel

Pore Sealing

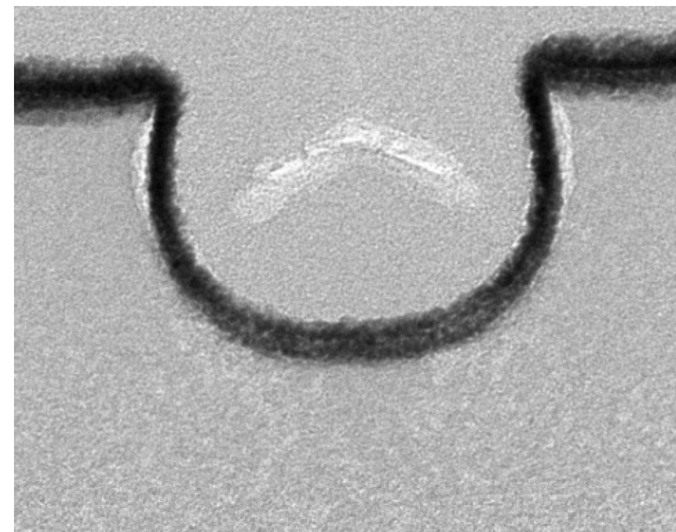
Like trying to deposit a gas onto the surface (but not into the bulk) of a sponge.

ALD Liner Dep on a Porous ILD: No Pore Sealing



ALD Precursor fully penetrates the ILD and decorates the pore structure.

With Pore Sealing



No Penetration into the ILD

Continual struggle of thin ALD with films of increasing porosity. Strive for no degradation in capacitance or reliability.

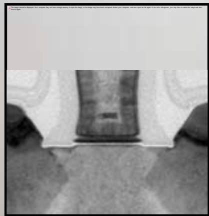
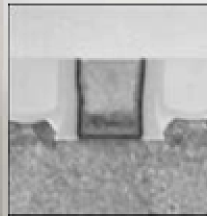
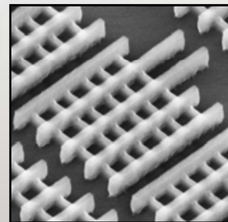
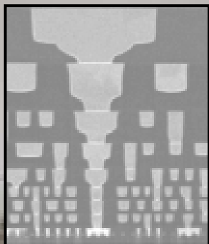
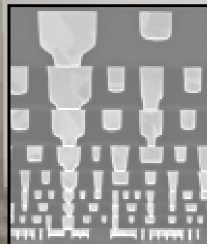
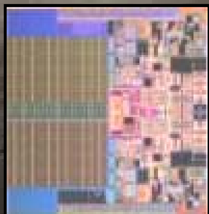
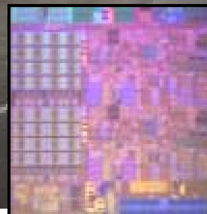
From J. Clarke, Intel

Limit to visibility remains ~ decade

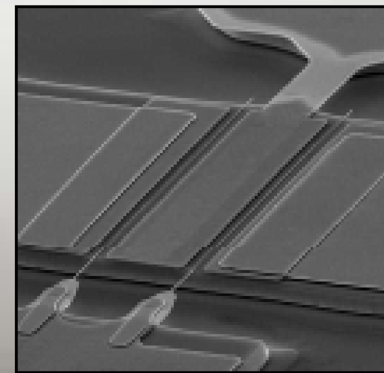
TECHNOLOGY GENERATION

45nm 2007	32nm 2009	22nm 2011	14nm 2013	10nm 2015	7nm 2017	Beyond 2020

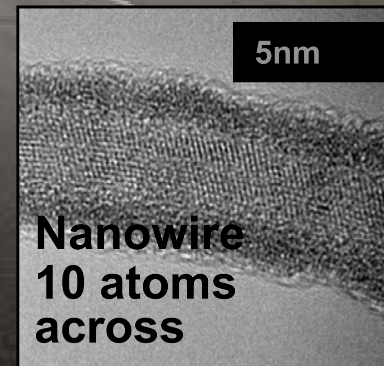
MANUFACTURING — DEVELOPMENT — RESEARCH

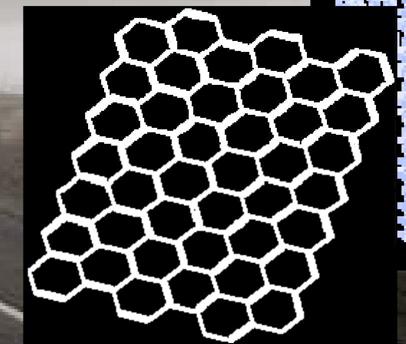
Not to scale



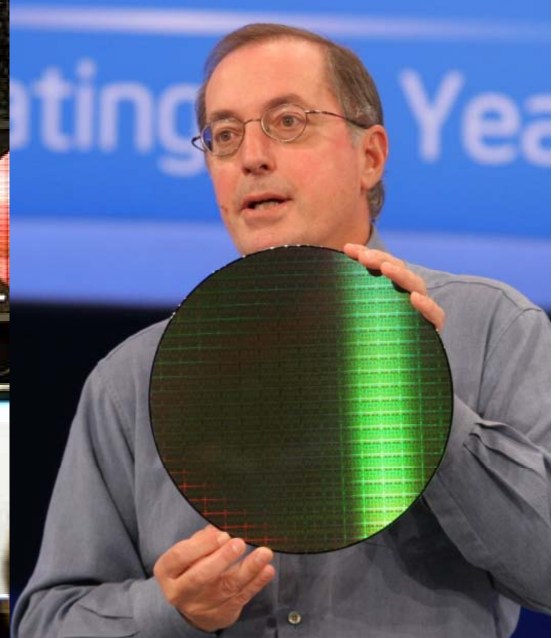
QW III-V Device



Carbon Nanotube ~1nm diameter



Graphene
1 atom thick



Q&A