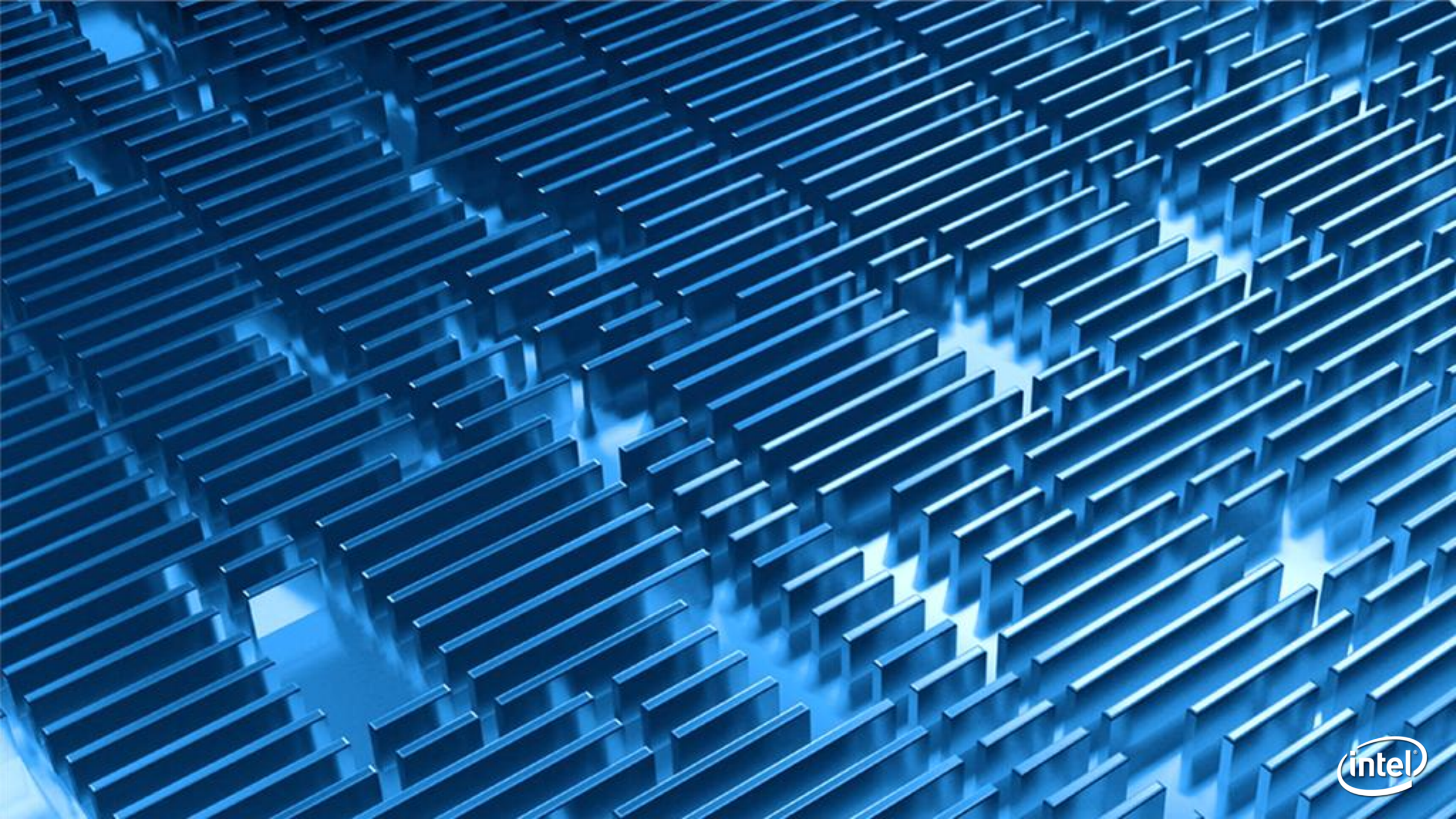
# Risk Factors

- Today's presentations contain forward-looking statements. All statements made that are not historical facts are subject to a number of risks and uncertainties, and actual results may differ materially. Please refer to our most recent Earnings Release and our most recent Form 10-Q or 10-K filing for more information on the risk factors that could cause actual results to differ.

- If we use any non-GAAP financial measures during the presentations, you will find on our website, intc.com, the required reconciliation to the most directly comparable GAAP financial measure.

Rev. 4/19/11



# Today's News

The world's first 3-D Tri-Gate transistors on a production technology

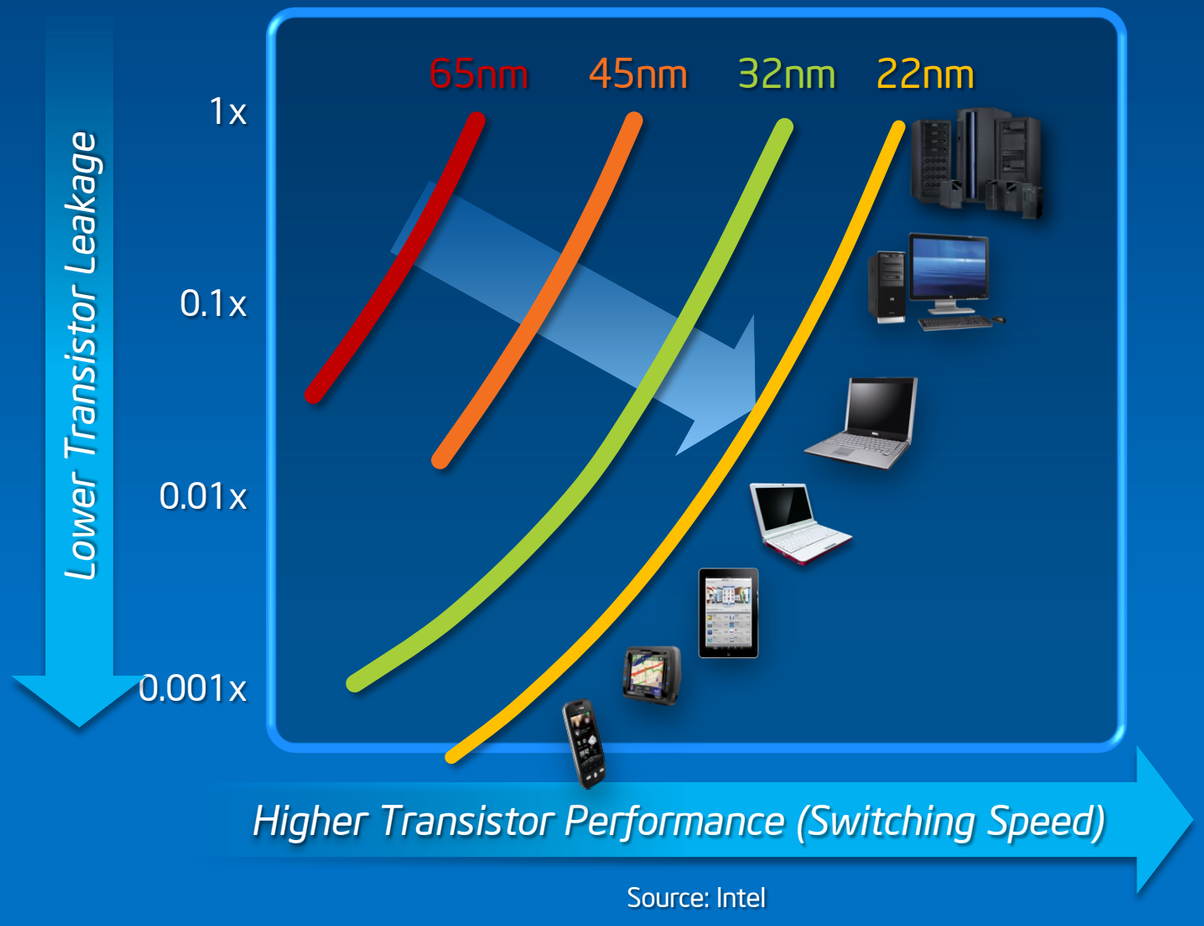
New 22nm transistors have an unprecedented combination of power savings and performance gains.

These benefits will enable new innovations across a broad range of devices from the smallest handheld devices to powerful cloud-based servers.

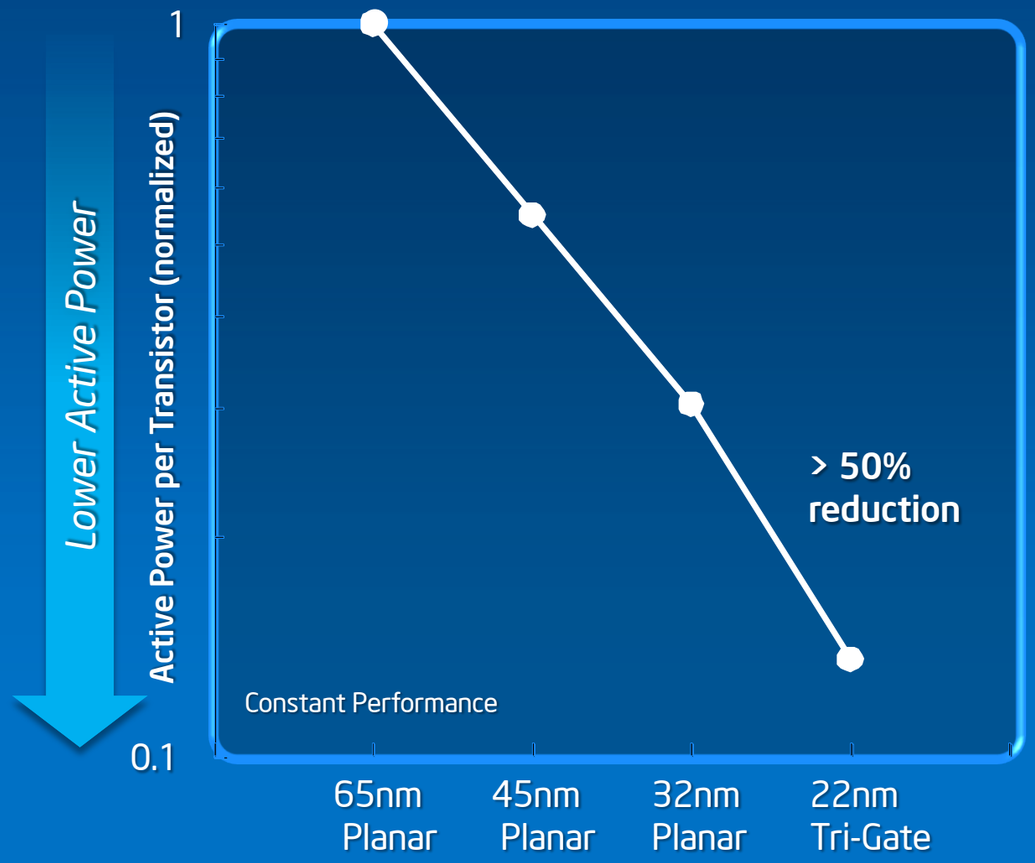
The transition to 3-D transistors continues the pace of technology advancement, fueling Moore's Law for years to come.

The world's first demonstration of a 22nm microprocessor -- code-named Ivy Bridge -- that will be the first high-volume chip to use 3-D Tri-Gate transistors.

# Energy-Efficient Performance Built on Moore's Law



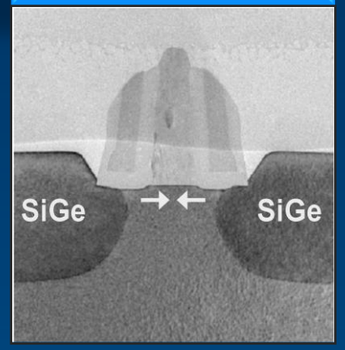
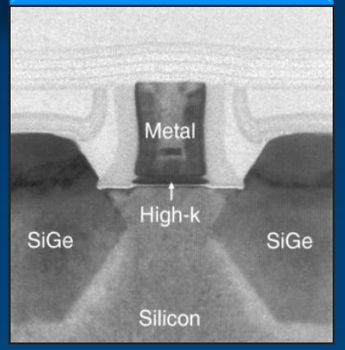
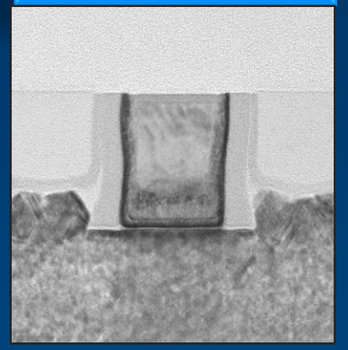
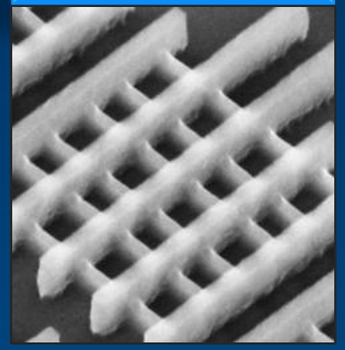

Source: Intel




**22 nm Tri-Gate transistors increase the benefit from a new technology generation**

Source: Intel

# Transistor Innovations Enable Technology Cadence

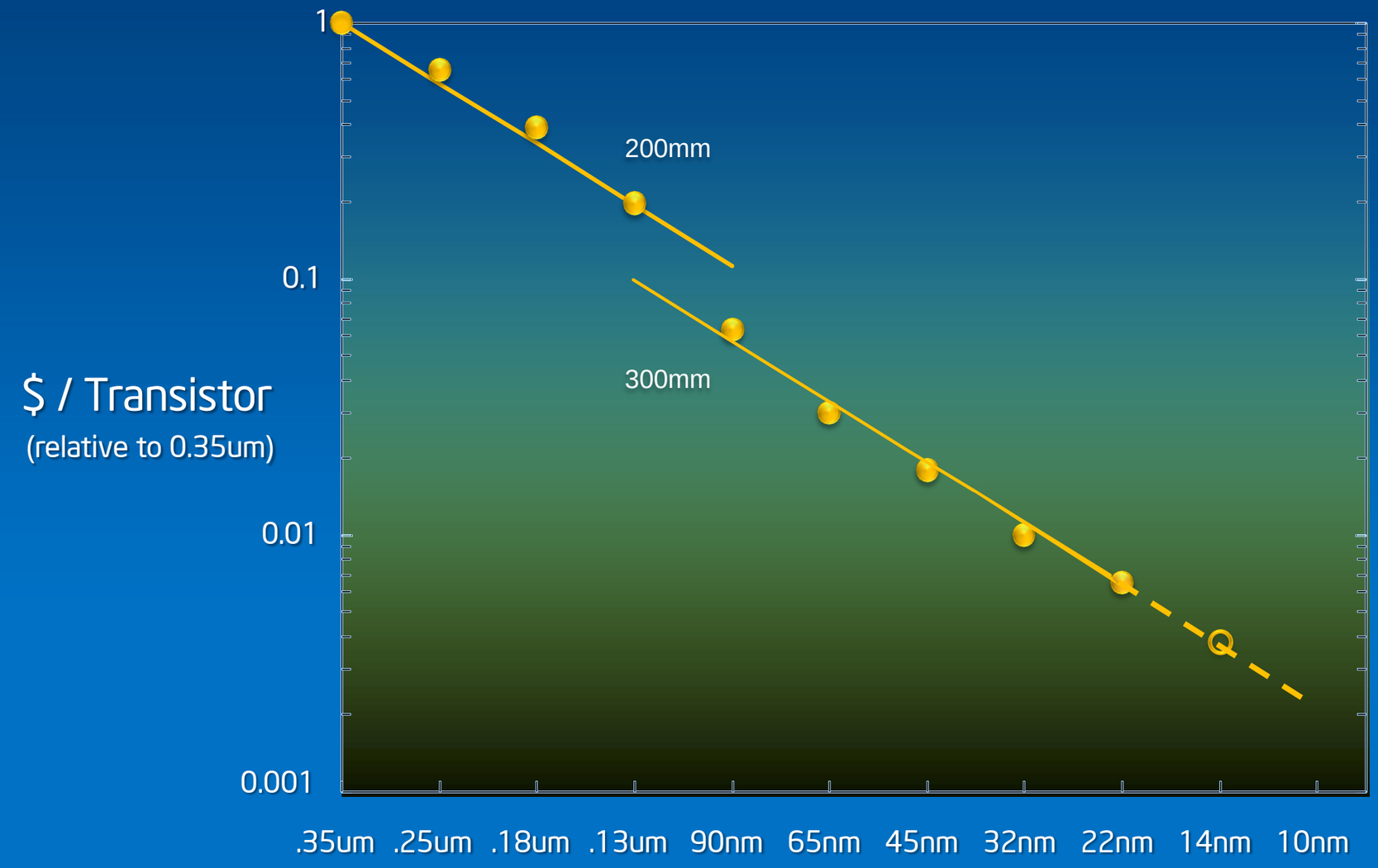
| 2003 | 2005 | 2007 | 2009 | 2011 |
|---|---|---|---|---|
| 90 nm | 65 nm | 45 nm | 32 nm | 22 nm |
|   |  |   |  |  |
| Invented SiGe Strained Silicon | 2nd Gen. SiGe Strained Silicon | Invented Gate-Last High-k Metal Gate | 2nd Gen. Gate-Last High-k Metal Gate | First to Implement Tri-Gate |

Strained Silicon

High k Metal gate

Tri-Gate

# Transistor Innovations Enable Cost Benefits of Moore's Law to Continue




Source: Intel

# 22 nm Manufacturing Fabs

D1D -- Oregon

D1C -- Oregon

Fab 32 -- Arizona

Fab 28 -- Israel

Fab 12 -- Arizona

22nm upgrades to be completed 2011-12

# Tri-Gate Achievement Results from Long Term Commitment to Research

Internal Research

Pathfinding

Development

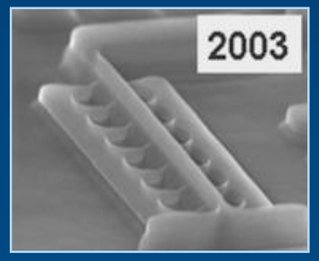
CE! transfer

Manufacturing

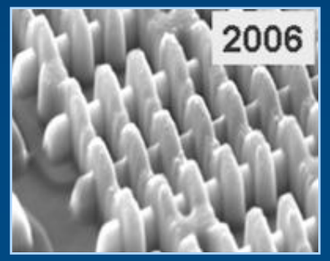
*Tri-Gate Invented*

*Tri-Gate Selected for 22nm node*

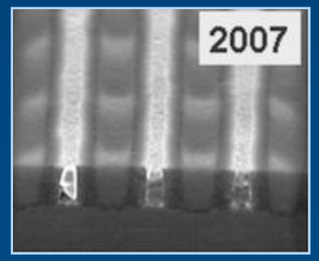

Single-fin transistor demonstrated



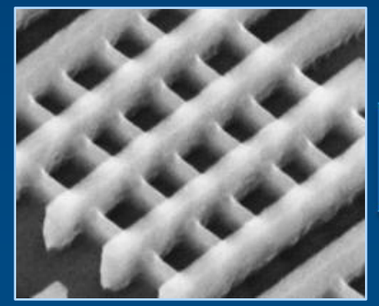

Multi-fin transistor demonstrated




Tri-gate SRAM cells demonstrated




Tri-gate RMG process flow developed



Tri-gate optimized for HVM

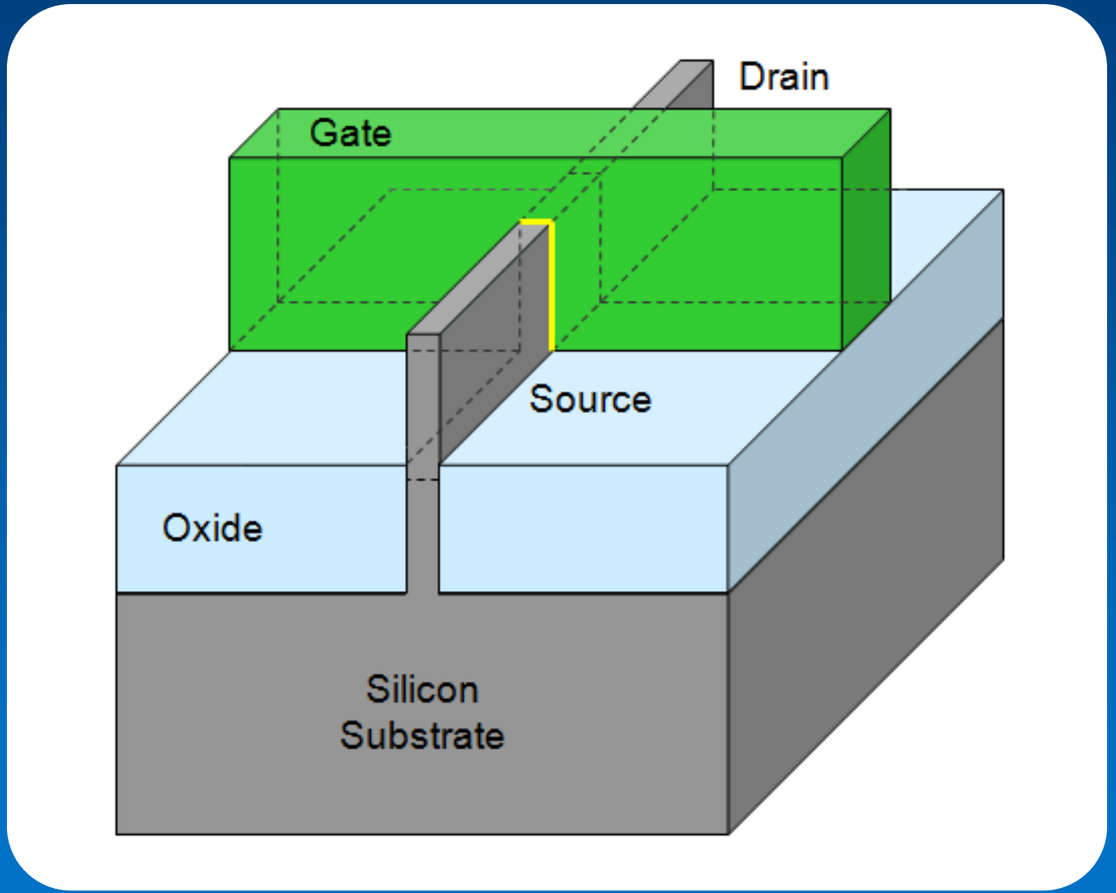
Tri-Gate Mfg

**Bringing innovative technologies to HVM is the result of a highly coordinated internal research-development-manufacturing pipeline**

intel

"For years we have seen limits to how small transistors can get," said Gordon E. Moore. "This change in the basic structure is a truly revolutionary approach, and one that should allow Moore's Law, and the historic pace of innovation, to continue."

# 22 nm 3-D Tri-Gate Transistor

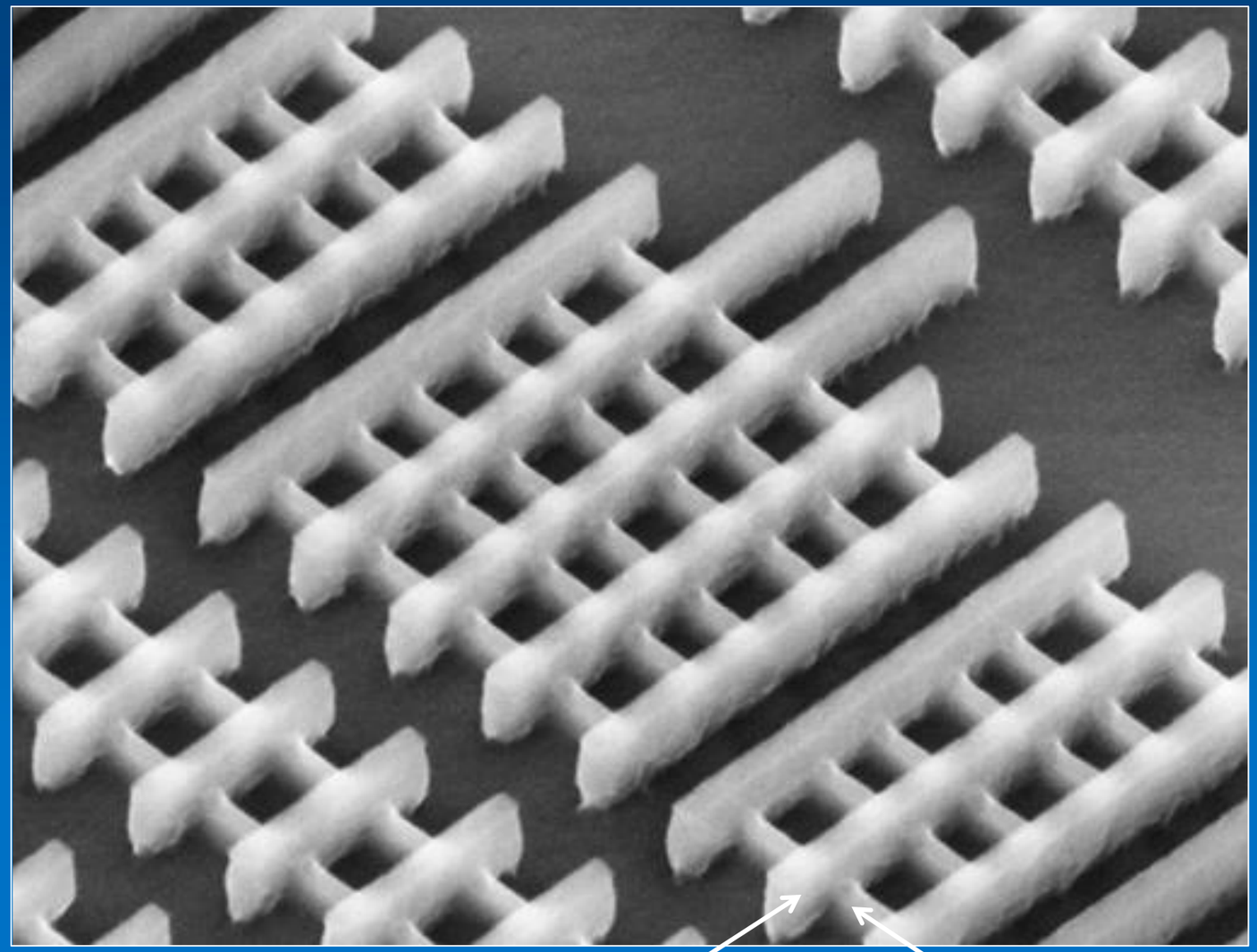



3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

*Transistors have now entered the third dimension!*

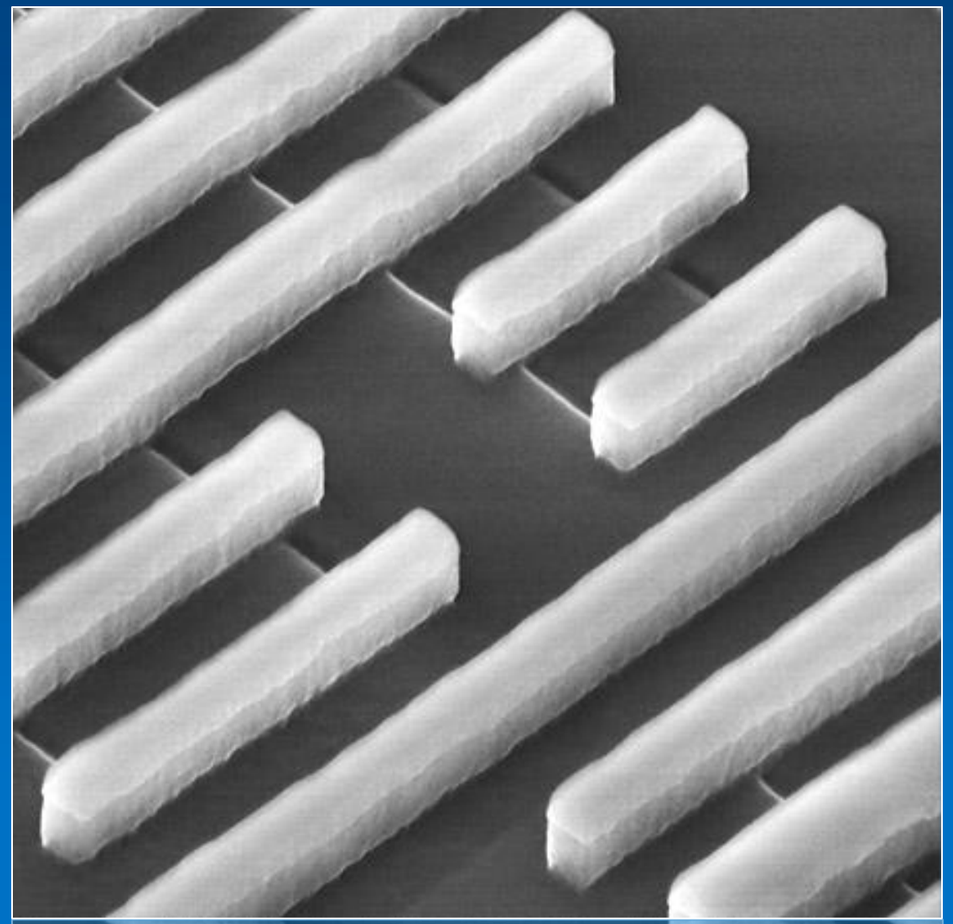
Source: Intel

# 22 nm 3-D Tri-Gate Transistor

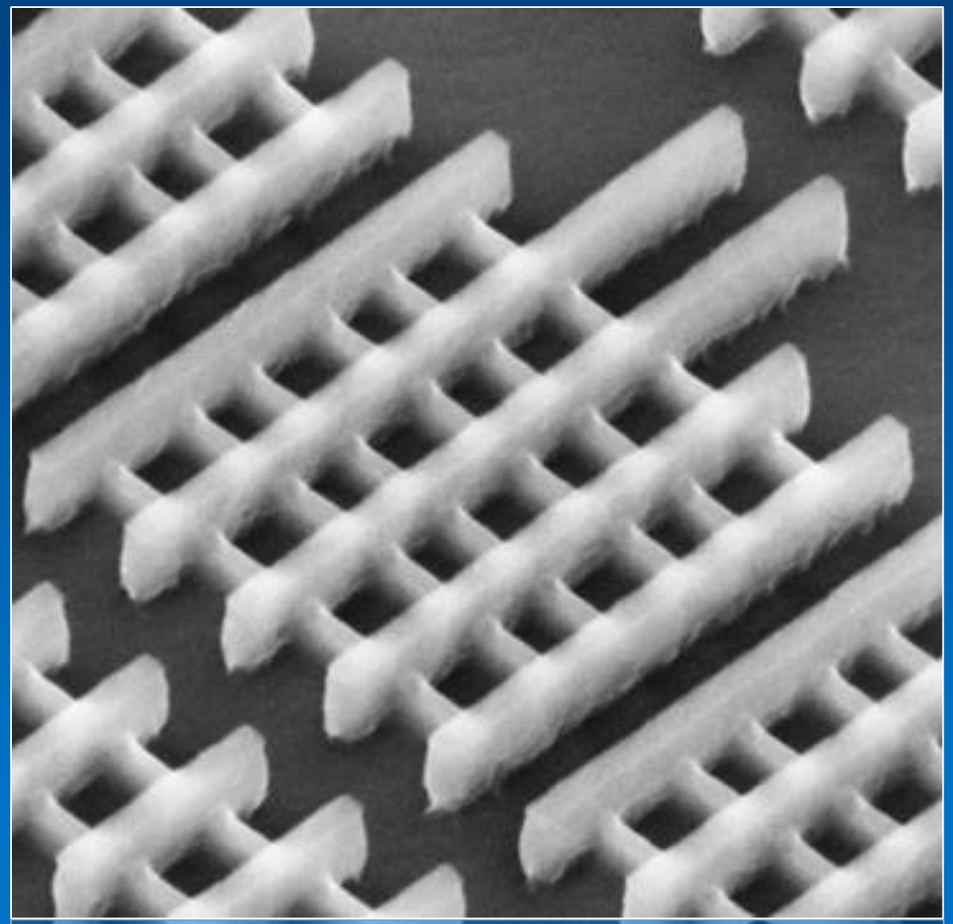



Source: Intel

## 32 nm Planar Transistors



## 22 nm Tri-Gate Transistors

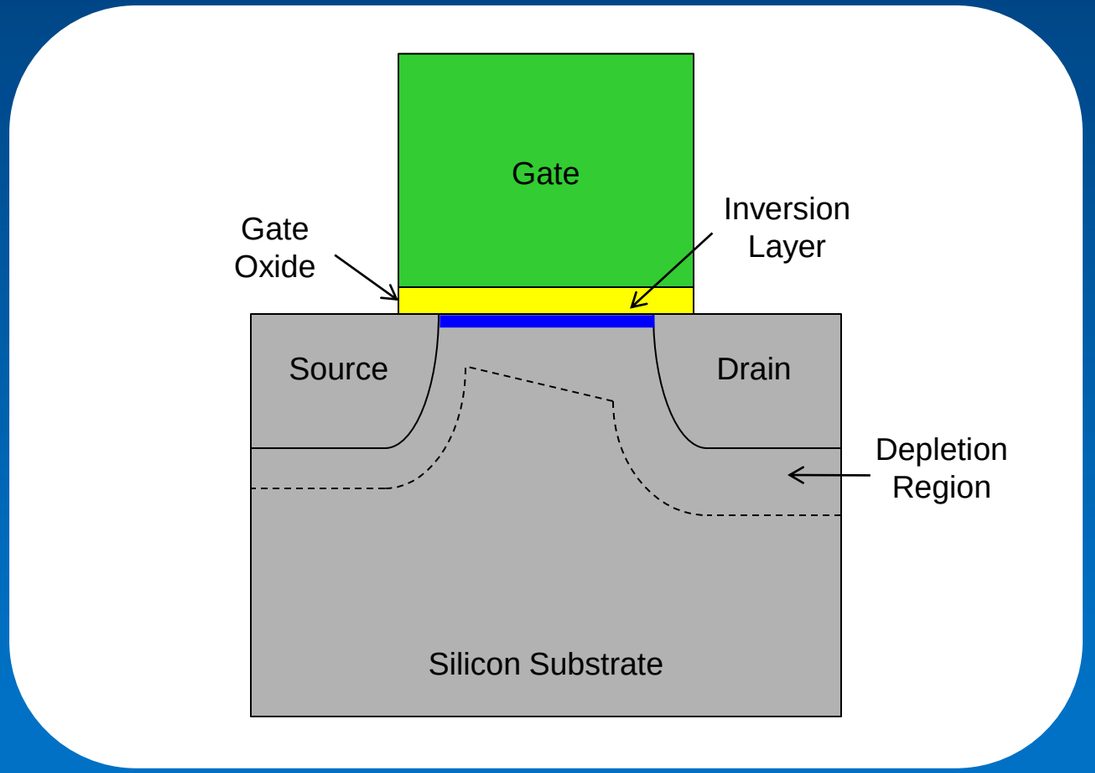


Source: Intel

# Std vs. Fully Depleted Transistors

## Bulk Transistor

"Transistor 101"




Substrate voltage exerts some electrical influence on the inversion layer (where source-drain current flows)

The influence of substrate voltage degrades electrical sub-threshold slope (transistor turn-off characteristics)

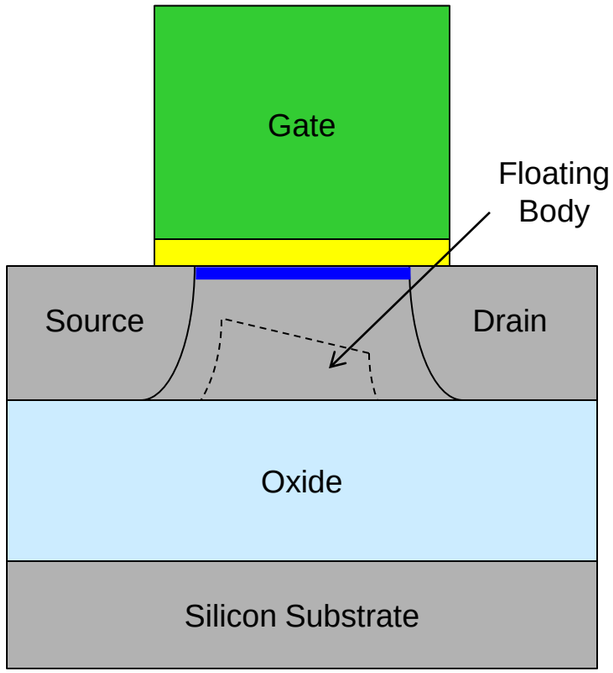
NOT fully depleted

Source: Intel

# Std vs. Fully Depleted Transistors

## Partially Depleted SOI (PDSOI)

"Transistor 101"




Floating body exerts some electrical influence on inversion layer, degrading sub-threshold slope

NOT fully depleted

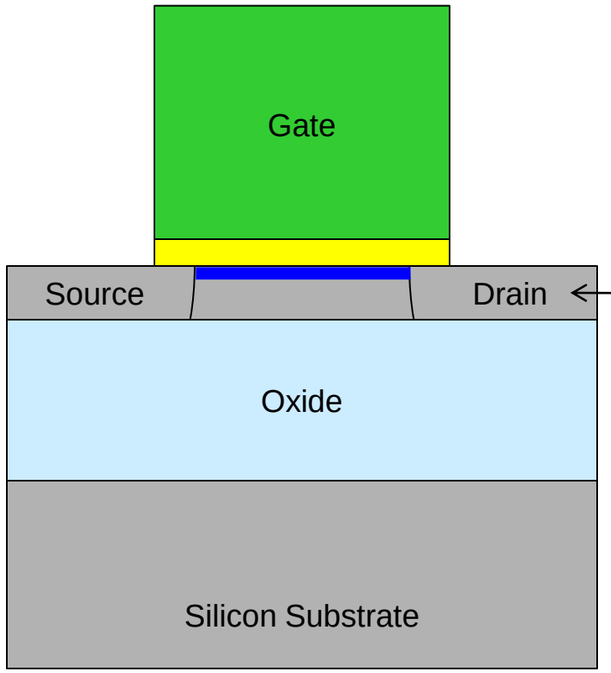
Not used by Intel

Source: Intel

# Std vs. Fully Depleted Transistors

## Fully Depleted SOI (FDSOI)

"Transistor 101"




Floating body eliminated and sub-threshold slope improved

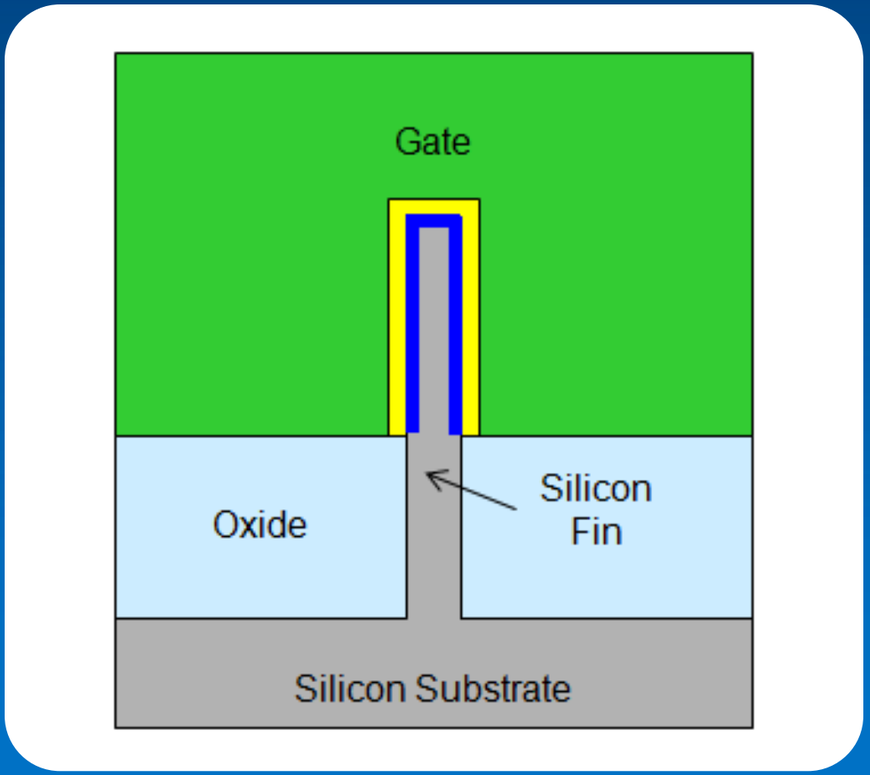
Requires expensive extremely thin SOI wafer, which adds ~10% to total process cost

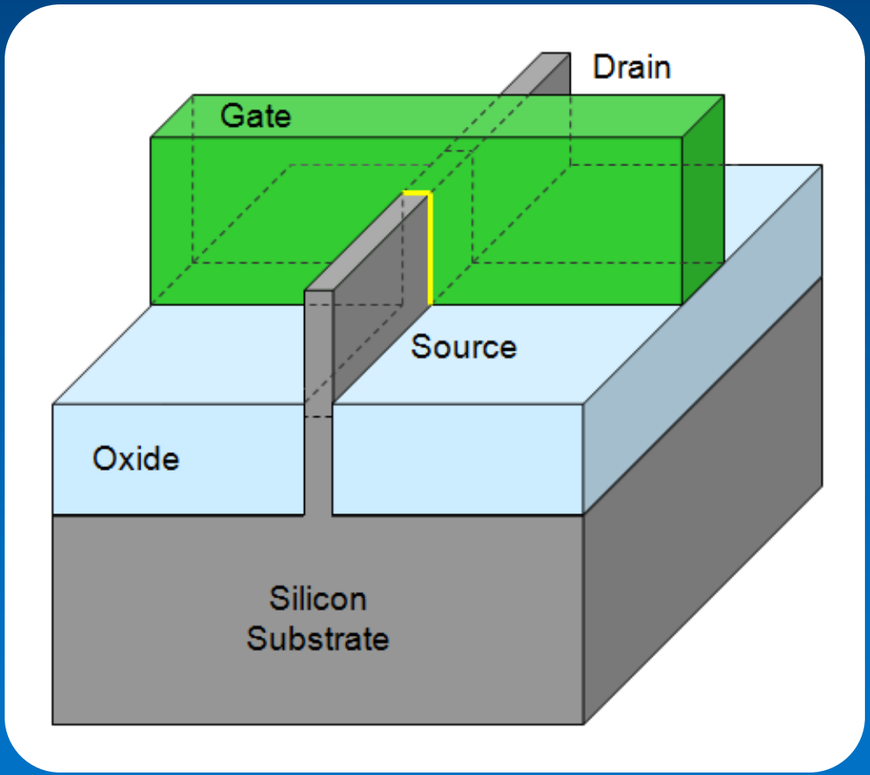
Not used by Intel

Source: Intel

# Std vs. Fully Depleted Transistors

## Fully Depleted Tri-Gate Transistor




Gate electrode controls silicon fin from three sides providing improved sub-threshold slope

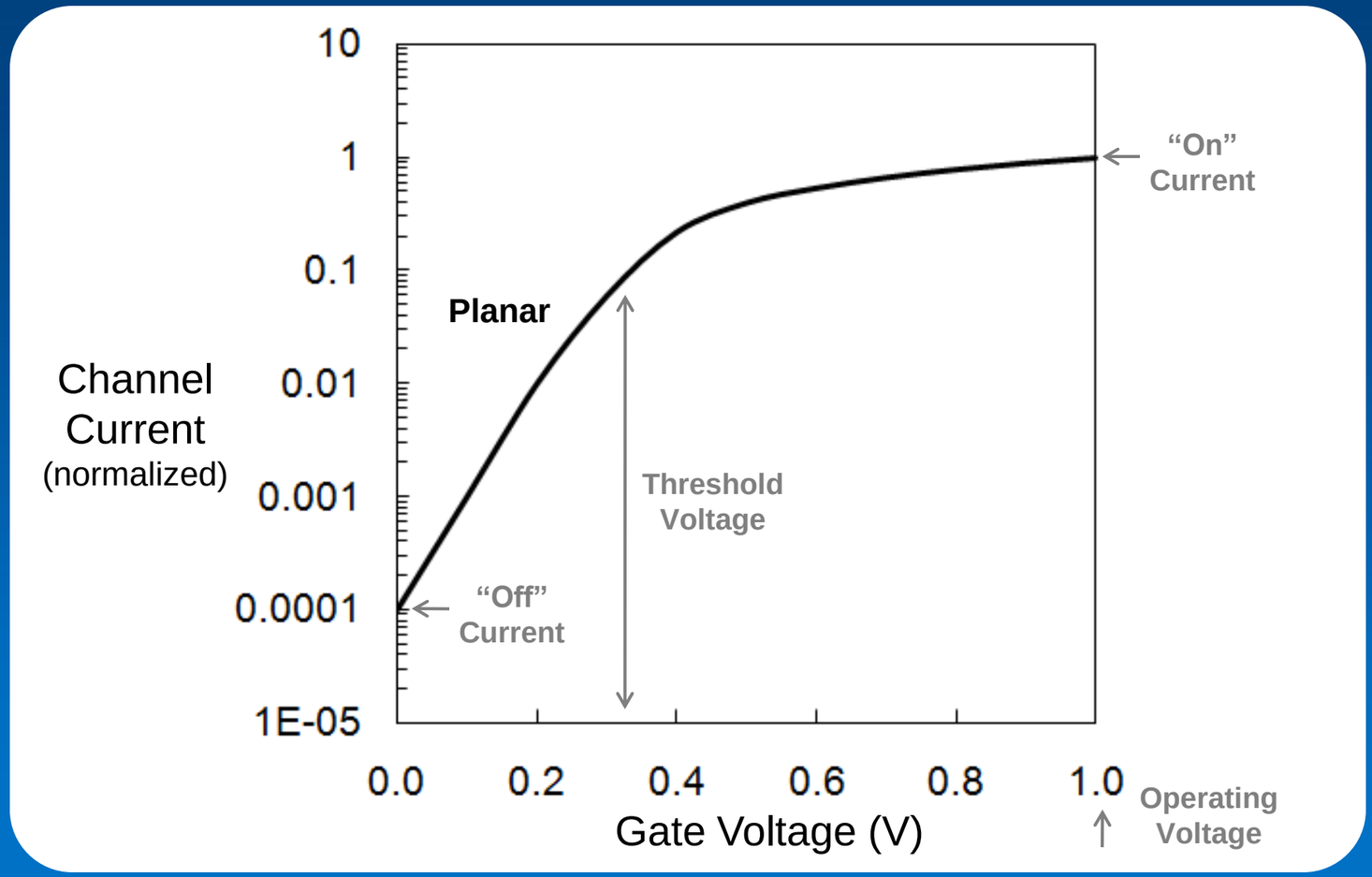
Inversion layer area increased for higher drive current

Process cost adder is only 2-3%

Source: Intel

# Transistor Operation

"Transistor 101"



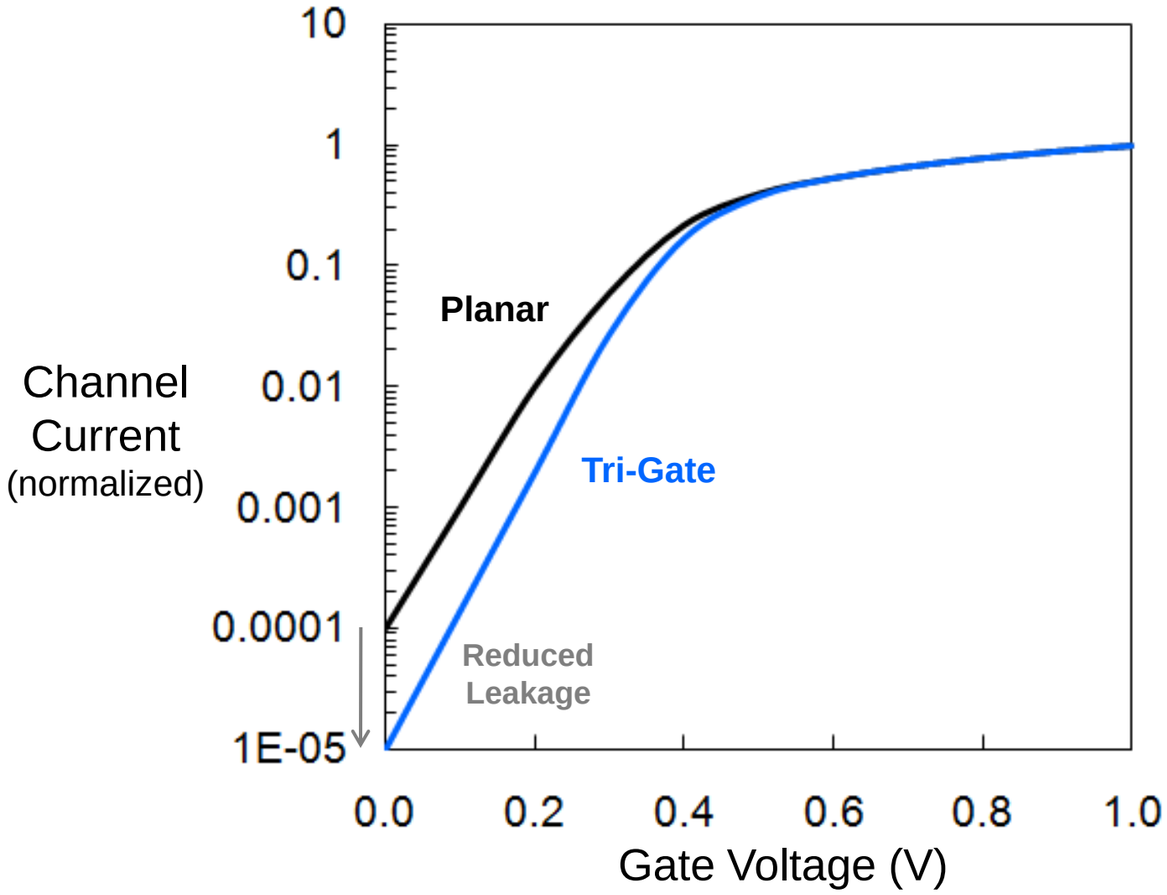

Maximize current in "on" state (for improved performance)

Minimize current in "off" state (for lower power)

Switch very quickly between the two states (for performance)

Source: Intel

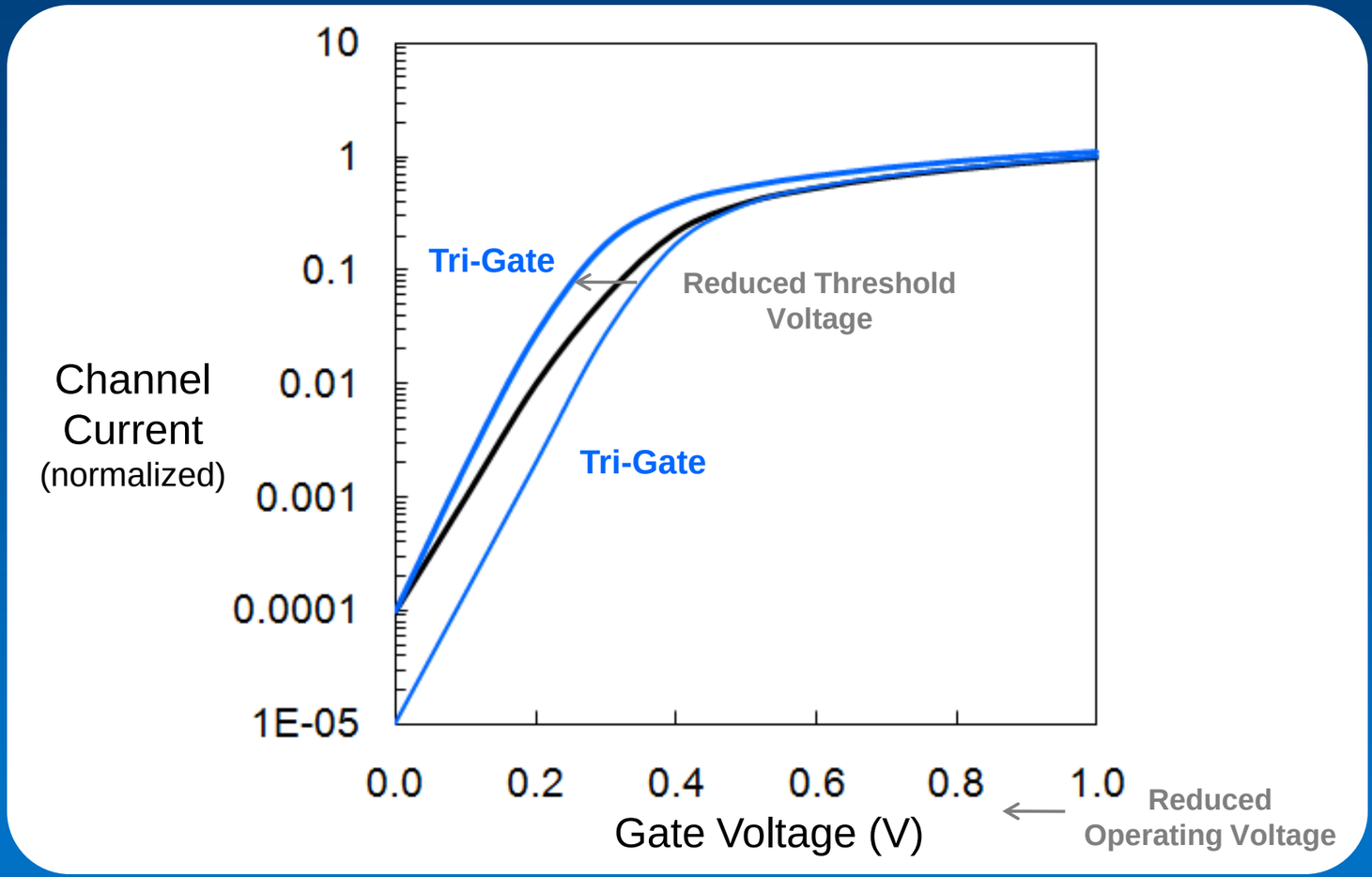
# Transistor Operation




The “fully depleted” characteristics of Tri-Gate transistors provide a steeper sub-threshold slope that reduces leakage current

Source: Intel

# Transistor Operation

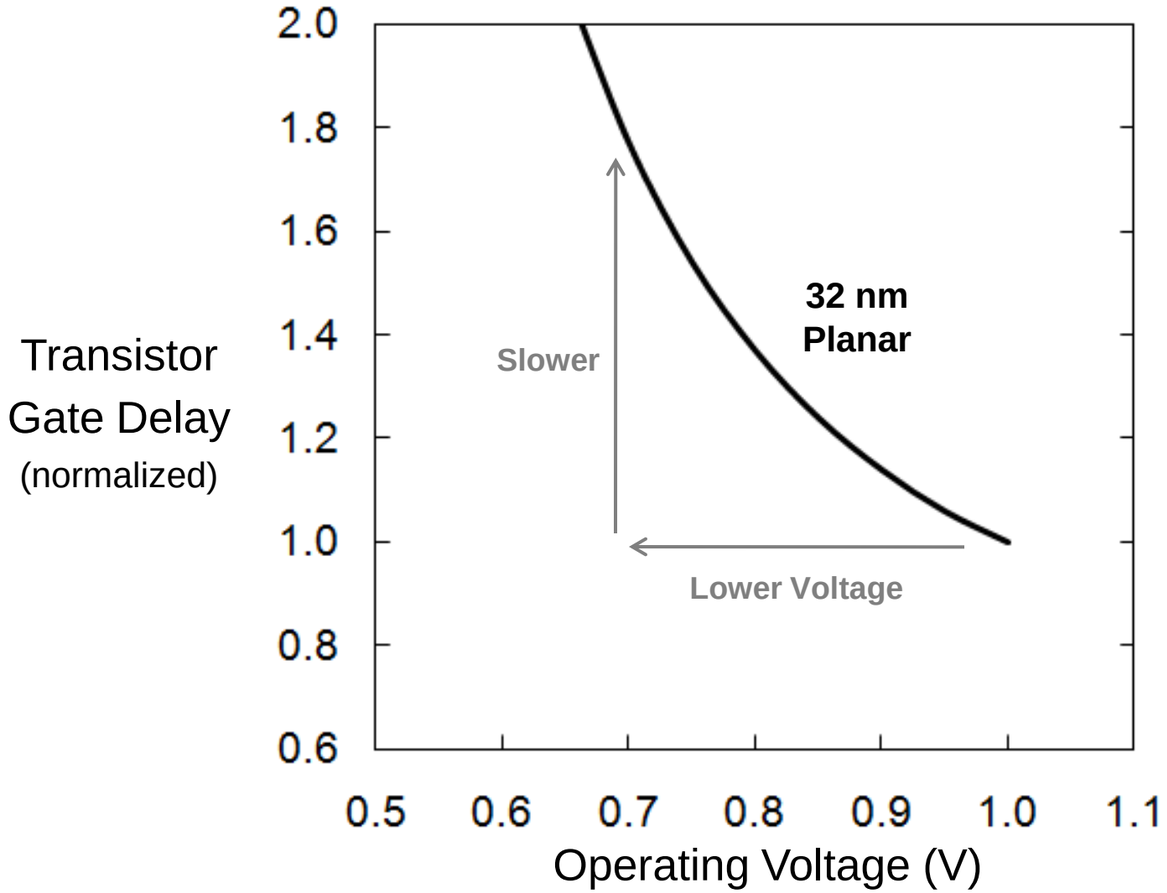



The steeper sub-threshold slope can also be used to target a lower threshold voltage, allowing transistors to operate at lower voltage to reduce power and/or improve switching speed

Source: Intel

# Transistor Gate Delay

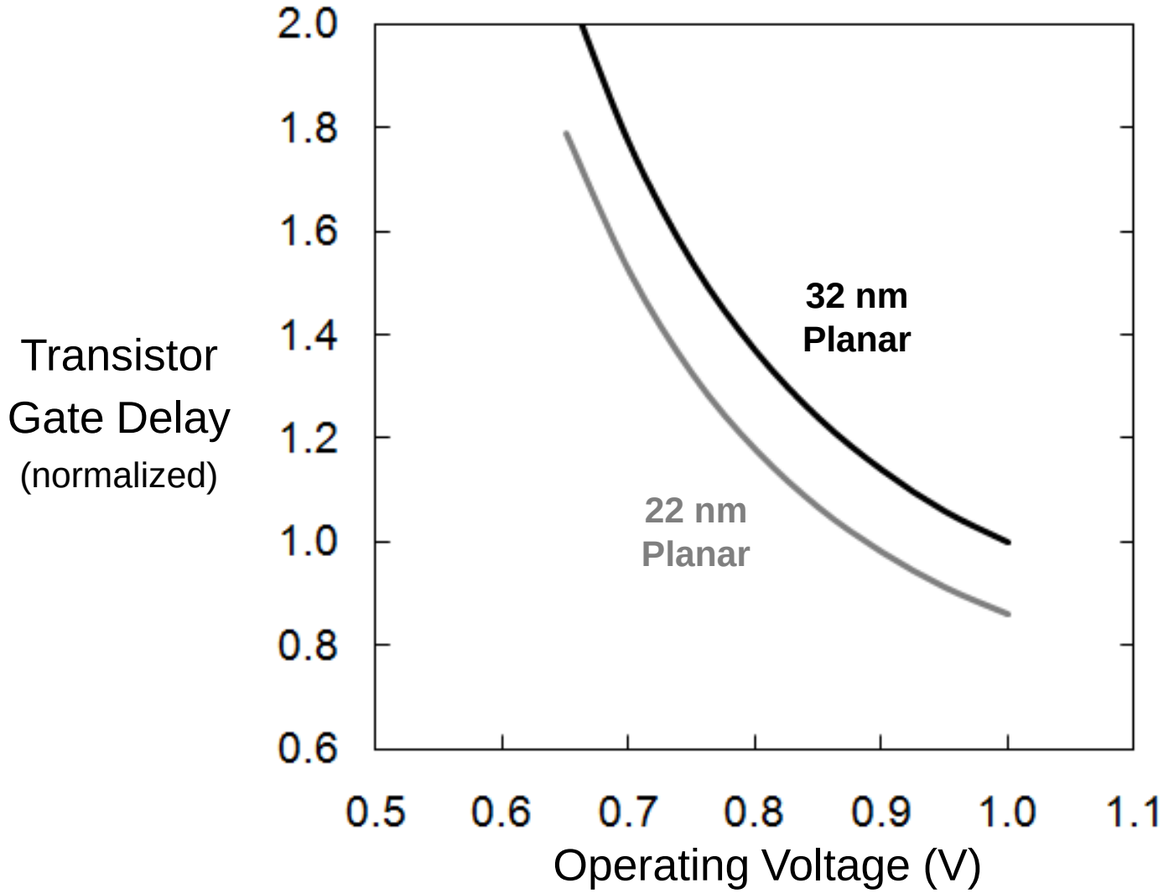
"Transistor 101"




Transistor gate delay (switching speed) slows down as operating voltage is reduced

Source: Intel

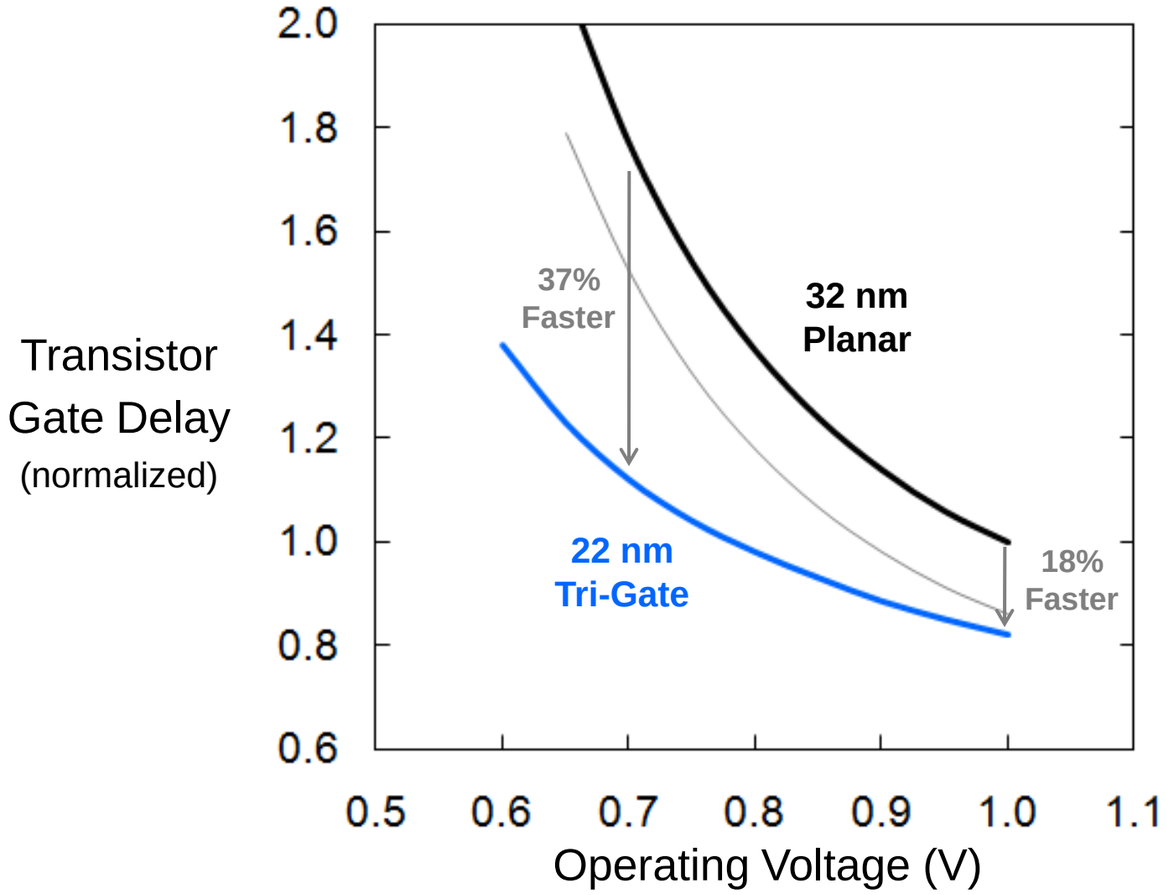
# Transistor Gate Delay




22 nm planar transistors could provide some performance improvement, but would still have poor gate delay at low voltage

Source: Intel

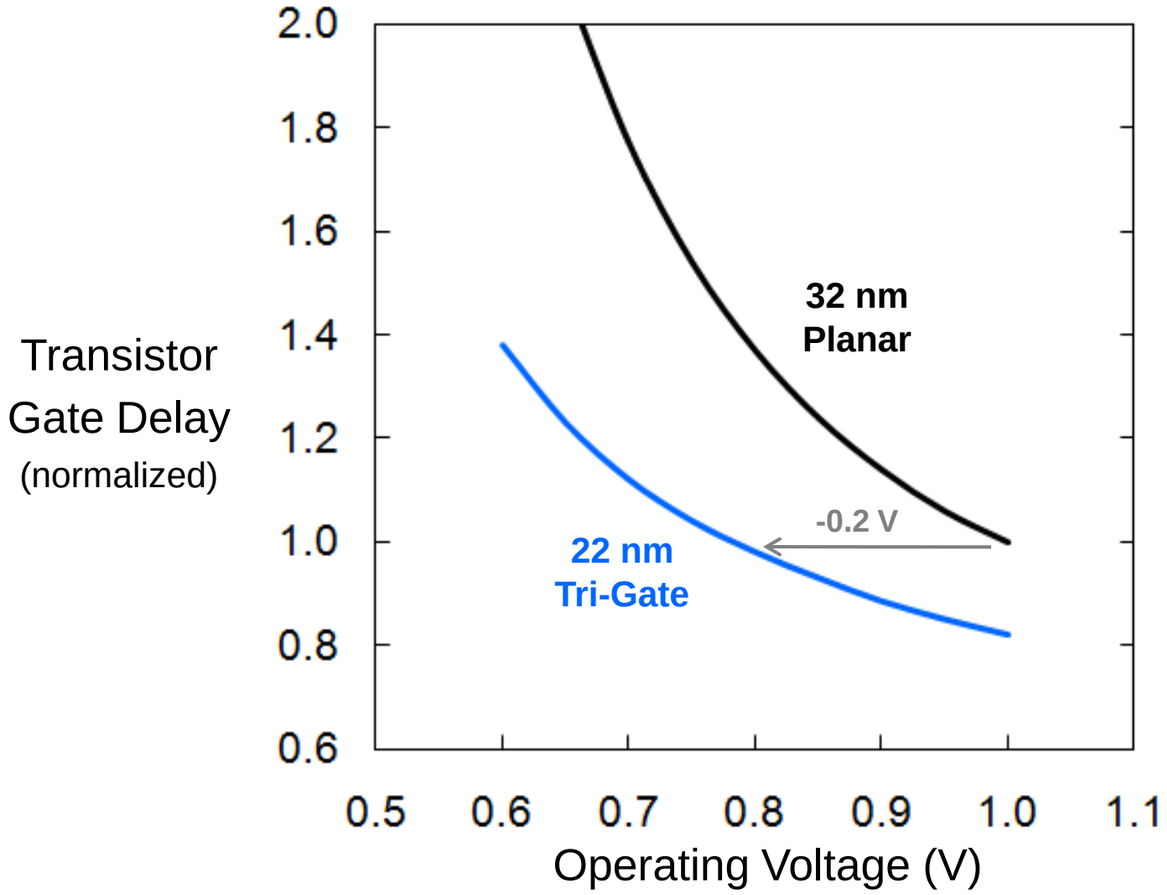
# Transistor Gate Delay




22 nm 3-D Tri-Gate transistors provide improved performance at high voltage and an *unprecedented* performance gain at low voltage

Source: Intel

# Transistor Gate Delay

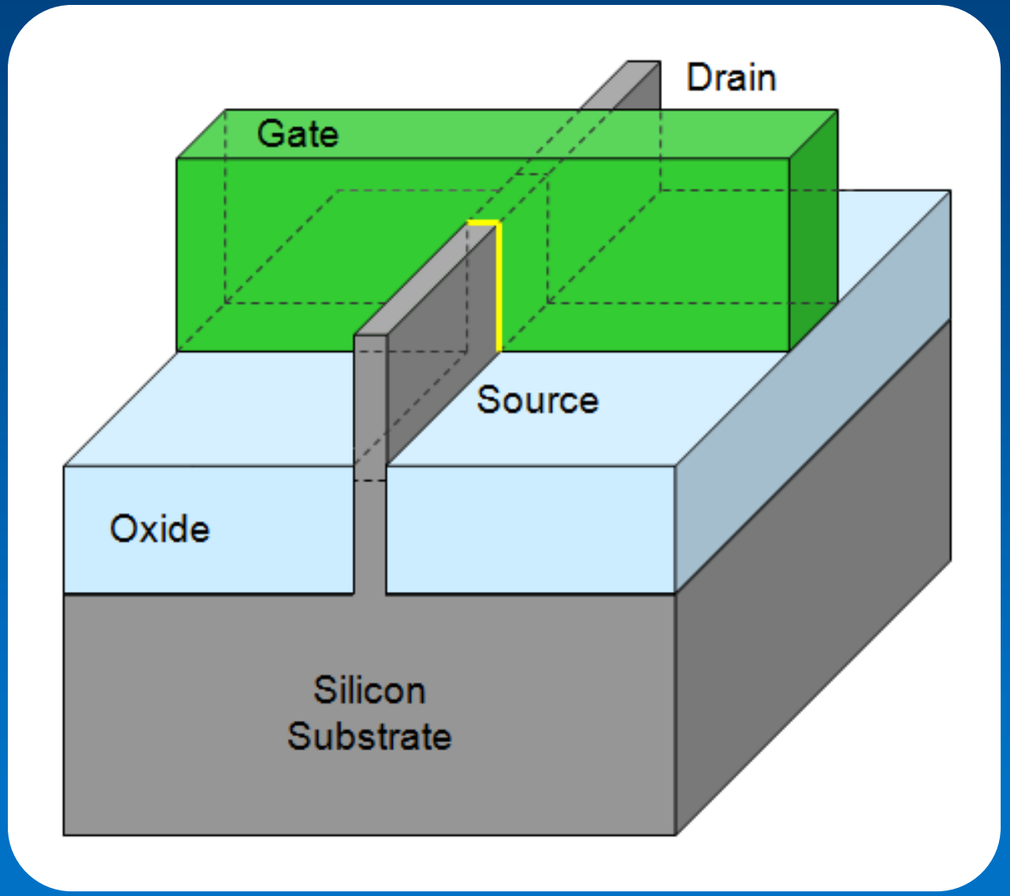



22 nm 3-D Tri-Gate transistors can operate at lower voltage with good performance, reducing active power by >50%

Source: Intel

# 3-D Tri-Gate Transistor Benefits

- Dramatic performance gain at low operating voltage, better than Bulk, PDSOI or FDSOI
  - 37% performance increase at low voltage
  - >50% power reduction at constant performance
- Improved switching characteristics (On current vs. Off current)
- Higher drive current for a given transistor footprint
- Only 2-3% cost adder (vs. ~10% for FDSOI)




3-D Tri-Gate transistors are an important innovation needed to continue Moore's Law

Source: Intel

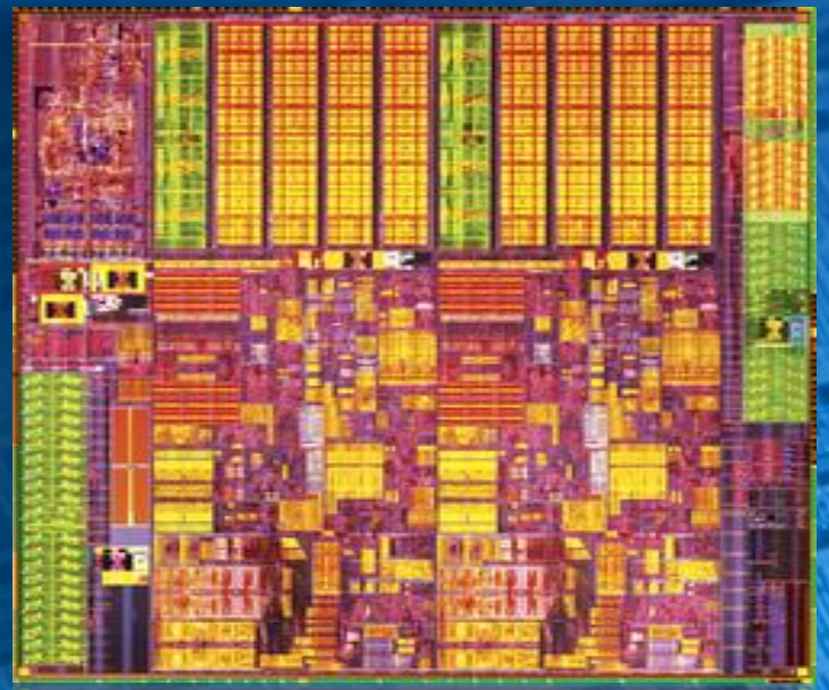
# 22nm Product Update

**Dadi Perlmutter**
Executive Vice President
General Manager,
Intel Architecture Group

# 22nm Silicon Technology Breakthrough Benefits Broad Range of Intel Architecture Devices

New 22nm 3-D transistors deliver unprecedented performance improvement and power reduction for Intel's product portfolio

- This benefits smallest handhelds to powerful cloud-based servers
- 37% performance increase at low voltage vs. 32nm planar transistors*
- Consumes only half the power at the same performance level as 2-D transistors on 32nm planar chips*



* Based on Intel Internal Data

# Intel Architecture Spans The Compute Continuum

# Newest Manufacturing Technology Delivers Ivy Bridge

| 45 nm Process Technology | | 32 nm Process Technology | | 22 nm Process Technology |
|---|---|---|---|---|
| **Penryn** | **Nehalem** | **Westmere** | **Sandy Bridge** | **Ivy Bridge** |
| Intel® Core™ Microarchitecture | NEW Intel® Microarchitecture | Intel® Microarchitecture (Nehalem) | NEW Intel® Microarchitecture | Intel® Microarchitecture (Sandy Bridge) |
| TICK | TOCK | TICK | TOCK | TICK |
| | | | | Intel's First 22 nm Processor |

## Cadence of Innovation Delivers New Microprocessor Efficiency on the 22 nm Process

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# Ivy Bridge

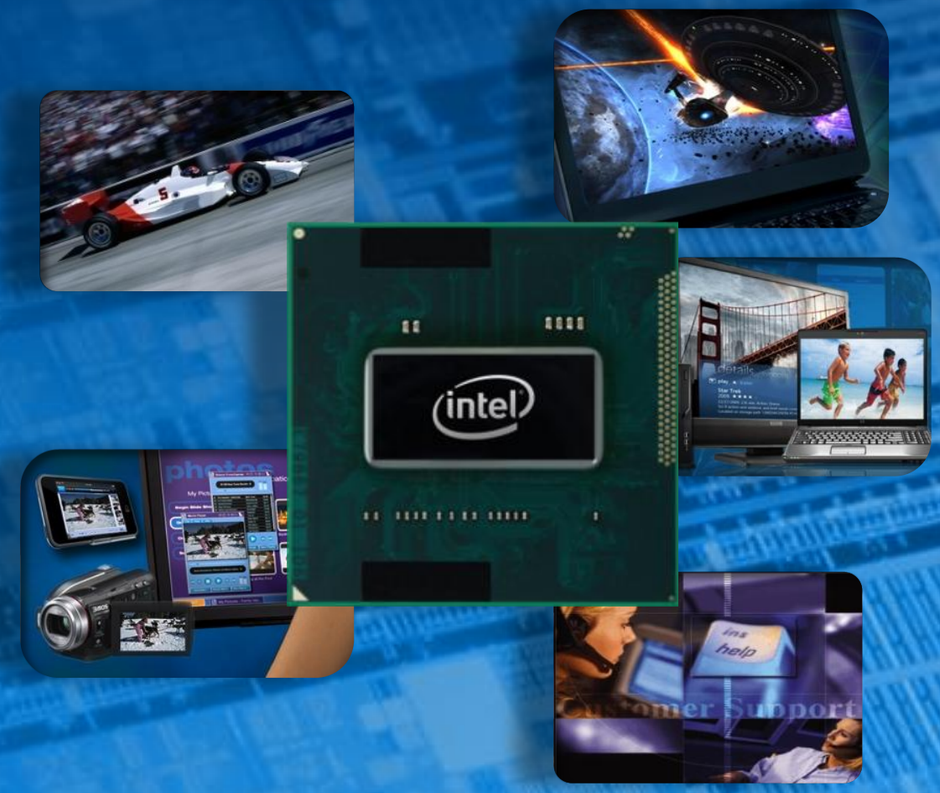
## Sandy Bridge Migrated to 22nm Process Technology

**Client: Efficient performance for thin and light form factors**

- Increased performance vs. today's 2nd generation Intel® Core™ product family
- Enhanced media and graphics performance with processor graphics
- Enhanced security features

**Server: Increased performance and improved efficiency**

- Integrated Storage Features




**Further Demonstrating Intel Product and Process Leadership**

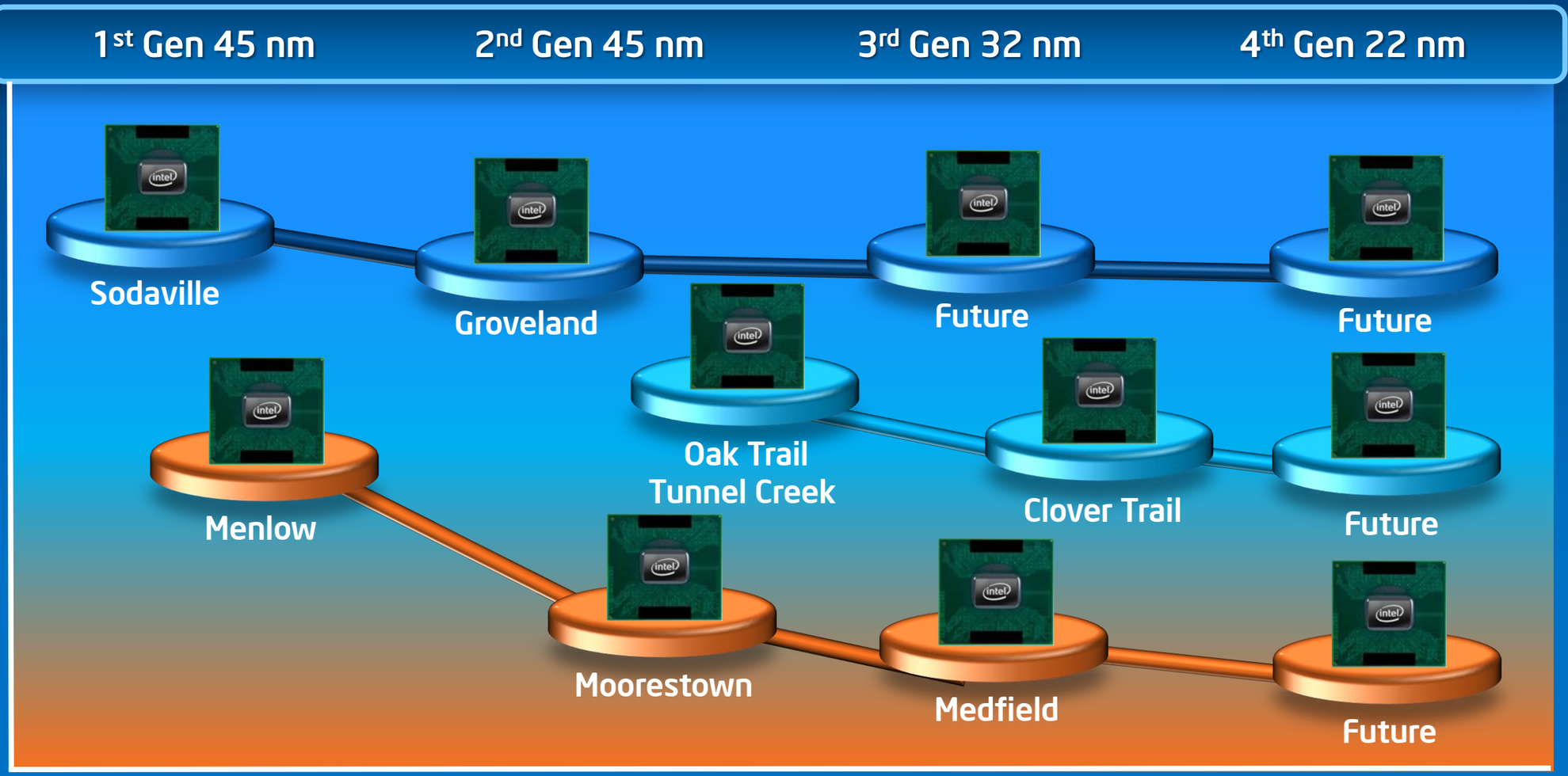
# IA Platforms for Low Power Segments

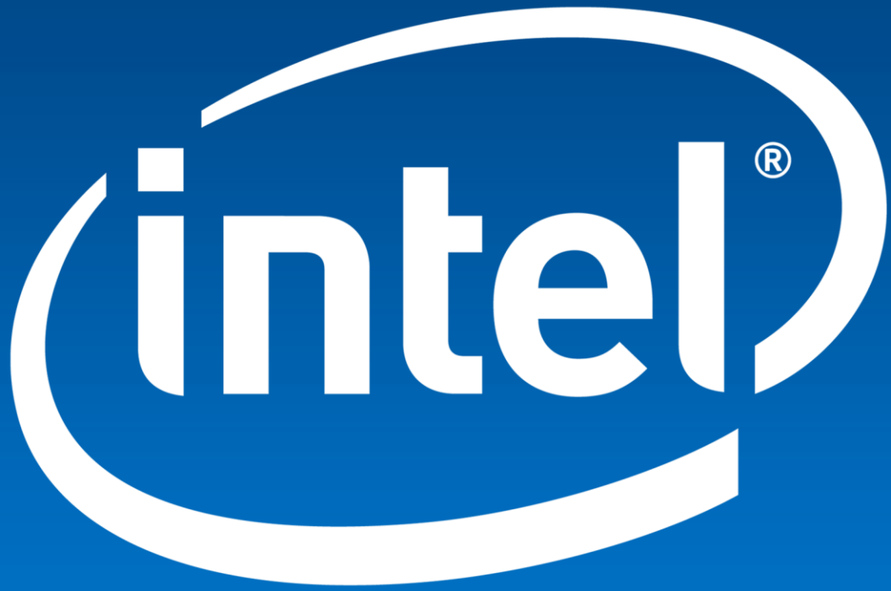
*Optimized Performance for Phones, Tablets, and Consumer Electronics*

Consumer Electronics

Tablets

Smart Phones

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