



History of Many-Core Leading to Intel® Xeon Phi™

The Intel® Xeon Phi™ co-processor marks a new era for Intel and technical computing. The co-processor culminates more than eight years of collaboration across Intel. The challenge of many-core computing and its broad implication to hardware and software design galvanized best minds from product groups and Intel Labs. Here are a few of the highlights from this journey.

- **February 2004.** Visionary future application research by Intel Fellow Pradeep Dubey demonstrating the need for highly parallel architectures is shown at IDF in a CTO keynote titled "The Era of Tera."
- **August 2004.** Intel senior technologists brief executives for a full day on the results of a months-long investigation into the strategic technology challenges in scaling multi-core to many-core.
- **2005-2009.** The development of a broad many-core research agenda commences along with the Larrabee prototype targeting highly parallel visual computing applications. Over this time period, Intel Labs works with Intel business units to develop many-core workloads, simulators, runtimes and other technologies in support of Larrabee.
- **March 2006.** Justin Rattner, Intel CTO unveils the Tera-scale Computing Research Program at Spring IDF. Led by Jim Held, Intel fellow, the program aligned more than 80 research projects aimed at scaling processors from a few cores to many.
- **August 2006.** Intel releases Threading Building Blocks to help mainstream software developers with the transition to programming for increasingly parallel microprocessors.
- **February 2007.** The 80-core Teraflops Research Processor, codenamed "Polaris" is detailed at ISSCC. A concept vehicle from Intel Labs, Polaris demonstrated the basic capability to perform 1 Trillion Floating Point Operations (1 Teraflops) on a single chip.
- **March 2008.** Intel and Microsoft launch two Universal Parallel Computing Research Centers at UC Berkeley and the University of Illinois at Urbana-Champaign to catalyze software innovation in preparation for the shift to many-core.

- **November 2009.** Justin Rattner shows the potential of many-core Intel Architecture (IA) for supercomputing by demonstrating a Larrabee prototype that exceeded 1 Teraflops on a standard HPC benchmark (SGEMM).
- **December 2009.** The Single-Chip Cloud Computer (SCC), codenamed Rock Creek, is unveiled to the press. The second concept vehicle from Intel Labs, Rock Creek contained 48 IA cores connected by a mesh network, the most ever integrated on a single chip at the time.
- **May 2010.** Kirk Skaugen, vice president, general manager of Intel's PC Client Group, unveils plans for Many Integrated Core (MIC) architecture for high performance computing at the International Supercomputing Conference. MIC draws upon application research by Pradeep Dubey and the work of Polaris, Rock Creek and Larrabee.
- **September 2010.** The Many-core Applications Research Community is launched, which allows hundreds of researchers worldwide to develop innovation in parallel software using the Single-chip Cloud Computer.
- **June 2012.** Raj Hazra, vice president, general manager of Intel High Performance Computing, announces the Xeon Phi co-processor and demonstrates the first Teraflop single-node DP Linpack at the International Supercomputing Conference, the first product based on the MIC architecture. Even before launch, the first Xeon Phi cluster enters the Top500 at #150.
- **November 2012.** Intel® Xeon Phi™ ships.

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