Intel Demonstrates High-k + Metal Gate Transistor Breakthrough on 45 nm Microprocessors

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Key Messages

- Intel has achieved a significant breakthrough in transistor technology by developing high-k + metal gate transistors for its 45 nm process that significantly reduce leakage power
- High-k + metal gate transistors are the biggest advancement in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s
- Working 45 nm microprocessors have been made using these revolutionary high-k + metal gate transistors
- These new 45 nm multi-core microprocessors will deliver higher performance and greater energy efficiency
- Intel's 45 nm products are on track to begin production in 2H '07 with three factories scheduled to be manufacturing 45 nm by 1H '08

Intel's Logic Technology Evolution

Process Name:	P1262	P1264	P1266	P1268	P1270
Lithography:	90 nm	65 nm	45 nm	32 nm	22 nm
1st Production:	2003	2005	2007	2009	2011

Moore's Law continues!

Intel continues to develop a new technology generation every 2 years

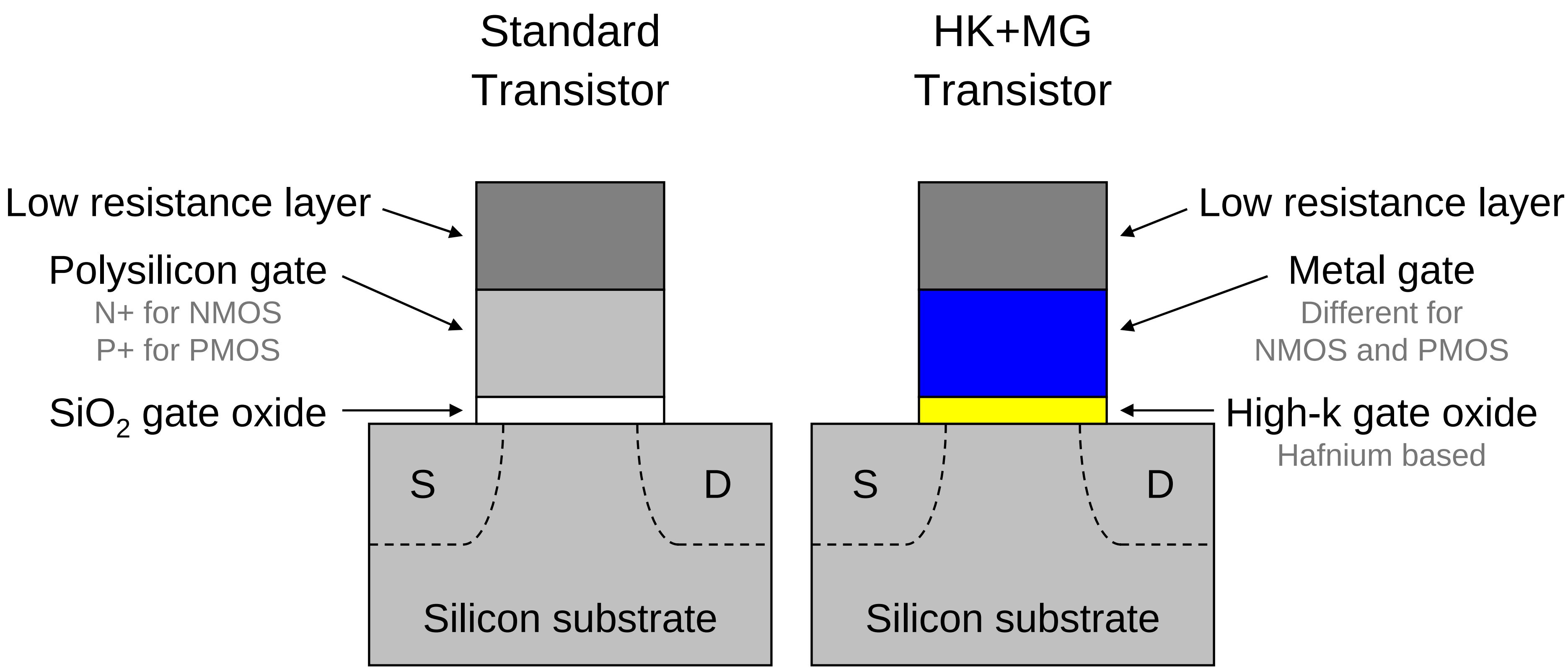
45 nm Technology Benefits

- Compared to today's 65 nm technology, Intel's 45 nm technology will provide the following product benefits:

~2x	improvement in transistor density, for either smaller chip size or increased transistor count
~30%	reduction in transistor switching power
>20%	improvement in transistor switching speed or
>5x	reduction in source-drain leakage power
>10x	reduction in gate oxide leakage power

- These performance and leakage improvements would not be possible without high-k + metal gate
- This process technology will provide the foundation to deliver improved performance/watt that will enhance the user experience

High-k + Metal Gate Transistors



High-k + metal gate transistors provide significant performance increase and leakage reduction, ensuring continuation of Moore's Law

High-k + Metal Gate Transistors

Metal Gate

- Increases the gate field effect

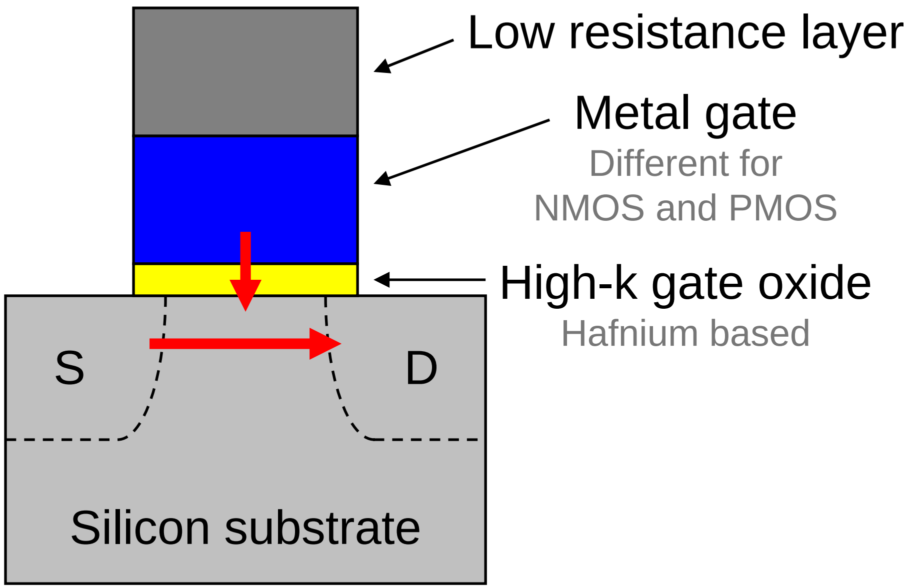
High-k Dielectric

- Increases the gate field effect
- Allows use of thicker dielectric layer to reduce gate leakage

HK + MG Combined

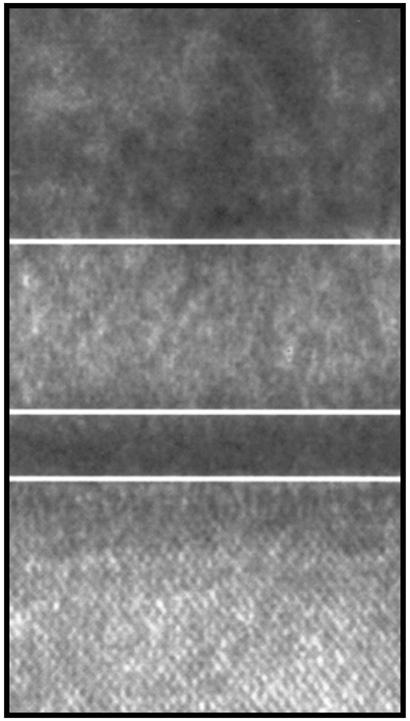
- Drive current increased >20% (>20% higher performance)
- Or source-drain leakage reduced >5x
- Gate oxide leakage reduced >10x

HK+MG Transistor



High-k + Metal Gate Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s"

Gordon Moore

High-k + Metal Gate Transistors

- Specific metal gate and high-k dielectric materials are not being disclosed at this time
- There are hundreds of material options for metal gate electrodes and high-k dielectrics
- Identifying the HK+MG material combination that meets high performance, low leakage, reliability and manufacturing requirements is a very significant accomplishment
- No other company has reached this level of success and they are not expected to have HK+MG until the 32 nm generation or later

2003 HK+MG Announcement

What are we announcing?

- Intel has made significant progress in future transistor materials
- Two key parts of this new transistor are:
  - The gate dielectric consists of a “high-k” material
  - The gate electrode is made of metal
- Intel has succeeded in integrating these innovations and creating transistor with *record-setting performance*, and with dramatically reduced leakage current
- Intel believes that high-k/metal gate can be implemented in the 45nm manufacturing process, to be in production in 2007

Nov. 2003

Intel’s Components Research group announced first working high-k + metal gate transistors in 2003

2006 45 nm SRAM Announcement

45 nm SRAM Chip

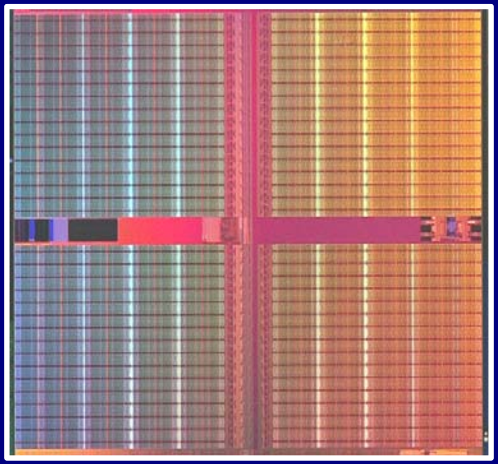
0.346 μm² cell

153 Mbit density

119 mm² chip size

>1 billion transistors

Functional silicon in Jan ‘06

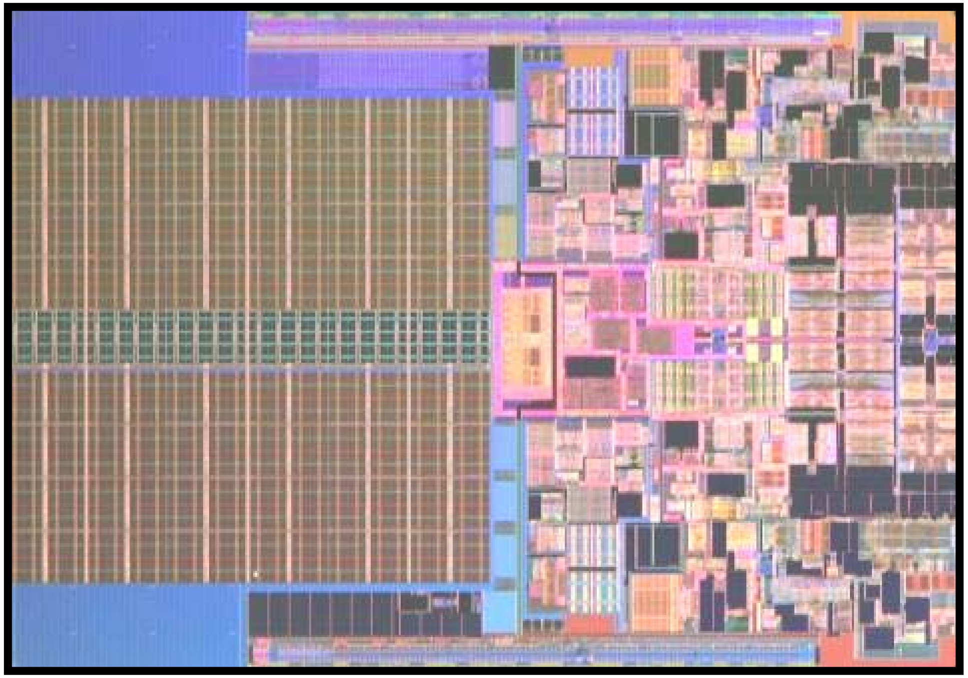


45 nm SRAM test vehicle includes all transistor and interconnect features to be used on 45 nm microprocessors

January 2006

153 Mbit SRAM in Jan ‘06 used same process features as today’s 45 nm CPU, including high-k + metal gate transistors and cost effective 193 nm dry lithography

Penryn Die Photo



45 nm next generation Intel® Core™2 family processor

410 million transistors for dual core, 820 million for quad core

World's first working 45 nm CPU

Penryn Family Processors

Grows the performance and energy efficiency lead established by Intel® Core^{TM}2 family and Intel® Xeon^{TM} family processors

- Next step in Intel's rapid technology cadence with *second generation quad core in production 2H '07*
- Family codename *Penryn* with server, workstation, desktop, and mobile optimized versions
- New microarchitecture features for even greater performance and new capabilities
- New Intel® SSE4 instructions expand capabilities and performance for media/HPC applications
- Higher core speeds and larger caches
- Leading energy efficiency through design, new power management modes and Intel's 45 nm silicon process

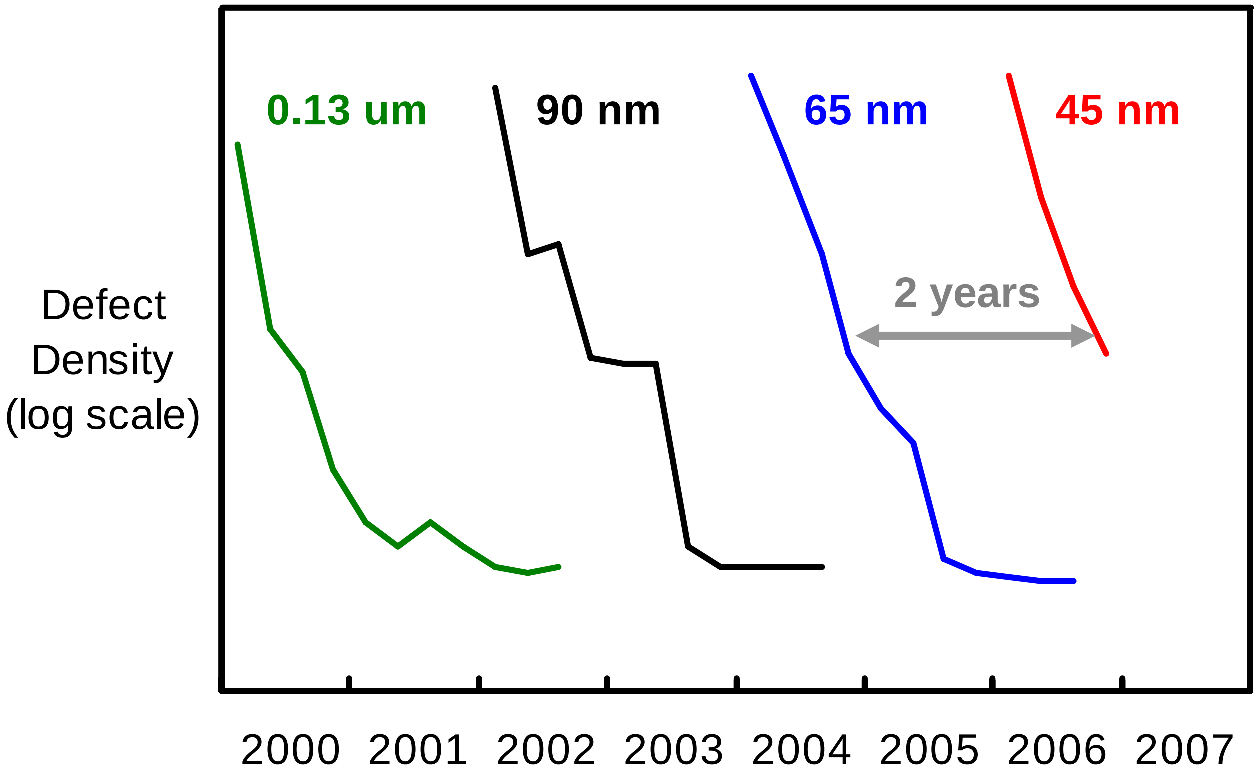
Design is out of fab and working

Penryn First Silicon Boots

Windows* Vista*, Mac OS X*, Windows* XP and Linux

* Other names and brands may be claimed as the property of others.

45 nm Yield Improvement Trend



45 nm defect reduction trend at expected 2 year offset from 65 nm

45 nm on track for production ramp in 2H '07

45 nm Manufacturing Fabs

D1D
Oregon

Ramp in 2H '07

Fab 32
Arizona

Ramp in 2H '07

Fab 28
Israel

Ramp in 1H '08

Three 300 mm factories are planned to be manufacturing 45 nm products by 1H '08

Summary

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- Working 45 nm microprocessors have been made using these revolutionary high-k + metal gate transistors
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Intel is pulling further ahead of the competition

Risk Factors

This presentation contains forward-looking statements that involve a number of risks and uncertainties. These statements do not reflect the potential impact of any mergers, acquisitions, divestitures, investments or other similar transactions that may be completed in the future. The information presented is accurate only as of today's date and will not be updated. In addition to any factors discussed in the presentation, the important factors that could cause actual results to differ materially include the following: Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term, significant pricing pressures, and product demand that is highly variable and difficult to forecast. Additionally, Intel is transitioning to a new microarchitecture on 65nm process technology in all major product segments, and there could be execution issues associated with these changes, including product defects and errata along with lower than anticipated manufacturing yields. Revenue and the gross margin percentage are affected by the timing of new Intel product introductions and the demand for and market acceptance of Intel's products; actions taken by Intel's competitors, including product offerings, marketing programs and pricing pressures and Intel's response to such actions; Intel's ability to respond quickly to technological developments and to incorporate new features into its products; and the availability of sufficient inventory of Intel products and related components from other suppliers to meet demand. Factors that could cause demand to be different from Intel's expectations include customer acceptance of Intel and competitors' products; changes in customer order patterns, including order cancellations; changes in the level of inventory at customers; and changes in business and economic conditions. The gross margin percentage could vary significantly from expectations based on changes in revenue levels; product mix and pricing; capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; excess or obsolete inventory; manufacturing yields; changes in unit costs; impairments of long-lived assets, including manufacturing, assembly/test and intangible assets; and the timing and execution of the manufacturing ramp and associated costs, including start-up costs. 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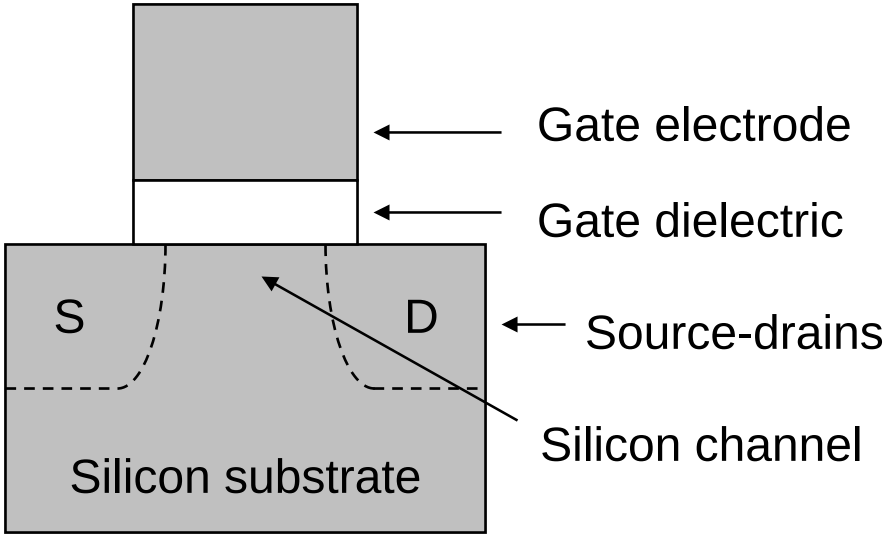
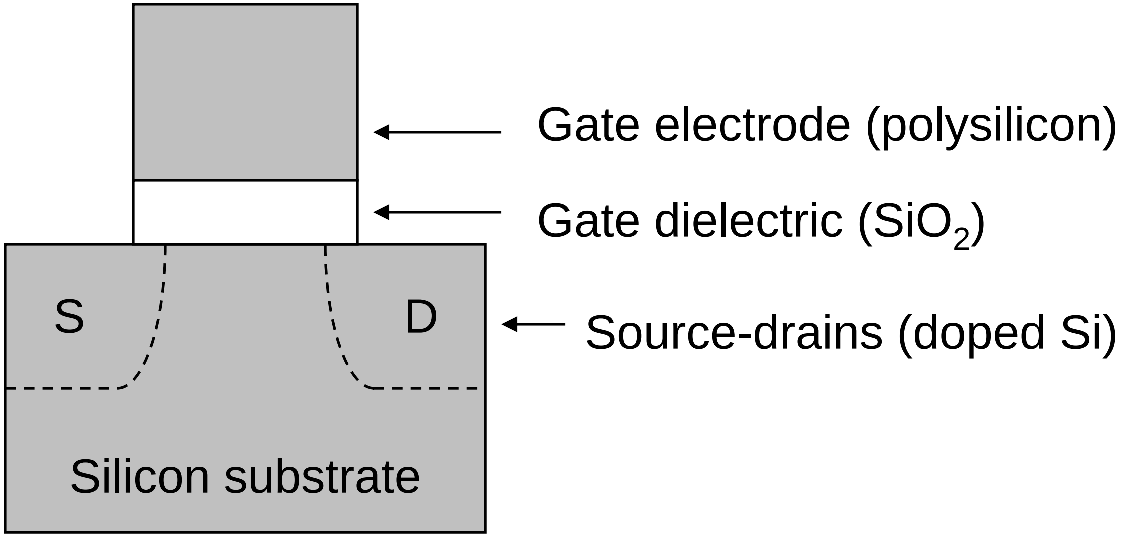
Background Information

High-k + Metal Gate Transistor Tutorial



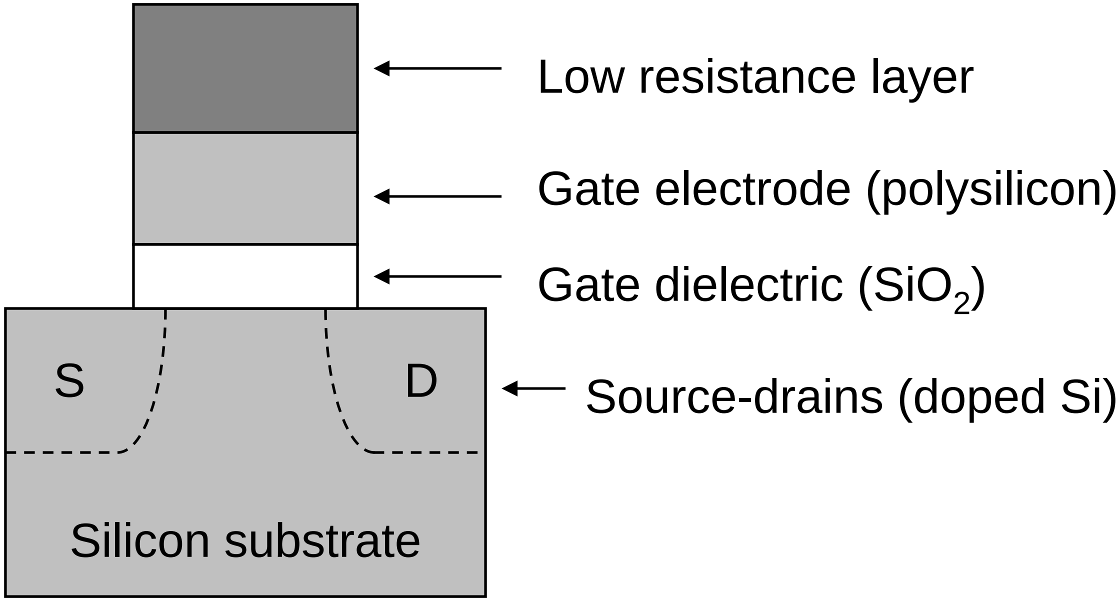
Transistors consist of these key structures

High-k + Metal Gate Transistor Tutorial



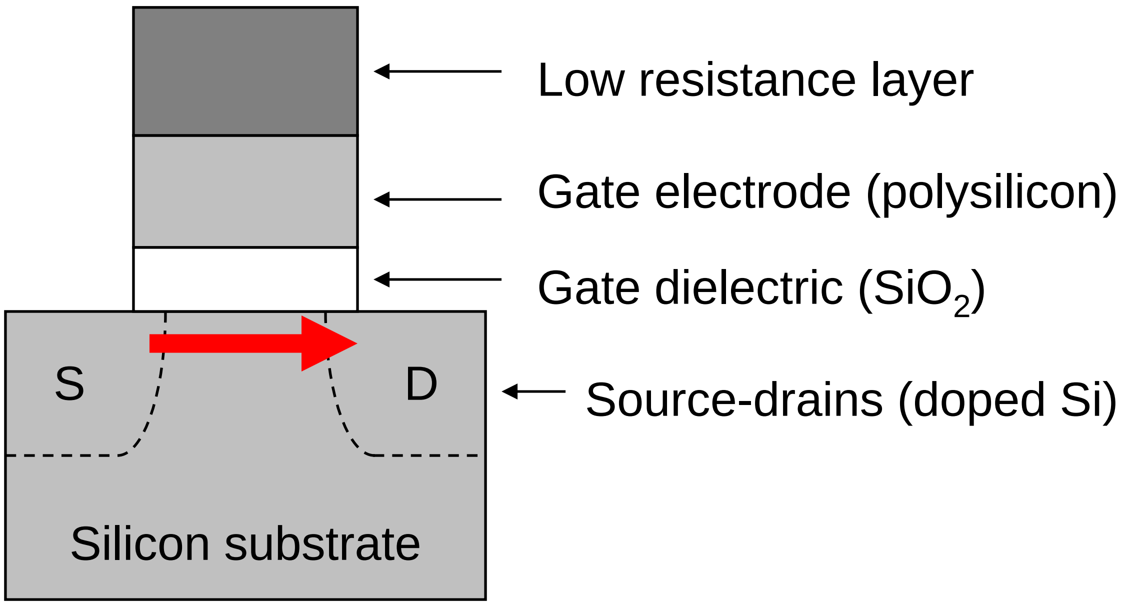
Since the late 1960's transistors have been made with these basic materials

High-k + Metal Gate Transistor Tutorial



A low resistance capping layer was added in the 1980's to help improve transistor performance

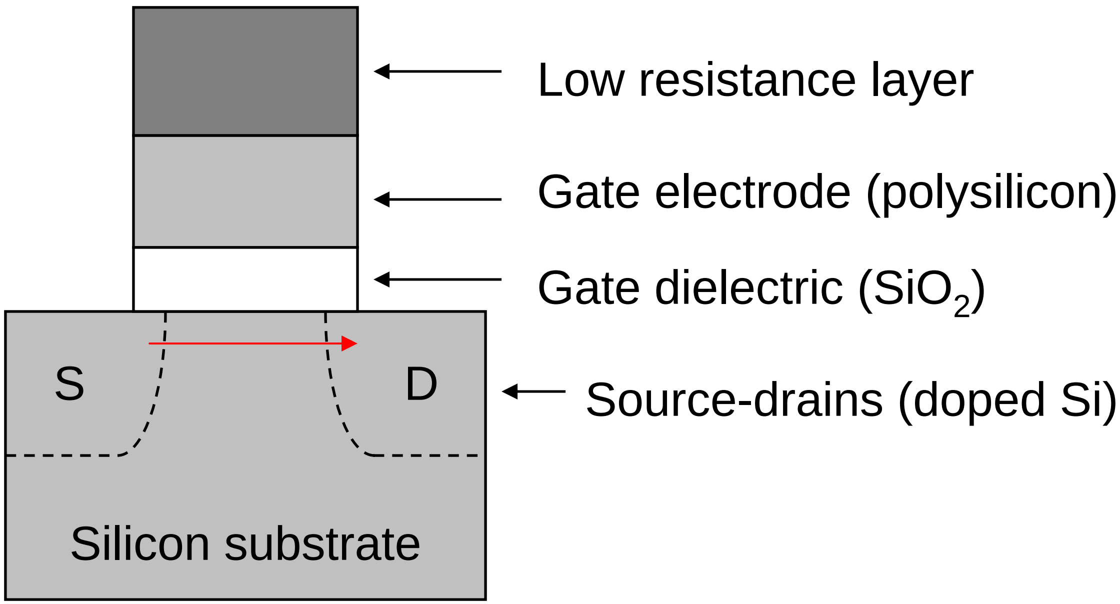
High-k + Metal Gate Transistor Tutorial



Transistors act as an electrical switch

In the “on” state current flow from source to drain should be high

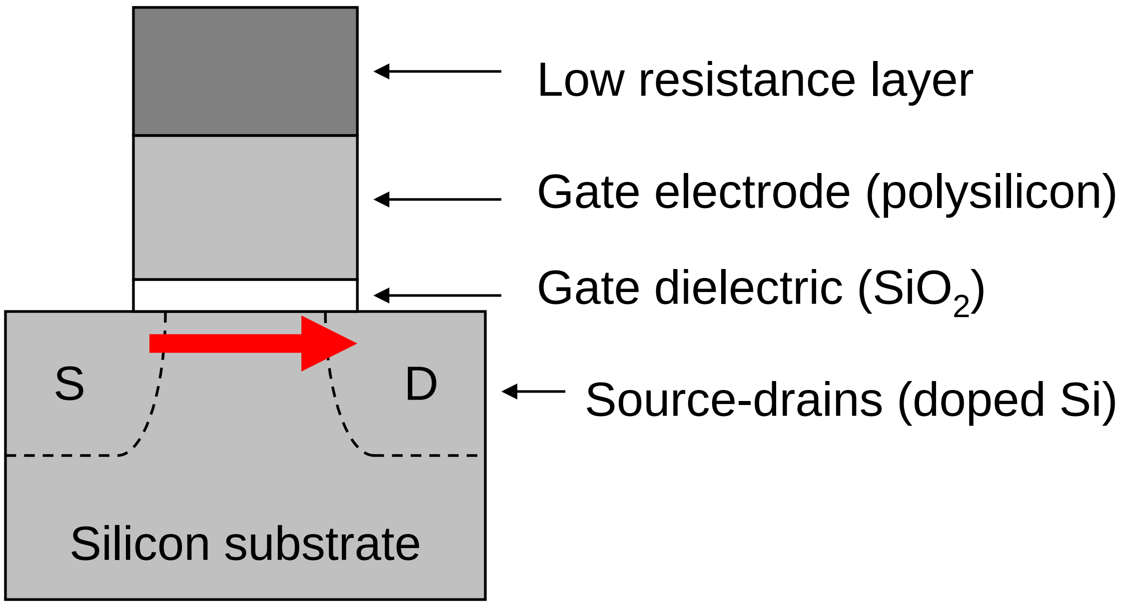
High-k + Metal Gate Transistor Tutorial



Transistors act as an electrical switch

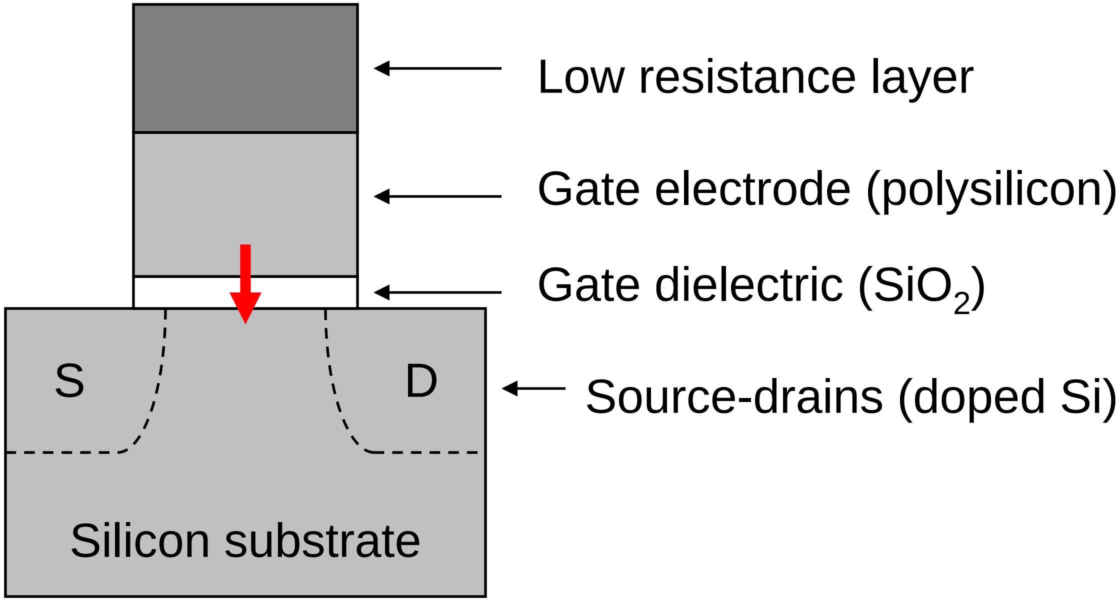
In the “off” state current flow from source to drain should be low

High-k + Metal Gate Transistor Tutorial



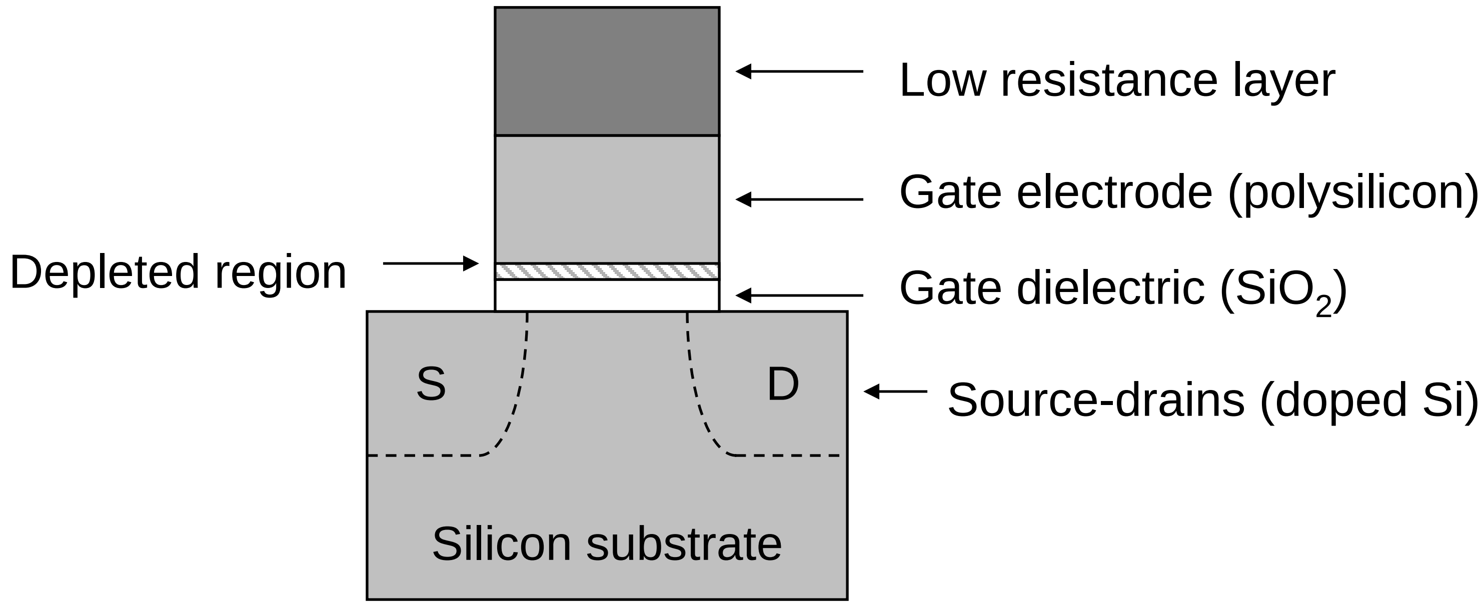
Thinning the gate dielectric increases gate electrode coupling to the Si channel (increases gate field effect) and helps to increase "on" current and reduce "off" current

High-k + Metal Gate Transistor Tutorial



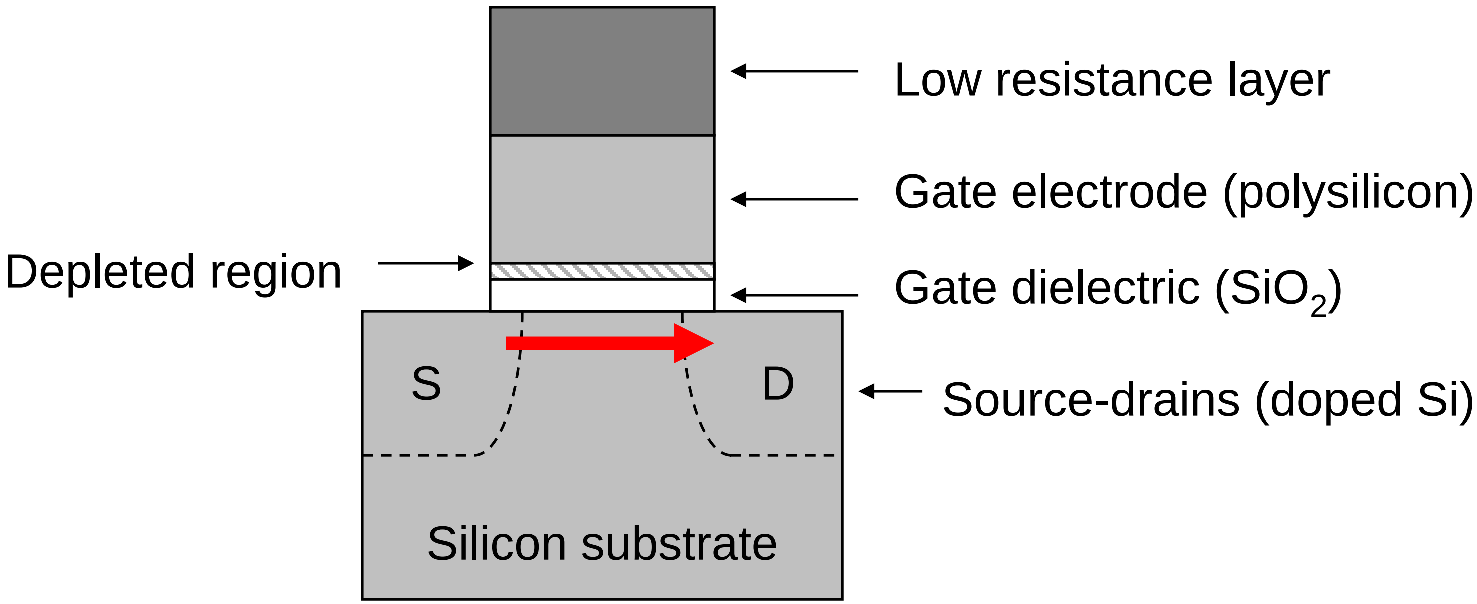
Thinning the gate dielectric too much can cause leakage current to flow through the normally insulating gate dielectric

High-k + Metal Gate Transistor Tutorial



During normal operation a thin region depleted of conducting carriers is formed at the bottom of polysilicon gates, resulting in an undesired increase in the effective thickness of the gate dielectric

High-k + Metal Gate Transistor Tutorial



The thicker effective gate dielectric results in degraded “on” current and increased “off” current

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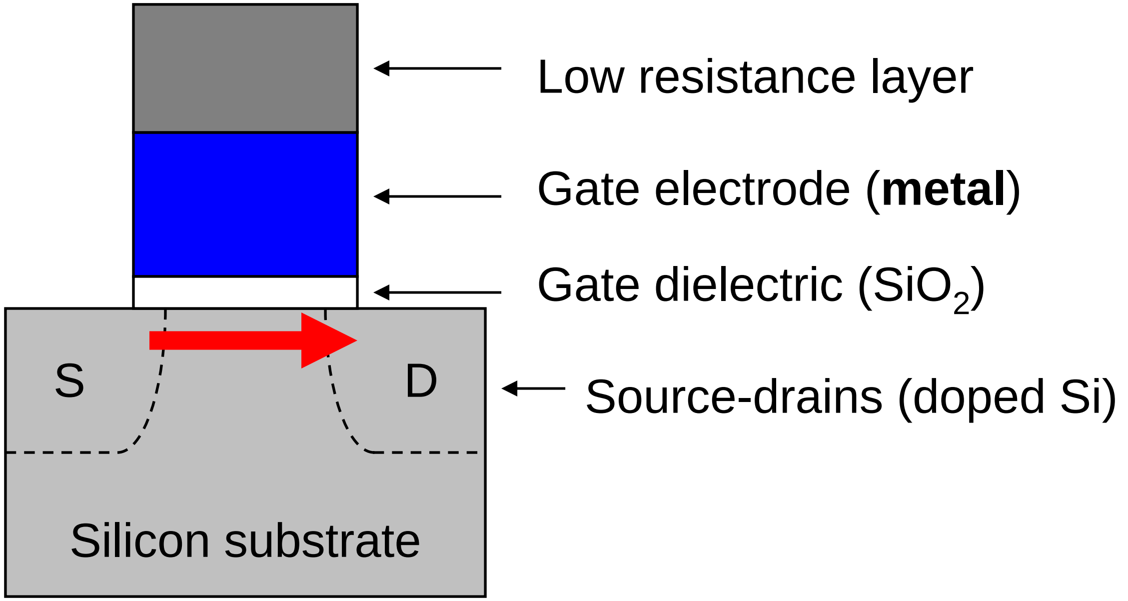
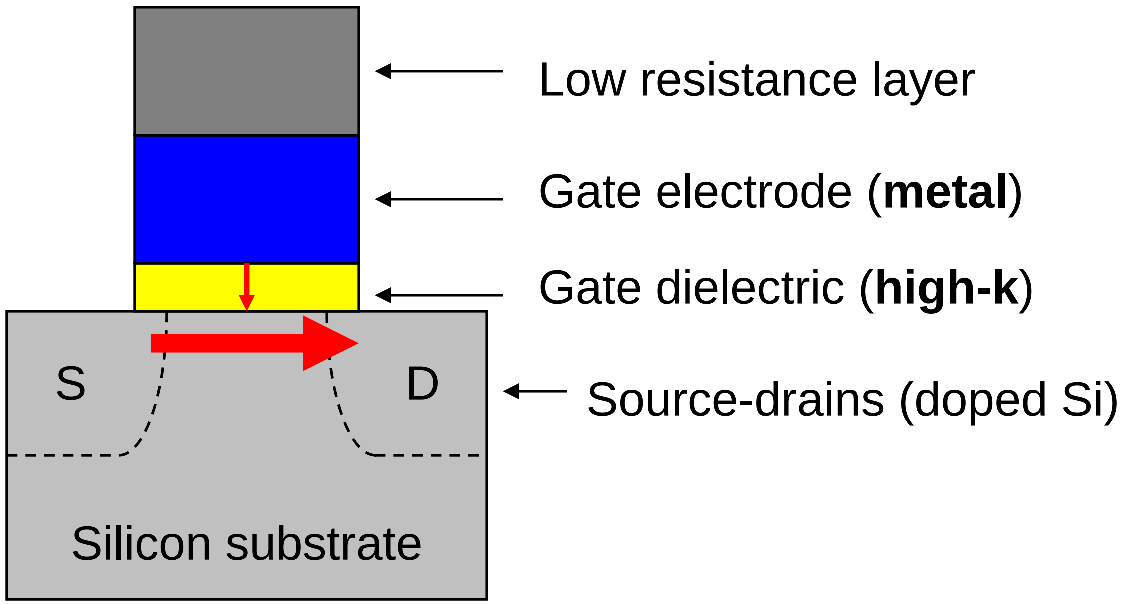


Converting the polysilicon gate electrode to metal eliminates the depleted region and increases the gate field effect resulting in increased “on” current and decreased “off” current

High-k + Metal Gate Transistor Tutorial



Converting SiO_2 gate dielectric to high-k allows thickening the dielectric layer while also increasing the gate field effect resulting in increased “on” current, decreased “off” current and significantly decreased gate leakage