45nm High-k + Metal Gate Strain-Enhanced Transistors

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Abstract

Two key process features that are used to make 45nm generation metal gate + high-k gate dielectric CMOS transistors are highlighted in this paper. The first feature is the integration of stress-enhancement techniques with the dual metal-gate + high-k transistors. The second feature is the extension of 193nm dry lithography to the 45nm technology node pitches. Use of these features has enabled industry-leading transistor performance and the first high volume 45nm high-k + metal gate technology.

Introduction

High-k + metal gate transistors have been incorporated into our 45nm logic technology to provide improved performance and significantly reduced gate leakage [1]. Hi-k + Metal gates have also been shown to have improved variability at the 45nm node [2]. The transistors in this work feature 1.0nm EOT high-k gate dielectrics with dual workfunction metal gate electrodes and 35nm gate lengths. The addition of new gate materials is complicated by the need to mesh the process requirements of the metal gate process with the uniaxial strain-inducing components that have become central to the transistor architecture. The resultant process flow needs to ensure that the performance benefits of both elements are fully realized.

The standard scaling requirements for the strained silicon components and for the gate and contact pitches also needs to be addressed at the 45nm node. Using 193nm dry lithography for critical layers at the 45nm technology node is preferred over moving to 193nm immersion lithography due to lower cost and greater maturity of the toolset. In order to achieve the 160nm gate and contact pitch requirements, unique gate and contact patterning process flows have been implemented.

Strain + Metal Gate: Key process considerations/results

The most commonly used techniques for implementing strain in the transistors include embedded SiGe in the PMOS S/D, stress memorization for the NMOS and a nitride stress capping layer for NMOS and PMOS devices. The two common methods for introducing a metal gate to the standard CMOS flow include, either "gate-first" or "gate-last" process. Most comparisons of these two process flows focus on the ability to select the appropriate workfunction metals, the ease of integration or the ability to scale but typically fail to comprehend the interaction with the strain-inducing techniques.

In the gate-first flow (Fig. 1), the dual-metal processing is completed prior to the polysilicon gate deposition. The metal-gates are then subtractively etched along with the poly gates prior to S/D formation. In contrast, for the gate-last flow, a standard polysilicon gate is deposited after the high-k gate dielectric deposition, which is followed by standard polysilicon processing through the salicide and the 1st ILD deposition. The wafer is then planarized and the dummy poly gate removed. The dual-metal gates are then deposited along with a low-resistance gate fill material. The excess metal is then polished off and followed by contact processing (Fig. 2).

By removing the poly gate from transistor after the stress-enhancement techniques are in place, it has been shown that the stress benefit from the embedded S/D SiGe process can be enhanced [3]. This is a key benefit for the gate-last process and can be illustrated in simulation with an estimated 50% increase in lateral compressive stress by removal of the polysilicon gate (Fig. 3). The Ge concentration of the SiGe stressors was increased from 22% in our 65nm technology [4] to 30% in 45nm. The combined impact of the increased Ge fraction and the strain enhancement from the gate last process allow for 1.5x higher hole mobility compared to 65nm despite the scaling of the transistor pitch from 220nm to 160nm.

Two methods of stress enhancement have been employed on the NMOS in this technology. First, the loss of the nitride stress layer benefit due to scaling the pitch from 65nm has been overcome by the introduction of trench contacts and tailoring the contact fill material to induce a tensile stress in the channel. The NMOS response to tensile vs. compressive contact fill materials is shown in figure 4. The trench contact fill material impact on the PMOS device is mitigated by use of the raised S/D inherent to the embedded SiGe S/D process.

The S/D component of stress memorization is compatible with the gate-last flow while the poly gate component would be compromised [5]. The poly gate component is replaced by Metal Gate Stress (MGS): modifying the metal-gate fill material to directly induce stress in the channel [6]. By introducing a compressive stress gate fill material the performance of the NMOS device is enhanced and additive to the contact fill technique [Fig. 5]. By use of a dual-metal process with PMOS 1st, the stress of the NMOS gate is decoupled from the PMOS gate through optimization of the PMOS gate stack to buffer the stress.

Through the strain enhancement and elimination of poly depletion both the saturation and linear drive currents improved (Fig. 6,7). Subthreshold characteristics are well-behaved (Fig. 8). Ring oscillator data for a fanout of 2 gate delay shows an improvement of 23% is demonstrated (Fig. 9). The table in figure 10 breaks out the RO gains between Idsat, Idlin and the gate and junction capacitances.

193nm Dry Patterning @ 45nm

The gate patterning process uses a double patterning scheme. Initially the gate stack is deposited including the polysilicon and hardmask deposition. The first lithography step patterns a series of parallel, continuous lines. Only discrete pitches are allowed, with the smallest at 160nm. A second masking step is then used to define the cuts in the lines. The 2-step process enables abrupt poly endcap regions allowing tight CTG design rules (Fig. 11).

The contact patterning process also uses a similar restriction to facilitate lithography. Trench diffusion contacts run parallel to the gates with discrete pitches, while trench gate contacts run orthogonal to the gates. Use of trench contacts has the added benefits of lowering the contact resistance by >50% and allowing use as a local interconnect which improves SRAM/logic density by up to 10%.

Conclusion

High-k + metal gate transistors have been integrated into a manufacturable 45nm CMOS process using 193nm dry lithography. The significant strain enhancement benefits of the gate-last process flow have been highlighted. The process has demonstrated record drive current at low leakage.

References

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Gate-First	Gate-Last
-Isolation	-Isolation
-Hi-k gate deposition	-Hi-k gate deposition
-Dual Metal-Gate Dep	-Poly-Si gate dep/patterning
-Poly-Silicon deposition	-S/D formation
-Poly-Si/metal etch	-Salicide/Contact etch stop
-S/D formation	-1st ILD dep/polish
-Salicide/Contact etch stop	**-Poly Si gate removal**
-1st ILD dep/polish	**-Dual-Metal Gate dep**
-Contact formation	-Contact formation

Fig.1 Comparison of unique steps in gate-first and gate-last process flows. Key differences are highlighted in bold.

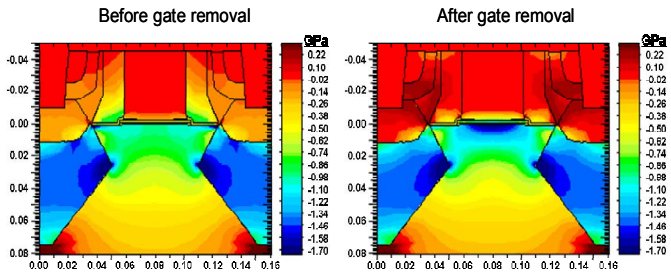

Fig.3 Stress contours in the PMOS transistor before and after the removal of the polysilicon dummy gate. Stress in the channel is shown to increase 50% from ~0.8GPa to >1.2 GPa.

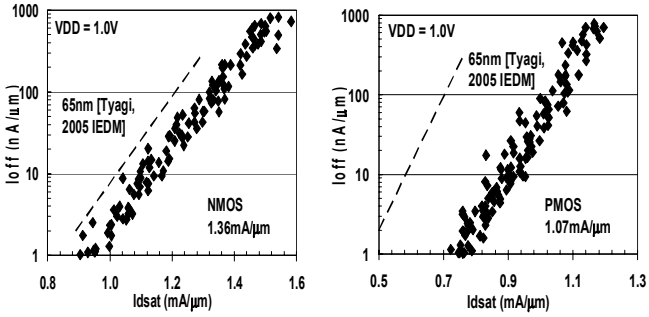

Fig.6 Overall Ion-Ioff for NMOS & PMOS relative to previous generation. 45nm transistors are benchmarked at 160nm pitch.

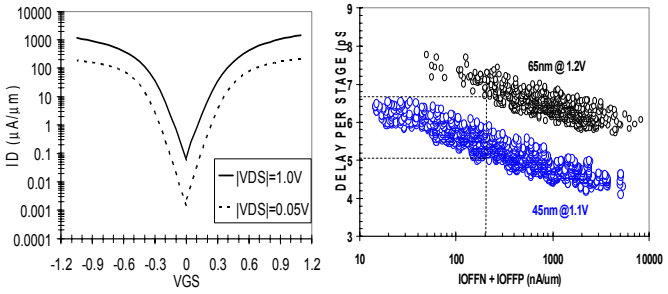

Fig.8 Subthreshold Id-Vgs for both NMOS and PMOS transistors

Fig.9 RO data for a fanout of 2 showing 23% improvement in gate delay vs. 65nm, despite voltage scaling from 1.2V to 1.1V.

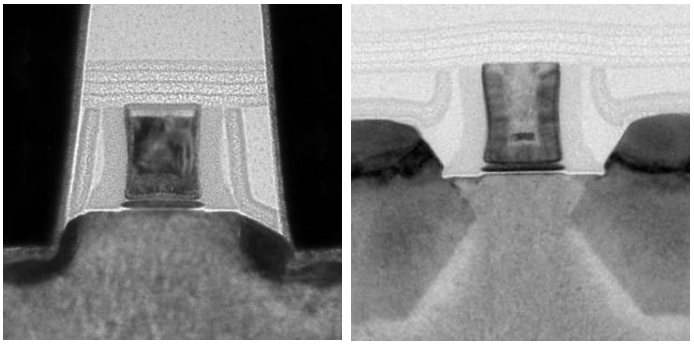

Fig.2 TEMs of High-k + Metal Gate NMOS and PMOS transistors

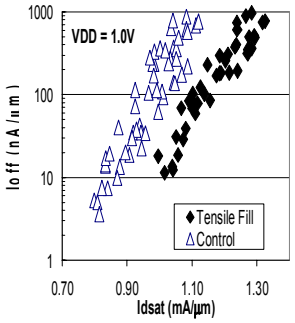

Fig.4 Ion-Ioff benefit of tensile Contact Fill showing a 10% NMOS Idsat benefit. Contact resistance is matched for the two fill materials.

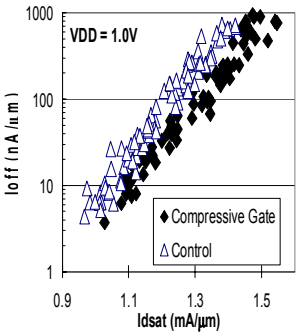

Fig.5 Ion-Ioff benefit of compressive gate stress showing a 6% NMOS Idsat gain. Tensile Contact Fill is used on both sets of data.

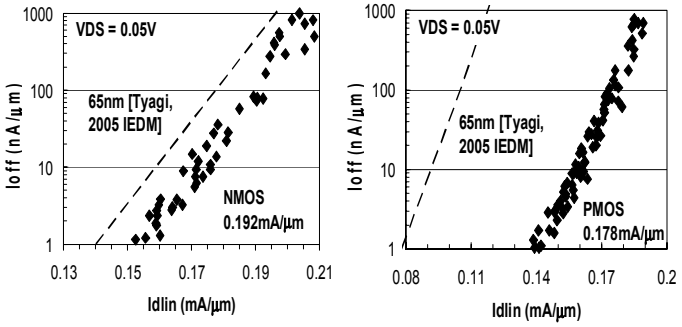

Fig. 7 NMOS/PMOS Idlin vs. Ioff relative to previous generation. 45nm transistors are benchmarked at 160nm pitch

Component	Benefit
PMOS Idsat	+13
PMOS Idlin	+18
NMOS Idsat	+3
NMOS Idlin	+2
Cjunction	+2
Cgate/Cov	-8%
Voltage Scaling	-7%
Total	+23%

Fig. 10 Breakdown of RO gains vs. 65nm results. The voltage scaling term accounts for the reduction in VDD from 1.2V (65nm) to 1.1V (45nm).

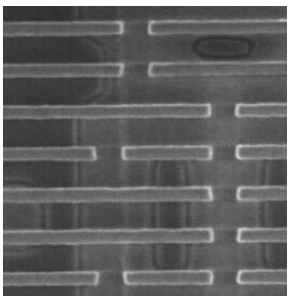

Fig.11 Top-down SEM post poly patterning process showing 160nm poly pitch and square poly ends, devoid of rounding.