45nm High-k + Metal Gate Strain-Enhanced Transistors

C. Auth, A. Cappellani, J.-S. Chun, A. Dalis, A. Davis, T. Ghani, G. Glass, T. Glassman, M. Harper, M. Hattendorf, P. Hentges, S. Jaloviar, S. Joshi, J. Klaus, K. Kuhn, D. Lavric, M. Lu, H. Mariappan, K. Mistry, B. Norris, N. Rahhal-orabi, P. Ranade, J. Sandford, L. Shifren%, V. Souw, K. Tone, F. Tambwe, A. Thompson, D. Towner, T. Troeger, P. Vandervoorn, C. Wallace, J. Wiedemer, C. Wiegand

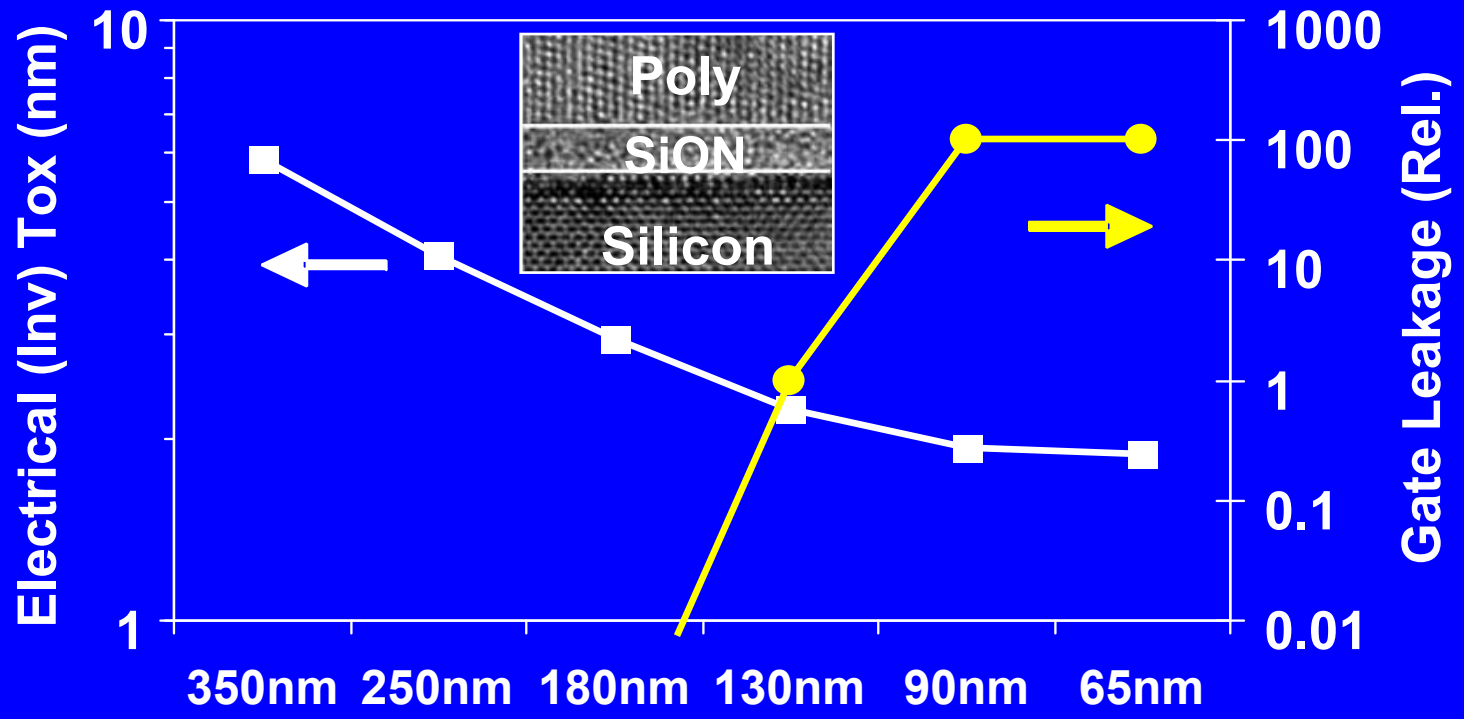
Portland Technology Development, %PTM
Intel Corporation

Outline

- Introduction
- Metal-Gate + Strain Integration
- Transistor/Circuit Results
- Manufacturing
- Conclusions

Introduction

- SiON scaling running out of atoms
- Poly depletion limits inversion T_{OX} scaling
  - -> Need High-K + Metal Gate



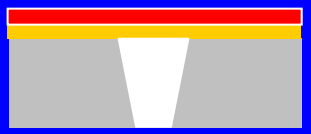
High-k + Metal Gate Benefits

- High-k gate dielectric
  - Reduced gate leakage
  - T_{OX} scaling
- Metal gates
  - Eliminate polysilicon depletion
  - Resolves V_T pinning and poor mobility for high-k gate dielectrics

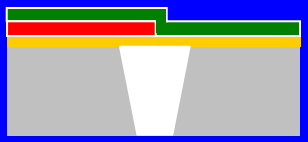
Metal Gate Flow Options

Gate-First

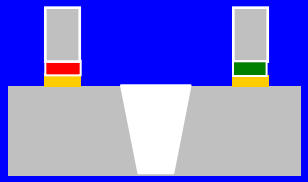
Dep Hi-k & Met 1



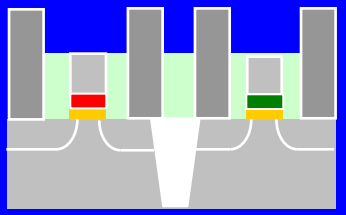
Patt Met 1 & Dep Met 2



Patt Met 2 & Etch Gates

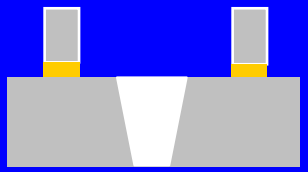


S/D formation & Contacts

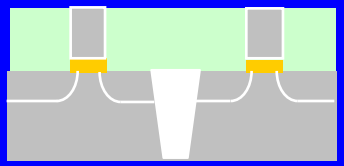


Hik-First, Gate-Last

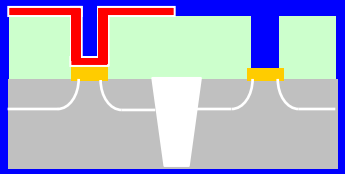
Dep & Patt Hik+Gate



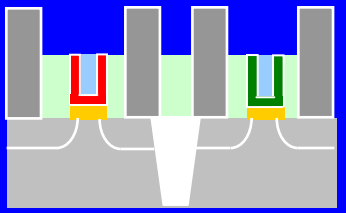
S/D formation & ILD dep/polish



Rem Gate & Patt Met 1



Dep Met 2+Fill & Polish



Metal Gate-Last Benefits

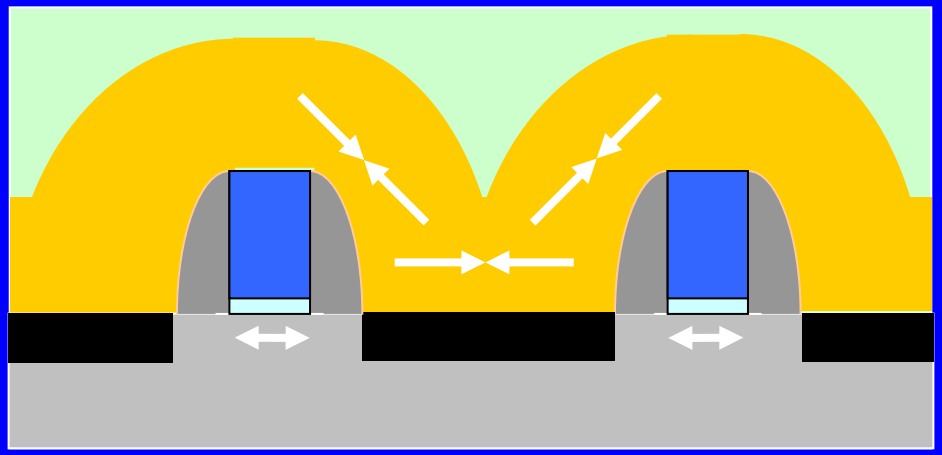
- High Thermal budget available for Midsection
  - Better Activation of S/D Implants
- Low thermal budget for Metal Gate
  - Large range of Gate Materials available
- Significant enhancement of strain
  - Both NMOS and PMOS benefits
- Low cost
  - Total wafer cost adder - 4%

Outline

- Introduction
- Metal-Gate + Strain Integration
- Transistor/Circuit Results
- Manufacturing
- Conclusions

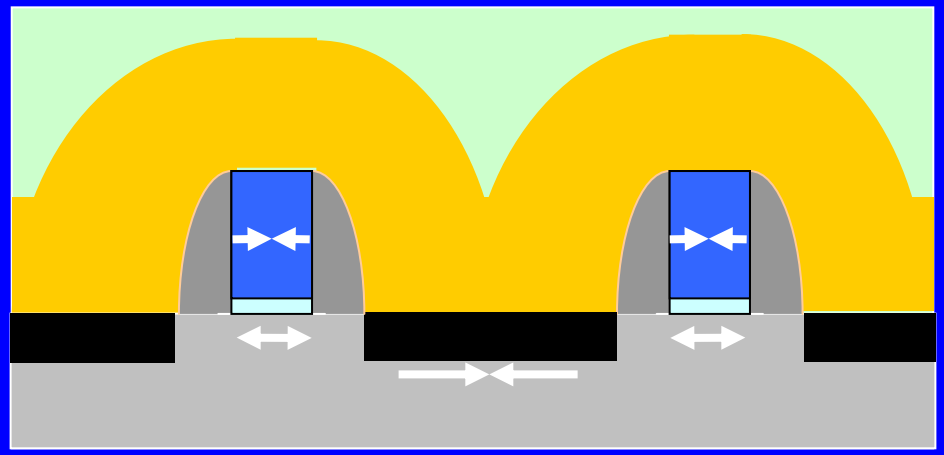
Methods of NMOS Strain at 65nm

- Tensile Nitride Cap
- Stress Memorization
  → Gate + S/D



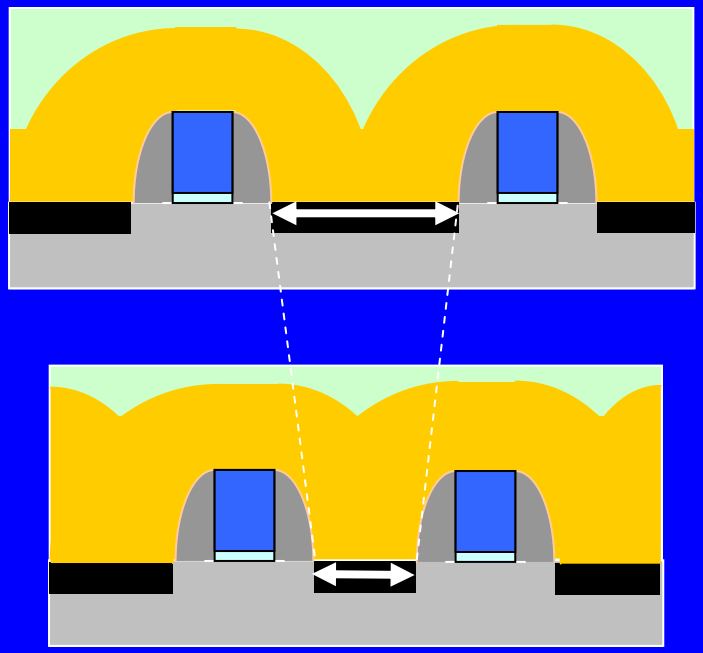
Methods of NMOS Strain at 65nm

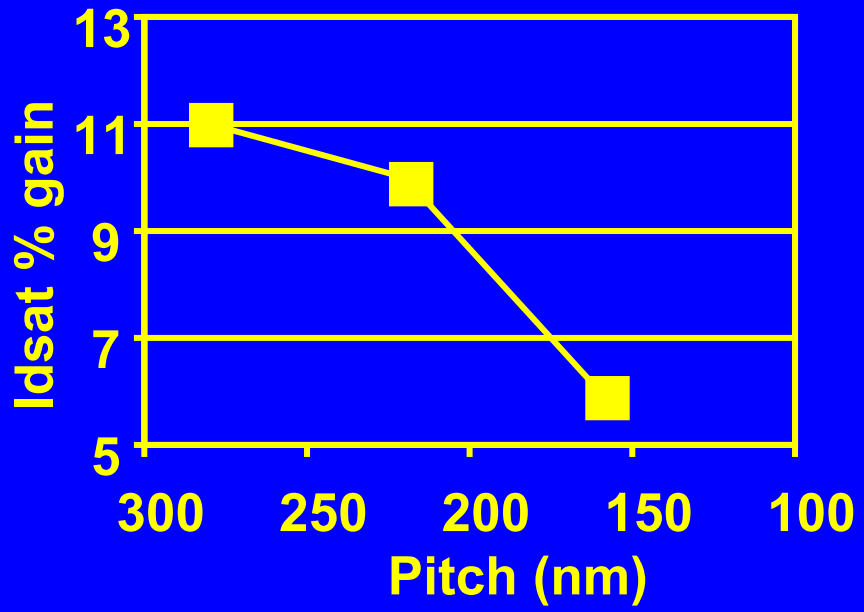
- Tensile Nitride Cap
- Stress Memorization
  → Gate + S/D



NMOS strain: Tensile Cap Layer

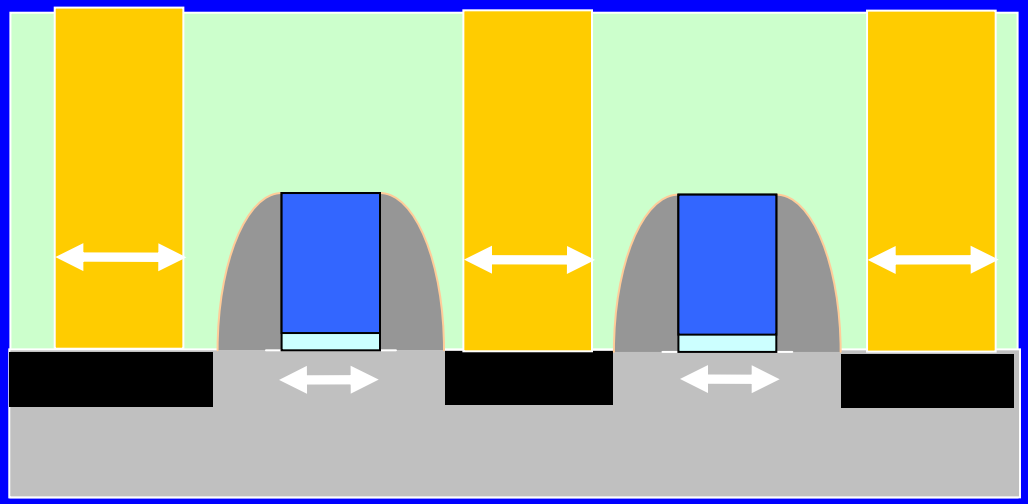
- Running out of space for Nitride Cap Layer
  - Pitch degradation increases with pinchoff of film
  - Requires higher stress & thinner films

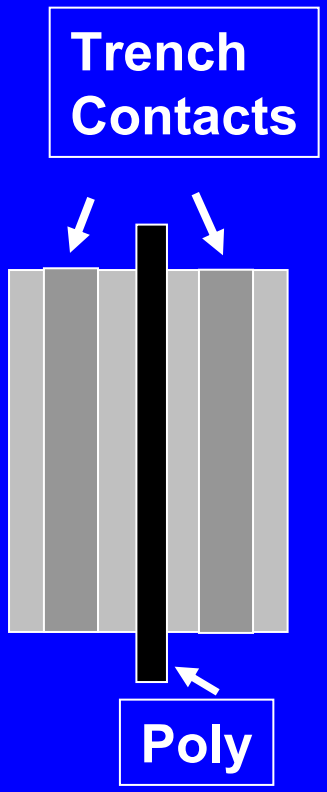




Tensile Contact Stress

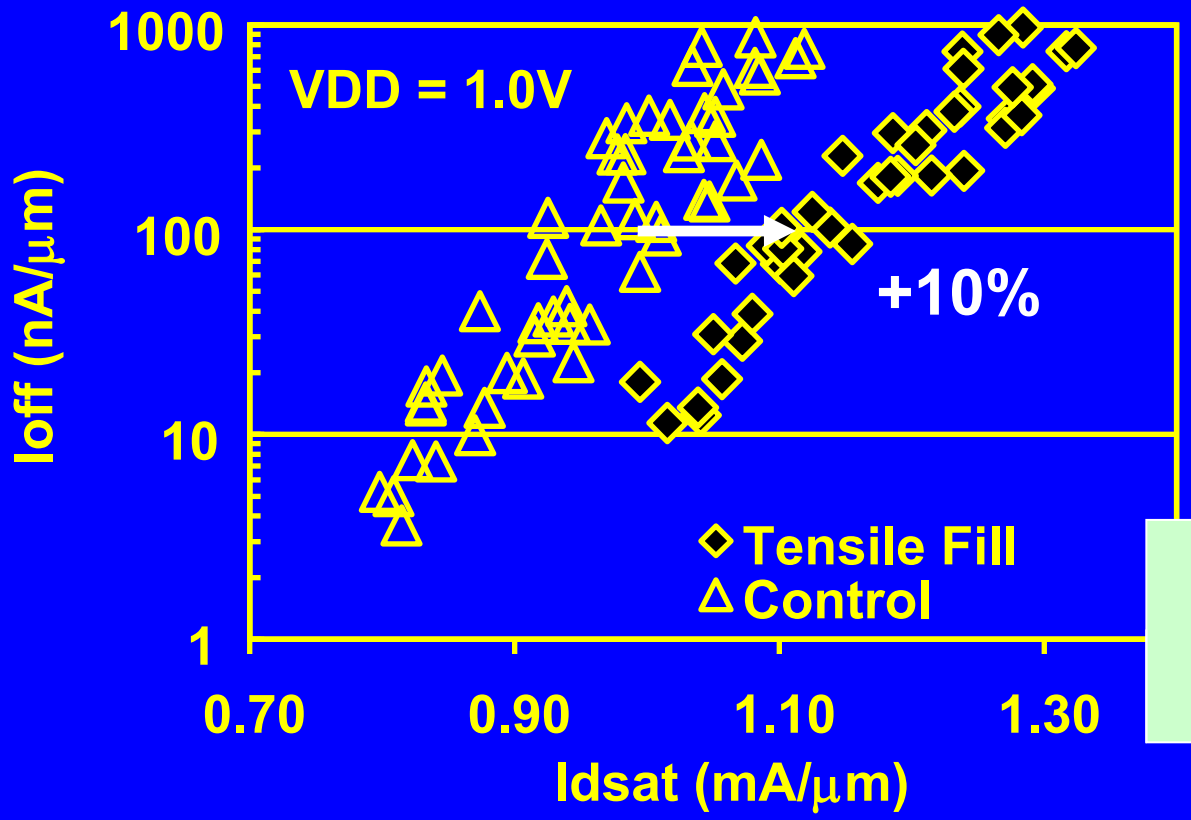
- Use Tensile trench contacts to stress channel

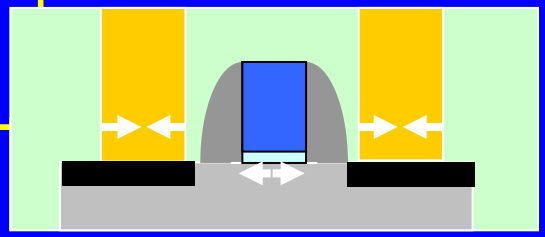




Tensile Contact Stress

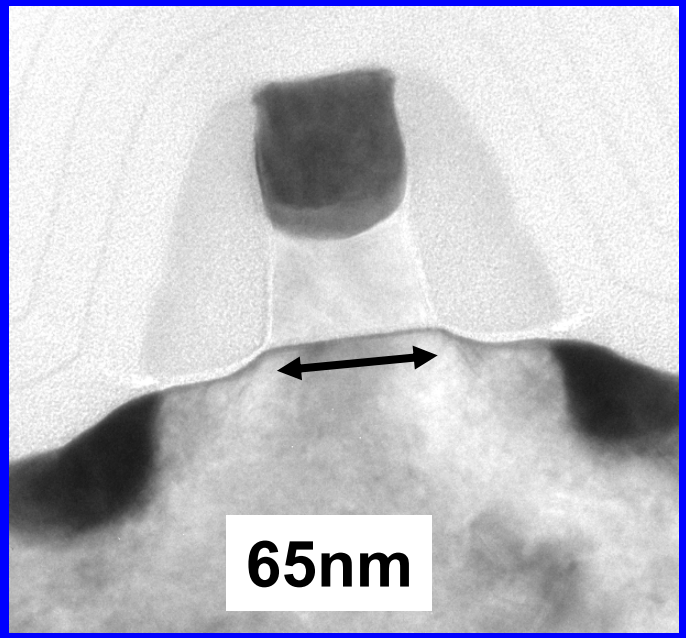
- Use of Tensile trench contacts provide 10% Idsat improvement
- Matched Contact Resistance

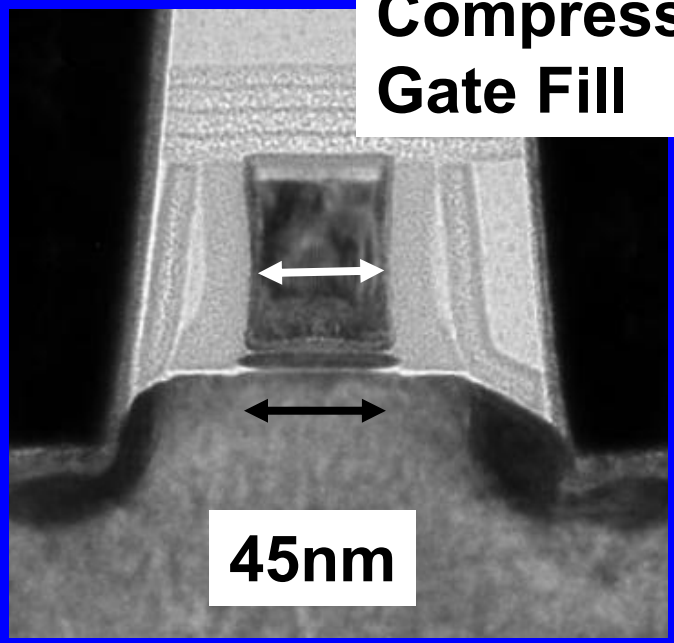




NMOS strain: Metal Gate Stress

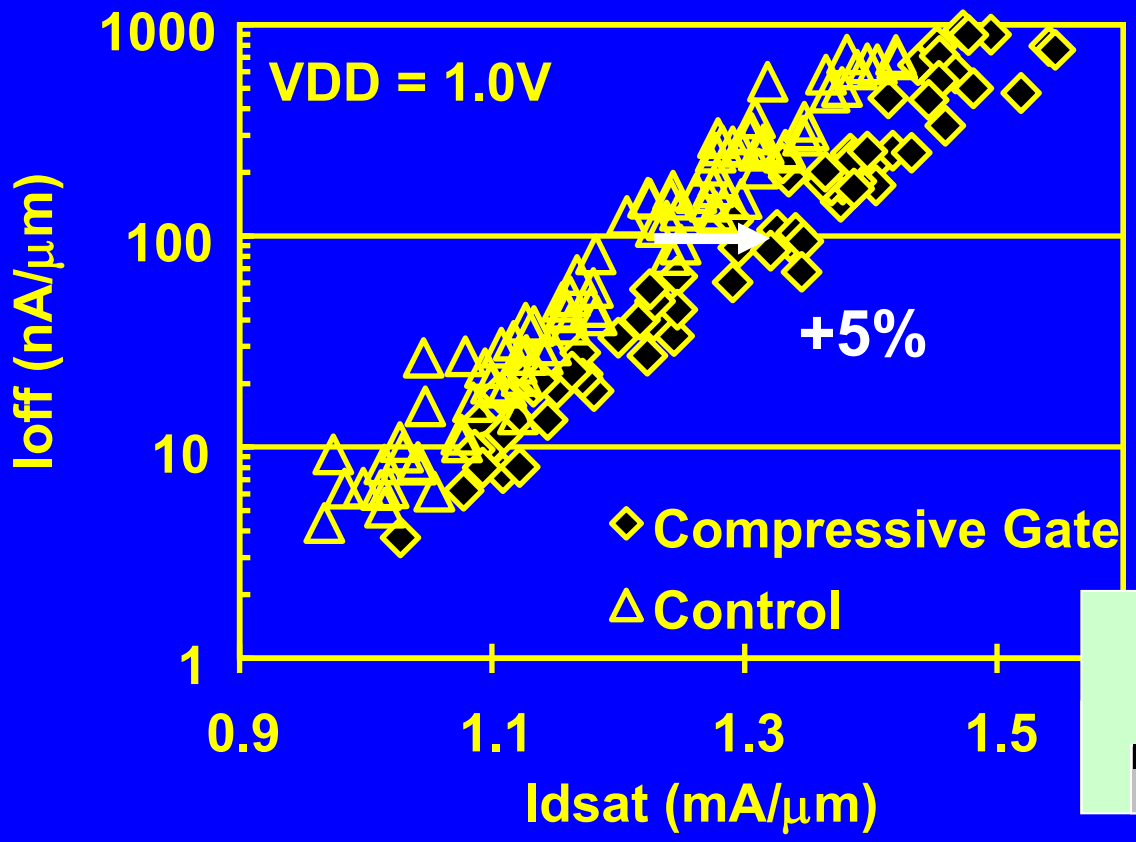
- Gate Stress Memorization incompatible with Gate-Last
- Compressive Gate fill material induces strain directly*
  - **C. Kang, et al, IEDM 2006*

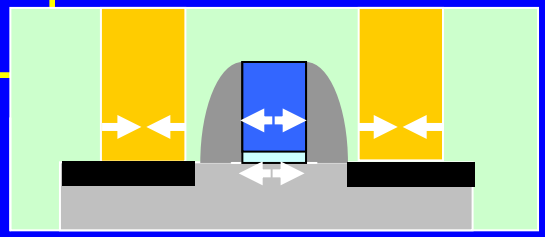




Compressive Gate Stress

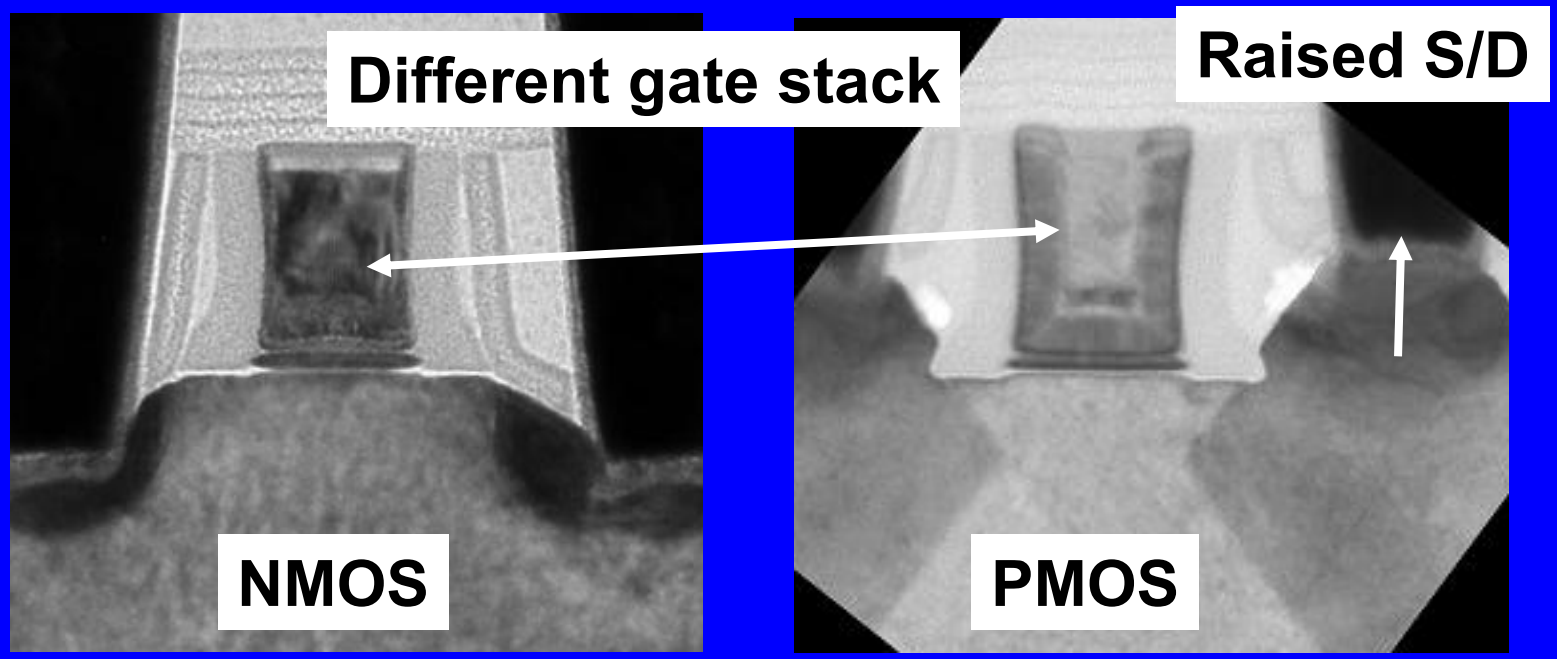
- Compressive Gate Fill shows 5% Idsat improvement
- Additive with Tensile Trench contacts





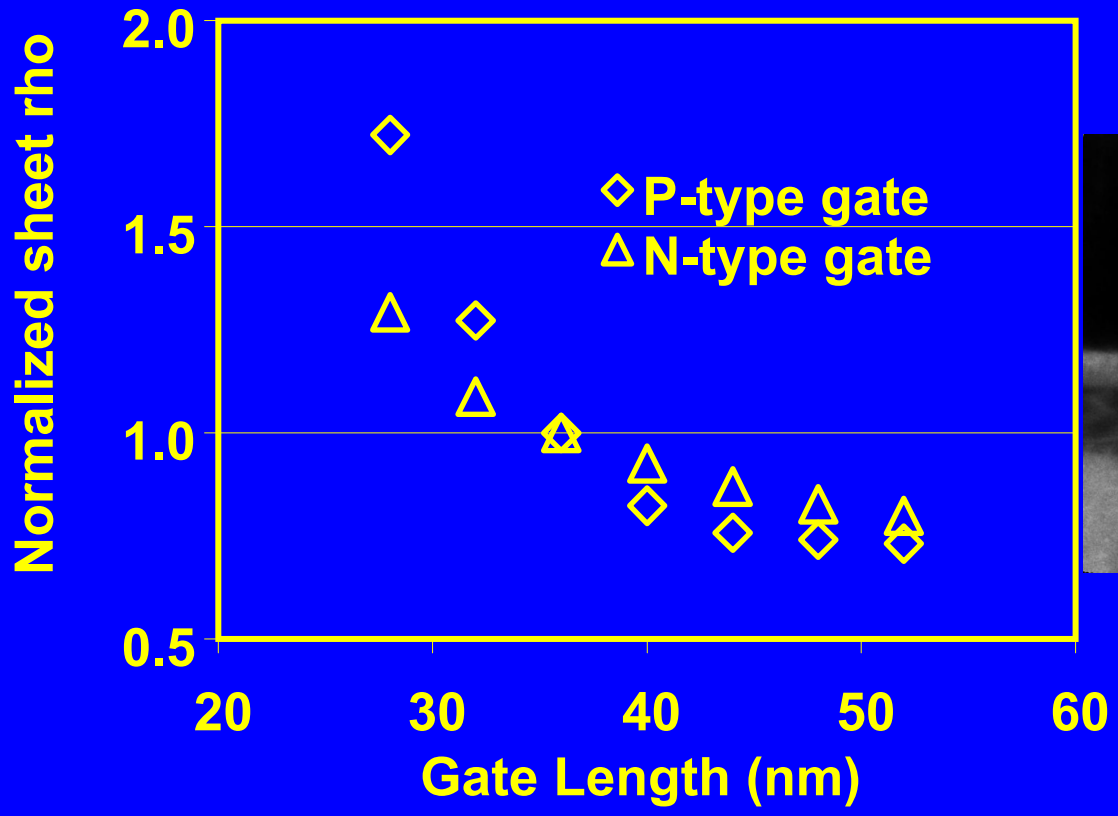
Mitigation of NMOS stress on PMOS

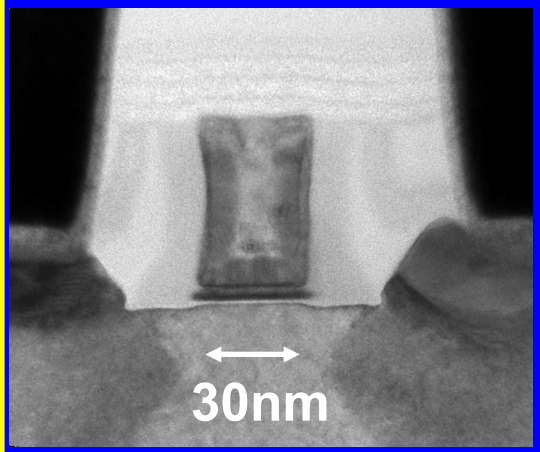
- Tensile Contact fill mitigated by raised SiGe S/D
- Metal Gate Strain compensated by PMOS WFM



Gate Fill scalability for Gate-Last

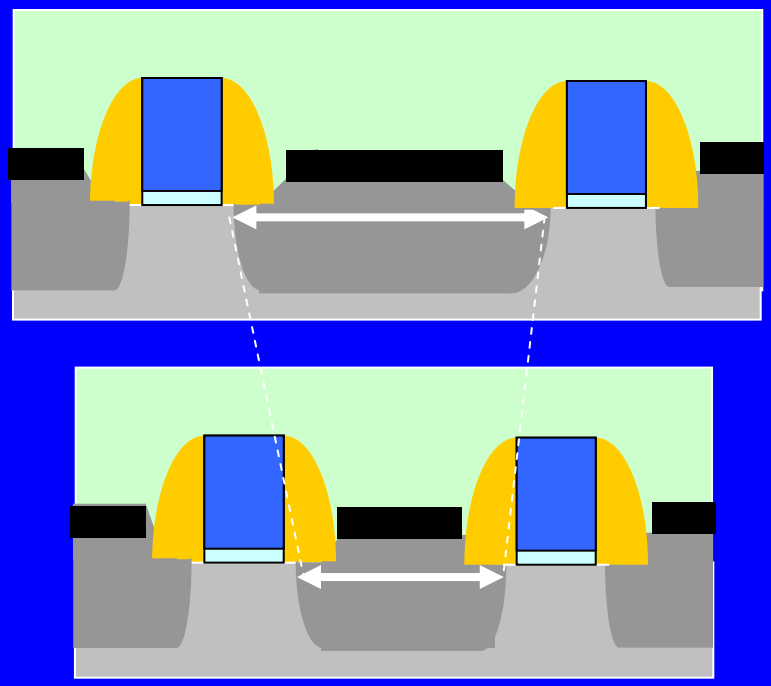
- Capability to <30nm demonstrated

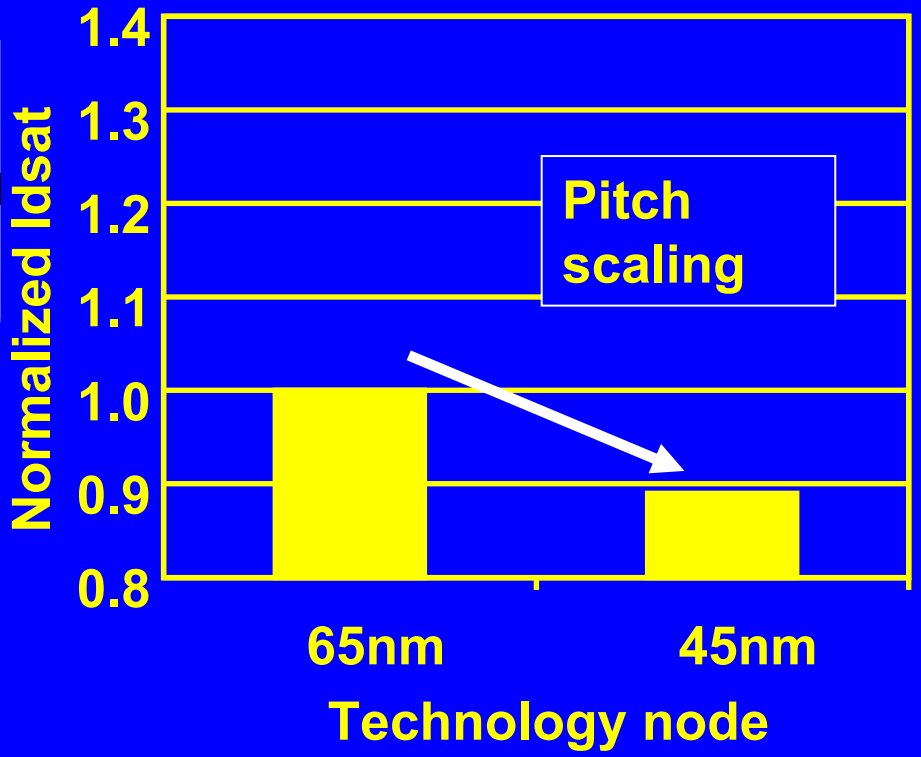




PMOS strain: Pitch dependence

- Embedded SiGe S/D mobility enhancement strongly dependent on pitch



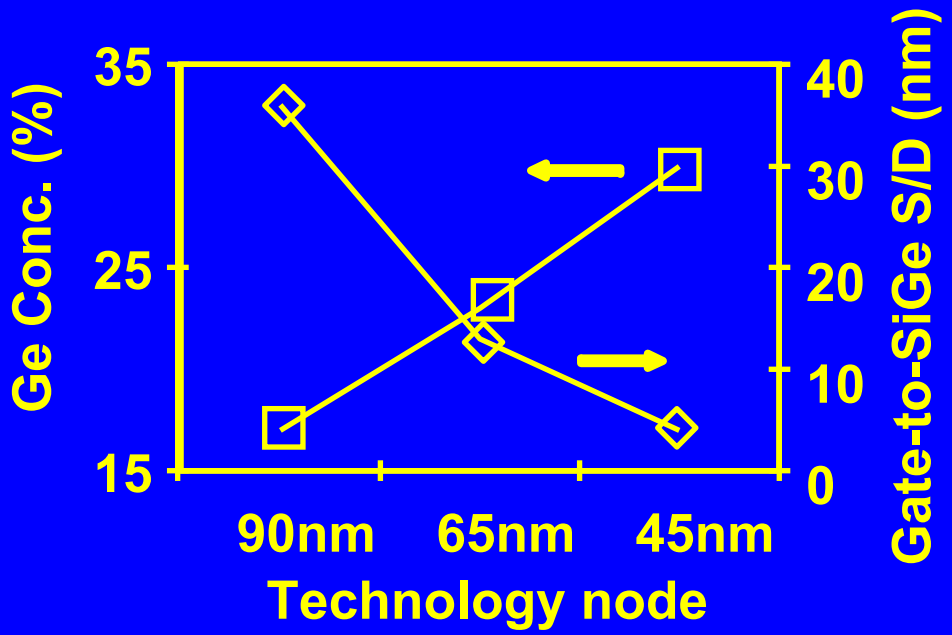


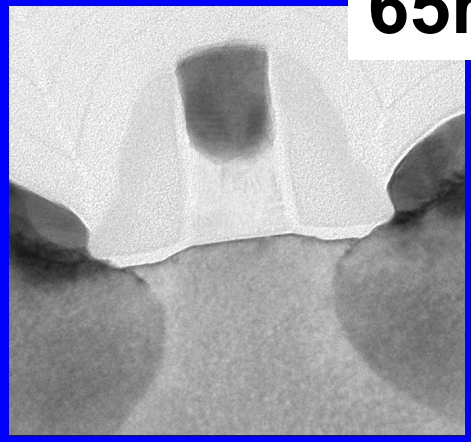
Embedded SiGe S/D

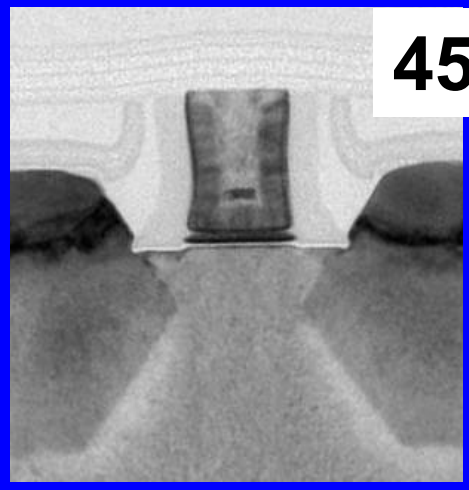
- Continued Scaling for SiGe S/D

1. Ge concentration inc. to 30%

2. Gate → S/D distance reduced



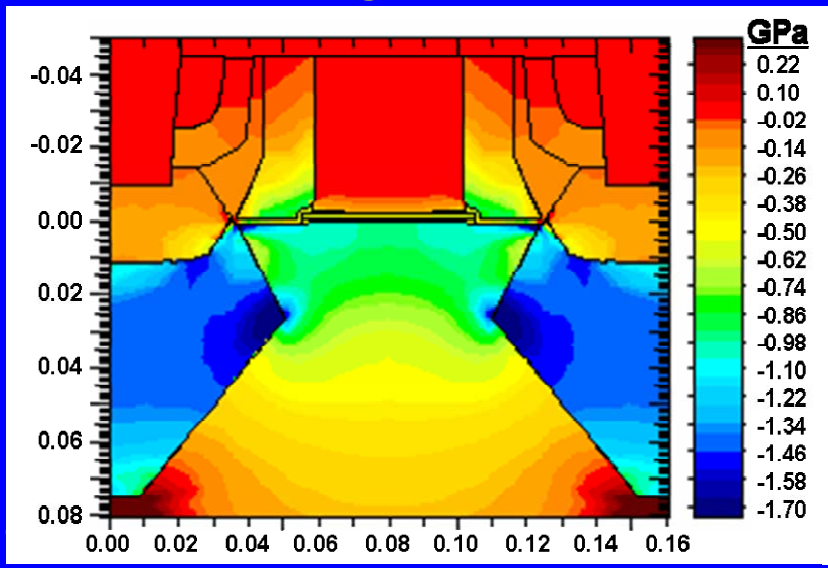




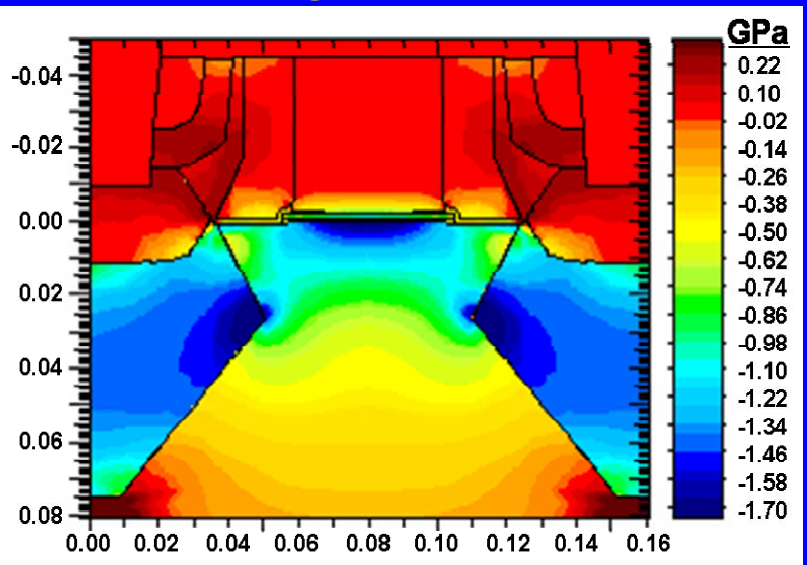
PMOS Strain: Gate-Last Flow

- Use of Gate-Last Flow enhances Embedded SiGe S/D*
  - *J. Wang, et al, VLSI 2007
- Removal of poly gate increases channel stress by 50%

Before gate removal



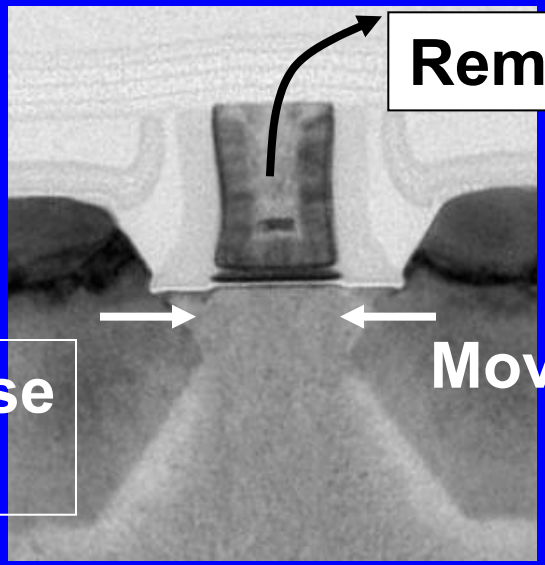
After gate removal



PMOS Strain Components

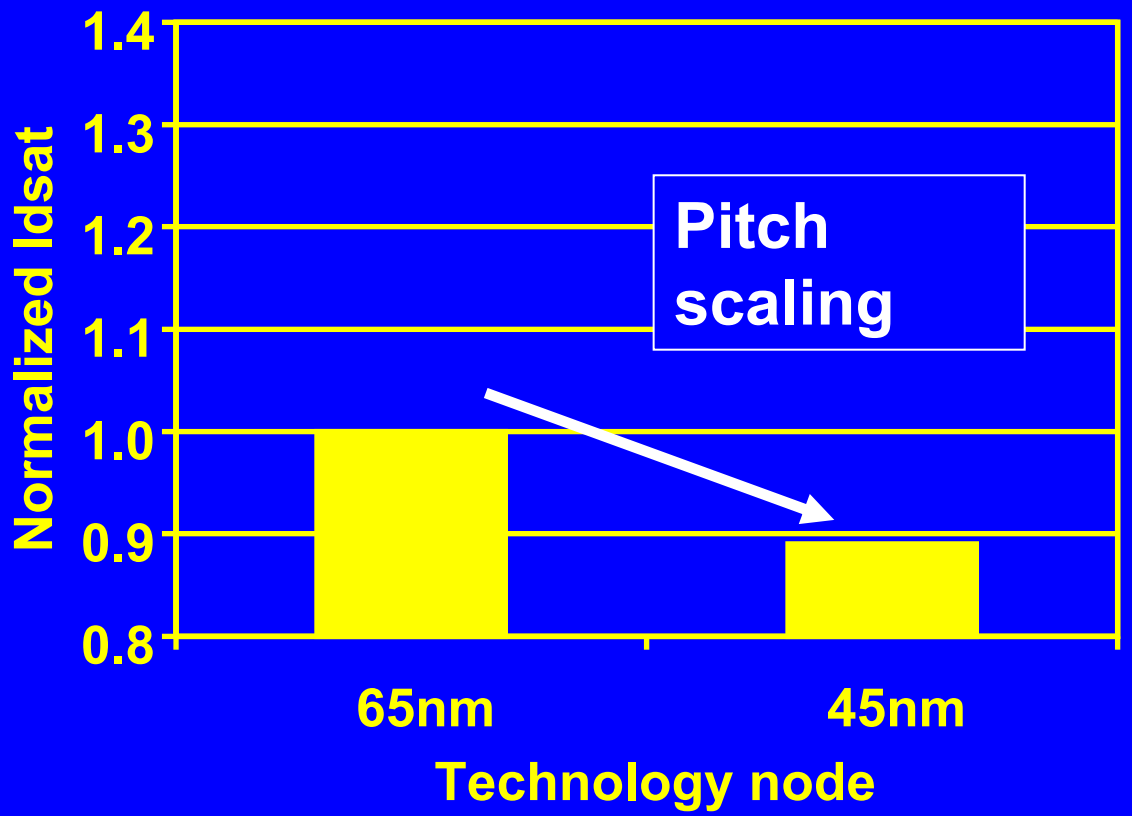
- Three methods used enhance PMOS performance

1. Increase Ge Concentration in Embedded SiGe S/D
2. Move Embedded SiGe S/D closer to Gate
3. Remove dummy poly gate with Metal Gate-Last flow



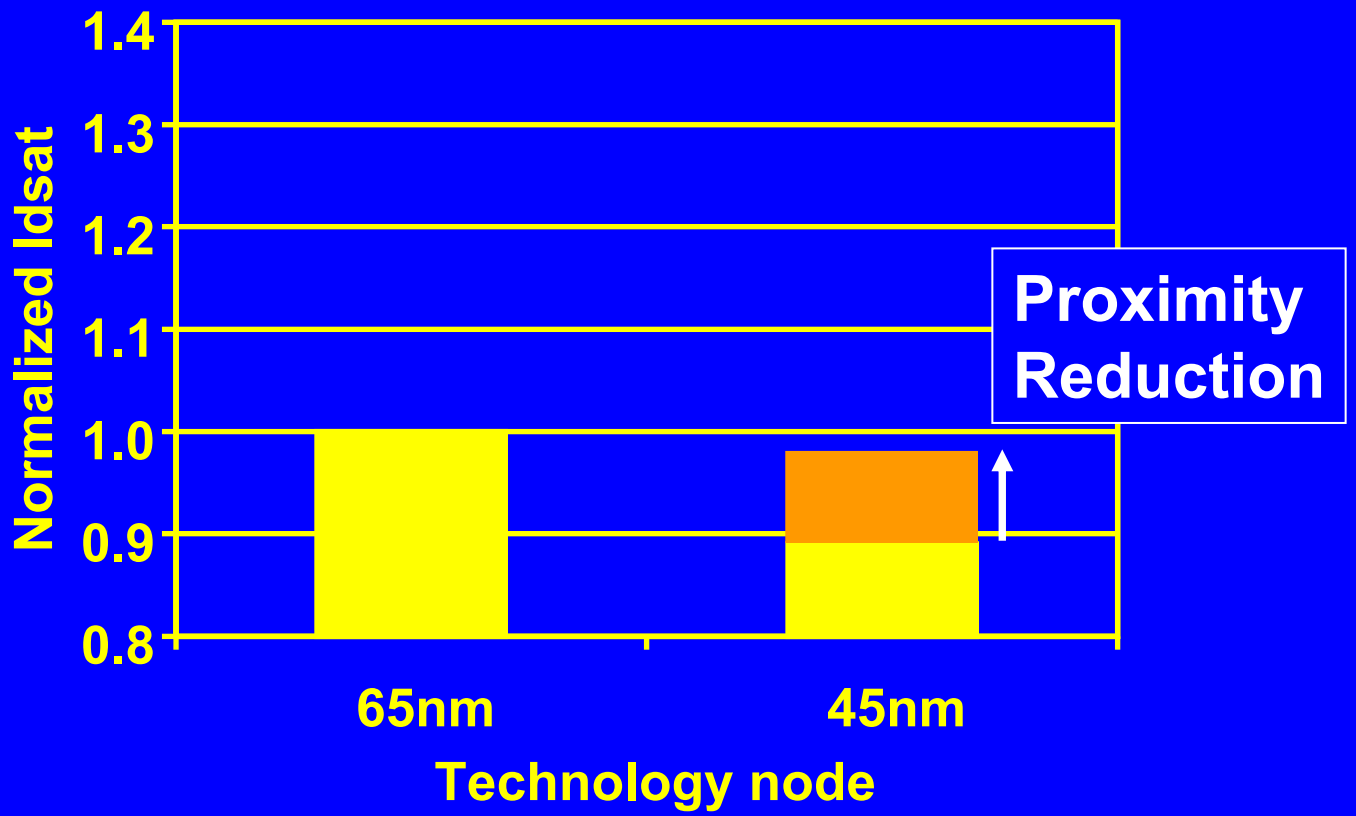
PMOS strain: Pitch dependence

- Stress degraded due to Pitch Scaling



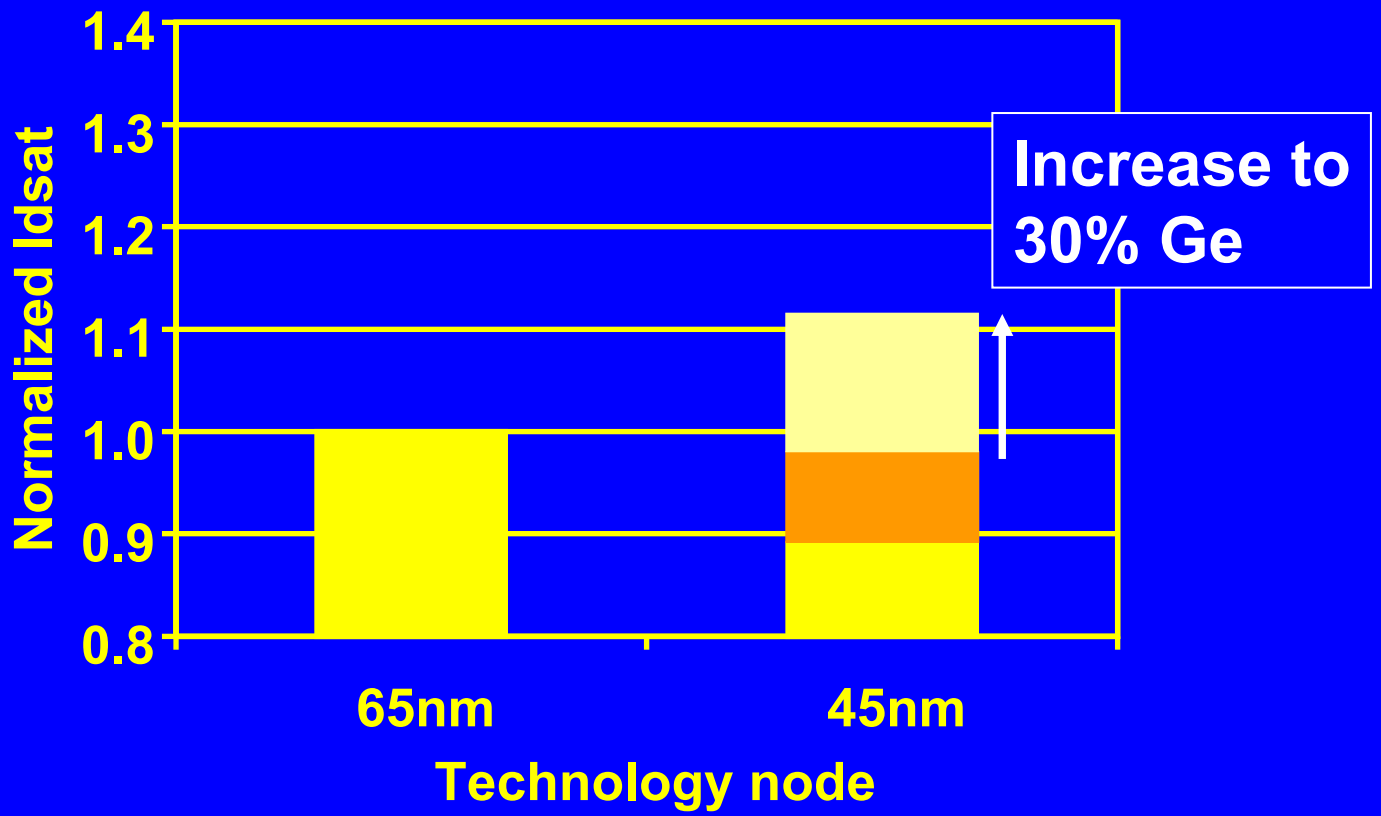
PMOS strain: Pitch dependence

- Proximity scaling recovers majority of pitch degradation



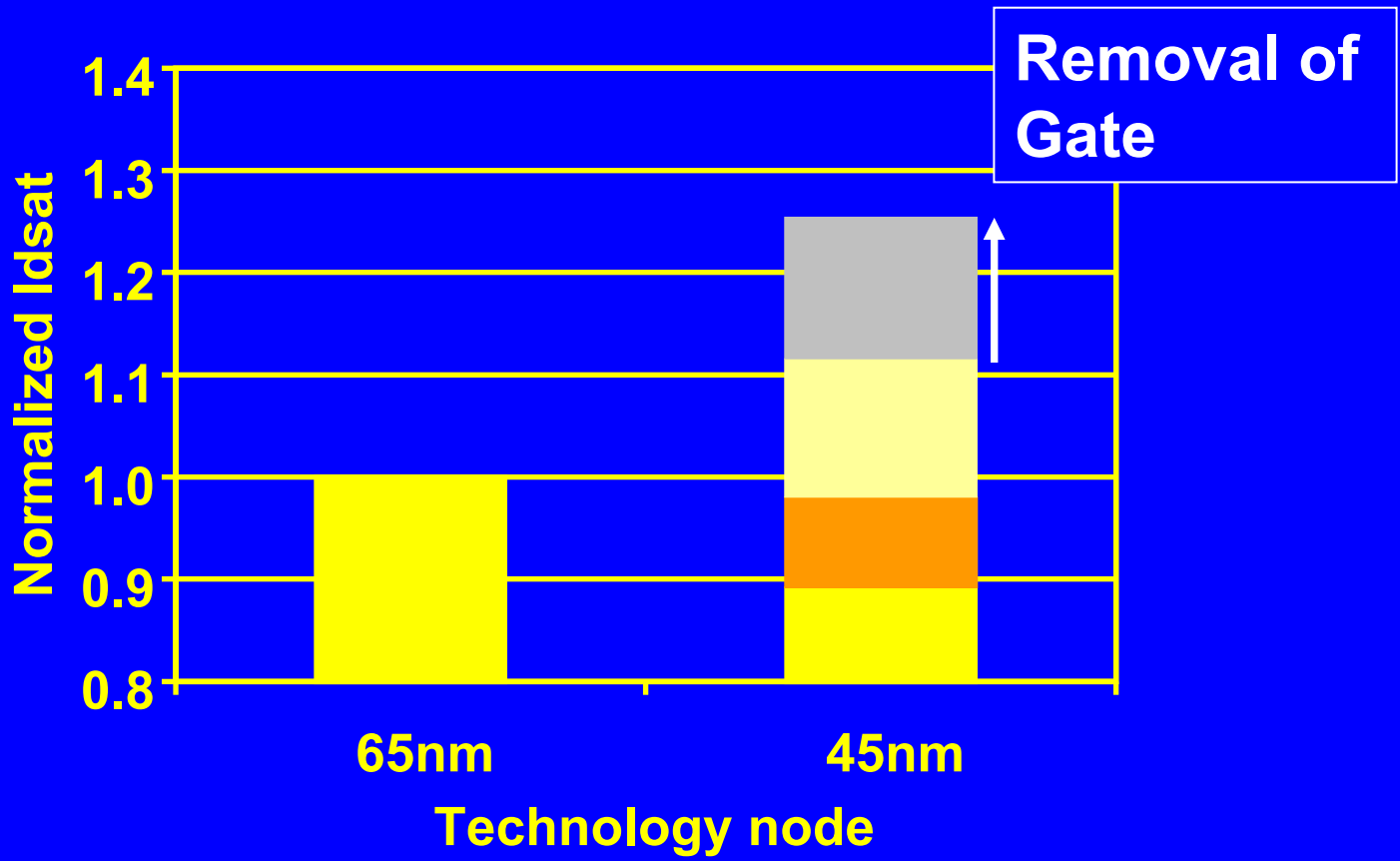
PMOS strain: Pitch dependence

- %Ge provides strain benefit



PMOS strain: Pitch dependence

- Gate-Last provides significant increase in performance



Strain Comparison

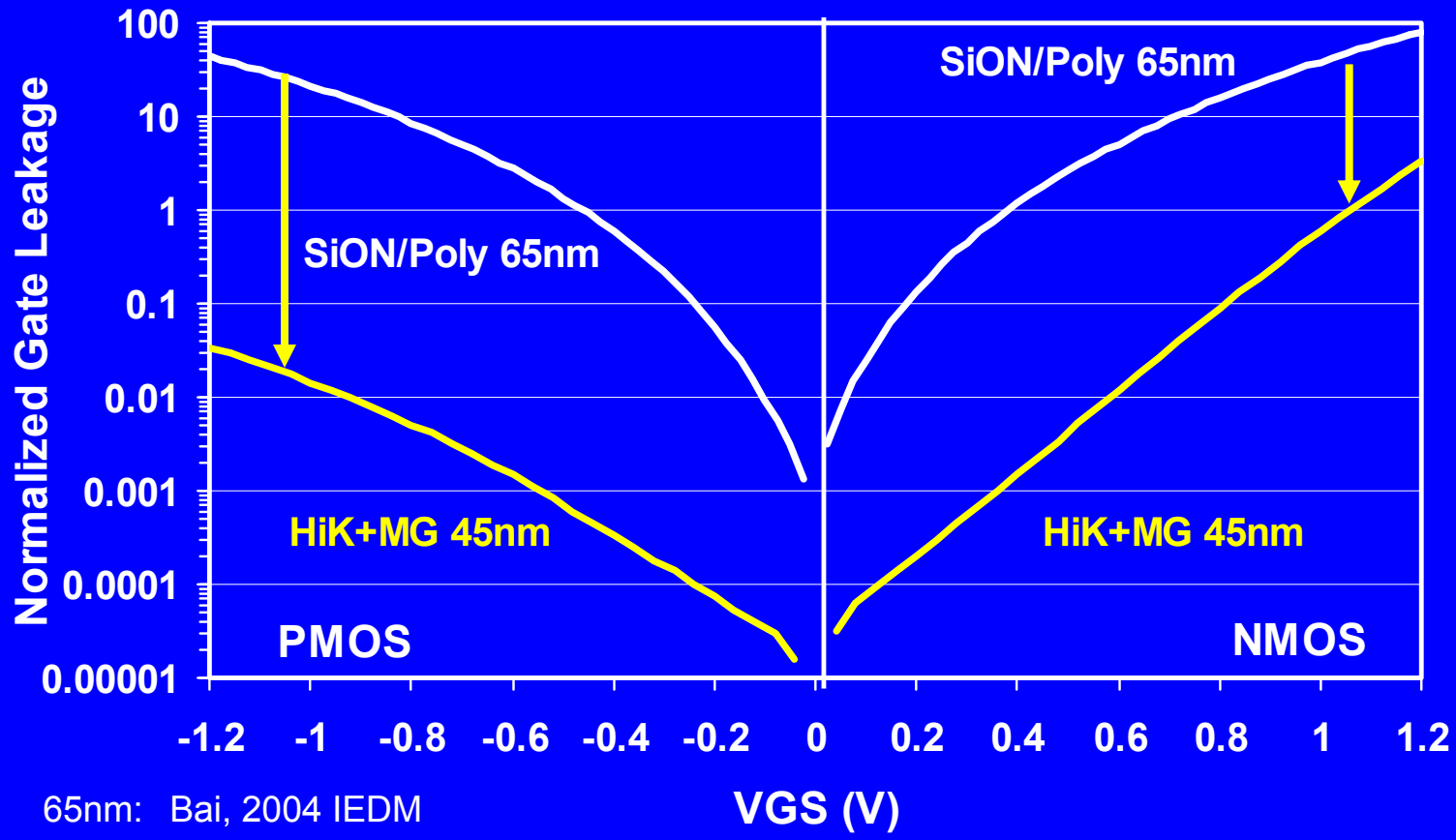
65nm Method	45nm Method
NMOS	**NMOS**
Tensile Nitride Cap	**Tensile Trench Contacts**
Gate Stress Memorization + S/D Stress Memorization	**Metal Gate Stress (MGS)** + S/D Stress Memorization
PMOS	**PMOS**
Embedded SiGe S/D	**Embedded SiGe S/D** (higher %Ge + reduced S/D)
	Replacement Gate Enhancement

Outline

- Introduction
- Metal-Gate + Strain Integration
- Transistor/Circuit Results
- Manufacturing
- Conclusions

Gate Leakage

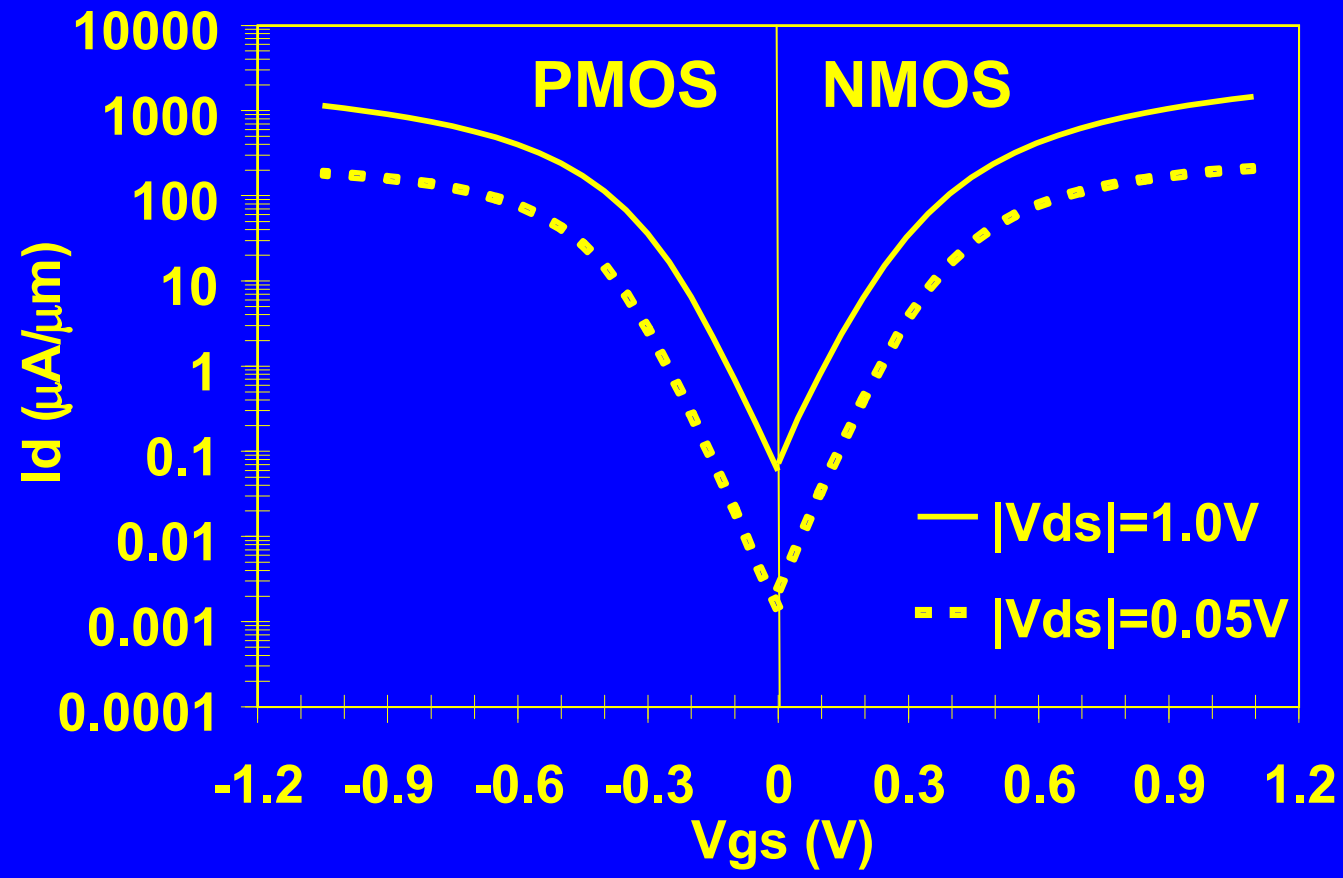
- Gate leakage is reduced >25X for NMOS and 1000X for PMOS



65nm: Bai, 2004 IEDM

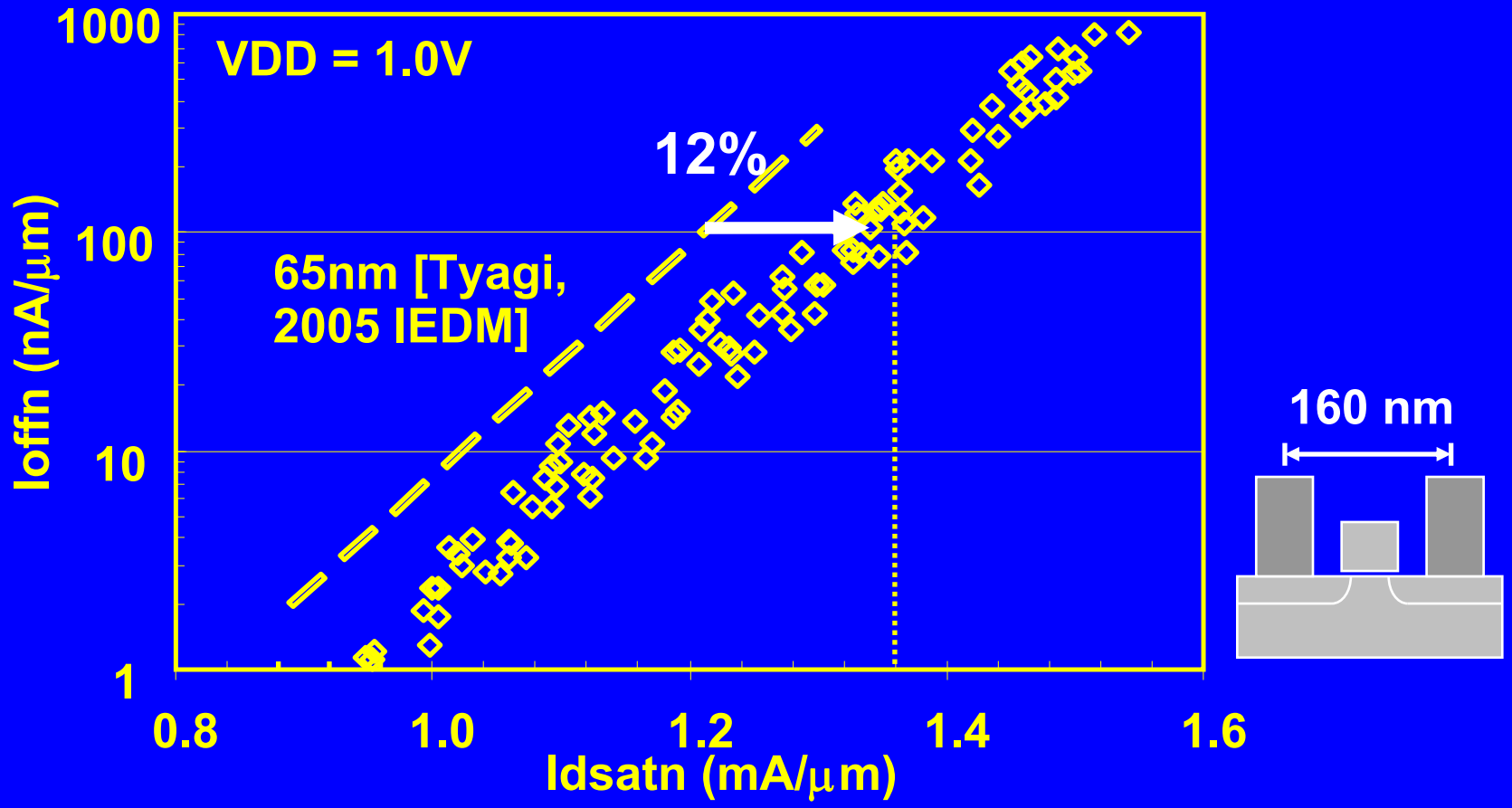
Excellent short channel effects

- Subthreshold slope - 100mV/decade
- DIBL - 140mV/V NMOS & 200mV/V PMOS



NMOS I_{DSAT} vs. I_{OFF}

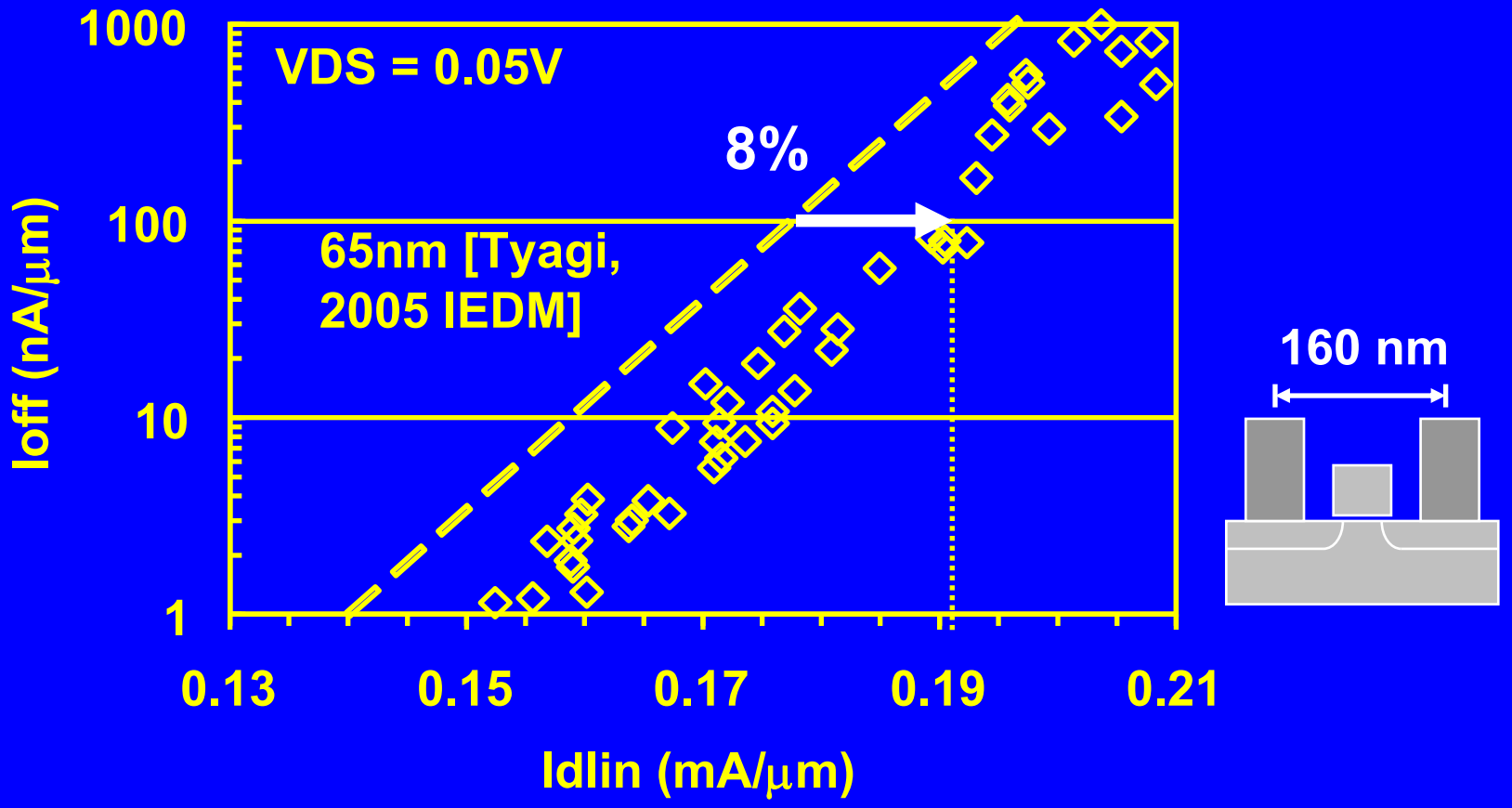
- Best drives for 45nm or 32nm technology



1.36 mA/μm at I_{OFF} = 100 nA/μm & 1.0V

12% better than 65 nm

NMOS I_{Dlin} vs. I_{OFF}

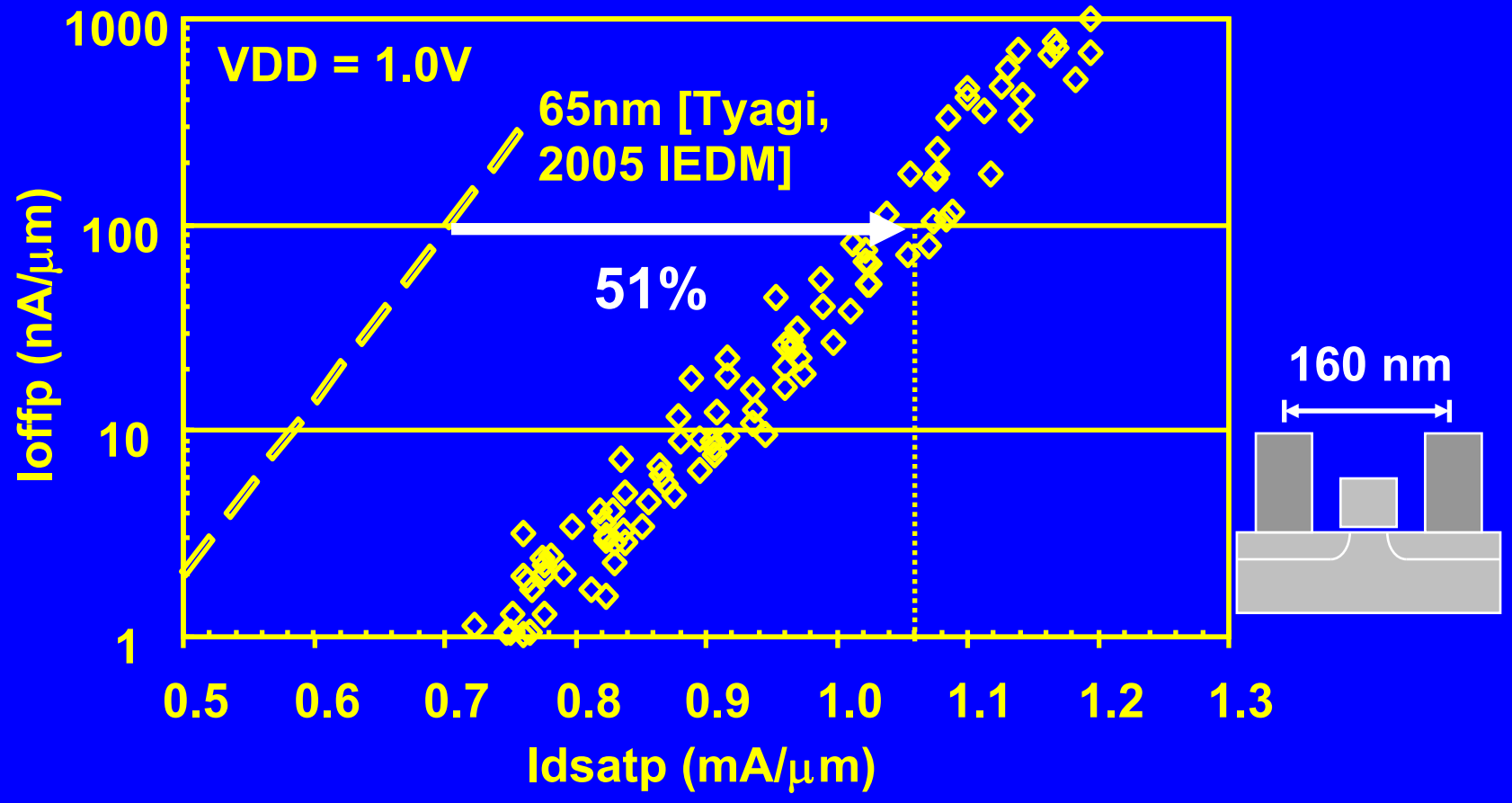


0.192 mA/μm at I_{OFF} = 100 nA/μm

8% better than 65 nm

PMOS I_{DSAT} vs. I_{OFF}

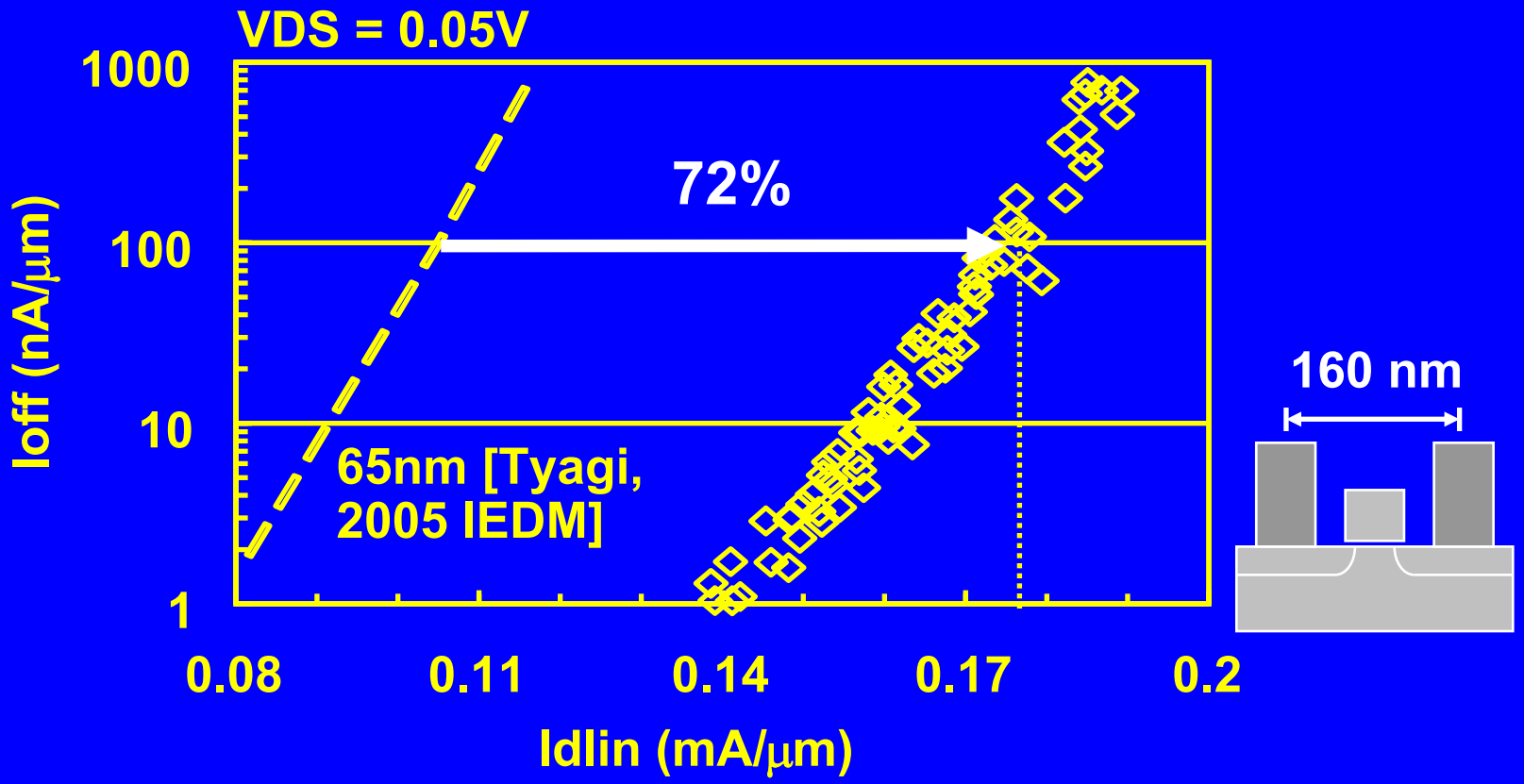
- Best drives for 45nm or 32nm technology



1.07 mA/μm at I_{OFF} = 100 nA/μm & 1.0V

51% better than 65nm

PMOS I_{Dlin} vs. I_{OFF}



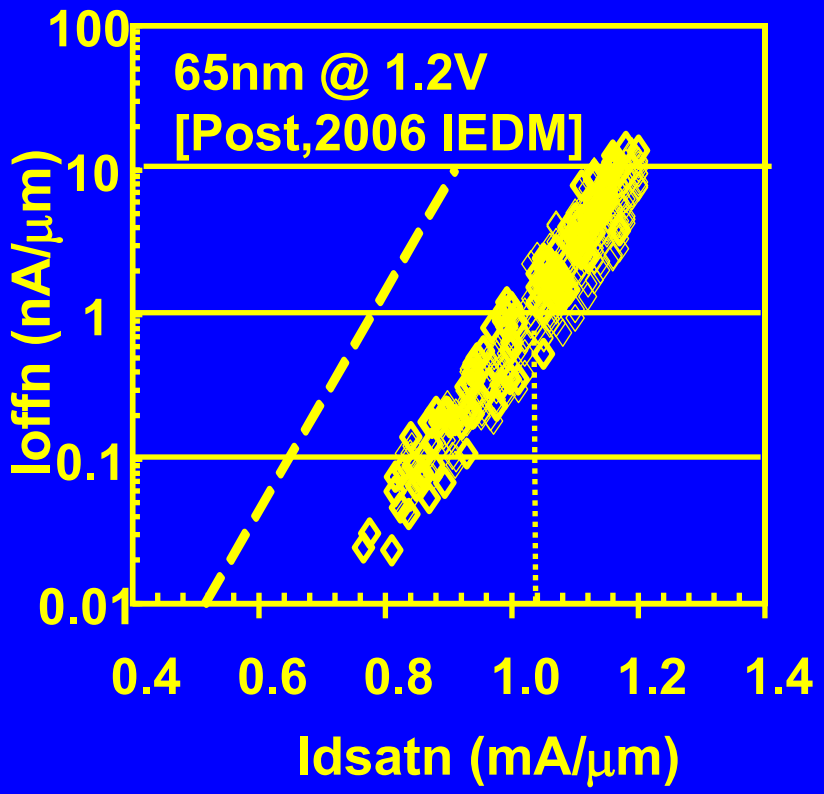
0.178 mA/μm at I_{OFF} = 100 nA/μm

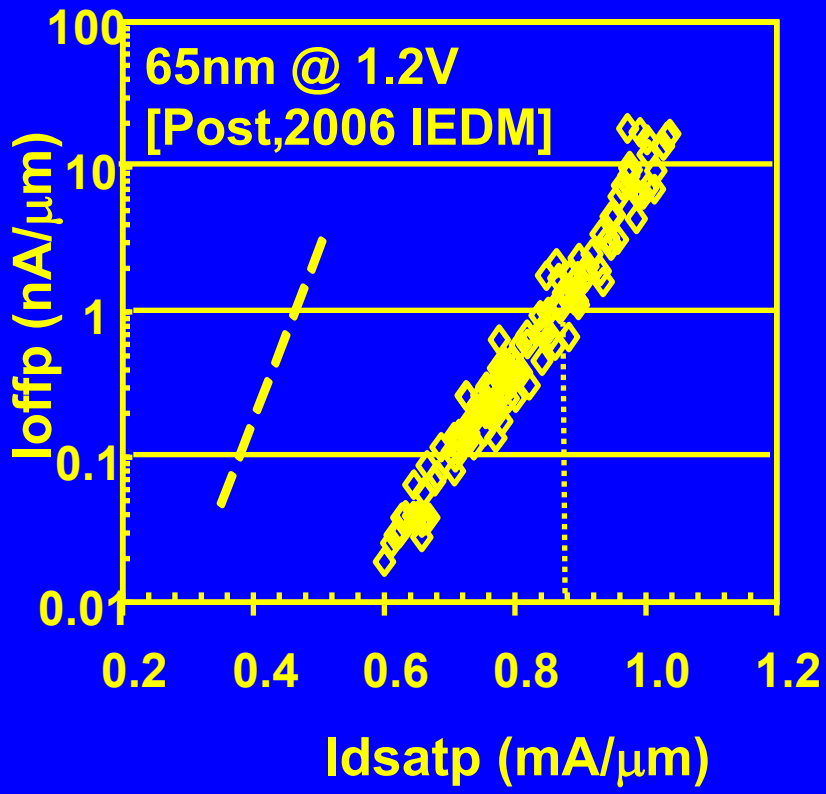
72% better than 65nm!

7% from NMOS

SOC Application

- LSTP benchmark (1nA & 1.1V)

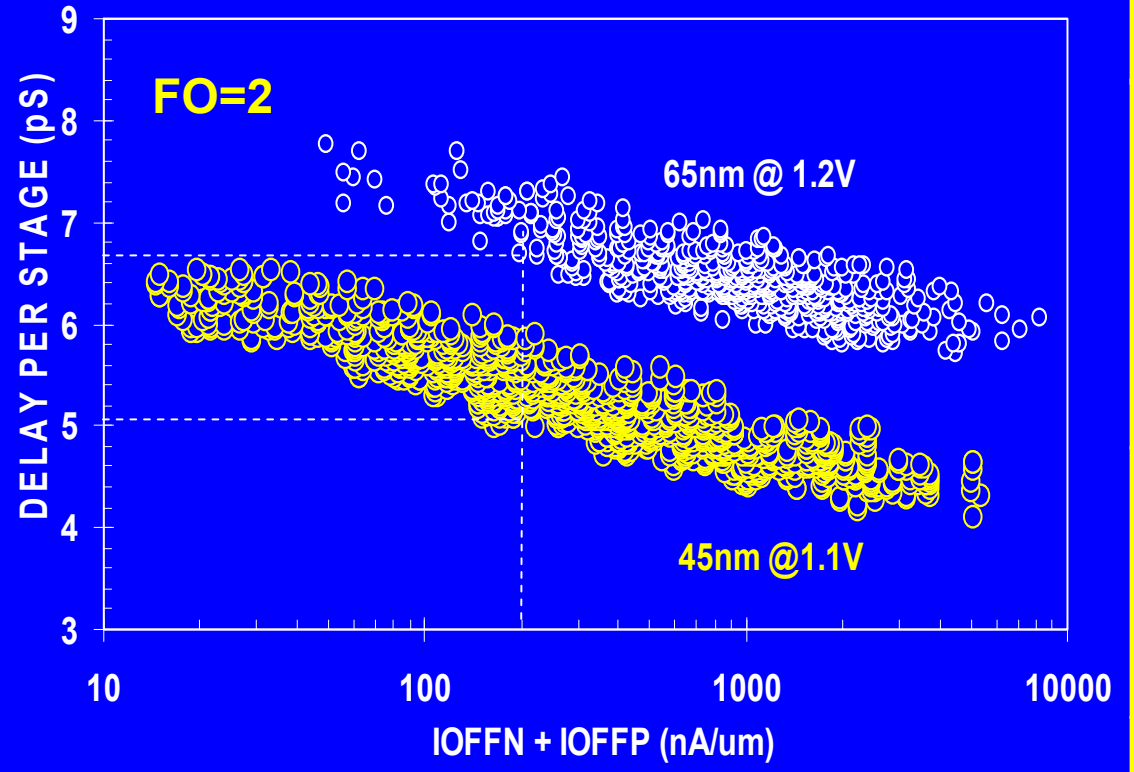




NMOS: 1.04 mA/μm at I_{OFF} = 1 nA/μm & 1.1V

PMOS: 0.88 mA/μm at I_{OFF} = 1 nA/μm & 1.1V

Ring Oscillator Speed

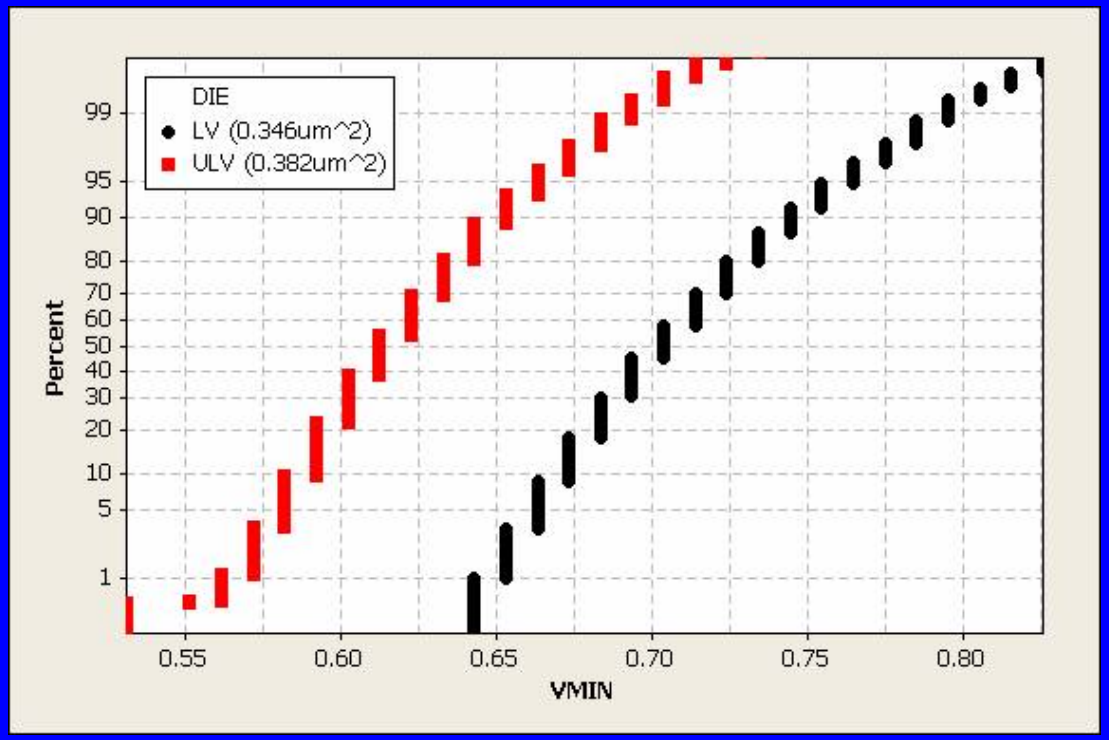


Component	Benefit (%)
PMOS Idsat	+13
PMOS Idlin	+18
NMOS Idsat	+3
NMOS Idlin	+2
Cjunction	+2
Cgate/Cov	-8
Voltage Scaling	-7
Total	+23

Metal Gate Last flow enables 23% reduction in RO delay at the same leakage

Power: SRAM VCCmin

- Low active VCCmin important for low power applications
- 3Mb SRAM
  - 0.346μm² cell median active VCCmin of 0.70V
  - 0.382μm² cell median active VCCmin of 0.625V



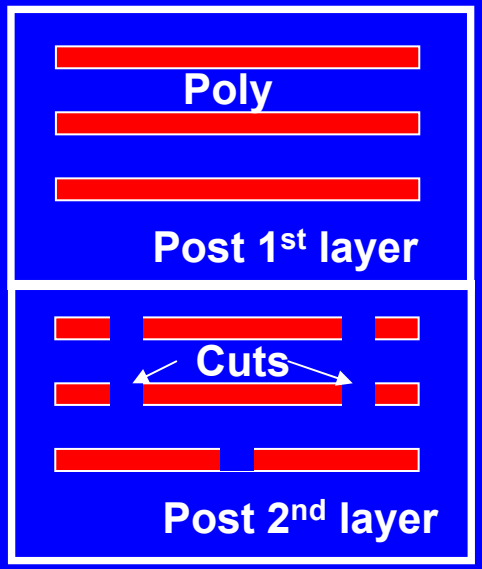
Outline

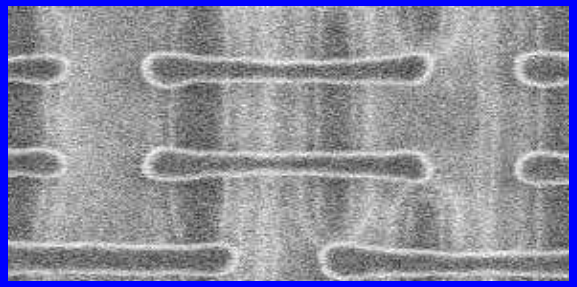
- Introduction
- Metal-Gate + Strain Integration
- Transistor/Circuit Results
- Manufacturing
- Conclusions

193nm Dry lithography - Poly

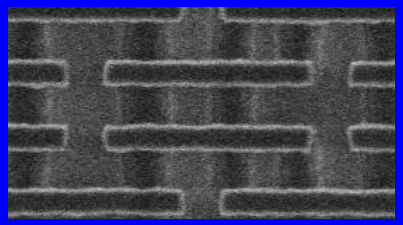
- Critical Layers patterned with 193nm Dry lithography
  - Lower cost & Mature toolset
  - Transistor Formation Mask Count Neutral with 65nm

- Double Patterning used at Poly
  - Array of Poly lines are patterned
  - Discrete allowed pitches
  - Poly lines are Cut



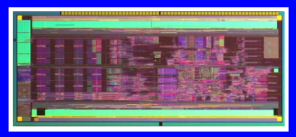


65nm SRAM

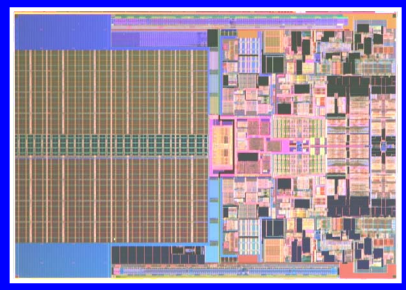


45nm SRAM

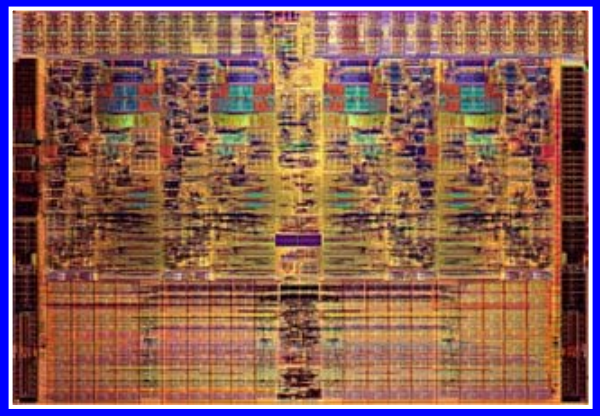
Multiple Microprocessors



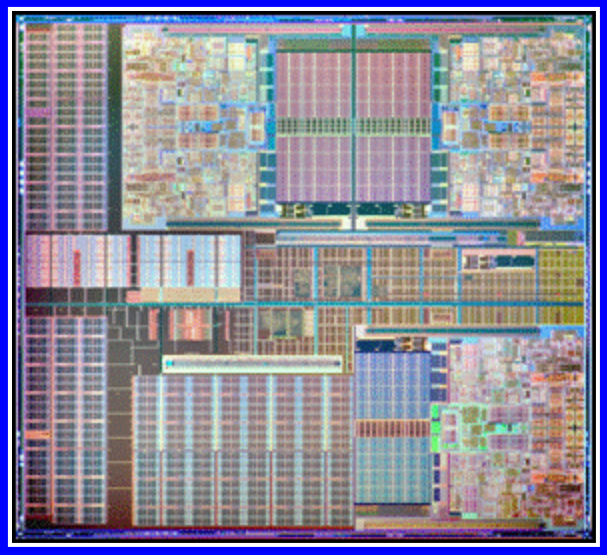
Single Core



Dual Core



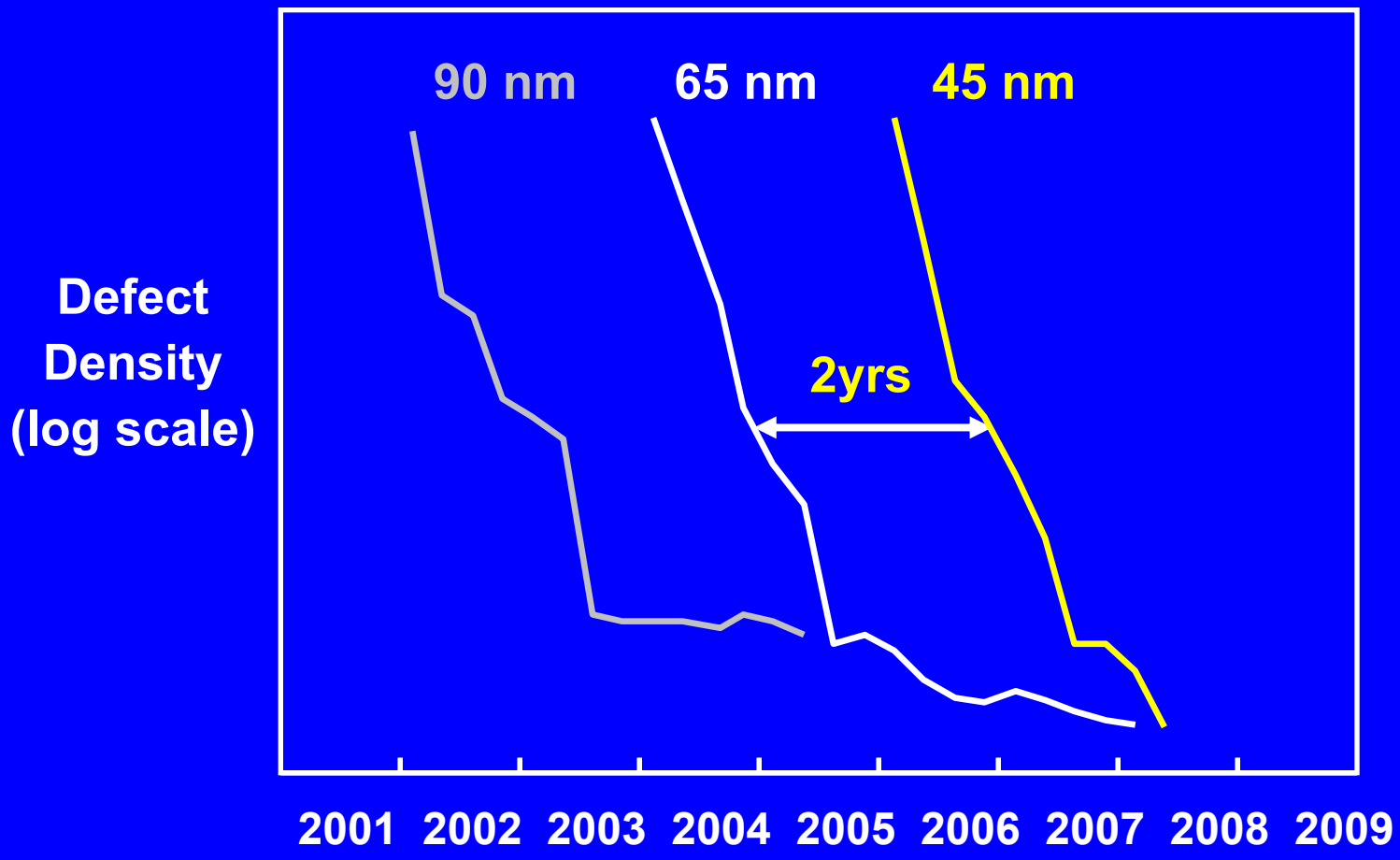
Quad Core



Six Core

Defect Reduction Trend

- Record yields demonstrated <2 years after 65 nm
  - Fastest Ramp to high yield ever at Intel



Conclusions

- High-k + Metal Gate transistors have been integrated with Novel Strain techniques
- Gate-Last flow provides significant strain enhancements both on NMOS and PMOS
  - Key driver for process flow decision
  - Achieve record drive currents at tight gate pitch
- 193nm Dry lithography can be extended to the 45nm technology node
- The technology is already in high volume manufacturing
  - High yields demonstrated on multiple microprocessors

Acknowledgements

- The authors gratefully acknowledge the many people in the following organizations at Intel who contributed to this work:
  - Portland Technology Development
  - Quality and Reliability Engineering
  - Process & Technology Modeling
  - Assembly & Test Technology Development

For further information on Intel's silicon technology, please visit our Technology & Research page at

www.intel.com/technology