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News Fact Sheet

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Intel News Highlights at the 2009 International Solid-State Circuits Conference

Feb. 4, 2009 — At the International Solid-State Circuits Conference, scheduled for Feb. 8-12 in San Francisco, Intel Corporation will present 15 papers and Intel senior Fellow Mark Bohr will hold a keynote in a special invite-only plenary session.

Bohr will discuss the new system-on-a-chip (SoC) era, which will require a fundamental shift in the way semiconductor manufacturers will innovate to keep Moore's Law alive and well in the next decade. A few of the research presentations throughout the week will discuss technologies expected to enable more capabilities in the future SoC including wireless radio and better graphics on mobile devices.

Intel will lead over half of the microprocessor sessions with four papers discussing the latest 45nm enterprise processors.

A few of the highlighted research papers and presentations from Intel are described in detail below:

System-on-a-chip will keep Moore's Law alive in the future

"The New Era of Scaling in an SoC World"

Mark Bohr, Intel senior Fellow, Technology and Manufacturing Group, and director, Process Architecture and Integration

Plenary Session 1.3: 10:35 a.m., Feb. 9

The trend of using smaller transistors to build larger microprocessor cores with higher operating frequency is coming to an end as Intel focuses on developing products that deliver energy-efficient computing and increased mobility. Bohr will discuss fundamental shifts required in both transistor development and circuit design to continue innovation in microprocessors. The new era is called system-on-a-chip (SoC), and complete system integration is the future challenge. Intel plans to use its chip design expertise, factory capacity, advanced manufacturing techniques and the economics of Moore's Law to usher in a new category of highly integrated, purpose-built and Web-savvy SoC designs and products.

Innovating Digital Radio technologies for future system-on-a-chip designs

Future SoCs will have flexible radios included on-chip to enable a new era of mobile communications. The “connect anywhere, anytime” expectation requires additional radios (e.g. WiFi, WiMAX, 3G, Bluetooth) to be added to the platform which takes up space, consumes power and impacts performance of the computing experience. Intel researchers are actively looking at ways to provide solutions with technologies that move more radio components to silicon, and improve cost and performance. Intel researchers will present three milestones which describe new ideas that will enable the digital radio and full capability of the future SoC.

“A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP Digital”

Session 4.2: 2 p.m., Feb 9

In this paper, a new technique is detailed for 60GHz wireless radio. The technique converts analog signals to digital by coupling together multiple, less complex ADCs, called SAR ADCs and spreading the task across all of them. This method has resulted in:

- Data rates in excess of 5Gb/s to allow a DVD-quality movie to transfer in less than 10 seconds wirelessly.
- The first ADC that can resolve 7bits at 2.5Gb/s in pure CMOS, a key step toward digital radios at these performance levels.
- Comparable power efficiency to state of the art ADCs available today, but with better accuracy.

“A 4.75GHz Fractional Frequency Divider with Digital Spur Calibration in 45nm CMOS”

Session 12.6: 10:15 a.m., Feb 10

Analog radio signal processing is often inherently inefficient, thereby requiring filtering in order to correct spectral impurities (which could be described as frequency mis-matches). The filtering is necessary because pure local oscillator (LO) signals are required for good sensitivity and robust data transfer. Previous approaches used many inductors which require space, consume power and add cost. This paper, in an industry first, shows how we can use digital techniques to perform the required voltage controlled oscillator (VCO) frequency translation and calibrate the circuits for excellent LO purity. The digital techniques resulted in:

- Reduced amount of components required, thereby saving silicon area.
- A novel technique that uses the inherent variability of gate delays in 45nm CMOS processes to measure and calibrate mismatches.

“A 1.05V 1.6mW 0.45°C 3 σ -Resolution $\Delta\Sigma$ -Based Temperature Sensor with Parasitic-Resistance Compensation in 32nm CMOS”

Session: 20.1: 8:30 a.m., Feb 10

This paper introduces the first-ever temperature sensor for microprocessor applications in high-k metal gate digital 32nm CMOS. Numerous remote sensors are used to measure temperature over the entire multi-core die. The processor control unit can then work with these sensors and provide accurate temperature information to higher level software components for various housekeeping and optimization tasks. In the multi-core era, thermal/power management is crucial to platform performance and energy efficiency. This achievement results in:

- Improved processor power management.

- Ability to maximize microprocessor performance reliably.
- Limit leakage through load-balancing with multiple location hot spot temperature measurements.
- Extend life of processor components by maintaining lower operational stress.
- Multiple sensors allow more precise identification and intervention.

Better graphics on small mobile devices

Increasing energy efficiency for the most performance and power-hungry operations in multimedia, graphics and signal processing, SIMD computations is critical for mobile form factors. A SIMD is a Single Instruction which is applied to Multiple Data elements (such as all the pixels in an image). With devices becoming smaller and applications becoming more visual, better techniques are needed to do more SIMD processing while using less energy. Today's SIMD accelerations circuits have high leakage currents and limited power management, and do not scale well to reduced voltages.

“A 300mV 494GOPS/W Reconfigurable Dual-Supply 4-Way SIMD Vector Processing Accelerator in 45nm CMOS”

Session 14.6: 4:15 p.m., Feb 10

This paper presents a 45nm prototype SIMD accelerator chip that could enable richer multimedia and more immersive visuals across all platforms, particularly on notebooks, MID's and other small devices. The new technique achieves:

- 10x better energy-efficiency vs. today's products at standard voltages.
- Circuits that scale smoothly to ultra-low voltages (from 1.3V to 230mV).
- Voltage reduction to 300mV, which further increases energy efficiency by 8x.

Industry-leading enterprise processors on 45nm

“A 45nm 8-Core Enterprise Xeon® Processor”

Session 3.1: 1:30 p.m., Feb 9

- 8-core 16-thread enterprise Xeon® processor has 2.3B transistors in 9M 45nm CMOS.
- I/O links use per-lane TX and RX compensation to enable operation up to 6.4GT/s.

“A Family of 45nm IA Processors”

Session 3.2: 2 p.m., Feb 9

- A family of next-generation IA processors with up to 8 cores, enhanced Core™ microarchitecture, 3-level caches and 2-way SMT is implemented in 45nm high-k metal-gate CMOS.
- The family has a coherent point-to-point link and integrates memory controller, power-management microcontroller and power-gate transistors

“Dynamic Frequency-Switching Clock System on A Quad-Core Itanium® Processor”

Session 3.4: 3:15 p.m., Feb 9

- The next Intel® Itanium® processor, codenamed “Tukwila,” integrates four cores and a system interface with six Intel QuickPath® Interconnect channels and four memory interconnect channels.
- Its 700 mm² die footprint and high level of integration present clock system design challenges in power consumption and variability compensation.

- This paper addresses these challenges and explains how the voltage-frequency management solution optimizes the processor's power and thermal envelope.

“Over 1 Million TPCC with a 45nm 6-Core Xeon® CPU”

Session 3.8: 4:45 p.m., Feb 9

- A monolithic 6-core Xeon® processor has 1.9B transistors in 9M 45nm CMOS with a 9MB L2 and 16MB L3 cache and exceeds 1M transactions/minute TPCC in 8-socket configuration.
- The FSB I/O circuits are implemented in the center of the die to reduce I/O latency.

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