UPCRC Overview

Universal Computing Research Centers launched at UC Berkeley and UIUC

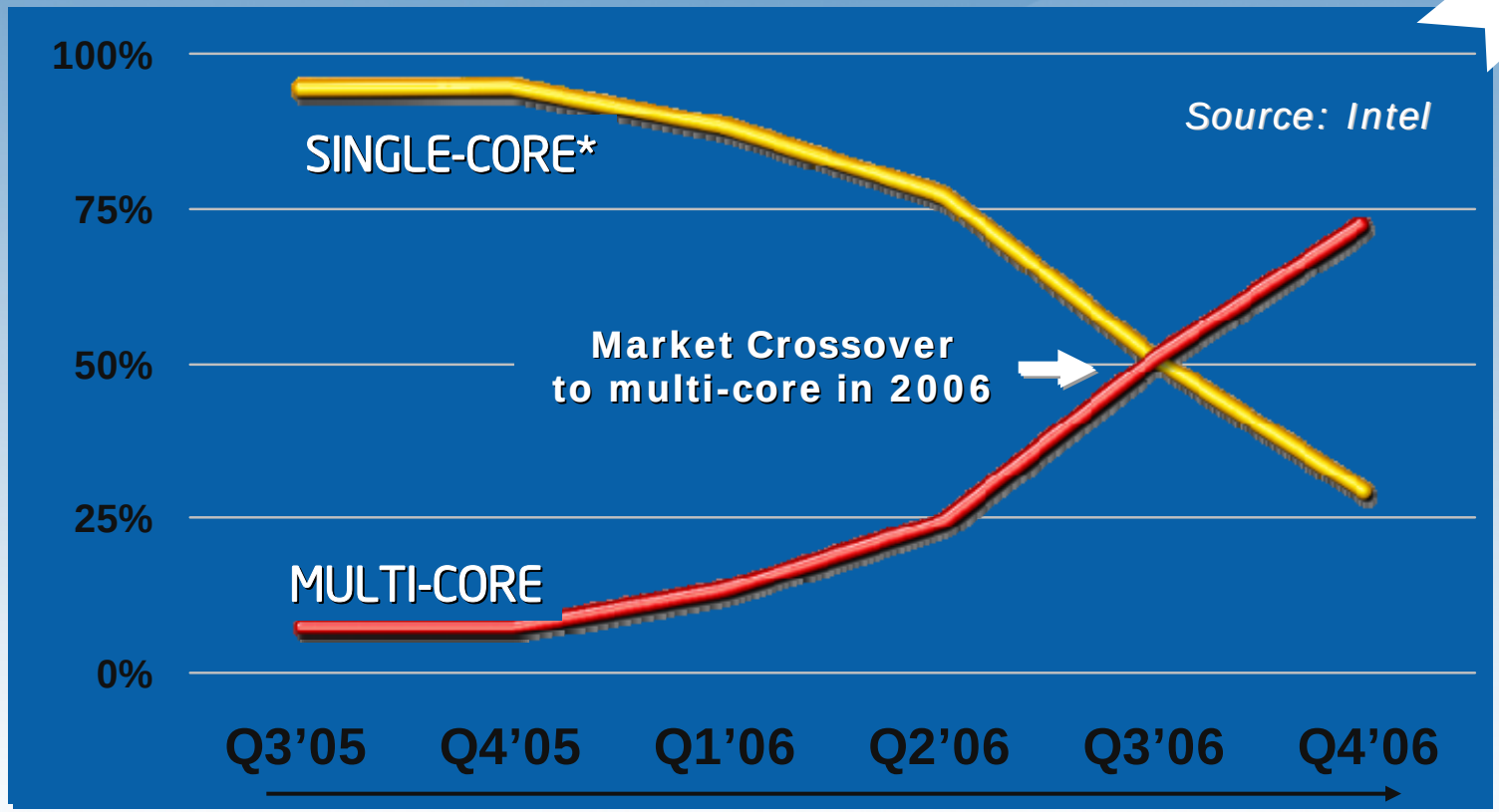
Andrew A. Chien
Vice President of Research
Intel Corporation

Announcement Key Messages

- Microsoft and Intel are announcing the establishment of two "Universal Parallel Computing Research Centers" with the first locations at the University of Illinois at Urbana-Champaign and the University of California at Berkeley.
- Under this alliance, Microsoft and Intel have committed to invest a combined $20 million in the center over the next five years
- The center will explore the next generation of hardware and software for parallel computing and enable a revolutionary change in the way people use technology.

Multi-core is now mainstream

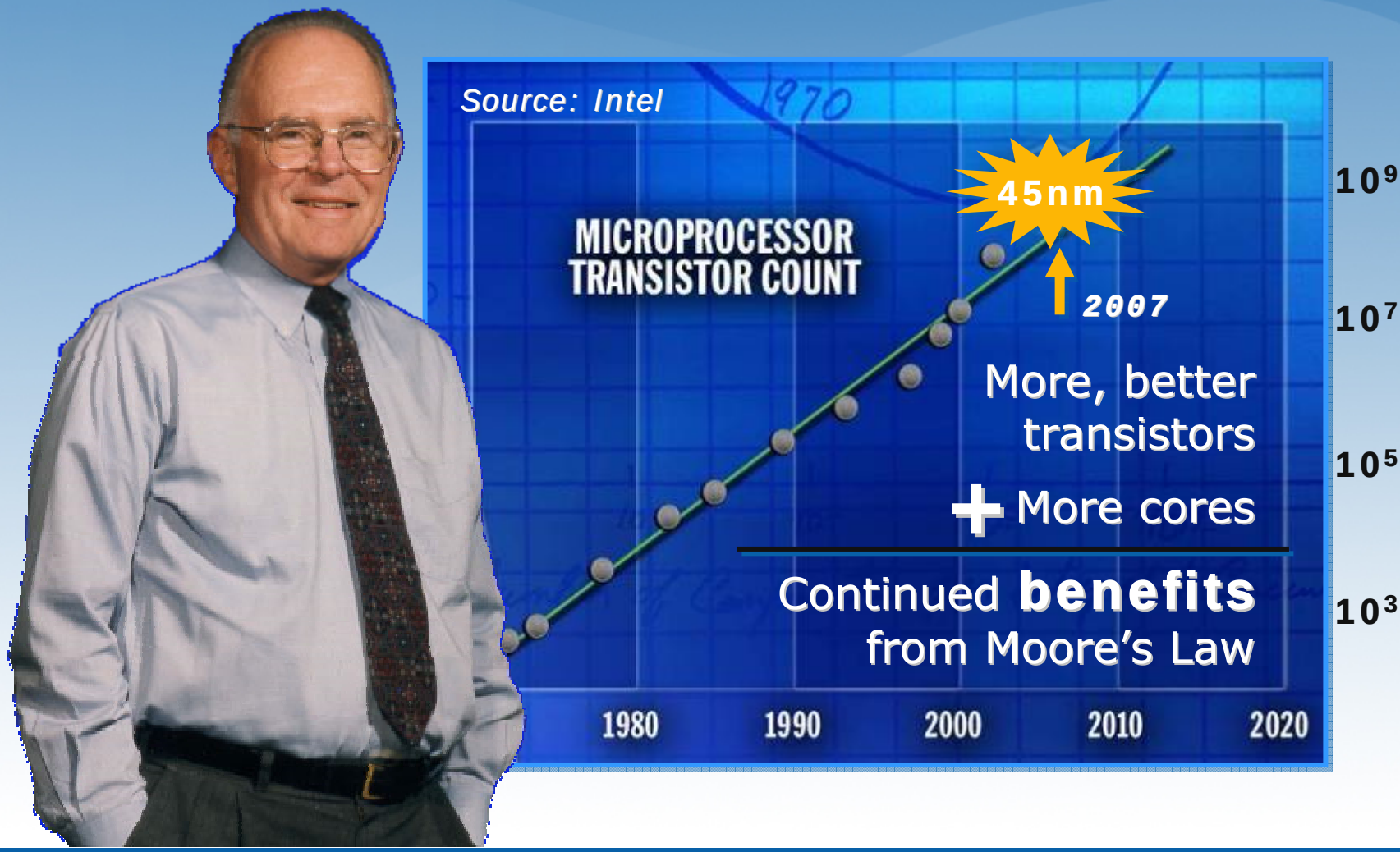
Motivated by a need for better performance/watt



Over 6 MU
Quad-core
In 2007

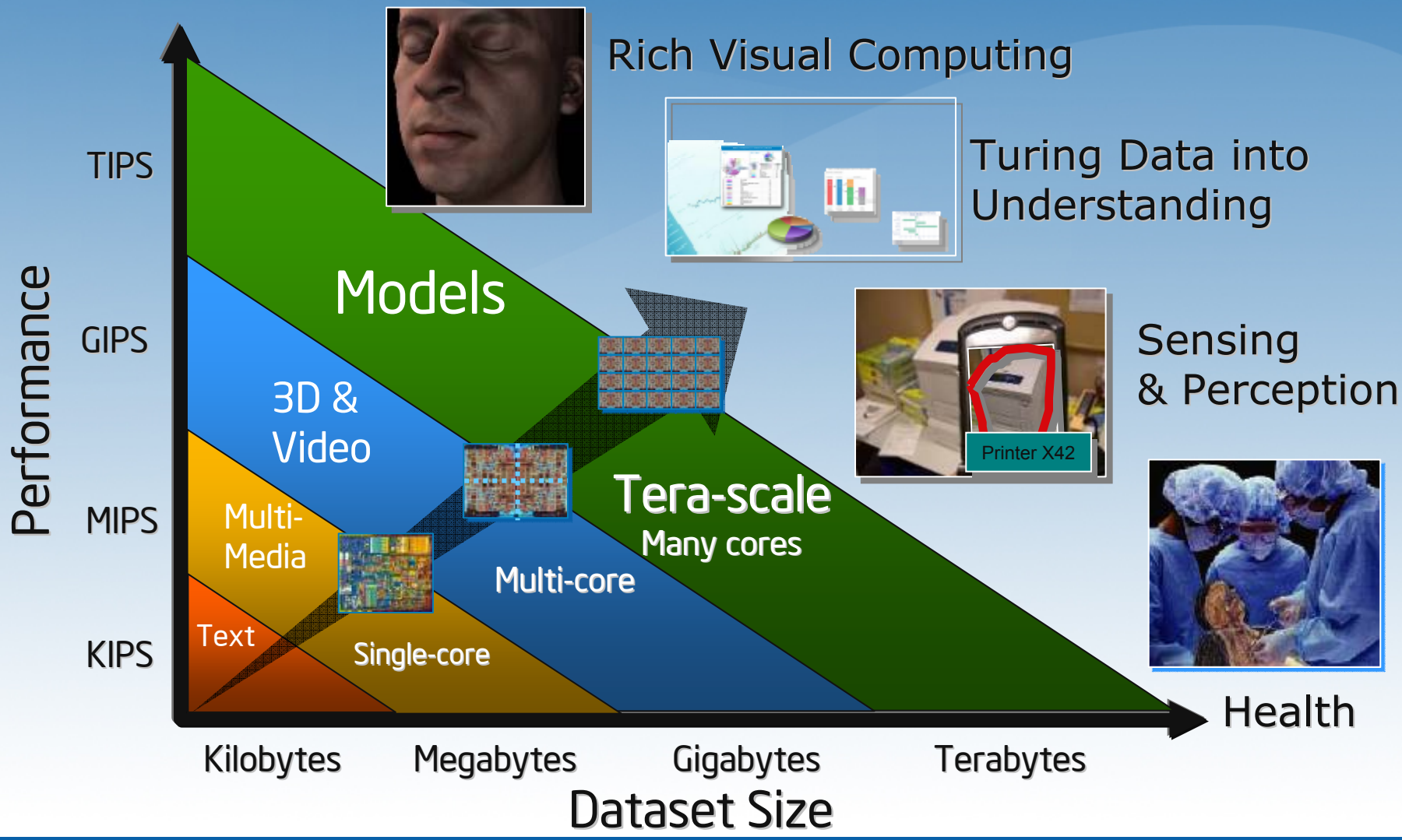
Multi-core Top to Bottom

Moore's Law Motivates Multi-Core



A Shift to Many Cores

Parallelism will enable tera-scale performance for new apps

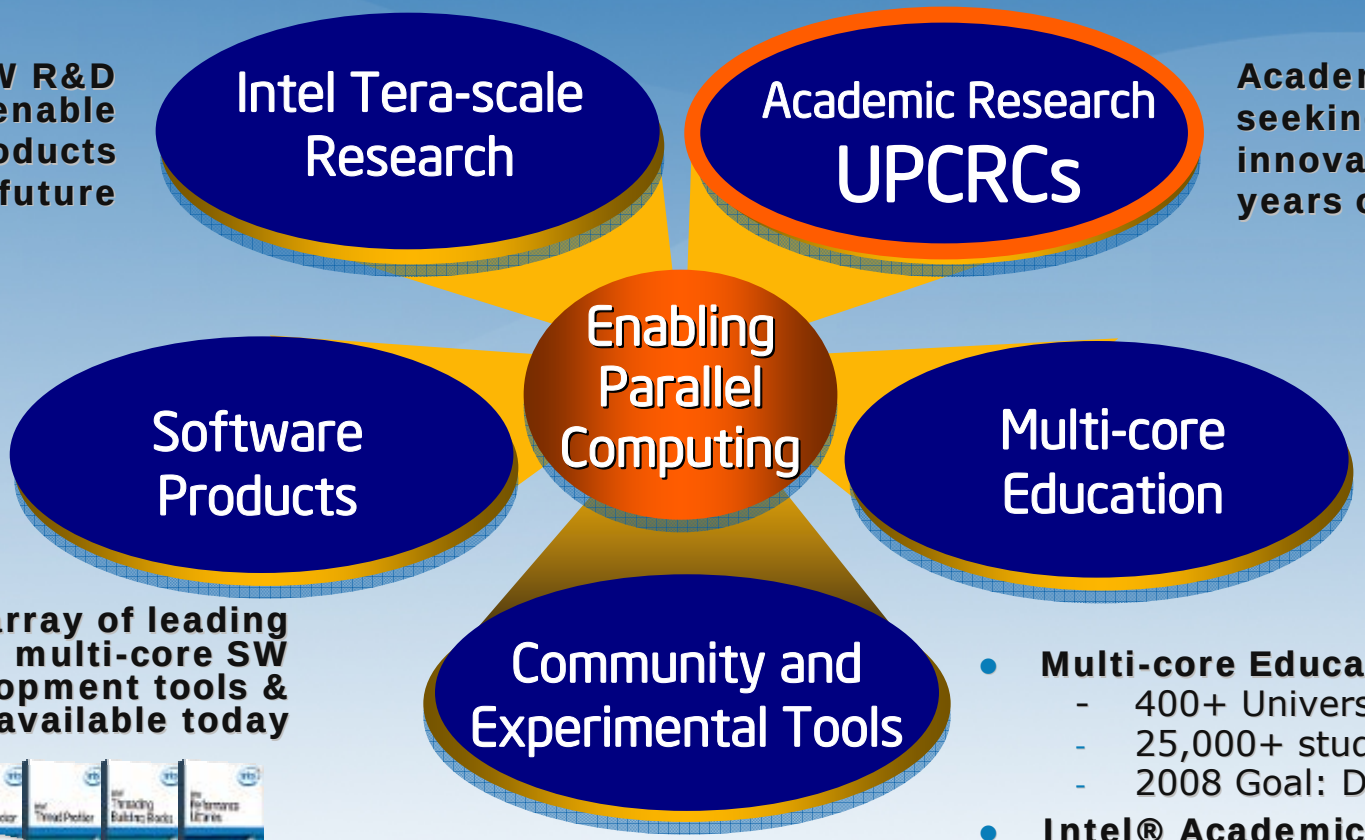


Wanted: Breakthrough Innovations in Parallelism

- P Programming Effort ≤ Sequential Programming Effort
- P Programming that doesn't increase programming complexity
  - Productivity, Modularity, Interactions, Performance Tuning, etc.
- P Programming Approaches that have "forward scalability"
  - Application implementation gets faster (more parallel) on succeeding generations of hardware platforms
  - Scale data sets, scale output quality – more parallelism without reprogramming or retuning
- P Programming implementation techniques that deliver high and robust parallel performance
  - Enable programming at a high level
  - Manage workload, algorithm, and data irregularlity
  - Manage hardware differences and irregularity
- HW Architecture Innovations that Support Parallel Programs

Intel: Making Parallel Computing Pervasive

Joint HW/SW R&D program to enable Intel products 3-7+ in future



Academic research seeking disruptive innovations 7-10+ years out

Wide array of leading multi-core SW development tools & info available today

- **TBB Open Sourced**
- **STM-Enabled Compiler on Whatif.intel.com**
- **Parallel Benchmarks at Princeton's PARSEC site**

- **Multi-core Education Program**
  - 400+ Universities
  - 25,000+ students
  - 2008 Goal: Double this
- **Intel® Academic Community**
- **Threading for Multi-core SW community**
- **Multi-core books**

Today: Universal Parallel Computing Research Centers

- Catalyze breakthrough research enabling pervasive use of parallel computing

Parallel Programming

Languages, Compilers, Runtime, Tools

Parallel Applications

For desktop, gaming, and mobile systems

Parallel Architecture

Support new generation of programming models and languages

Parallel Sys. S/W

Performance scaling, memory Utilization, & power consumption

UPCRC Partners in Research

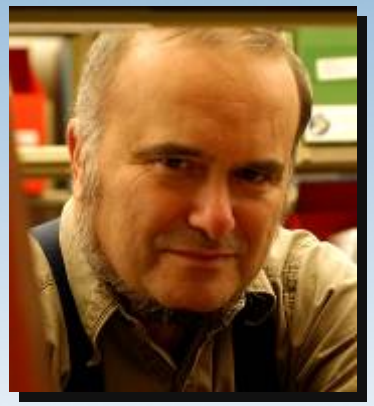
- Intel & Microsoft provide funding and guidance
- Universities direct groundbreaking research

Berkeley
University of California

Professor David Patterson
UCB UPCRC Director

Prof. Wen-Mei Hwu

ILLINOIS
1867
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN



Prof. Marc Snir

UIUC UPCRC
Co-Directors

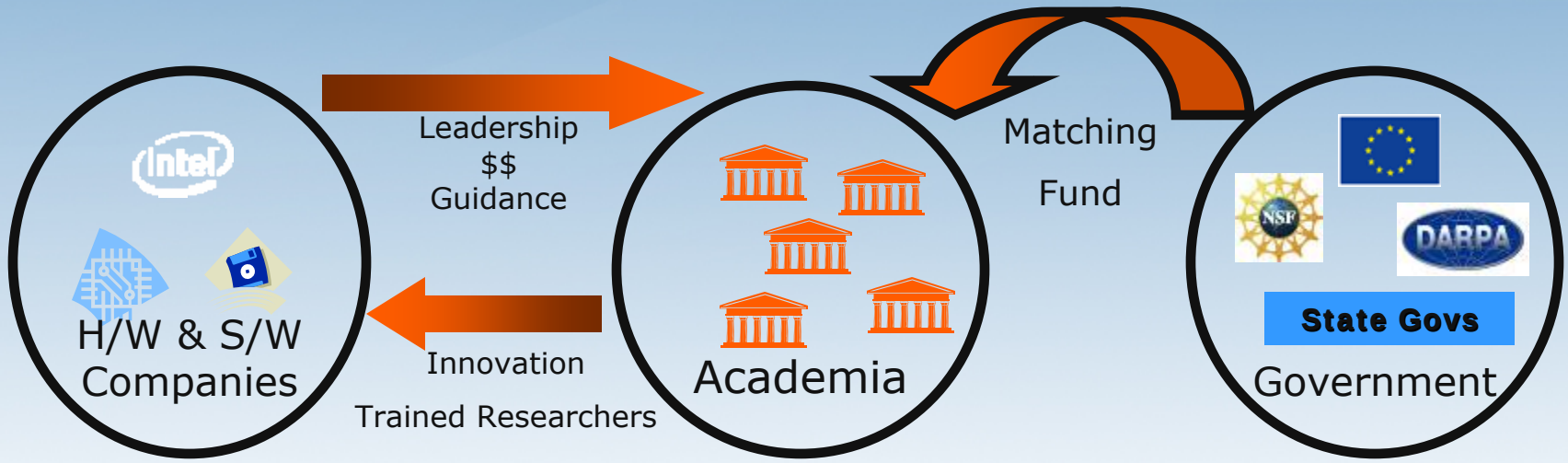
UPCRC Funding Strategy

Intel + Microsoft

$20 Million over 5 years

Matching University Investments

- **University of Illinois: $8 mil (committed)**
- **UC Berkeley: $7 mil (grant application)**



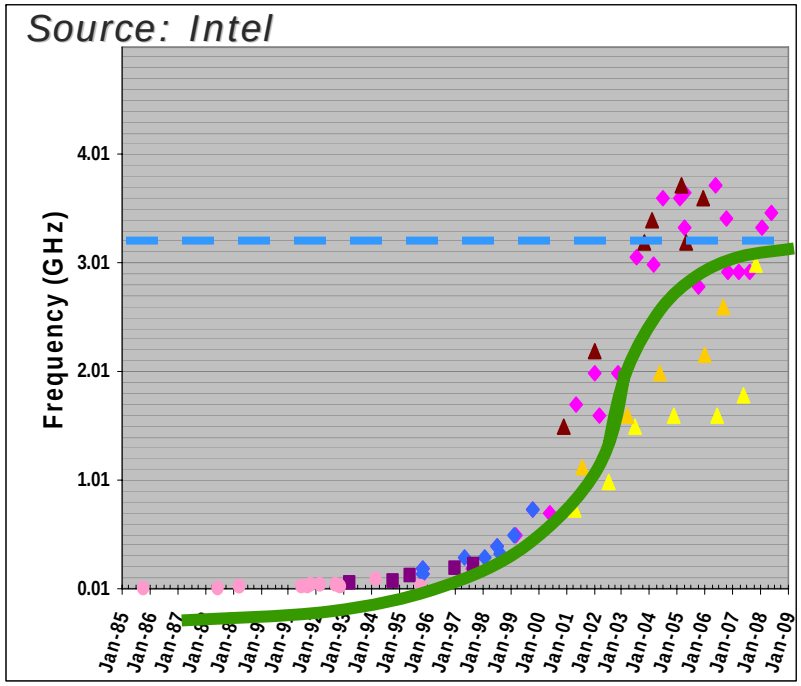
Major investment in mainstream parallel programming

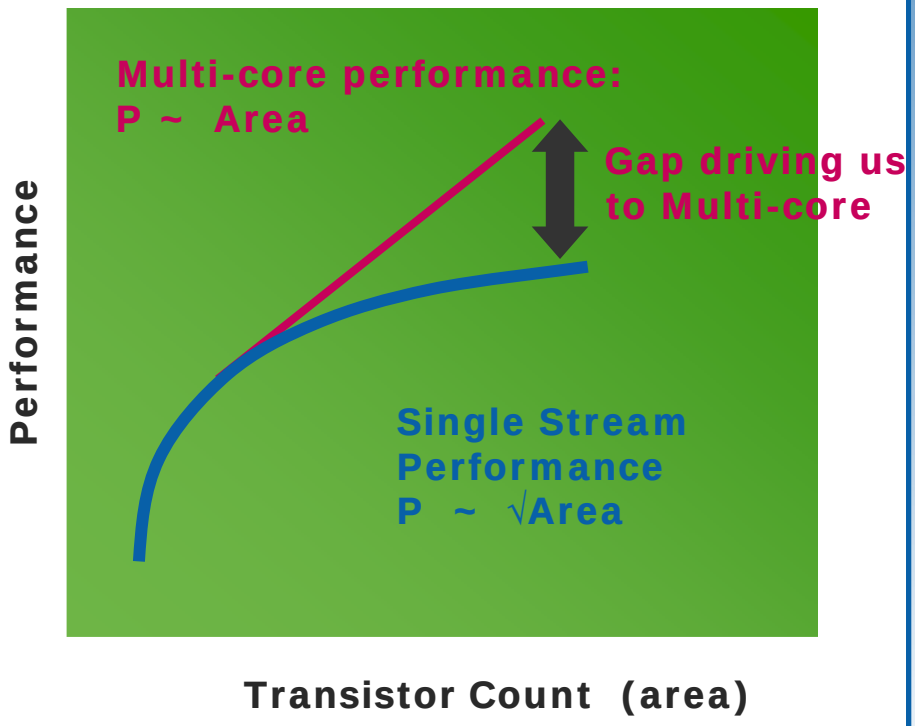
Future of Parallelism Computing

- **For Software and Hardware**
  - Parallelism in all computing systems
  - Dramatic new capabilities enabled by performance and performance / unit power
  - Established and varied software models for portable parallelism
  - Architecture support for Parallel Software and other capabilities

BACKGROUND

Single Core Performance is Stagnant

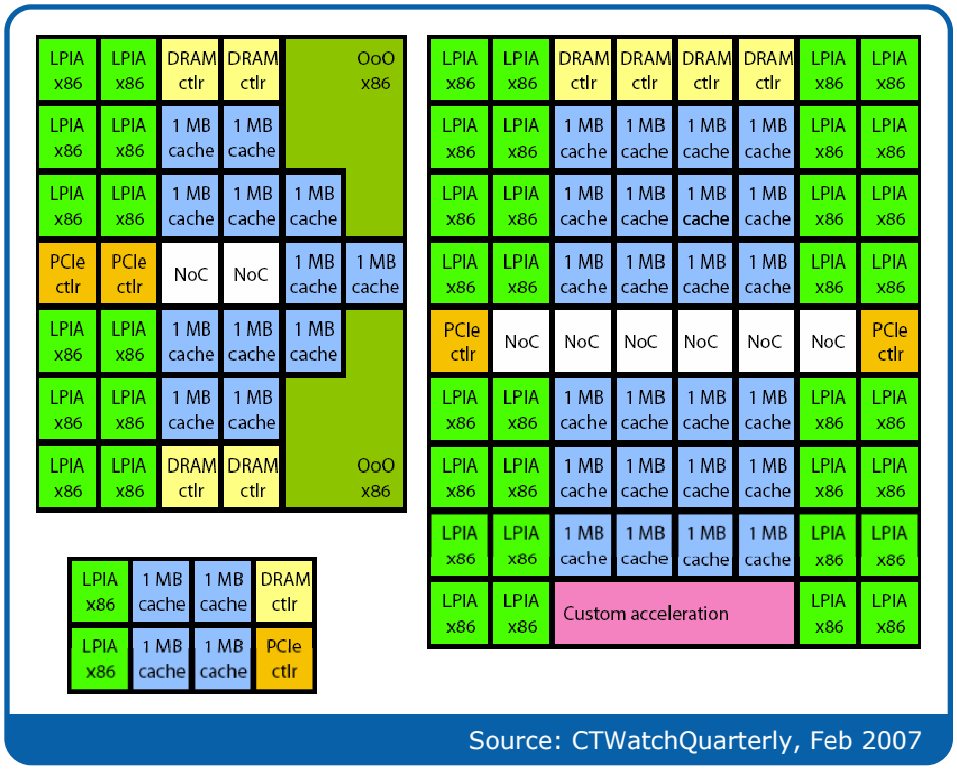




Frequency limited by leakage and power. Transistor counts continue to increase.

Many-core Research Questions Abound

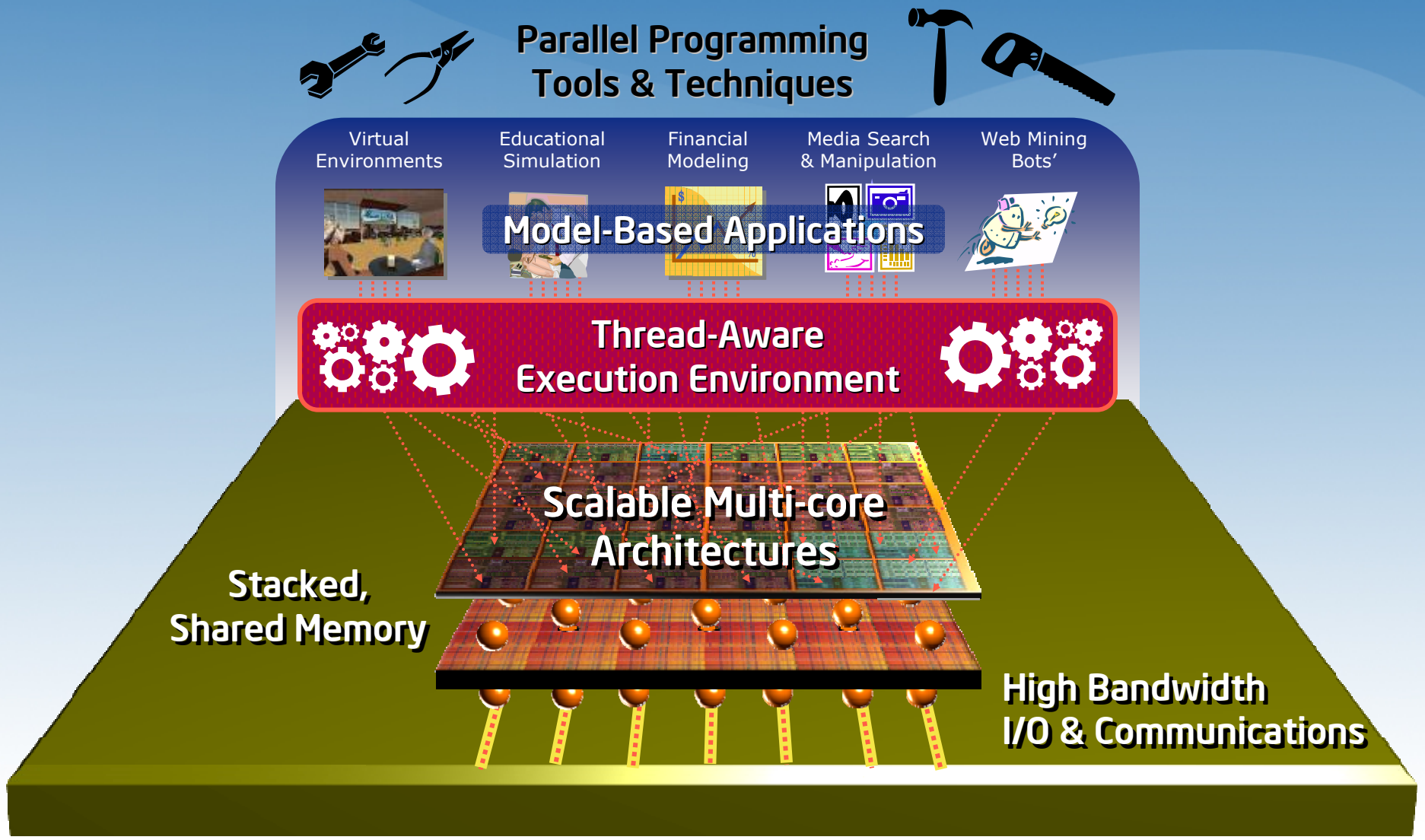
- **Cores**
  - How many? What size?
  - Homogenous, Heterogeneous
  - Programmable, Configurable, Fixed-function
- **Chip-level**
  - Interconnect: Topology, Bandwidth
  - Coordination
  - Management
- **Memory Hierarchy**
  - # of levels, sharing, inclusion
  - Bandwidth, novel Technology
  - Integration/Packaging
- **I/O Bandwidth**
  - Silicon-based photonics
  - Terabit links



Source: CTWatchQuarterly, Feb 2007

Manycore Chips (circa. 2012)?

Intel's Tera-scale Research Vision



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