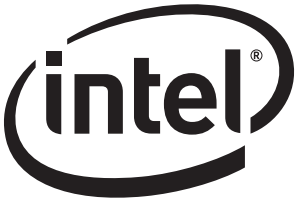


Intel® Desktop Board DP43TF

Technical Product Specification

July 2008

Order Number: E41955-001US

The Intel® Desktop Board DP43TF may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board DP43TF Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board DP43TF Technical Product Specification	July 2008

This product specification applies to only the standard Intel® Desktop Board DP43TF with BIOS identifier NBG4310A.86A.

Changes to this specification will be published in the Intel Desktop Board DP43TF Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board DP43TF. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the Intel Desktop Board DP43TF and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	A description of the BIOS error messages, beep codes, and POST codes
5	Regulatory compliance and battery disposal information

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

INTEGRATOR'S NOTES

Integrator's notes are used to call attention to information that may be useful to system integrators.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
Gbit	Gigabit (1, 073,741,824 bits)
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

Figures

Tables

1 Product Description

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of the Intel Desktop Board DP43TF.

Table 1. Feature Summary

Form Factor	ATX (11.60 inches by 9.60 inches [294.60 millimeters by 243.84 millimeters])
Processor	Support for the following: • Intel® Core™2 Quad processor in an LGA775 socket • Intel® Core™2 Duo processor in an LGA775 socket • Intel® Pentium® Dual-Core processor in an LGA775 socket • Intel® Celeron® Dual-Core processor in an LGA775 socket • Intel® Celeron® processor Sequence 400 in an LGA775 socket
Memory	• Four 240-pin DDR2 SDRAM Dual Inline Memory Module (DIMM) sockets • Support for DDR2 667 MHz or DDR2 800 MHz DIMMs • Support for up to 8 GB of system memory
Chipset	Intel® P43 Express Chipset, consisting of: • Intel® 82P43 Memory Controller Hub (MCH) • Intel® 82801JIB I/O Controller Hub (ICH10)
Audio	5.1+2-channel audio subsystem using the Realtek* ALC888VC audio codec
Legacy I/O Control	Legacy I/O controller for serial and PS/2* ports
Peripheral Interfaces	• Twelve USB 2.0 ports: six back panel connectors and six front panel headers • Six Serial ATA (SATA) interfaces • One Parallel ATA IDE interface with UDMA 33, ATA-66/100 support • Two IEEE 1394a interfaces: one port on the back panel and one front panel header • PS/2 keyboard and mouse ports • One serial port header (may require specialized chassis or cable for use)
LAN Support	Gigabit (10/100/1000 Mbits/sec) LAN subsystem using the Intel® 82567V Gigabit Ethernet Controller
BIOS	• Intel® BIOS (resident in the SPI Flash device) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Instantly Available PC Technology	• Support for PCI* Local Bus Specification Revision 2.3 • Support for PCI Express* Revision 1.1 • Suspend to RAM support • Wake on PCI, RS-232, front panel, PS/2 devices, and USB ports

continued

Table 1. Feature Summary (continued)

Expansion Capabilities	• Three PCI Conventional bus connectors • Three PCI Express x1 bus add-in card connector • One PCI Express x16 bus add-in card connector
Hardware Monitor Subsystem	• Intel® Quiet System Technology (Intel® QST) implemented through the Intel® Management Engine in ICH10 • Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values • Four fan headers • Four fan sense inputs used to monitor fan activity

1.1.2 Board Layout

Figure 1 shows the location of the major components.

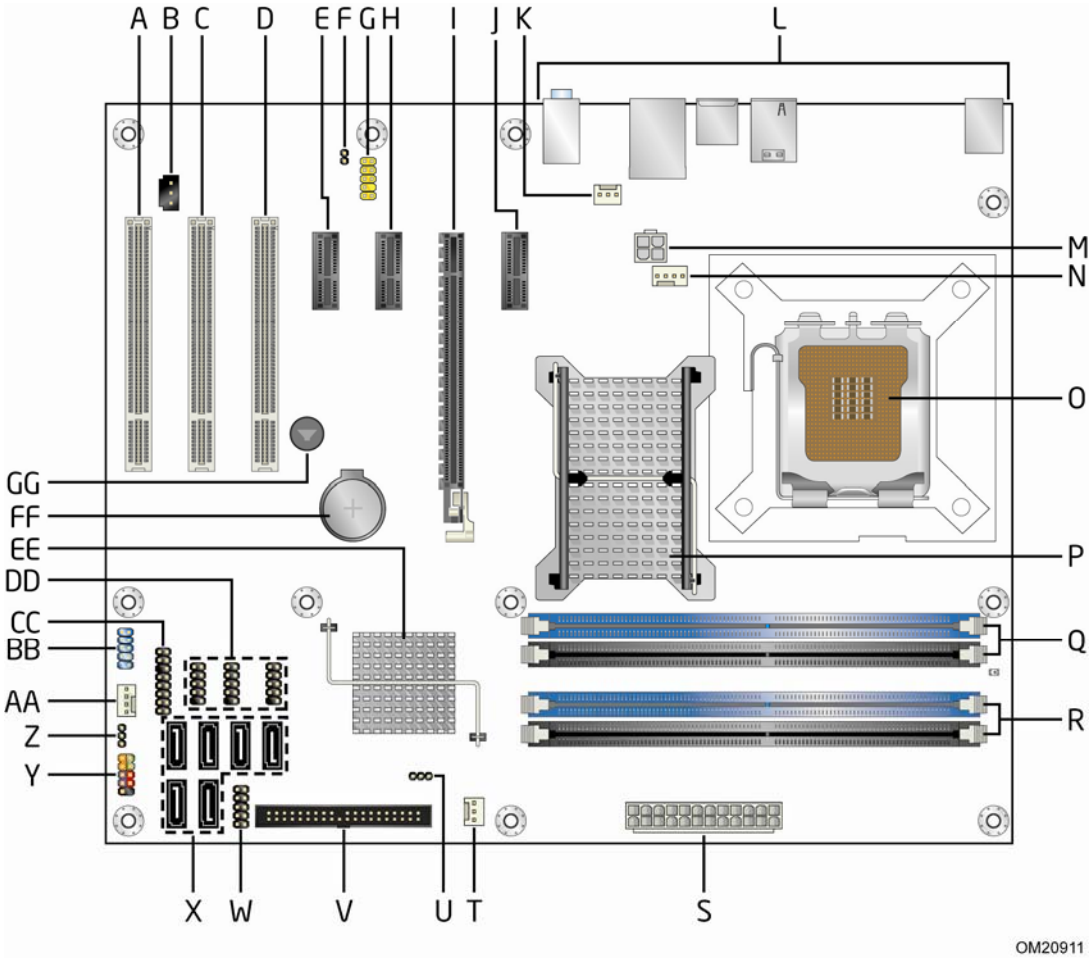


Figure 1. Major Board Components

Table 2 lists the components identified in Figure 1.

Table 2. Board Components Shown in Figure 1

Item/callout from Figure 1	Description
A	PCI Conventional bus add-in card connector
B	S/PDIF connector
C	PCI Conventional bus add-in card connector
D	PCI Conventional bus add-in card connector
E	PCI Express x1 connector
F	Chassis intrusion header
G	Front panel audio header
H	PCI Express x1 connector
I	PCI Express x16 connector
J	PCI Express x1 connector
K	Rear chassis fan header
L	Back panel connectors
M	Processor core power connector (2 X 2)
N	Processor fan header
O	LGA775 processor socket
P	Intel 82P43 MCH
Q	DIMM Channel A sockets
R	DIMM Channel B sockets
S	Main Power connector (2 X 12)
T	Front chassis fan header
U	BIOS Setup configuration jumper block
V	Parallel ATA IDE connector
W	Serial port header
X	Serial ATA connectors [6]
Y	Front panel header
Z	Auxiliary front panel power LED header
AA	Auxiliary front chassis fan header
BB	IEEE 1394a header
CC	High Definition Audio Link header
DD	Front panel USB headers [3]
EE	Intel 82801JIB I/O Controller Hub (ICH10)
FF	Battery
GG	Speaker

1.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas.

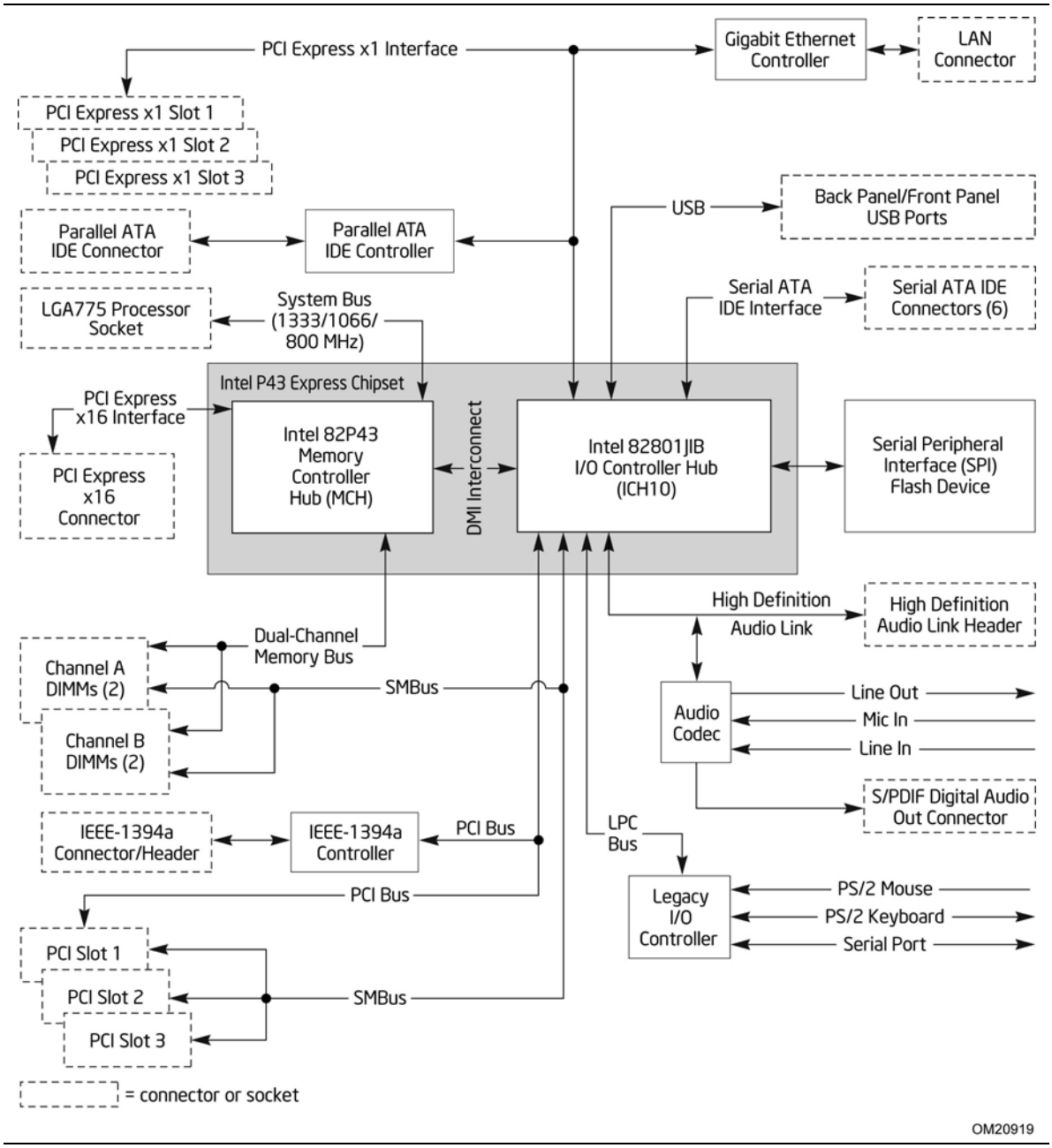


Figure 2. Block Diagram

1.2 Legacy Considerations

This board differs from other Intel® Desktop Board products, with specific changes including (but not limited to) the following:

- No parallel port
- No floppy drive connector
- No serial port on the back panel
- The serial port header is located near the SATA ports and may require a specialized chassis or cabling solution to use

1.3 Online Support

To find information about…	Visit this World Wide Web site:
Intel Desktop Board DP43TF	http://www.intel.com/products/motherboard/DP43TF/index.htm
Desktop Board Support	http://support.intel.com/support/motherboards/desktop
Available configurations for the Intel Desktop Board DP43TF	http://www.intel.com/products/motherboard/DP43TF/index.htm
Supported processors	http://processormatch.intel.com
Chipset information	http://www.intel.com/products/desktop/chipsets/index.htm
BIOS and driver updates	http://downloadcenter.intel.com
Tested Memory	http://support.intel.com/support/motherboards/desktop/sb/CS-025414.htm

1.4 Processor

The board is designed to support the following processors:

- Intel Core 2 Quad processor in an LGA775 socket
- Intel Core 2 Duo processor in an LGA775 socket
- Intel Pentium Dual-Core processor in an LGA775 socket
- Intel Celeron Dual-Core processor in an LGA775 socket
- Intel Celeron processor Sequence 400 in an LGA775 socket

Other processors may be supported in the future. This board is designed to support processors with a maximum wattage of 95 W. The processors listed above are only supported when falling within the wattage requirements of the board. See the Intel web site listed below for the most up-to-date list of supported processors.

For information about…	Refer to:
Supported processors	http://processormatch.intel.com

⚠ CAUTION

Use only the processors listed on the web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

INTEGRATOR'S NOTE

Use only ATX12V-compliant power supplies.

For information about	Refer to
Power supply connectors	Section 2.2.2.4, page 47

1.5 System Memory

The board has four DIMM sockets and supports the following memory features:

- 1.8 V DDR2 SDRAM DIMMs with gold plated contacts, with the option to raise the voltage to support higher performance DDR2 SDRAM DIMMs
- Dual channel interleaved mode support
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:

  Double-sided DIMMs with x16 organization are not supported.
- 8 GB maximum total system memory. Refer to Section 2.1.1 on page 37 for information on the total amount of addressable memory.
- Minimum total system memory: 512 MB
- Non-ECC DIMMs
- Serial Presence Detect
- DDR2 667 MHz or DDR2 800 MHz SDRAM DIMMs
- DDR2 667 MHz DIMMs with SPD timings of only 5-5-5 (tCL-tRCD-tRP)
- DDR2 800 MHz DIMMs with SPD timings of only 5-5-5 or 6-6-6 (tCL-tRCD-tRP)

NOTE

To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This enables the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.

Table 3 lists the supported DIMM configurations.

Table 3. Supported Memory Configurations

DIMM Type	SDRAM Technology	Smallest usable DIMM (one x16 Single-sided DIMM)	Largest usable DIMM (one x8 Double-sided DIMM)	Maximum capacity with four identical x8 Double-sided DIMMs
DDR2 667	512 Mbit	256 MB	1 GB	4 GB
DDR2 667	1 Gbit	512 MB	2 GB	8 GB
DDR2 800	512 Mbit	256 MB	1 GB	4 GB
DDR2 800	1 Gbit	512 MB	2 GB	8 GB

For information about...	Refer to:
Tested Memory	http://support.intel.com/support/motherboards/desktop/sb/CS-025414.htm

1.5.1 Memory Configurations

The Intel 82P43 MCH supports the following types of memory organization:

- **Dual channel (Interleaved) mode**. This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Single channel (Asymmetric) mode**. This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Flex mode**. This mode provides the most flexible performance characteristics. The bottommost DRAM memory (the memory that is lowest within the system memory map) is mapped to dual channel operation; the topmost DRAM memory (the memory that is nearest to the 8 GB address space limit), if any, is mapped to single channel operation. Flex mode results in multiple zones of dual and single channel operation across the whole of DRAM memory. To use flex mode, it is necessary to populate both channels.

For information about…	Refer to:
Memory Configuration Examples	http://www.intel.com/support/motherboards/desktop/sb/cs-011965.htm

Figure 3 illustrates the memory channel and DIMM configuration.

NOTE

The DIMM 0 sockets of both channels are blue. The DIMM 1 sockets of both channels are black.

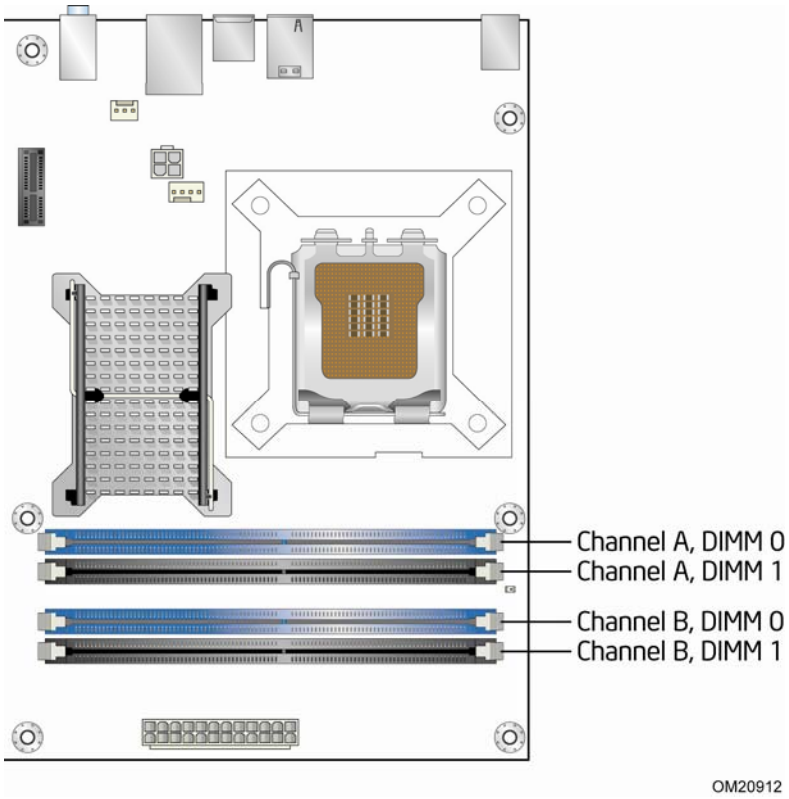


Figure 3. Memory Channel Configuration and DIMM Configuration

INTEGRATOR'S NOTE

Regardless of the memory configuration used (dual channel, single channel, or flex mode), DIMM 0 of Channel A must always be populated. This is a requirement of the Intel Management Engine in ICH10.

1.6 Intel® P43 Express Chipset

The Intel P43 Express chipset consists of the following devices:

- Intel 82P43 Memory Controller Hub (MCH) with Direct Media Interface (DMI) interconnect
- Intel 82801JIB I/O Controller Hub (ICH10)

The MCH component provides interfaces to the CPU, memory, PCI Express, and the DMI interconnect. The ICH10 is a centralized controller for the board's I/O paths.

The chipset supports the following features:

- USB
- Serial ATA
- Parallel IDE

For information about	Refer to
The Intel P43 Express chipset	http://www.intel.com/products/desktop/chipsets/index.htm
Resources used by the chipset	Chapter 2

1.6.1 PCI Express x16 Graphics

The MCH also supports add in discrete graphics card via the PCI Express 2.0 graphics connector.

- PCI Express 2.0 x16:
  - Supports PCI Express GEN1 frequency of 1.25 GHz resulting in 2.5 Gb/s each direction (500 MB/s total). Maximum theoretical bandwidth on interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when operating in x16 mode.
  - Supports PCI Express GEN2 frequency of 2.5 GHz resulting in 5.0 Gb/s each direction (1000 MB/s total). Maximum theoretical bandwidth on interface of 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s when operating in x16 mode.

For information about	Refer to
PCI Express technology	http://www.pcisig.com

1.6.2 USB

The board supports up to twelve USB 2.0 ports, supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers.

The ICH10 provides the USB controller for all ports. The port arrangement is as follows:

- Six ports are implemented with stacked back panel connectors
- Six ports are routed to three separate front panel USB headers

For information about	Refer to
The location of the USB connectors on the back panel	Figure 9, page 41
The location of the front panel USB headers	Figure 10, page 42

1.6.3 Serial ATA Interfaces

The board provides four Serial ATA (SATA) connectors, which support one device per connector.

1.6.3.1 Serial ATA Support

The board's Serial ATA controller offers six independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbits/sec per port. One device can be installed on each port for a maximum of six Serial ATA devices. A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows* XP operating system.

NOTE

Many Serial ATA drives use new low-voltage power connectors and require adapters or power supplies equipped with low-voltage power connectors.

For more information, see: http://www.serialata.org/

For information about	Refer to
The location of the Serial ATA connectors	Figure 10, page 42

1.7 Parallel IDE Controller

The Parallel ATA IDE controller has one bus-mastering Parallel ATA IDE interface. The Parallel ATA IDE interface supports the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The Parallel ATA IDE interface also supports ATAPI devices (such as CD-ROM drives) and ATA devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

For information about	Refer to
The location of the Parallel ATA IDE connector	Figure 10, page 42

1.8 Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 11 shows the location of the battery.

1.9 Legacy I/O Controller

The I/O controller provides the following features:

- One serial port header
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

1.9.1 Serial Port Interface

The serial port header is located on the component side of the board. The serial port supports data transfers at speeds up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port header	Figure 10, page 42
The serial port header signal mapping	Table 14, page 44

1.9.2 PS/2 Keyboard and Mouse Interface

The PS/2 keyboard and mouse connectors are located on the back panel.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 9, page 41

1.10 Audio Subsystem

The onboard audio subsystem consists of the following:

- Intel 82801JIB (ICH10)
- Realtek ALC888VC audio codec
- Back panel audio connectors
- Component-side audio header:
  - Intel® High Definition Audio front panel header

The audio subsystem supports the following features:

- A signal-to-noise (S/N) ratio of 95 dB
- Independent 5.1 audio playback from back panel connectors and stereo playback from the Intel High Definition Audio front panel header.

NOTE

Systems built with an AC 97 front panel will not be able to obtain the Microsoft Windows Vista logo.*

Table 4 lists the supported functions of the front panel and back panel audio jacks.

Table 4. Audio Jack Support

Audio Jack	Supports Line in?	Supports Rear Surround?	Supports Center/ LFE?	Supports Micro-phone?	Supports Line/Head-phones out?
Front panel – Green	No	No	No	No	Yes
Front panel – Pink	No	No	No	Yes	No
Back panel – Blue	Yes	Yes	No	No	No
Back panel – Green	No	No	No	No	Yes
Back panel – Pink	No	No	Yes	Yes	No

1.10.1 Audio Subsystem Software

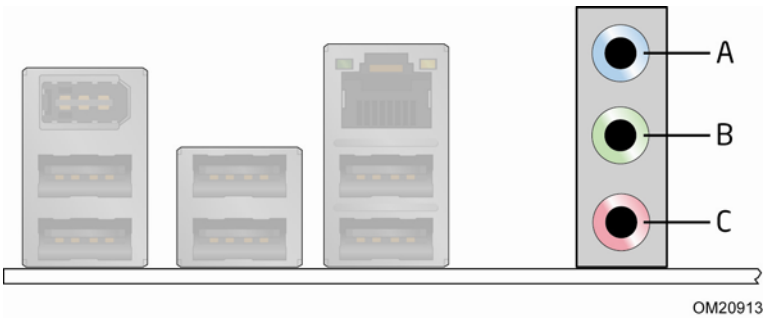
Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.2, page 14

1.10.2 Audio Connectors and Headers

The board contains audio connectors on the back panel and audio headers on the component side of the board. The front panel audio header provides mic in and line out signals for the front panel. Microphone bias is supported for both the front and back panel microphone connectors.

The front/back panel audio connectors are configurable through the audio device drivers. The available configurable audio ports are shown in Figure 4.



Item	Description
A	Line in
B	Line out
C	Mic in

Figure 4. Back Panel Audio Connector Options

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

For information about	Refer to
The location of the front panel audio header	Figure 10, page 42
The signal names of the front panel audio header	Table 18, page 45
The back panel audio connectors	Section 2.2.1, page 41

1.11 LAN Subsystem

The LAN subsystem consists of the following:

- Intel 82567V Gigabit Ethernet Controller (10/100/1000 Mbits/sec)
- Intel 82801JIB (ICH10)
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- CSMA/CD protocol engine
- LAN connect interface between ICH10 and the LAN controller
- PCI Conventional bus power management
  - ACPI technology support
  - LAN wake capabilities
- LAN subsystem software

For information about	Refer to
LAN software and drivers	http://downloadcenter.intel.com

1.11.1 Intel® 82567V Gigabit Ethernet Controller

The Intel 82567V Gigabit Ethernet Controller supports the following features:

- PCI Express link
- 10/100/1000 IEEE 802.3 compliant
- Compliant to IEEE 802.3x flow control support
- 802.1p and 802.1q
- TCP, IP, and UDP checksum offload (for IPv4 and IPv6)
- Transmit TCP segmentation
- Full device driver compatibility
- PCI Express power management support

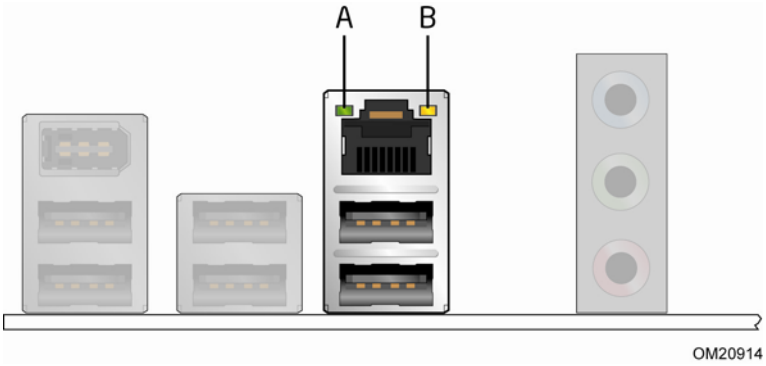
1.11.2 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 14

1.11.3 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 5 below).



Item	Description
A	Link LED (Green)
B	Data Rate LED (Green/Yellow)

Figure 5. LAN Connector LED Locations

Table 5 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 5. LAN Connector LED States

LED	LED Color	LED State	Condition
Link	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Data Rate	Green/Yellow	Off	10 Mbits/sec data rate is selected.
		Green	100 Mbits/sec data rate is selected.
		Yellow	1000 Mbits/sec data rate is selected.

1.12 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Fan monitoring and control
- Thermal and voltage monitoring
- Chassis intrusion detection

1.12.1 Hardware Monitoring and Fan Control

The features of the hardware monitoring and fan control include:

- Intel Quiet System Technology, delivering acoustically-optimized thermal management
- Fan speed control controllers and sensors integrated into the ICH10
- Four thermal sensors (processor, 82P43 MCH, 82801JIB ICH10, and a remote thermal sensor)
- Power supply monitoring of five voltages (+5 V, +12 V, +3.3 V, +1.25 V, and +VCCP) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control, for all four fans, that can adjust the fan speed according to thermal conditions

1.12.2 Fan Monitoring

Fan monitoring can be implemented using Intel® Desktop Utilities or third-party software.

For information about	Refer to
The functions of the fan headers	Section 1.13.2.2, page 34
Location of the fan headers	Figure 6, page 29

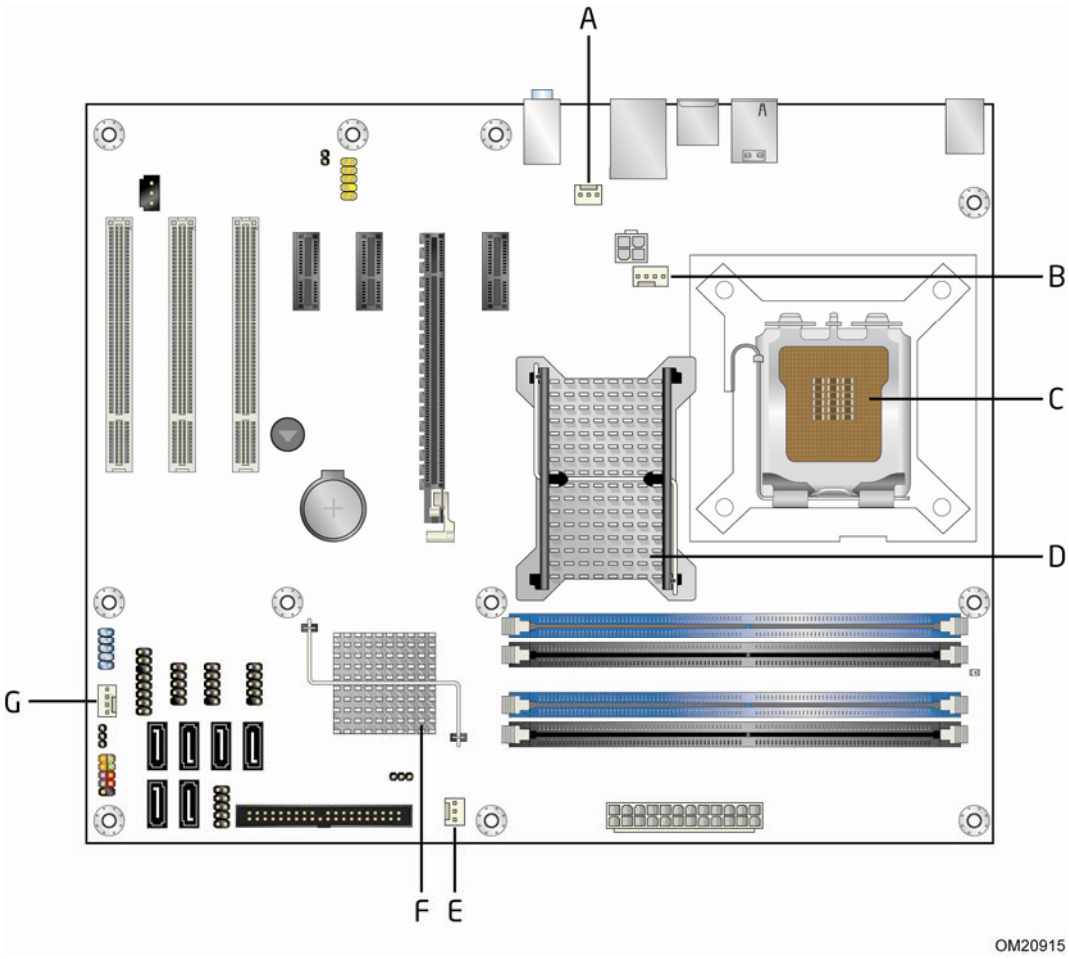
1.12.3 Chassis Intrusion and Detection

The board supports a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion header. When the chassis cover is removed, the mechanical switch is in the closed position.

For information about	Refer to
The location of the chassis intrusion header	Figure 10, page 42

1.12.4 Thermal Monitoring

Figure 6 shows the locations of the thermal sensors and fan headers.



Item	Description
A	Rear chassis fan
B	Processor fan
C	Thermal diode, located on processor die
D	Thermal diode, located on the MCH die
E	Front chassis fan
F	Thermal diode, located on the ICH10 die
G	Auxiliary front chassis fan

Figure 6. Thermal Sensors and Fan Headers

NOTE

The minimum thermal reporting threshold for the MCH is 66 °C. The MCH thermal sensor will display 66 °C until the temperature rises above this point.

1.13 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan headers
  - LAN wake capabilities
  - Instantly Available PC technology
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support

1.13.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 8 on page 32)
- Support for a front panel power and sleep mode switch

Table 6 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 6. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

1.13.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 7 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 7. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off. AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.13.1.2 Wake-up Devices and Events

Table 8 lists the devices or specific events that can wake the computer from specific states.

Table 8. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
LAN	S1, S3, S4, S5 (Note 1)
PME# signal	S1, S3, S4, S5 (Note 1)
Power switch	S1, S3, S4, S5
PS/2 devices	S1, S3, S5 (Note 2)
RTC alarm	S3, S4, S5
Serial port	S3
USB	S3
WAKE# signal	S1, S3, S4, S5

Notes:

1. For LAN and PME# signal, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.
2. S5 wake from PS/2 is disabled by default.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.13.2 Hardware Support

⚠ CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The board provides several power management hardware features, including:

- Power connector
- Fan headers
- LAN wake capabilities
- Instantly Available PC technology
- Wake from USB
- Wake from PS/2 keyboard
- PME# signal wake-up support
- WAKE# signal wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

NOTE

The use of Wake from USB from an ACPI state requires an operating system that provides full ACPI support.

1.13.2.1 Power Connector

ATX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the main power connector	Figure 10, page 42
The signal names of the main power connector	Table 22, page 47

1.13.2.2 Fan Headers

The function/operation of the fan headers is as follows:

- The fans are on when the board is in the S0 state.
- The fans are off when the board is off or in the S3, S4, or S5 state.
- The processor fan header is wired to a fan tachometer input. The front and rear fan headers each have independent tachometer input to the hardware monitoring and fan control device. All fan headers support closed-loop fan control that can adjust the fan speed according to thermal conditions.
- All fan headers have a +12 V DC connection.

For information about	Refer to
The locations of the fan headers and thermal sensors	Figure 6, page 29
The signal names of the processor fan header	Table 17, page 45
The signal names of the chassis fan headers	Table 15, page 45

1.13.2.3 LAN Wake Capabilities

CAUTION

For LAN wake capabilities, the +5 V standby line from the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the board supports LAN wake capabilities with ACPI in the following ways:

- The PCI Express WAKE# signal
- The PCI bus PME# signal for PCI 2.3 compliant LAN designs
- The onboard LAN subsystem

1.13.2.4 Instantly Available PC Technology

CAUTION

For Instantly Available PC technology, the +5 V standby line from the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 8 on page 32 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.3 compliant add-in cards and drivers.

1.13.2.5 Wake from USB

USB bus activity wakes the computer from ACPI S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.13.2.6 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1, S3, and S5 state.

1.13.2.7 PME# Signal Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state (with Wake on PME enabled in BIOS).

1.13.2.8 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state.

1.13.2.9 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 7 shows the location of the standby power indicator LED.

CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

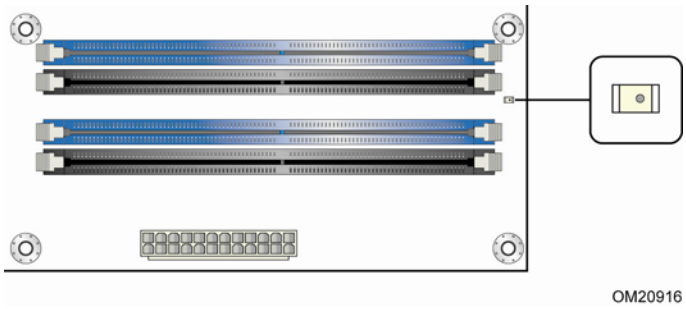


Figure 7. Location of the Standby Power Indicator LED

1.13.3 ENERGY STAR*

In 2007, the US Department of Energy and the US Environmental Protection Agency revised the ENERGY STAR* requirements. Intel has worked directly with these two governmental agencies to define the new requirements. This Intel Desktop Board meets the Category C requirements.

For information about	Refer to
ENERGY STAR requirements and recommended configurations	http://www.intel.com/go/energystar

2 Technical Reference

2.1 Memory Map

2.1.1 Addressable Memory

The board utilizes 8 GB of addressable system memory. Typically the address space that is allocated for PCI Conventional bus add-in cards, PCI Express configuration space, BIOS (SPI Flash), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 8 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/ SPI Flash (32 Mbits)
- Local APIC (19 MB)
- Direct Media Interface (40 MB)
- Front side bus interrupts (17 MB)
- PCI Express configuration space (256 MB)
- MCH base address registers, internal graphics ranges, PCI Express ports (up to 512 MB)
- Memory-mapped I/O that is dynamically allocated for PCI Conventional and PCI Express add-in cards
- Intel® Management Engine (Intel® ME) support (6 MB)
- Base graphics memory support (1 MB or 8 MB)

NOTE

System resources and hardware (such as PCI and PCI Express) require physical memory address locations that can reduce available addressable system memory. This could result in a reduction of as much as 1 GB or more of physical addressable memory being available to the operating system and applications, depending on the system configuration and operating system.*

The amount of installed memory that can be used will vary based on add-in cards and BIOS settings. Figure 8 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses.

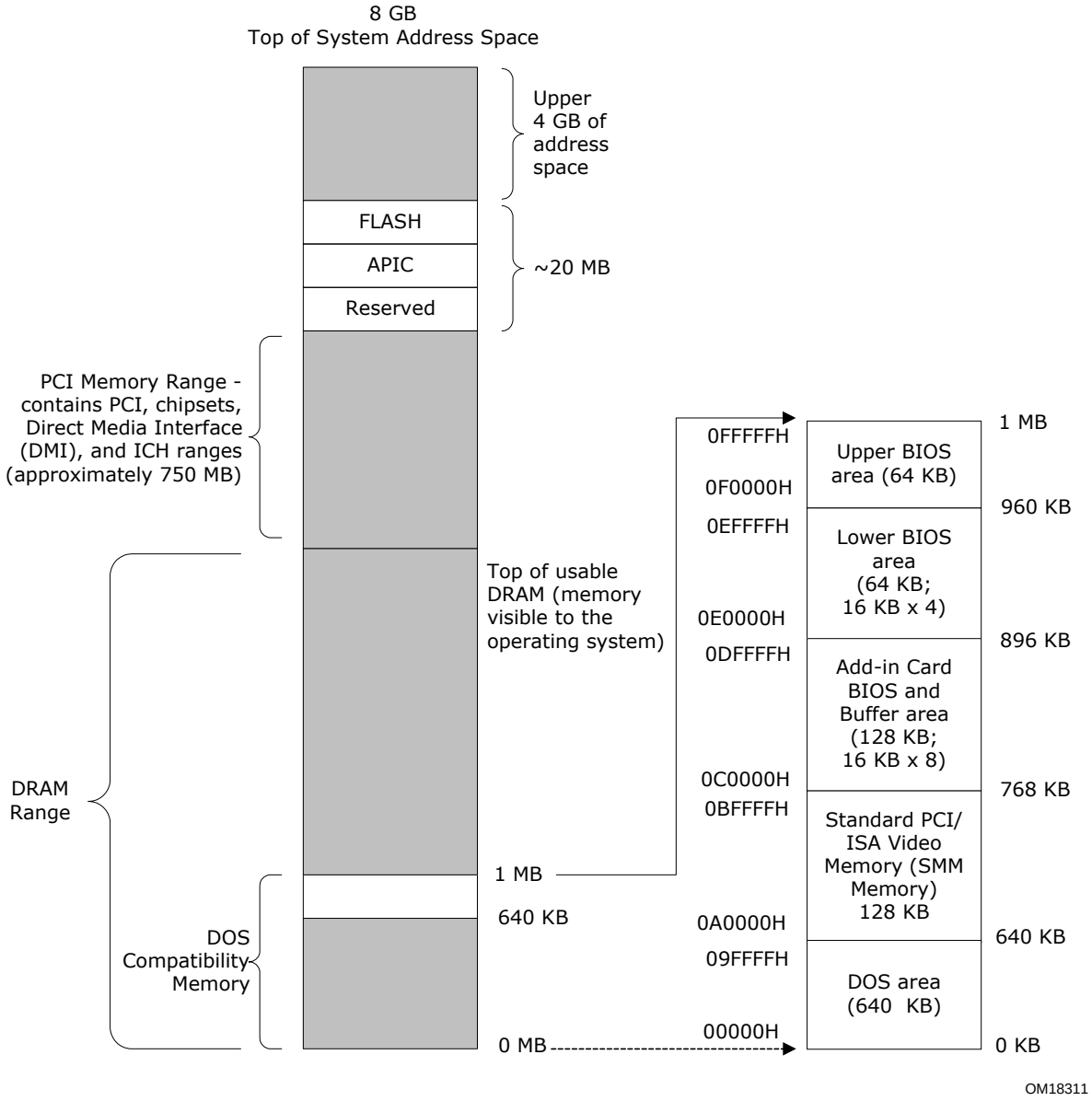


Figure 8. Detailed System Memory Address Map

Table 9 lists the system memory map.

Table 9. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 8388608 K	100000 - 1FFFFFFFF	8191 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.2 Connectors and Headers

CAUTION

Only the following connectors and headers have overcurrent protection: Back panel and front panel USB and PS/2.

The other internal connectors/headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors/headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

NOTE

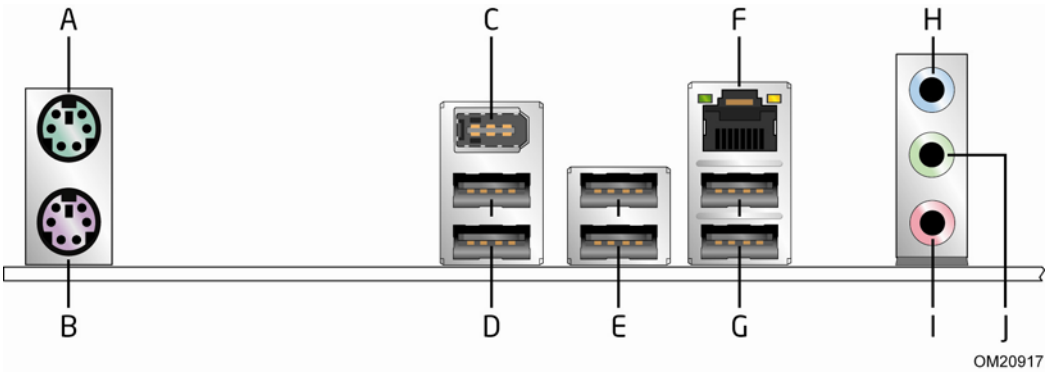
Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

This section describes the board's connectors and headers. The connectors and headers can be divided into these groups:

- Back panel I/O connectors (see page 41)
- Component-side connectors and headers (see page 42)

2.2.1 Back Panel Connectors

Figure 9 shows the locations of the back panel connectors.



Item	Description
A	PS/2 mouse port
B	PS/2 keyboard port
C	IEEE 1394a port
D	USB ports [2]
E	USB ports [2]
F	LAN
G	USB ports [2]
H	Line in
I	Mic in
J	Line out

Figure 9. Back Panel Connectors

2.2.2 Component-side Connectors and Headers

Figure 10 shows the locations of the component-side connectors and headers.

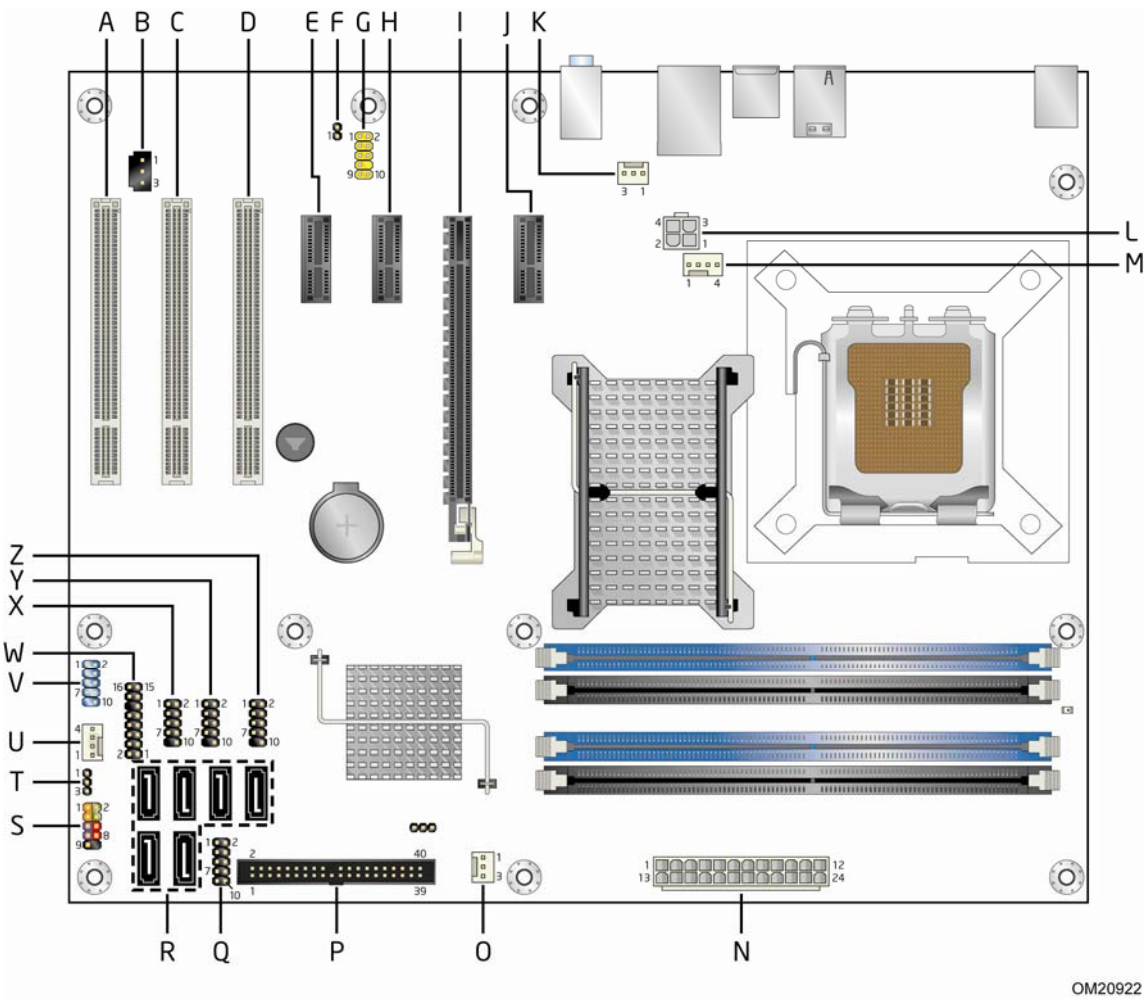


Figure 10. Component-side Connectors and Headers

Table 10 lists the component-side connectors and headers identified in Figure 10.

Table 10. Component-side Connectors and Headers Shown in Figure 10

Item/callout from Figure 10	Description
A	PCI Conventional bus add-in card connector
B	S/PDIF connector
C	PCI Conventional bus add-in card connector
D	PCI Conventional bus add-in card connector
E	PCI Express x1 connector
F	Chassis intrusion header
G	Front panel audio header
H	PCI Express x1 connector
I	PCI Express x16 connector
J	PCI Express x1 connector
K	Rear chassis fan header
L	Processor core power connector (2 X 2)
M	Processor fan header
N	Main Power connector (2 X 12)
O	Front chassis fan header
P	Parallel ATA IDE connector
Q	Serial port header
R	Serial ATA connectors [6]
S	Front panel header
T	Auxiliary front panel power LED header
U	Auxiliary front chassis fan header
V	IEEE 1394a header
W	High Definition Audio Link header
X	Front panel USB header
Y	Front panel USB header
Z	Front panel USB header

2.2.2.1 Signal Tables for the Connectors and Headers

Table 11. HD Audio Link Header

Pin	Signal Name	Pin	Signal Name
1	BCLK	2	Ground
3	RST#	4	DVDD IO
5	SYNC	6	Ground
7	SDO	8	3.3 V DVDD CORE
9	SDI0	10	+12 V
11	SDI1	12	Key (no pin)
13	Not connected	14	3.3 V DUAL
15	Not connected	16	Ground

Table 12. Serial ATA Connectors

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

Table 13. Chassis Intrusion Header

Pin	Signal Name
1	Intruder
2	Ground

Table 14. Serial Port Header

Pin	Signal Name	Pin	Signal Name
1	DCD	2	RXD#
3	TXD#	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	Key (no pin)

Table 15. Front and Rear Chassis Fan Headers

Pin	Signal Name
1	Control
2	+12 V
3	Tach

Table 16. Auxiliary Chassis Fan Header

Pin	Signal Name
1	Ground
2	+12 V
3	FAN_TACH
4	FAN_CONTROL

Table 17. Processor Fan Header

Pin	Signal Name
1	Ground
2	+12 V
3	FAN_TACH
4	FAN_CONTROL

Table 18. Front Panel Audio Header for Intel HD Audio

Pin	Signal Name	Pin	Signal Name
1	[Port 1] Left channel	2	Ground
3	[Port 1] Right channel	4	PRESENCE# (Dongle present)
5	[Port 2] Right channel	6	[Port 1] SENSE_RETURN
7	SENSE_SEND (Jack detection)	8	Key (no pin)
9	[Port 2] Left channel	10	[Port 2] SENSE_RETURN

Table 19. Front Panel Audio Header for AC ’97 Audio

Pin	Signal Name	Pin	Signal Name
1	MIC	2	AUD_GND
3	MIC_BIAS	4	AUD_GND
5	FP_OUT_R	6	FP_RETURN_R
7	AUD_5V	8	KEY (no pin)
9	FP_OUT_L	10	FP_RETURN_L

2.2.2.2 Add-in Card Connectors

The board has the following add-in card connectors:

- One PCI Express 2.0 x16 connector:
  - Supports PCI Express 1.1 frequency of 1.25 GHz resulting in 2.5 Gb/s each direction (500 MB/s total). The maximum theoretical bandwidth on the interface is 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when operating in x16 mode.
  - Supports PCI Express 2.0 frequency of 2.5 GHz resulting in 5.0 Gb/s each direction (1000 MB/s total). The maximum theoretical bandwidth on the interface is 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s when operating in x16 mode.
- PCI Express x1: three PCI Express x1 connectors. The x1 interfaces support simultaneous transfer speeds up to 250 Mbytes/sec of peak bandwidth per direction and up to 500 MB/sec concurrent bandwidth.
- PCI Conventional (rev 2.3 compliant) bus: three PCI Conventional bus add-in card connectors. The SMBus is routed to all PCI Conventional bus connectors. PCI Conventional bus add-in cards with SMBus support can access sensor data and other information residing on the board.

Note the following considerations for the PCI Conventional bus connectors:

- All of the PCI Conventional bus connectors are bus master capable.
- SMBus signals are routed to all PCI Conventional bus connectors. This enables PCI Conventional bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.

2.2.2.3 Auxiliary Front Panel Power/Sleep LED Header

Pins 1 and 3 of this header duplicate the signals on pins 2 and 4 of the front panel header.

Table 20. Auxiliary Front Panel Power/Sleep LED Header

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.2.2.4 Power Supply Connectors

The board has the following power supply connectors:

- **Main power** – a 2 x 12 connector. This connector is compatible with 2 x 10 connectors previously used on Intel Desktop boards. The board supports the use of ATX12V power supplies with either 2 x 10 or 2 x 12 main power cables. When using a power supply with a 2 x 10 main power cable, attach that cable on the rightmost pins of the main power connector, leaving pins 11, 12, 23, and 24 unconnected.
- **Processor core power** – a 2 x 2 connector. This connector provides power directly to the processor voltage regulator and must always be used. Failure to do so will prevent the board from booting.

Table 21. Processor Core Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	+12 V	4	+12 V

Table 22. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	Ground	15	Ground
4	+5 V	16	PS-ON# (power supply remote on/off)
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	PWRGD (Power Good)	20	No connect
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V (Note)	23	+5 V (Note)
12	2 x 12 connector detect (Note)	24	Ground (Note)

Note: When using a 2 x 10 power supply cable, this pin will be unconnected.

For information about	Refer to
Power supply considerations	Section 2.5.1, page 53

2.2.2.5 Front Panel Header

This section describes the functions of the front panel header. Table 23 lists the signal names of the front panel header. Figure 11 is a connection diagram for the front panel header.

Table 23. Front Panel Header

Pin	Signal	In/ Out	Description	Pin	Signal	In/ Out	Description
Hard Drive Activity LED				**Power LED**			
1	HD_PWR	Out	Hard disk LED pull-up to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
Reset Switch				**On/Off Switch**			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Power				**Not Connected**			
9	+5 V		Power	10	N/C		Not connected

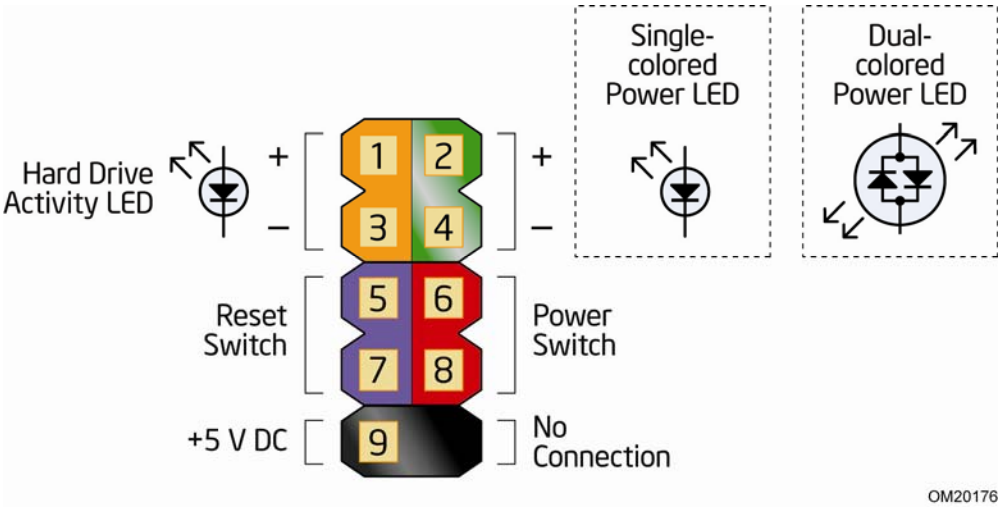


Figure 11. Connection Diagram for Front Panel Header

2.2.2.5.1 Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires one of the following:

- A Serial ATA hard drive connected to an onboard Serial ATA connector
- A Parallel ATA IDE hard drive connected to an onboard Parallel ATA IDE connector

2.2.2.5.2 Reset Switch Header

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.2.2.5.3 Power/Sleep LED Header

Pins 2 and 4 can be connected to a one- or two-color LED. Table 24 shows the possible states for a one-color LED. Table 25 shows the possible states for a two-color LED.

Table 24. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running

Table 25. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Steady Yellow	Sleeping

NOTE

The colors listed in Table 24 and Table 25 are suggested colors only. Actual LED colors are chassis-specific.

2.2.2.5.4 Power Switch Header

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.2.2.6 Auxiliary Front Panel Power LED Header

Pins 1 and 3 of this header duplicate the signals on pins 2 and 4 of the front panel header.

Table 26. Auxiliary Front Panel Power LED Header

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.2.2.7 Front Panel USB Headers

Figure 12 is a connection diagram for the front panel USB headers.

INTEGRATOR'S NOTES

- *The +5 V DC power on the front panel USB headers is fused.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

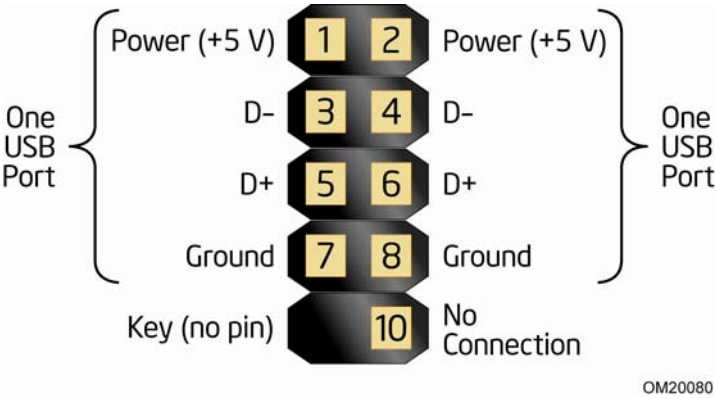


Figure 12. Connection Diagram for Front Panel USB Headers

2.2.2.8 Front Panel IEEE 1394a Header

Figure 13 is a connection diagram for the IEEE 1394a header.

INTEGRATOR'S NOTES

- *The +12 V DC power on the IEEE 1394a header is fused.*
- *The IEEE 1394a header provides one IEEE 1394a port.*

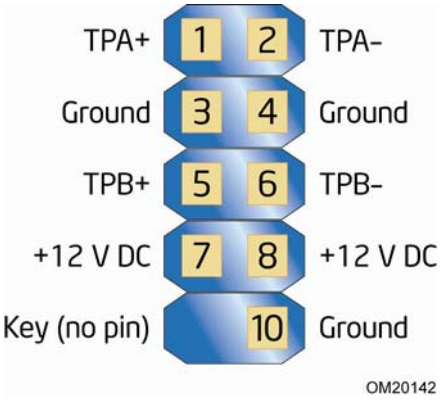


Figure 13. Connection Diagram for IEEE 1394a Header

2.3 Jumper Block

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 14 shows the location of the jumper block. The jumper determines the BIOS Setup program's mode. Table 27 lists the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

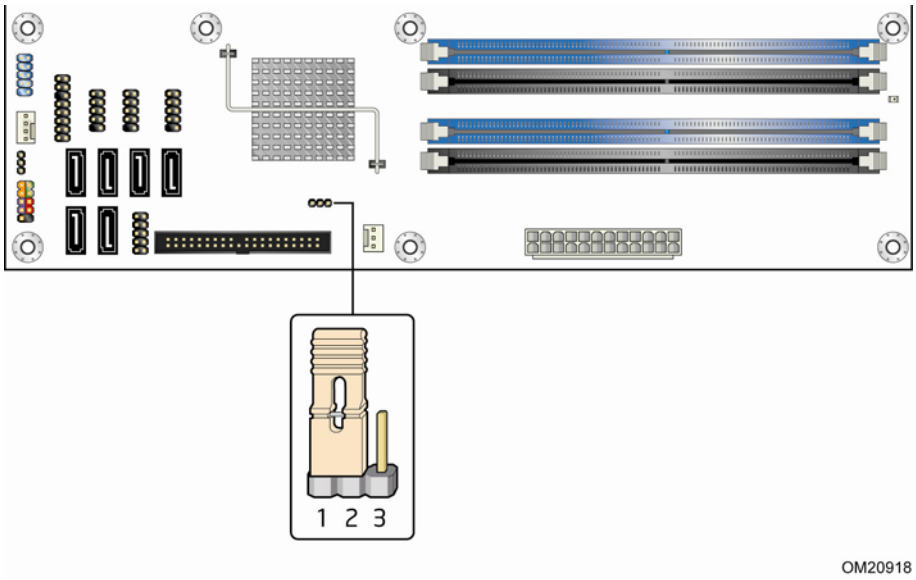
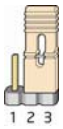
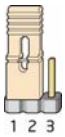


Figure 14. Location of the Jumper Block

Table 27. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. See Section 3.7 for more information on BIOS recovery.

2.4 Mechanical Considerations

2.4.1 Form Factor

The board is designed to fit into an ATX-form-factor chassis. Figure 15 illustrates the mechanical form factor of the board. Dimensions are given in inches [millimeters]. The outer dimensions are 11.60 inches by 9.60 inches [294.60 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

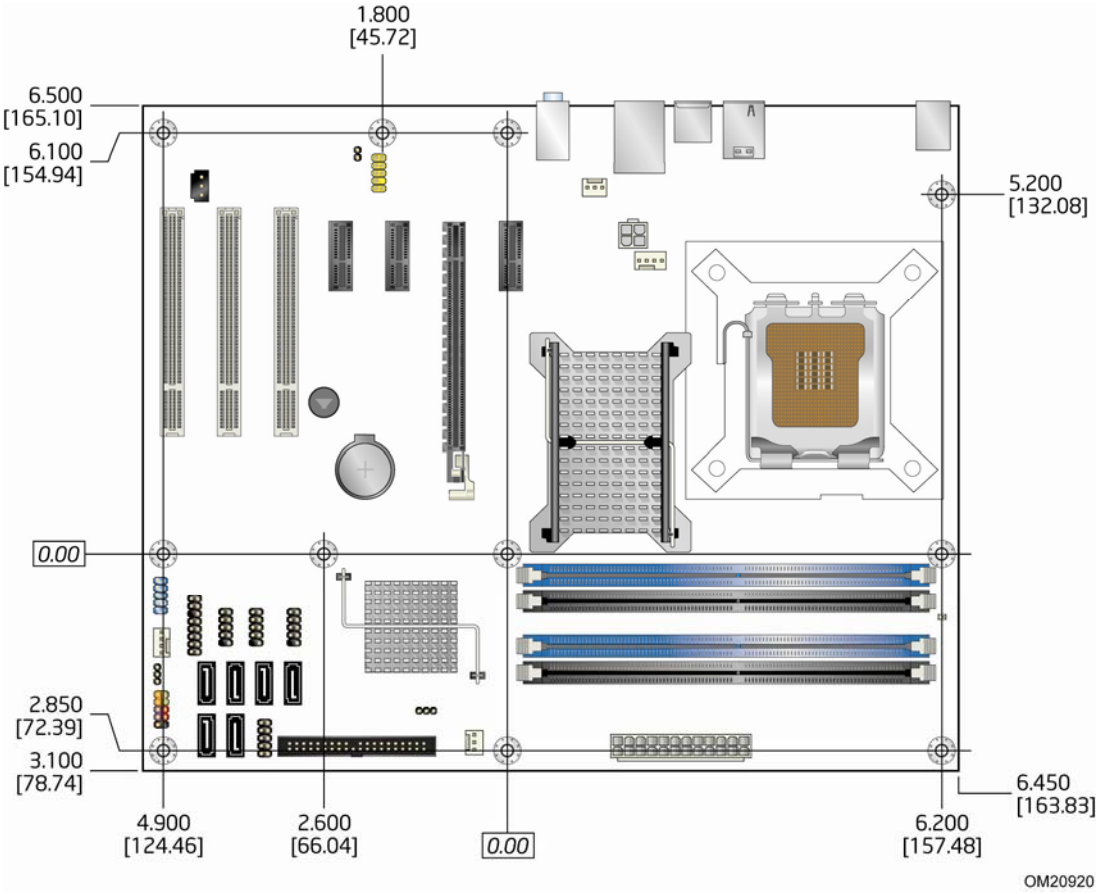


Figure 15. Board Dimensions

2.5 Electrical Considerations

2.5.1 Power Supply Considerations

⚠ CAUTION

The +5 V standby line from the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the indicated parameters of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails
- The current capability of the +5 VSB line
- All timing parameters
- All voltage tolerances

For example, for a system consisting of a supported 65 W processor (see Section 1.4 on page 14 for a list of supported processors), 1 GB DDR2 RAM, one mainstream video card, one hard disk drive, one optical drive, and all board peripherals enabled, the minimum recommended power supply is 300 W. Table 28 lists the recommended power supply current values.

Table 28. Recommended Power Supply Current Values

Output Voltage	3.3 V	5 V	12 V1	12 V2	-12 V	5 VSB
Current	15 A	15 A	10 A	10 A	0.3 A	3.0 A

2.5.2 Fan Header Current Capability

CAUTION

The processor fan must be connected to the processor fan header, not to a chassis fan header. Connecting the processor fan to a chassis fan header may result in onboard component damage that will halt fan operation.

Table 29 lists the current capability of the fan headers.

Table 29. Fan Header Current Capability

Fan Header	Maximum Available Current
Processor fan	2.0 A
Front chassis fan	1.5 A
Rear chassis fan	1.5 A
Auxiliary chassis fan	2.0 A

2.5.3 Add-in Board Considerations

The board is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards for a fully loaded board (all three expansion slots filled and the PCI Express x16 connector filled) must not exceed 8 A.

2.6 Thermal Considerations

CAUTION

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:

http://developer.intel.com/design/motherbd/cooling.htm

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

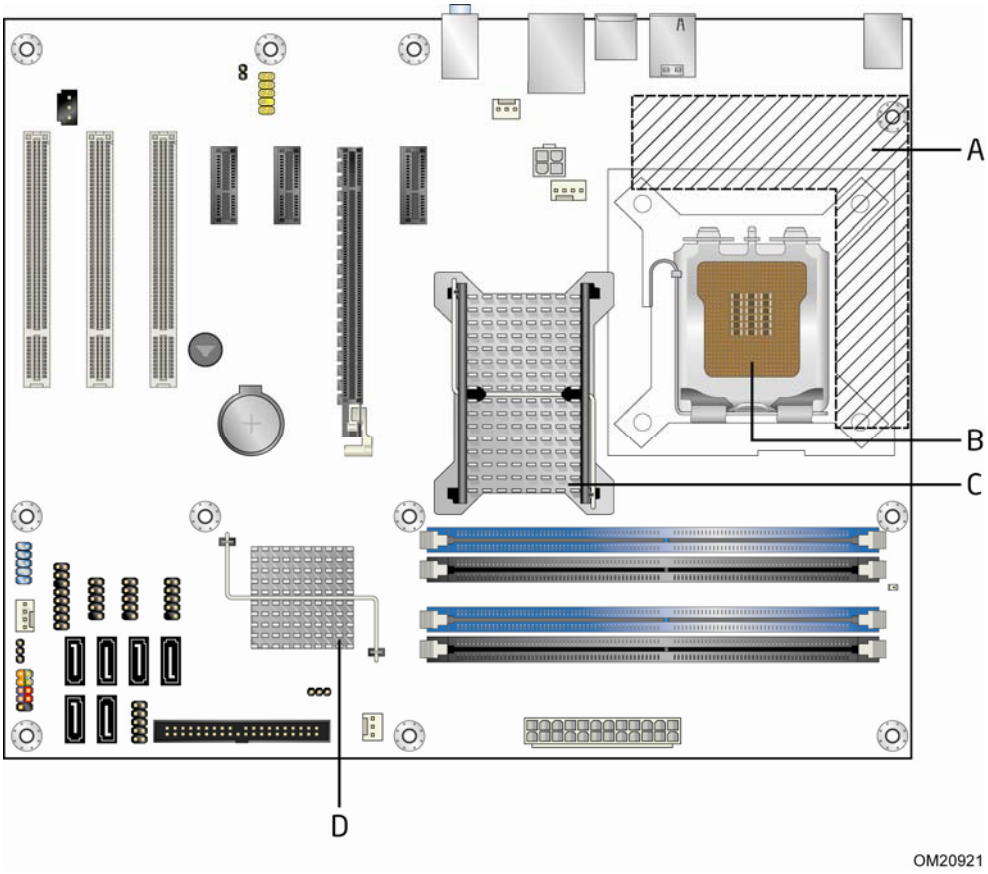
CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.8.

⚠ CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (shown in Figure 16) can reach a temperature of up to 95 °C in an open chassis.

Figure 16 shows the locations of the localized high temperature zones.



Item	Description
A	Processor voltage regulator area
B	Processor
C	Intel 82P43 MCH
D	Intel 82801JIB (ICH10)

Figure 16. Localized High Temperature Zones

Table 30 provides maximum case temperatures for the board components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 30. Thermal Considerations for Components

Component	Maximum Case Temperature
Processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82P43 MCH	97 °C (under bias)
Intel 82801JIB (ICH10)	92 °C (under bias)

For information about	Refer to
Processor datasheets and specification updates	Section 1.2, page 14

2.7 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC. The Intel Desktop Board DP43TF MTBF is 32067.84 hours.

2.8 Environmental

Table 31 lists the environmental specifications for the board.

Table 31. Intel® Desktop Board DP43TF Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-20 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second²		
Packaged	Half sine 2 millisecond		
	Product weight (pounds)	Free fall (inches)	Velocity change (inches/sec²)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz: 0.02 g² Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g² Hz (flat)		
	40 Hz to 500 Hz: 0.015 g² Hz sloping down to 0.00015 g² Hz		

3 Overview of BIOS Features

3.1 Introduction

The board uses an Intel BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated using a disk-based program. The SPI Flash contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as NBG4310A.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

NOTE

The maintenance menu is displayed only when the board is in configure mode. Section 2.3 on page 51 shows how to put the board in configure mode.

Table 32 lists the BIOS Setup program menu features.

Table 32. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features and power supply controls	Selects boot options	Saves or discards changes to Setup program options

Table 33 lists the function keys available for menu screens.

Table 33. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

3.2 BIOS Flash Memory Organization

The Serial Peripheral Interface Flash Memory (SPI Flash) includes an 32 Mbit (4096 KB) flash memory device.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the PCI IDE connector with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information. Additional board information can be found in the BIOS under the Additional Information header under the Main BIOS page.

3.5 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.
7. Additional USB legacy feature options can be access by using Intel Integrator Toolkit.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires booting from DOS. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or a CD-ROM.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
BIOS update utilities	http://support.intel.com/support/motherboards/desktop/sb/CS-022312.htm.

3.6.1 Language Support

The BIOS Setup program and help messages are supported in US English. Additional languages are available in the Intel® Integrator Toolkit utility. Check the Intel website for details.

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Intel® Integrator Toolkit or Intel® Integrator Assistant that are available from Intel can be used to create a custom splash screen.

NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
Intel Integrator Toolkit	http://developer.intel.com/design/motherbd/software/itk/
Additional Intel® software tools	http://developer.intel.com/products/motherboard/DP43TF/tools.htm and http://developer.intel.com/design/motherbd/software.htm

3.7 BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs, the BIOS could be damaged. Table 34 lists the drives and media types that can and cannot be used for BIOS recovery. The BIOS recovery media does not need to be made bootable.

Table 34. Acceptable Drives/Media Types for BIOS Recovery

Media Type	Can be used for BIOS recovery?
CD-ROM drive connected to the Parallel ATA interface	Yes
CD-ROM drive connected to the Serial ATA interface	Yes
USB removable drive (a USB flash drive, for example)	Yes
USB diskette drive (with a 1.44 MB diskette)	No
USB hard disk drive	No
Legacy diskette drive (with a 1.44 MB diskette) connected to the legacy diskette drive interface	No

For information about	Refer to
BIOS recovery	http://support.intel.com/support/motherboards/desktop/sb/CS-023360.htm

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drive, USB drive, USB flash drive, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.8.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

3.8.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

3.8.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.8.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 35 lists the boot device menu options.

Table 35. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.9 Adjusting Boot Speed

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Optimized BIOS boot parameters

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.9.2 BIOS Boot Optimizations

Use of the following BIOS Setup program settings reduces the POST execution time.

- In the Boot Menu, set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 36 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 36. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

4 Error Messages and Beep Codes

4.1 Speaker

The board-mounted speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, page 11

4.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's speaker to beep an error message describing the problem (see Table 37).

Table 37. Beep Codes

Type	Pattern	Frequency
Memory error	Three long beeps	1280 Hz
Thermal warning	Four alternating beeps: High tone, low tone, high tone, low tone	High tone: 2000 Hz Low tone: 1600 Hz

4.3 BIOS Error Messages

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem. Table 38 lists the error messages and provides a brief description of each.

Table 38. BIOS Error Messages

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
No Boot Device Available	System did not find a device to boot.

4.4 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in PCI bus connector 1.

The following tables provide information about the POST codes generated by the BIOS.

- Table 39 lists the Port 80h POST code ranges
- Table 40 lists the Port 80h POST codes themselves
- Table 41 lists the Port 80h POST sequence

NOTE

In the tables listed above, all POST codes and range values are listed in hexadecimal.

Table 39. Port 80h POST Code Ranges

Range	Category/Subsystem
00 – 0F	Debug codes: Can be used by any PEIM/driver for debug.
10 – 1F	Host Processors: 1F is an unrecoverable CPU error.
20 – 2F	Memory/Chipset: 2F is no memory detected or no useful memory detected.
30 – 3F	Recovery: 3F indicated recovery failure.
40 – 4F	Reserved for future use.
50 – 5F	I/O Buses: PCI, USB, ATA, etc. 5F is an unrecoverable error. Start with PCI.
60 – 6F	Reserved for future use (for new busses).
70 – 7F	Output Devices: All output consoles. 7F is an unrecoverable error.
80 – 8F	Reserved for future use (new output console codes).
90 – 9F	Input devices: Keyboard/Mouse. 9F is an unrecoverable error.
A0 – AF	Reserved for future use (new input console codes).
B0 – BF	Boot Devices: Includes fixed media and removable media. BF is an unrecoverable error.
C0 – CF	Reserved for future use.
D0 – DF	Boot device selection.
E0 – FF	E0 – EE: Miscellaneous codes. See Table 40. EF: boot/S3 resume failure. F0 – FF: FF processor exception.

Table 40. Port 80h POST Codes

POST Code	Description of POST Operation
	Host Processor
10	Power-on initialization of the host processor (Boot Strap Processor)
11	Host processor Cache initialization (including APs)
12	Starting Application processor initialization
13	SMM initialization
	Chipset
21	Initializing a chipset component
	Memory
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
24	Programming timing parameters in the memory controller and the DIMMs
25	Configuring memory
26	Optimizing memory settings
27	Initializing memory, such as ECC init
28	Testing memory
	PCI Bus
50	Enumerating PCI busses
51	Allocating resources to PCI bus
52	Hot Plug PCI controller initialization
53 – 57	Reserved for PCI Bus
	USB
58	Resetting USB bus
59	Reserved for USB
	ATA/ATAPI/SATA
5A	Resetting PATA/SATA bus and all devices
5B	Reserved for ATA
	SMBus
5C	Resetting SMBus
5D	Reserved for SMBus
	Local Console
70	Resetting the VGA controller
71	Disabling the VGA controller
72	Enabling the VGA controller
	Remote Console
78	Resetting the console controller
79	Disabling the console controller
7A	Enabling the console controller

continued

Table 40. Port 80h POST Codes (continued)

POST Code	Description of POST Operation
	Keyboard (PS/2 or USB)
90	Resetting keyboard
91	Disabling keyboard
92	Detecting presence of keyboard
93	Enabling the keyboard
94	Clearing keyboard input buffer
95	Instructing keyboard controller to run Self Test (PS/2 only)
	Mouse (PS/2 or USB)
98	Resetting mouse
99	Disabling mouse
9A	Detecting presence of mouse
9B	Enabling mouse
	Fixed Media
B0	Resetting fixed media
B1	Disabling fixed media
B2	Detecting presence of a fixed media (IDE hard drive detection etc.)
B3	Enabling/configuring a fixed media
	Removable Media
B8	Resetting removable media
B9	Disabling removable media
BA	Detecting presence of a removable media (IDE, CD-ROM detection, etc.)
BC	Enabling/configuring a removable media
	BDS
D*y*	Trying boot selection y (y=0 to 15)
	PEI Core
E0	Started dispatching PEIMs (emitted on first report of EFI_SW_PC_INIT_BEGIN EFI_SW_PEI_PC_HANDOFF_TO_NEXT)
E2	Permanent memory found
E1, E3	Reserved for PEI/PEIMs
	DXE Core
E4	Entered DXE phase
E5	Started dispatching drivers
E6	Started connecting drivers

continued

Table 40. Port 80h POST Codes (continued)

POST Code	Description of POST Operation
	DXE Drivers
E7	Waiting for user input
E8	Checking password
E9	Entering BIOS setup
EB	Calling Legacy Option ROMs
	Runtime Phase/EFI OS Boot
F4	Entering Sleep state
F5	Exiting Sleep state
F8	EFI boot service ExitBootServices ( ) has been called
F9	EFI runtime service SetVirtualAddressMap ( ) has been called
FA	EFI runtime service ResetSystem ( ) has been called
	PEIMs/Recovery
30	Crisis Recovery has initiated per User request
31	Crisis Recovery has initiated by software (corrupt flash)
34	Loading recovery capsule
35	Handing off control to the recovery capsule
3F	Unable to recover

Table 41. Typical Port 80h POST Sequence

POST Code	Description
21	Initializing a chipset component
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
25	Configuring memory
28	Testing memory
34	Loading recovery capsule
E4	Entered DXE phase
12	Starting application processor initialization
13	SMM initialization
50	Enumerating PCI busses
51	Allocating resourced to PCI bus
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test
EB	Calling Video BIOS
58	Resetting USB bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
01	INT 19
00	Ready to boot

5 Regulatory Compliance and Battery Disposal Information

5.1 Regulatory Compliance

This section contains the following regulatory compliance information for Intel Desktop Board DP43TF:

- Safety standards
- European Union Declaration of Conformity statement
- Product Ecology statements
- Electromagnetic Compatibility (EMC) standards
- Product certification markings

5.1.1 Safety Standards

The Intel Desktop Board DP43TF complies with the safety standards stated in Table 42 when correctly installed in a compatible host system.

Table 42. Safety Standards

Standard	Title
CSA/UL 60950-1, First Edition	Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada)
EN 60950-1:2006, Second Edition	Information Technology Equipment – Safety - Part 1: General Requirements (European Union)
IEC 60950-1:2005, Second Edition	Information Technology Equipment – Safety - Part 1: General Requirements (International)

5.1.2 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product Intel® Desktop Board DP43TF is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 2004/108/EC (EMC Directive) and 2006/95/EC (Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

This product follows the provisions of the European Directives 2004/108/EC and 2006/95/EC.

Čeština Tento výrobek odpovídá požadavkům evropských směrnic 2004/108/EC a 2006/95/EC.

Dansk Dette produkt er i overensstemmelse med det europæiske direktiv 2004/108/EC & 2006/95/EC.

Dutch Dit product is in navolging van de bepalingen van Europees Directief 2004/108/EC & 2006/95/EC.

Eesti Antud toode vastab Euroopa direktiivides 2004/108/EC ja 2006/95/EC kehtestatud nõuetele.

Suomi Tämä tuote noudattaa EU-direktiivin 2004/108/EC & 2006/95/EC määräyksiä.

Français Ce produit est conforme aux exigences de la Directive Européenne 2004/108/EC & 2006/95/EC.

Deutsch Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2004/108/EC & 2006/95/EC.

Ελληνικά Το παρόν προϊόν ακολουθεί τις διατάξεις των Ευρωπαϊκών Οδηγιών 2004/108/EC και 2006/95/EC.

Magyar E termék megfelel a 2004/108/EC és 2006/95/EC Európai Irányelv előírásainak.

Icelandic Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2004/108/EC & 2006/95/EC.

Italiano Questo prodotto è conforme alla Direttiva Europea 2004/108/EC & 2006/95/EC.

Latviešu Šis produkts atbilst Eiropas Direktīvu 2004/108/EC un 2006/95/EC noteikumiem.

Lietuvių Šis produktas atitinka Europos direktyvų 2004/108/EC ir 2006/95/EC nuostatas.

Malti Dan il-prodott hu konformi mal-provvedimenti tad-Direttivi Ewropej 2004/108/EC u 2006/95/EC.

Norsk Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2004/108/EC & 2006/95/EC.

Polski Niniejszy produkt jest zgodny z postanowieniami Dyrektyw Unii Europejskiej 2004/108/EC i 73/23/EWG.

Portuguese Este produto cumpre com as normas da Diretiva Européia 2004/108/EC & 2006/95/EC.

Español Este producto cumple con las normas del Directivo Europeo 2004/108/EC & 2006/95/EC.

Slovensky Tento produkt je v súlade s ustanoveniami európskych direktív 2004/108/EC a 2006/95/EC.

Slovenščina Izdelek je skladen z določbami evropskih direktiv 2004/108/EC in 2006/95/EC.

Svenska Denna produkt har tillverkats i enlighet med EG-direktiv 2004/108/EC & 2006/95/EC.

Türkçe Bu ürün, Avrupa Birliği'nin 2004/108/EC ve 2006/95/EC yönergelerine uyar.

5.1.3 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

5.1.3.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

5.1.3.2 Recycling Considerations

As part of its commitment to environmental responsibility, Intel has implemented the Intel Product Recycling Program to allow retail consumers of Intel's branded products to return used products to selected locations for proper recycling.

Please consult the http://www.intel.com/intel/other/ehs/product_ecology for the details of this program, including the scope of covered products, available locations, shipping instructions, terms and conditions, etc.

中文

作为其对环境责任之承诺的部分，英特尔已实施 Intel Product Recycling Program（英特尔产品回收计划），以允许英特尔品牌产品的零售消费者将使用过的产品退还至指定地点作恰当的重复使用处理。

请参考http://www.intel.com/intel/other/ehs/product_ecology 了解此计划的详情，包括涉及产品之范围、回收地点、运送指导、条款和条件等。

Deutsch

Als Teil von Intels Engagement für den Umweltschutz hat das Unternehmen das Intel Produkt-Recyclingprogramm implementiert, das Einzelhandelskunden von Intel Markenprodukten ermöglicht, gebrauchte Produkte an ausgewählte Standorte für ordnungsgemäßes Recycling zurückzugeben.

Details zu diesem Programm, einschließlich der darin eingeschlossenen Produkte, verfügbaren Standorte, Versandanweisungen, Bedingungen usw., finden Sie auf der http://www.intel.com/intel/other/ehs/product_ecology

Español

Como parte de su compromiso de responsabilidad medioambiental, Intel ha implantado el programa de reciclaje de productos Intel, que permite que los consumidores al detalle de los productos Intel devuelvan los productos usados en los lugares seleccionados para su correspondiente reciclado.

Consulte la http://www.intel.com/intel/other/ehs/product_ecology para ver los detalles del programa, que incluye los productos que abarca, los lugares disponibles, instrucciones de envío, términos y condiciones, etc.

Français

Dans le cadre de son engagement pour la protection de l'environnement, Intel a mis en œuvre le programme Intel Product Recycling Program (Programme de recyclage des produits Intel) pour permettre aux consommateurs de produits Intel de recycler les produits usés en les retournant à des adresses spécifiées.

Visitez la page Web http://www.intel.com/intel/other/ehs/product_ecology pour en savoir plus sur ce programme, à savoir les produits concernés, les adresses disponibles, les instructions d'expédition, les conditions générales, etc.

日本語

インテルでは、環境保護活動の一環として、使い終えたインテル
ブランド製品を指定の場所へ返送していただき、リサイクルを適切に行えるよう、インテル製品リサイクル
プログラムを発足させました。

対象製品、返送先、返送方法、ご利用規約など、このプログラムの詳細情報は、http://www.intel.com/intel/other/ehs/product_ecology（英語）をご覧ください。

Malay

Sebagai sebahagian daripada komitmennya terhadap tanggungjawab persekitaran, Intel telah melaksanakan Program Kitar Semula Produk untuk membenarkan pengguna-pengguna runcit produk jenama Intel memulangkan produk terguna ke lokasi-lokasi terpilih untuk dikitarkan semula dengan betul.

Sila rujuk http://www.intel.com/intel/other/ehs/product_ecology untuk mendapatkan butir-butir program ini, termasuklah skop produk yang dirangkumi, lokasi-lokasi tersedia, arahan penghantaran, terma & syarat, dsb.

Portuguese

Como parte deste compromisso com o respeito ao ambiente, a Intel implementou o Programa de Reciclagem de Produtos para que os consumidores finais possam enviar produtos Intel usados para locais selecionados, onde esses produtos são reciclados de maneira adequada.

Consulte o site http://www.intel.com/intel/other/ehs/product_ecology (em Inglês) para obter os detalhes sobre este programa, inclusive o escopo dos produtos cobertos, os locais disponíveis, as instruções de envio, os termos e condições, etc.

Russian

В качестве части своих обязательств к окружающей среде, в Intel создана программа утилизации продукции Intel (Product Recycling Program) для предоставления конечным пользователям марок продукции Intel возможности возврата используемой продукции в специализированные пункты для должной утилизации.

Пожалуйста, обратитесь на веб-сайт http://www.intel.com/intel/other/ehs/product_ecology за информацией об этой программе, принимаемых продуктах, местах приема, инструкциях об отправке, положениях и условиях и т.д.

Türkçe

Intel, çevre sorumluluğuna bağımlılığının bir parçası olarak, perakende tüketicilerin Intel markalı kullanılmış ürünlerini belirlenmiş merkezlere iade edip uygun şekilde geri dönüştürmesini amaçlayan Intel Ürünleri Geri Dönüşüm Programı'nı uygulamaya koymuştur.

Bu programın ürün kapsamı, ürün iade merkezleri, nakliye talimatları, kayıtlar ve şartlar v.s dahil bütün ayrıntılarını ögrenmek için lütfen http://www.intel.com/intel/other/ehs/product_ecology

Web sayfasına gidin.

5.1.3.3 Lead Free Intel Desktop Board

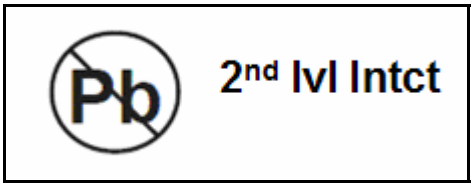
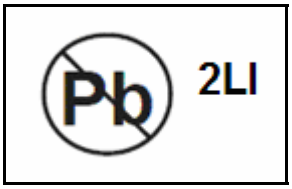
This Intel Desktop Board is a European Union Restriction of Hazardous Substances (EU RoHS Directive 2002/95/EC) compliant product. EU RoHS restricts the use of six materials. One of the six restricted materials is lead.

This board is lead free although certain discrete components used on the board contain a small amount of lead which is necessary for component performance and/or reliability. This Intel Desktop Board is referred to as "Lead-free second level interconnect." The board substrate and the solder connections from the board to the components (second-level connections) are all lead free.

China bans the same substances and has the same limits as EU RoHS; however it requires different product marking and controlled substance information. The required mark shows the Environmental Friendly Usage Period (EFUP). The EFUP is defined as the number of years for which controlled listed substances will not leak or chemically deteriorate while in the product.

Table 43 shows the various forms of the "Lead-Free 2nd Level Interconnect" mark as it appears on the board and accompanying collateral.

Table 43. Lead-Free Board Markings

Description	Mark
Lead-Free 2nd Level Interconnect: This symbol is used to identify electrical and electronic assemblies and components in which the lead (Pb) concentration level in the desktop board substrate and the solder connections from the board to the components (second-level interconnect) is not greater than 0.1% by weight (1000 ppm).	 or  or 

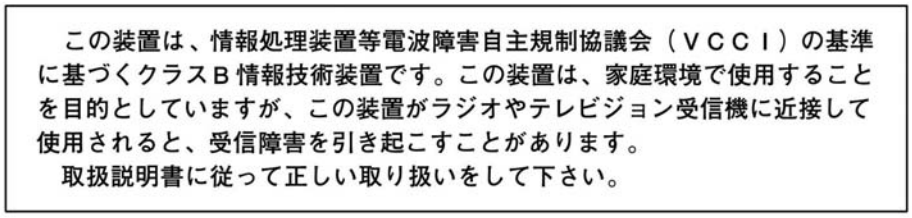
5.1.4 EMC Regulations

The Intel Desktop Board DP43TF complies with the EMC regulations stated in Table 44 when correctly installed in a compatible host system.

Table 44. EMC Regulations

Regulation	Title
FCC 47 CFR Part 15, Subpart B	Title 47 of the Code of Federal Regulations, Part15, Subpart B, Radio Frequency Devices. (USA)
ICES-003 Issue 4 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022:2006 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024:1998 (Class B)	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
EN55022:2006 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22:2005 +A1:2005 +A2:2006 (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24:1997 +A1:2001 +A2:2002 (Class B)	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurement. (International)
VCCI V-3/2007.04, V-4/2007.04, Class B	Voluntary Control for Interference by Information Technology Equipment. (Japan)

Japanese Kanji statement translation: this is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI). If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.



Korean Class B statement translation: this is household equipment that is certified to comply with EMC requirements. You may use this equipment in residential environments and other non-residential environments.

이 기기는 가정용으로 전자파적합등록을 한 기기로서
주거지역에서는 물론 모든 지역에서 사용할 수 있습니다.

5.1.5 Product Certification Markings (Board Level)

Intel Desktop Board DP43TF has the product certification markings shown in Table 45:

Table 45. Product Certification Markings

Description	Mark
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Desktop Boards: E210882.	
FCC Declaration of Conformity logo mark for Class B equipment. Includes Intel name and DP43TF model designation.	
CE mark. Declaring compliance to European Union (EU) EMC directive and Low Voltage directive.	
Australian Communications Authority (ACA) and New Zealand Radio Spectrum Management (NZ RSM) C-tick mark. Includes adjacent Intel supplier code number, N-232.	
Japan VCCI (Voluntary Control Council for Interference) mark.	
S. Korea MIC (Ministry of Information and Communication) mark. Includes adjacent MIC certification number: CPU-DP43TF (B)	
Taiwan BSMI (Bureau of Standards, Metrology and Inspections) mark. Includes adjacent Intel company number, D33025.	
Printed wiring board manufacturer's recognition mark. Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	V-0
China RoHS/Environmentally Friendly Use Period Logo: This is an example of the symbol used on Intel Desktop Boards and associated collateral. The color of the mark may vary depending upon the application. The Environmental Friendly Usage Period (EFUP) for Intel Desktop Boards has been determined to be 10 years.	

5.2 Battery Disposal Information

CAUTION

Risk of explosion if the battery is replaced with an incorrect type. Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.

PRECAUTION

Risque d'explosion si la pile usagée est remplacée par une pile de type incorrect. Les piles usagées doivent être recyclées dans la mesure du possible. La mise au rebut des piles usagées doit respecter les réglementations locales en vigueur en matière de protection de l'environnement.

FORHOLDSREGEL

Eksplosionsfare, hvis batteriet erstattes med et batteri af en forkert type. Batterier bør om muligt genbruges. Bortskaffelse af brugte batterier bør foregå i overensstemmelse med gældende miljølovgivning.

OBS!

Det kan oppstå eksplosjonsfare hvis batteriet skiftes ut med feil type. Brukte batterier bør kastes i henhold til gjeldende miljølovgivning.

VIKTIGT!

Risk för explosion om batteriet ersätts med felaktig batterityp. Batterier ska kasseras enligt de lokala miljövårdsbestämmelserna.

VARO

Räjähdysvaara, jos pariston tyyppi on väärä. Paristot on kierrätettävä, jos se on mahdollista. Käytetyt paristot on hävitettävä paikallisten ympäristömääräysten mukaisesti.

VORSICHT

Bei falschem Einsetzen einer neuen Batterie besteht Explosionsgefahr. Die Batterie darf nur durch denselben oder einen entsprechenden, vom Hersteller empfohlenen Batterietyp ersetzt werden. Entsorgen Sie verbrauchte Batterien den Anweisungen des Herstellers entsprechend.

AVVERTIMENTO

Esiste il pericolo di un esplosione se la pila non viene sostituita in modo corretto. Utilizzare solo pile uguali o di tipo equivalente a quelle consigliate dal produttore. Per disfarsi delle pile usate, seguire le istruzioni del produttore.

PRECAUCIÓN

Existe peligro de explosión si la pila no se cambia de forma adecuada. Utilice solamente pilas iguales o del mismo tipo que las recomendadas por el fabricante del equipo. Para deshacerse de las pilas usadas, siga igualmente las instrucciones del fabricante.

WAARSCHUWING

Er bestaat ontploffingsgevaar als de batterij wordt vervangen door een onjuist type batterij. Batterijen moeten zoveel mogelijk worden gerecycled. Houd u bij het weggooien van gebruikte batterijen aan de plaatselijke milieuwetgeving.

ATENÇÃO

Haverá risco de explosão se a bateria for substituída por um tipo de bateria incorreto. As baterias devem ser recicladas nos locais apropriados. A eliminação de baterias usadas deve ser feita de acordo com as regulamentações ambientais da região.

AŚCIAROŽZNAŚĆ

Існуе рызыка выбуху, калі заменены акумулятар неправільнага тыпу. Акумулятары павінны, па магчымасці, перепрацоўвацца. Пазбаўляцца ад старых акумулятараў патрэбна згодна з мясцовым заканадаўствам па экалогіі.

UPOZORNÌNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

Προσοχή

Υπάρχει κίνδυνος για έκρηξη σε περίπτωση που η μπαταρία αντικατασταθεί από μία λανθασμένου τύπου. Οι μπαταρίες θα πρέπει να ανακυκλώνονται όταν κάτι τέτοιο είναι δυνατό. Η απόρριψη των χρησιμοποιημένων μπαταριών πρέπει να γίνεται σύμφωνα με τους κατά τόπο περιβαλλοντικούς κανονισμούς.

VIGYAZAT

Ha a telepet nem a megfelelő típusú telepre cseréli, az felrobbanhat. A telepeket lehetőség szerint újra kell hasznosítani. A használt telepeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

注意

異なる種類の電池を使用すると、爆発の危険があります。リサイクル
が可能な地域であれば、電池をリサイクルしてください。使用後の電
池を破棄する際には、地域の環境規制に従ってください。

AWAS

Risiko letupan wujud jika bateri digantikan dengan jenis yang tidak betul. Bateri sepatutnya dikitar semula jika boleh. Pelupusan bateri terpakai mestilah mematuhi peraturan alam sekitar tempatan.

OSTRZEŻENIE

Istnieje niebezpieczeństwo wybuchu w przypadku zastosowania niewłaściwego typu baterii. Zużyte baterie należy w miarę możliwości utylizować zgodnie z odpowiednimi przepisami ochrony środowiska.

PRECAUȚIE

Risc de explozie, dacă bateria este înlocuită cu un tip de baterie necorespunzător. Bateriile trebuie reciclate, dacă este posibil. Depozitarea bateriilor uzate trebuie să respecte reglementările locale privind protecţia mediului.

ВНИМАНИЕ

При использовании батареи несоответствующего типа существует риск ее взрыва. Батареи должны быть утилизированы по возможности. Утилизация батарей должна проводится по правилам, соответствующим местным требованиям.

UPOZORNENIE

Ak batériu vymeníte za nesprávny typ, hrozí nebezpečenstvo jej výbuchu.
Batérie by sa mali podľa možnosti vždy recyklovať. Likvidácia použitých batérií sa musí vykonávať v súlade s miestnymi predpismi na ochranu životného prostredia.

POZOR

Zamenjava baterije z baterijo drugačnega tipa lahko povzroči eksplozijo.
Če je mogoče, baterije reciklirajte. Rabljene baterije zavrzite v skladu z lokalnimi okoljevarstvenimi predpisi.

คำเตือน

ระวังการระเบิดที่เกิดจากเปลี่ยนแบตเตอรี่ผิดประเภท หากเป็นไปได้ ควรนำแบตเตอรี่ไปรีไซเคิล การทิ้งแบตเตอรี่ใช้แล้วต้องเป็นไปตามกฎข้อบังคับด้านสิ่งแวดล้อมของท้องถิ่น.

UYARI

Yanlış türde pil takıldığında patlama riski vardır. Piller mümkün olduğunda geri dönüştürülmelidir. Kullanılmış piller, yerel çevre yasalarına uygun olarak atılmalıdır.

ОСТОРОГА

Використовуйте батареї правильного типу, інакше існуватиме ризик вибуху. Якщо можливо, використані батареї слід утилізувати. Утилізація використаних батарей має бути виконана згідно місцевих норм, що регулюють охорону довкілля.

UPOZORNĚNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

ETTEVAATUST

Kui patarei asendatakse uue ebasobivat tüüpi patareiga, võib tekkida plahvatusoht. Tühjad patareid tuleb võimaluse korral viia vastavasse kogumispunkti. Tühjade patareide äraviskamisel tuleb järgida kohalikke keskkonnakaitse alaseid reegleid.

FIGYELMEZTETÉS

Ha az elemet nem a megfelelő típusúra cseréli, felrobbanhat. Az elemeket lehetőség szerint újra kell hasznosítani. A használt elemeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

UZMANĪBU

Pastāv eksplozijas risks, ja baterijas tiek nomainītas ar nepareiza veida baterijām. Ja iespējams, baterijas vajadzētu nodot attiecīgos pieņemšanas punktos. Bateriju izmešanai atkritumos jānotiek saskaņā ar vietējiem vides aizsardzības noteikumiem.

DĖMESIO

Naudojant netinkamo tipo baterijas įrenginys gali sprogti. Kai tik įmanoma, baterijas reikia naudoti pakartotinai. Panaudotas baterijas išmesti būtina pagal vietinius aplinkos apsaugos nuostatus.

ATTENZJONI

Riskju ta' splużjoni jekk il-batterija tinbidel b'tip ta' batterija mhux korrett. Il-batteriji għandhom jiġu riċiklati fejn hu possibbli. Ir-rimi ta' batteriji użati għandu jsir skond ir-regolamenti ambjentali lokali.

OSTRZEŻENIE

Ryzyko wybuchu w przypadku wymiany na baterie niewłaściwego typu. W miarę możliwości baterie należy poddać recyklingowi. Zużytych baterii należy pozbywać się zgodnie z lokalnie obowiązującymi przepisami w zakresie ochrony środowiska.