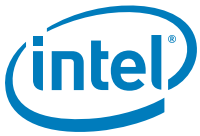


Intel® Server System SR1695GPRX

Technical Product Specification

Intel order number: G11332-002

Revision 1.1

July, 2010

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
June 30, 2010	1.0	Initial release.
July 5, 2010	1.1	Updated front panel connector pin definition.

Disclaimers

Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications. Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® Server System SR1695GPRX may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

This document and the software described in it is furnished under license and may only be used or copied in accordance with the terms of the license. The information in this manual is furnished for informational use only, is subject to change without notice, and should not be construed as a commitment by Intel Corporation. Intel Corporation assumes no responsibility or liability for any errors or inaccuracies that may appear in this document or any software that may be provided in association with this document.

Except as permitted by such license, no part of this document may be reproduced, stored in a retrieval system, or transmitted in any form or by any means without the express written consent of Intel Corporation.

Intel, Pentium and Xeon are trademarks or registered trademarks of Intel Corporation.

*Other brands and names may be claimed as the property of others.

Copyright © Intel Corporation 2010. Portions Copyright ® 2010 by LSI Corporation*.

Table of Contents

List of Figures

List of Tables

< This page intentionally left blank >

1. Introduction

This Technical Product Specification (TPS) provides system specific information detailing the features, functionality, and high-level architecture of the Intel® Server System SR1695GPRX. You should also reference the *Intel® Server Board S3420GPRX Technical Product Specification* to obtain greater detail of functionality and architecture of the server board integrated in this server system.

In addition, you can obtain design-level information for specific sub-systems by ordering the External Product Specifications (EPS) or External Design Specifications (EDS) for a given sub-system. EPS and EDS documents are not publicly available. They are only made available under NDA with Intel and must be ordered through your local Intel representative. For a complete list of available documents, refer to the *Reference Documents* section at the end of this document.

The Intel® Server System SR1695GPRX may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Refer to the *Intel® Server Board S3420GPRX/Intel® Server System SR1695GPRX Specification Update* for published errata.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Product Overview
- Chapter 3 – Power Sub-System
- Chapter 4 – Cooling Sub-System
- Chapter 5 – Peripheral Drive Support
- Chapter 6 – Hard Disk Drive Support
- Chapter 7 – Front Panel Control and Indicators
- Chapter 8 – Configuration Jumpers
- Chapter 9 – PCI Riser Card and Assembly
- Chapter 10 – Environmental and Regulatory Specifications
- Appendix A – Integration and Usage Tips
- Appendix B – POST code LED Decoder
- Appendix C – Video POST Code Errors
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental

conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The Intel® Server System SR1695GPRX is a rack mount 1U server system, purpose-built for high-energy efficiency and lowest total cost of ownership in dense computing applications. The system is integrated with an Intel® Server Board S3420GPRX and supports up to four hot-swap SAS or SATA hard drives.

This chapter provides a high-level overview of the system features. The following chapters provide greater detail for each major system component or feature.

Table 1. System Feature Set

Feature	Description
Processor	Support for one Intel® Xeon® 3400 Series Processor in FC-LGA 1156 socket package. 2.5 GT/s point-to-point DMI interface to PCH LGA 1156 pin socket Support for one Intel® Core™ i3® Processor 2.0 GT/s point-to-point DMI interface to PCH LGA 1156 pin socket
Memory	Two memory channels with support for 1066/1333 MHz ECC unbuffered (UDIMM) or ECC Registered (RDIMM) DDR3. Up to two UDIMMs or three RDIMM per channel 32 GB max with x8 ECC RDIMM (2 Gb DRAM) and 16 GB max with x8 ECC UDIMM (2 Gb DRAM) **Note**: Intel® i3® Processor support only UDIMMs
DIMM Slots	Six
Chipset	Intel® Chipset which includes the following components: Support for Intel® 3420 Chipset Platform Controller Hub (PCH) PCI Express* switch – 89HI0524G2PS
System Connectors / Headers	External I/O connectors: DB-15 video connectors RJ45 type serial Port A connector 2 USB 2.0 Ports Five 10/100/1000 Base-TX RJ45 LAN connector. Internal connectors/headers: Two USB 2x5 pin headers, each supporting two USB 2.0 ports One USB 2x5 pin header for Intel® USB SSD One USB 2.0 internal vertical connector One 2x5 Serial Port B header Six SATA II connectors One Intel® SAS Entry RAID Module connector Two Intel® I/O Expansion Module Slots One slot for optional Intel® Remote Management Module 3 Lite
System Fan Support	Two sets blowers for processor and memory One set rotor fan for PCI Express* add-in Card
Add-in Adapter Support	One PCI Express* Gen2 x16 (x8 throughput) connector.

Feature	Description
On-board Video	**On-board Server Engines* LLC Pilot II Controller** Integrated 2D Video Controller 64-MB DDR2 667 MHz Memory Uses 8 MB of the BMC 32 MB DDR2 Memory
External Drive Bays	Four hot-pluggable external drive bays
Hard Disk Drive Supported	3.5-inch SATA, SAS HDD. 2.5-inch SATA, SAS HDD.
RAID Support	Intel® Embedded Server RAID Technology II through onboard SATA connectors provides SATA RAID 0, 1, and 10. Intel® Embedded Server RAID Technology II through optional Intel® SAS Entry RAID Module AXX4SASMOD provides SAS RAID 0, 1, and 10 with optional RAID 5 support provided by the Intel® RAID Activation Key AXXRAKSW5 IT/IR RAID through optional Intel® SAS Entry RAID Module AXX4SASMOD provides entry level hardware RAID 0, 1, 10, and native SAS pass through mode 4 ports full featured SAS/SATA hardware RAID through optional Intel® Integrated RAID Module SROMBSASMR (AXXROMBSASMR), provides RAID 0, 1, 5, 6 and striping capability for spans 10, 50, 60.
LAN	One Gigabit Ethernet device 82574L connect to PCI-E x1interfaces on the PCH. Two Gigabit Ethernet devices 82576 connected to PCI-E switch through PCI-E x4 interface, each 82576 providing two Gigabit Ethernet ports.
System Power	400w AC power supply, 80 plus silver with PFC, supporting 1+1 redundant configuration(optional).
Server Management	Onboard LLC Pilot II Controller (iBMC) Integrated Baseboard Management Controller (Integrated BMC), IPMI 2.0 compliant Intel® Remote Management Module III (RMM3) Lite Intel® Light-Guided Diagnostics on field replaceable units Support for Intel® System Management Software 3.5.1 and beyond Support for Intel® Deployment Assistant 3.5.2 and beyond

The Intel® Server System SR1695GPRX system is supporting all Intel® Xeon® processor 3400 series and Intel® Core™ processor i3® series with TDP 95 W and below. You can find a full list of supported processors at the Intel Support Website:

http://www.intel.com/support/motherboards/server/s3420gp/sb/CS-030740.htm

2.1 System Views

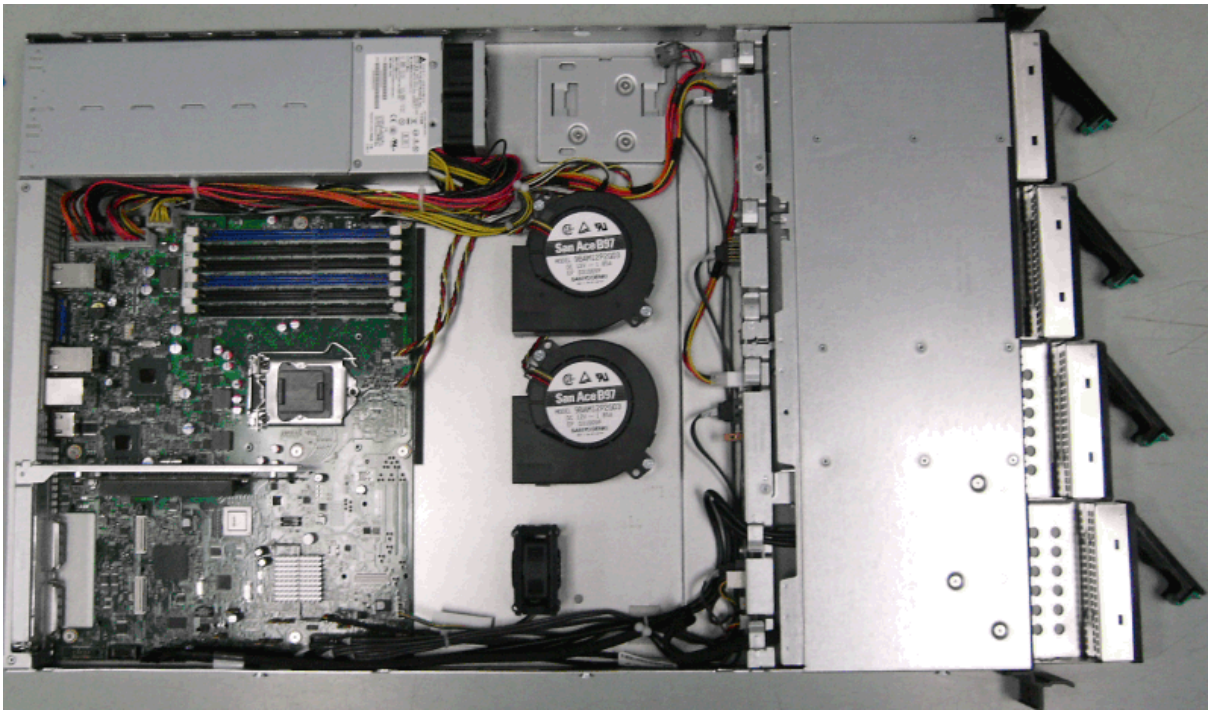


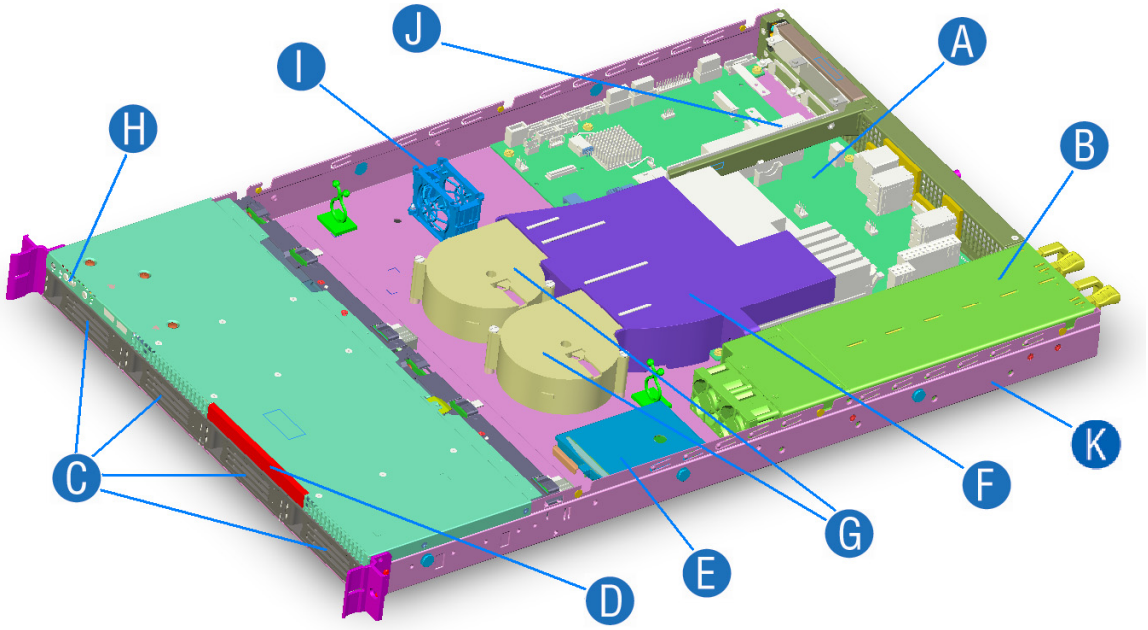
Figure 1. System Overview (Air Duct is removed)

2.2 System Dimensions

Table 2. Chassis Dimensions

Height	43 mm	1.69 inches
Width without rails	451.17 mm	17.76 inches
Width with rails	482 mm	18.97 inches
Depth without CMA	671.08 mm	26.42 inches
Weight Chassis – basic configured (1 PSU, 0 drives) Chassis – basic configured (2 PSU, 0 drives) Chassis – fully configured (2 PSU, 4 drives)	 9.36 kg 9.90 kg 12.20kg	 20.63 lbs 21.83 lbs 26.89 lbs

2.3 System Components



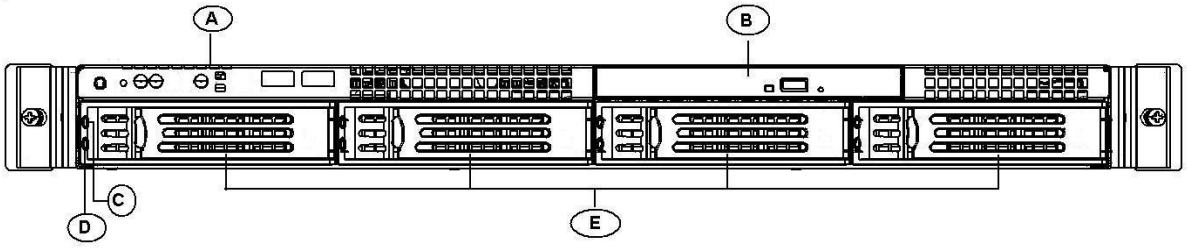
A	Mother Board	**F**	Air duct for processor and memory
B	Redundant Power Supply Cage	**G**	Blowers for processor and memory
C	External hot-swap HDD Carriers	**H**	Front Panel and Front USB module
D	Optional Slim-line Optical Drive Assembly	**I**	System Fan for PCIe add-in card
E	Optional BBU Assembly position	**J**	Optional PCI Express* Add-in Card
K	1U chassis		

Note: Not shown - Rack slide rail, and top cover.

Figure 2. Major Chassis Components

2.4 Hard Drive and Peripheral Bays

	Intel® Server System SR1695GPRX
Slim-line SATA Optical Drive	Supported
Slim-line USB Floppy Drive	No Support
SATA Drives (3.5-inch or 2.5-inch)	Up to four
SAS Drives (3.5-inch or 2.5-inch)	Up to four



A	System Control Panel
B	Slim-line optical drive bay
C	HDD Power LED
D	HDD Activity/Fault LED
E	Hard drive bays 0~3

Figure 3. Drive Bay Overview

2.5 Server Board Overview

The chassis is mechanically and functionally designed to support the Intel® Server Board S3420GPRX. The following sections provide an overview of the server board feature sets.

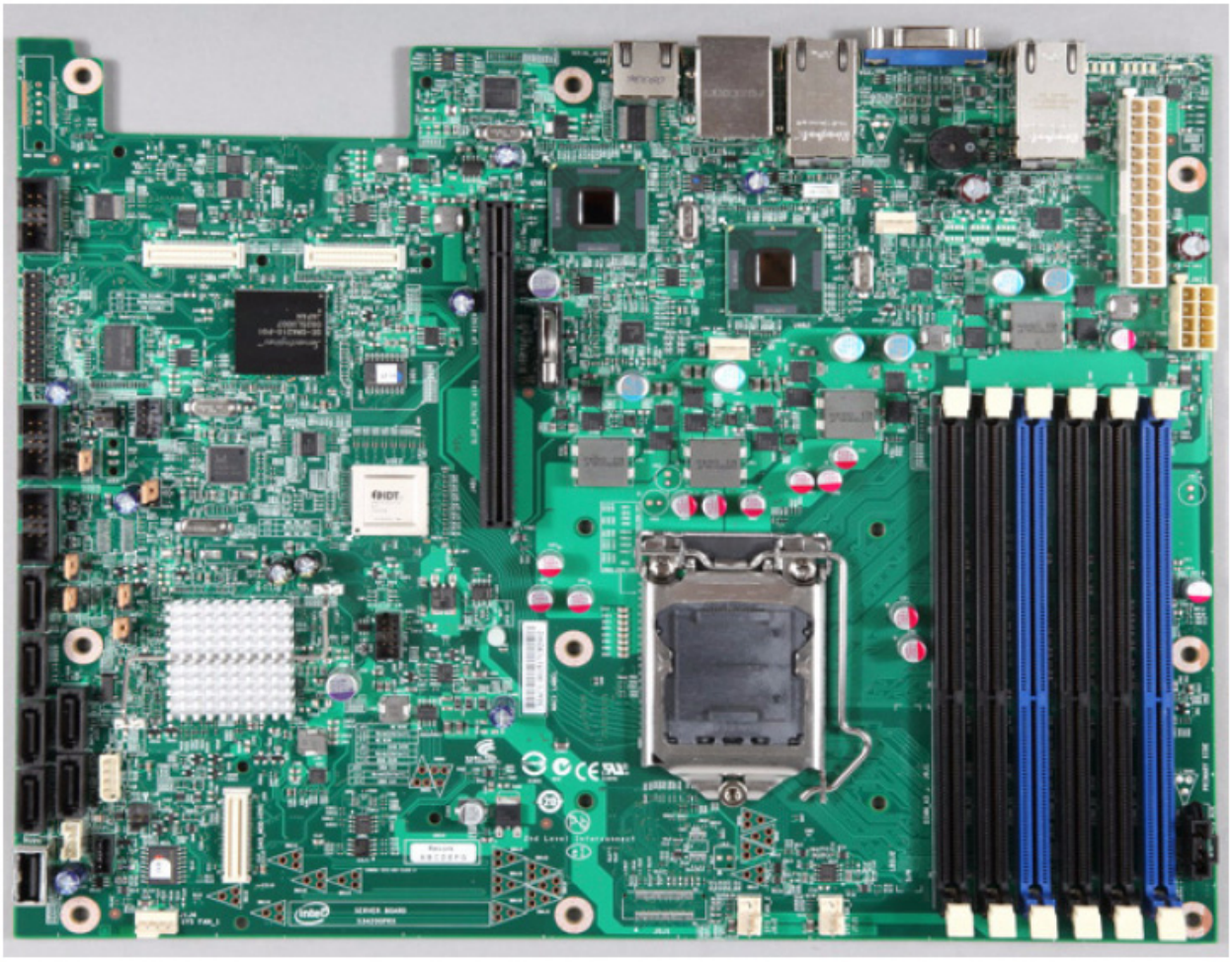


Figure 4. Intel® Server Board S3420GPRX

The following figure shows the layout of the server board. Each connector and major component is identified by a number or letter, and a description is given below the figure.

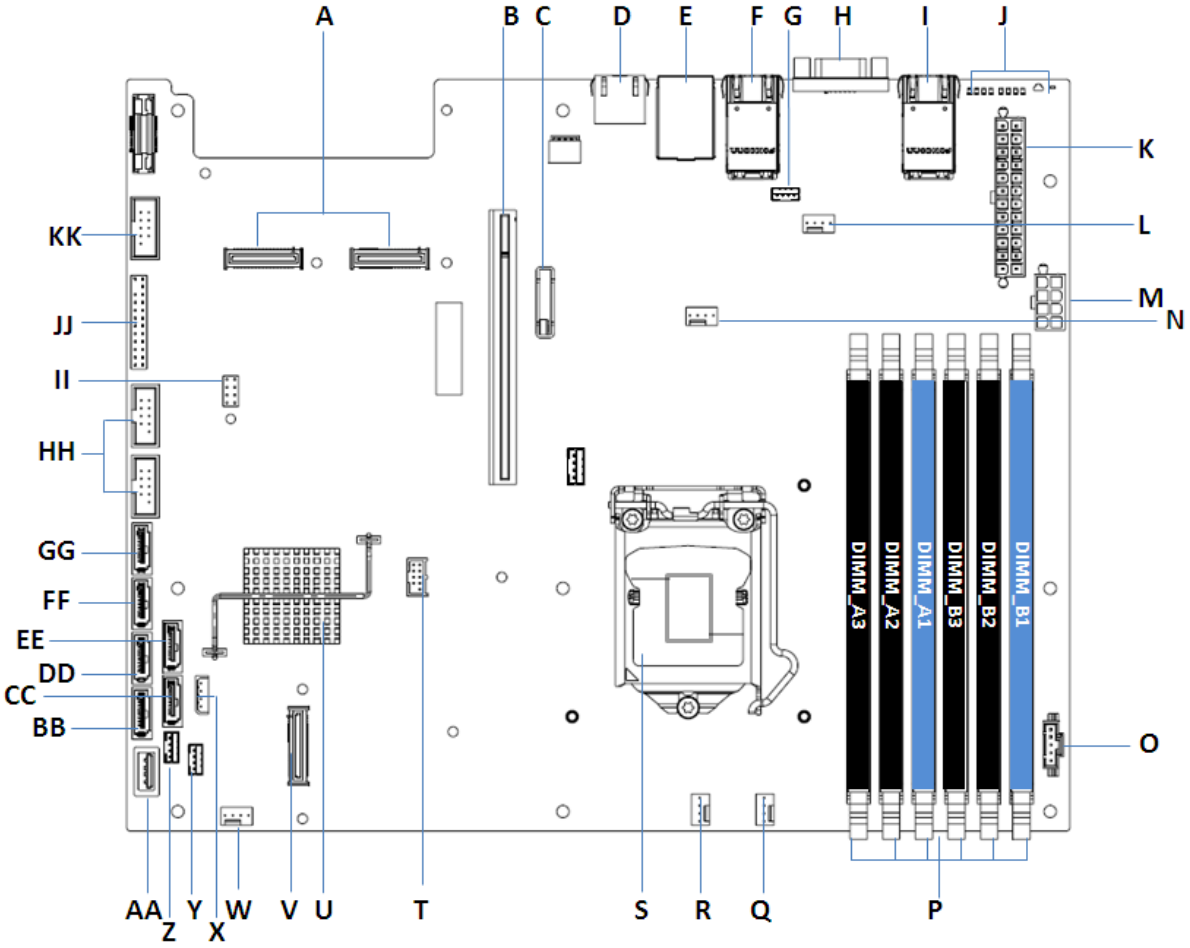
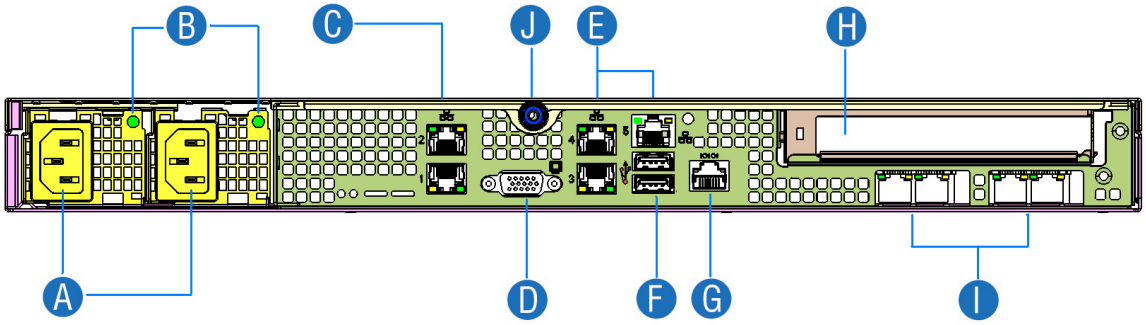


Figure 5. Intel® Server Board S3420GPRX Components

	Description		Description
A	Dual Intel® I/O Expansion Module Connectors	S	CPU Socket
B	PCI Express x16 Gen2	T	USB SSD Connector
C	CMOS Battery	U	PCH Chipset
D	RJ-45 Serial port Connector	V	SAS Module Connector
E	RJ-45 GbE(NIC5) and Dual USB combo connector	W	System FAN 1
F	Dual port RJ-45 GbE LAN Connector (NIC3 and NIC4)	X	IPMB Connector
G	SATA RAID key	Y	SATA SGPIO Connector
H	DB15 Video port	Z	HSBP Connector
I	Dual port RJ-45 GbE LAN Connector (NIC1 and NIC2)	AA	USB Floppy
J	Diagnostic/ID/Status LED	BB	SATA 0
K	Main Power Connector	CC	SATA 3

	Description		Description
L	System FAN 4	DD	SATA 1
M	CPU Power Connector	EE	SATA 4
N	CPU Fan	FF	SATA 2
O	Power Supply AUX Connector	GG	SATA 5
P	DIMM Slots	HH	Intelnal USB connector
Q	System FAN 3	II	Intel® RMM3 Lite
R	System FAN 2	JJ	Front Panel Connector
		KK	Internal Serial Port

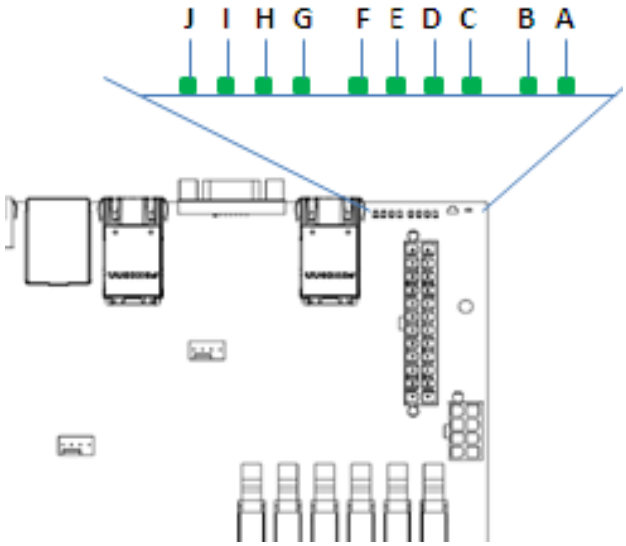
Figure 6. Connector and Component Definitions



A	Redundant Power Supply Units	G	RJ-45 Serial Port
B	Power Supply Status LED	H	PCI Express* Add-in slot
C	NIC 1 & 2 connectors RJ-45	I	Reserved for IO module external connectors
D	Video Out	J	Top Cover Thumb Screw
E	NIC 3, 4 & 5 connectors RJ-45		
F	Dual USB Ports		

Figure 7. Back Panel Feature Overview

Important Note: *The* ***Intel® Server System SR1695GPRX*** *requires the use of shielded LAN cable to comply with Emission/Immunity regulatory requirements. Use of non shield cables* ***may result in*** *product non-compliance.*



A	ID LED	B	Status LED
C	Diagnostic LED #7 MSB	G	Diagnostic LED #3 LSB
D	Diagnostic LED #6 MSB	H	Diagnostic LED #2 LSB
E	Diagnostic LED #5 MSB	I	Diagnostic LED #1 LSB
F	Diagnostic LED #4 MSB	J	Diagnostic LED #0 LSB

Figure 8. Light-Guided Diagnostic LED Locations

2.6 Rack and Cabinet Mounting Options

The chassis was designed to support 19 inches wide by up to 30 inches deep server cabinets. The system supports the following Intel rack mount options:

- A basic slide rail kit (Product order code – **AXXBASICRAIL**) is designed to mount the chassis into a standard (19 inches by up to 30 inches deep) EIA-310D compatible server cabinet.
- A tool-less slide rail kit (Product order code – **AXXHERAIL2**) is designed to mount the chassis into a standard (19 inches by up to 30 inches deep) EIA-310D compatible server cabinet.
- A chassis cable management arm (Product order code – **AXXRACKARM2**), which is compliant with **AXXHERAIL2**, is also available.

3. Power Sub-System

The system supports AC 400W 1+1 hot swap power supply module and one power distribution board which can support 1U rack server system. The single power supply module is 80 plus energy efficiency, demonstrating climate saver with silver rating.

3.1 Mechanical Overview

The power supply module has a simple retention mechanism to retain the module self once it is inserted. This mechanism shall withstand the specified mechanical shock and vibration requirements. The power distribution board will be fixed in the chassis with screws. This specification defines a 400W 1+1 hot swap redundancy power supply that supports a 1U server system. Using existing power supply module provided by vendor with updated PMBus* and custom-made power connector board to support Intel® server board S3420GPRX. The power supply shall have four outputs: 12V, 5V, 3.3V and 5VSB. The input shall be auto ranging and power factor corrected. The PMBus* features included in this specification are requirements for AC silver rated box power supply for use in server systems based on Intel® SR1695GPRX Server Platform. This specification is based on the PMBus* specifications part I and II, revision 1.1.

3.1.1 AC Power Supply Unit Dimension Overview

The casing dimension is W 47.0mm x L 233.0mm x H 37.8mm:

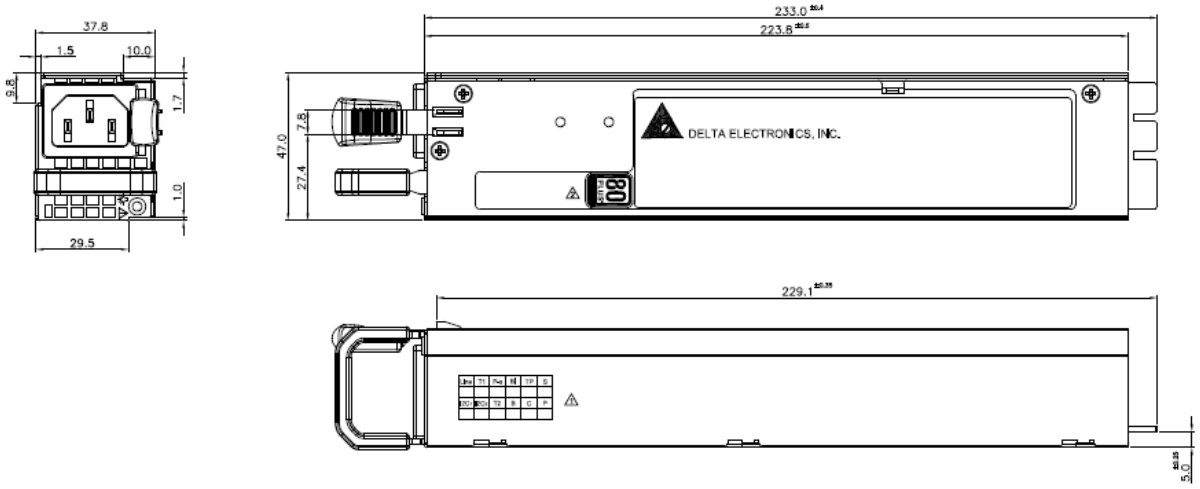


Figure 9. AC Power Supply Unit Dimension Overview

3.1.2 AC input connector

The power supply shall have an internal IEC320 C14 power inlet. The inlet is rated for a minimum of 10A at 250VAC.

3.1.3 AC Power Cord Specification Requirements

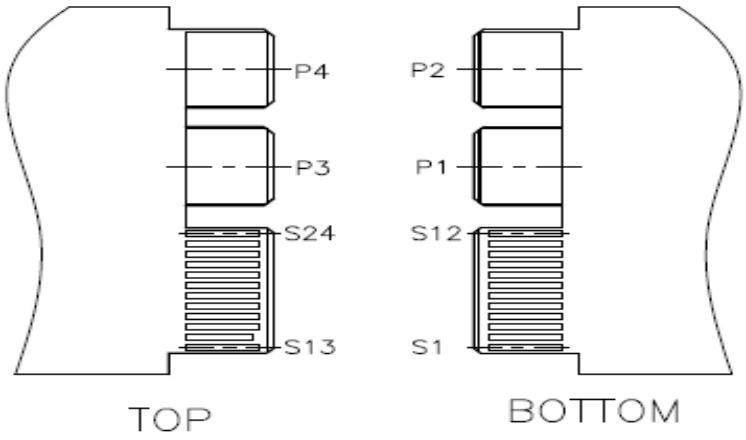
The AC power cord used must meet the following specification requirements:

Table 3. AC power cord specification

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105º C
Amperage Rating	13A
Cable Type	SJT

3.1.4 Power Supply Unit DC Output Connector

The DC output connector pin-out is defined as follow.



PSU Output Connector							
S1		**S8**	PSON	**S15**	A0	**S22**	RS-
S2		**S9**	PWOK	**S16**	VCC2	**S23**	5VSB
S3	IMON	**S10**	SGND	**S17**	SGND	**S24**	5VSB
S4	ALERT	**S11**	+5VSB	**S18**	FAN_PWM	**P1**	+12V
S5	SDA	**S12**	+5VSB	**S19**	FAN_PULSE	**P2**	+12V
S6	SCL	**S13**		**S20**	FAN_VS	**P3**	SGND
S7	PSKILL	**S14**		**S21**	RS+	**P4**	SGND

Figure 10. DC Output Power Connector

3.1.5 Power Cage with Power Distribution Board

The power cage dimension is W 96.8mm x L 317.7mm x H 40.0mm:

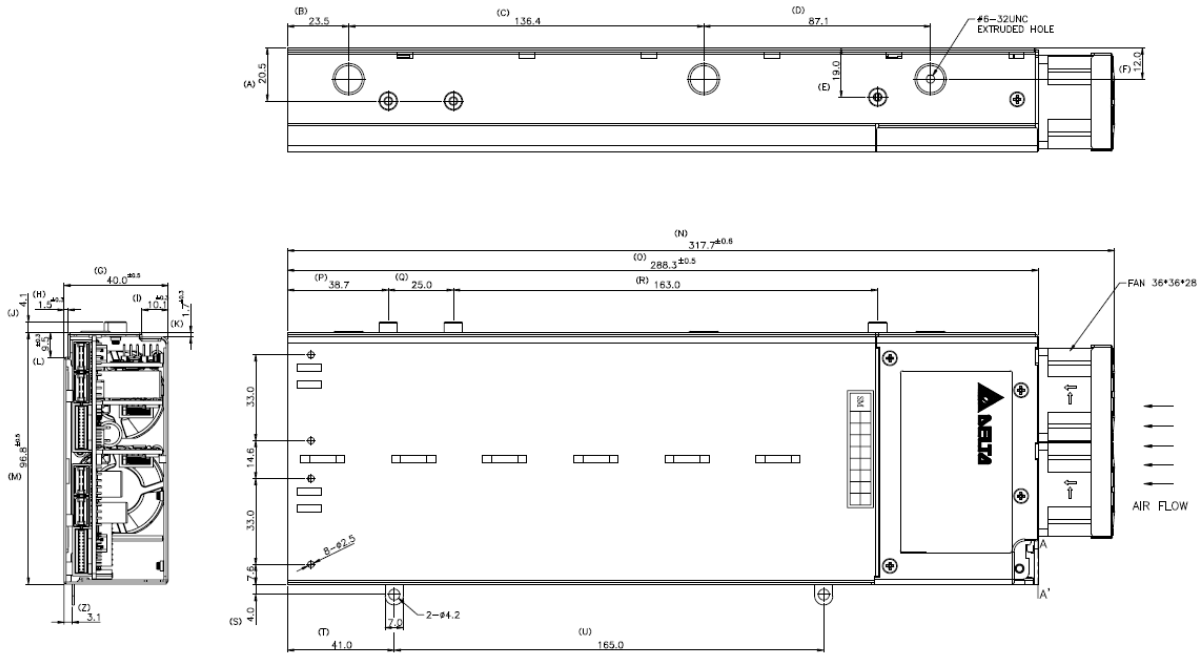


Figure 11. Power Cage Overview

3.1.6 Power Cage Output Pin Assignment

The power cage provides a cable harness for connectors to the various system boards. You can find the harness size, connectors (explained in the following table), and connectors' pin definitions in the power cage specification. Listed or recognized component appliance wiring material (AVL V2), CN, rated 105°C min, 300Vdc min shall be used for all output wiring.

Table 4. Cable Harness Definition

From	Length mm	To connector #	Number of pins	Description
Power Cage exit hole	360	P1	2x12	Main power connector
Power Cage exit hole	340	P2	2x4	Processor and memory power connector
Power Cage exit hole	480	P3	2x2	Cable for Backplane power1
Power Cage exit hole	270	P4	2x2	Cable for Backplane power2
Power Cage exit hole	300	P5	1x5	Cable for PMBUS
Power Cage exit hole	295	P6	1x4	CD/DVD drive SATA Power Connector

P1 – Main Power Connector

Connector housing: 24-Pin Molex* Mini-Fit Jr. 39-01-2245 or equivalent.

Table 5. P1 – Main Power Connector Pin-out

Pin	Signal	Wire & Color	Pin	Signal	Wire & Color
1	+3.3 VDC	AWG 20 Orange	13	+3.3 VDC	AWG 20 Orange
2a/2b	+3.3 VDC	AWG 20/24 Orange	14	Reserved	N.C.
3	GND	AWG 20 Black	15	GND	AWG 18 Black
4a/4b	+5 VDC*	AWG 18/24 Red	16	PSON#	AWG 24 Green
5a/5b	GND	AWG 18/24 Black	17	GND	AWG 18 Black
6	+5 VDC	AWG 20 Red	18	GND	AWG 18 Black
7	GND	AWG 20 Black	19	GND	AWG 18 Black
8	PWR OK	AWG 24 Gray	20	Reserved	N.C.
9	5VSB	AWG 20 Purple	21	+5 VDC	AWG 20 Red
10a/10b	+12V	AWG 18/24 Yellow	22	+5 VDC	AWG 20 Red
11	+12V	AWG 18 Yellow	23	+5 VDC	AWG 20 Red
12	+3.3 VDC	AWG 20 Orange	24	GND	AWG 20 Black

Notes:

1. 3.3V Locate Sense Double Crimped into pin 2.
2. 5V Remote Sense Double Crimped into pin 4.
3. 12V Locate Sense Double Crimped into pin 10.
4. GROUND Remote Sense Double Crimped into pin 5.

P2 – Processor and Memory Power Connector

Connector housing: 8-Pin Molex 39-01-2085 or equivalent

Table 6. P2 – Processor and Memory Connector Pin-out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	GND	Black	5	+12V	Yellow
2	GND	Black	6	+12V	Yellow
3	GND	Black	7	+12V	Yellow/Black Stripe
4	GND	Black	8	+12V	Yellow/Black Stripe

P3 & P4 – Cable for Backplane Power connector 1&2

Connector housing: 4-Pin Molex 39-01-2040 or equivalent

Table 7. P3 and P4 – Backplane Power Connector Pin-out

Pin	Signal	18AWG Color
1	GND	Black
2	+12V	Yellow/Black Strip
3	+5VDC	Red
4	+3.3VDC	Red

P5 – PMBus Connector

Connector housing: 5-pin Molex 50-57-9705 or equivalent

Table 8. P5 – PMBus / Power Signal Connector Pin-out

Pin	Signal	24 AWG Color
1	I2C Clock	White/Yellow Stripe
2	I2C Data	White/Yellow Stripe
3	I2C Alert	White
4	Return	Black
5	Reserved	N.C.

P6 – CD/DVD Drive SATA Power connector

Connector housing: 4-Pin Molex 43640-0400 or equivalent

Table 9. P6 – CD / DVD Drive SATA Power Connector Pin-out

Pin	Signal	22 AWG Color
1	+5VDC	Red
2	+5VDC	Red
3	GND	Black
4	GND	Black

3.1.7 Power Cage Output Specification

The power cage output from power distribution board provides four sets of DC power output to various system boards.

Minimum, nominal and maximum output voltage shall be within the limits in below table of the +12V,+3.3V,+5V, and +5VSB outputs along with the load current for adjustment / Measurement of the voltage Set point.

Table 10. Static Voltage Regulation

Parameter	Min	Nom	Max	Unit	Tolerance
+3.3V	+3.168V	+3.300V	+3.432V	Vrms	±4%
+5V	+4.800V	+5.000V	+5.200V	Vrms	±4%
+5VSB	+4.750V	+5.000V	+5.250V	Vrms	±5%
+12V	+11.520V	+12.000V	+12.480V	Vrms	±4%

The combined output continuous power of all outputs shall not exceed 360W. Each output has a maximum and minimum current rating shown in below table. The power supply shall meet both static and dynamic voltage regulation requirements for the minimum dynamic loading conditions. The power supply shall meet only the static load voltage regulation requirements for the minimum static load conditions.

Table 11. Load Ratings

	+3.3V	+5.0V	+12.0V	+5VSB
Max Continuous Current	12A	10A	30A	3A
Min Dynamic Current	0.5A	0.5A	2A	0.5A
Min Static Current	0.5A	0.5A	0.5A	0.1A

The power supply output voltages shall remain within limits specified in below table for the step loading and capacitive loading specified in Table 4 below. The load transient repetition rate shall be tested between 50 Hz and 5 kHz. The load transient repetition rate is only a test specification. Each rail's remote sense is connected to the respective output cable termination at the mating connector(s).

Table 12. Dynamic Tolerance Requirement

Ooutput	Min	Nom	Max	Tolerance
+3.3V	3.135 V	+3.300V	3.465 V	+/-5%
+5V	4.750 V	+5.000V	5.250 V	+/-5%
+5VSB	4.750 V	+5.000V	5.250 V	+/-5%
+12V	11.400 V	+12.000V	12.600 V	+/-5%

3.2 AC Voltage Input Specification

3.2.1 Input Voltage And Frequency

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% THD must not cause the power supply to go out of specific limits. The power supply shall be capable of start-up (power-on) with full rated power load, at line voltage as low as 90VAC.

Table 13. AC input rating.

Parameter	Min	Rated	Max	Start up VAC	Power Off VAC	Max Input Current at Min Vrms
120VAC	90 V_{rms}	100-127 V_{rms}	132 V_{rms}	< 85 V_{ac}	< 80V_{ac}	6 A_{rms}
220VAC	180 V_{rms}	200-240 V_{rms}	264 V_{rms}			3 A_{rms}
Frequency	47 Hz		63 Hz			

3.2.2 AC input Power Factor

3.2.2.1 The typical power factor shall be greater than 0.98 at 90Vac/47Hz with loading specified below.

Table 14. Typical power factor for 110VAC

90Vac/47Hz	5VSB	12V Main	Output Watts	Min PF
100% load	2.8 A	32.2A	400.4W	0.98

3.2.2.2 The typical power factor shall be greater than 0.94 at 90Vac/60Hz with loading specified below.

Table 15. Typical power factor for 110VAC

240Vac/60Hz	5VSB	12V Main	Output Watts	Min PF
100% load	2.8A	32.2A	400.4W	0.95

3.2.3 Efficiency

Test Condition: 230VAC line voltage, 60Hz, 25 +/-3C temperature, excluding FAN.
Minimum efficiency requirement at 230VAC is shown in below table.

Table 16. Efficiency requirement

	5VSB	12V Main	Output Watts	Minimum Efficiency
20% load current	0.4	6.5	80	85%
50% load current	1.4	16.1	200.2	89%
100% load current	2.8	32.2	400.4	85%

3.2.4 AC Line Fuse

Power supply shall have one line fuse, on the Line (Hot) wire of the AC input. AC line fusing must be acceptable for all safety agency requirements. AC inrush current shall not cause the AC line fuse to open under any conditions. All protection circuits in the power supply shall not cause the AC fuse to open, unless a component in the power supply has failed. This includes DC output overload or shorted output conditions.

3.2.5 AC Line Inrush

The AC line inrush current must not exceed 35A peak 0.1mS after application of AC power. The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during hot plug, during any AC dropout condition, over the specified temperature range (T_{op}), and during AC power cycling. The AC power cycling test condition is defined as cycling the AC power off and back on 5 times after the power supply has been operating at maximum load and has reached thermal stability. The period between the 5 AC power cycles could be anywhere between 100 msec to 10 seconds.

3.2.6 AC Line Leakage Current

Maximum input leakage current at 120VRMS shall not exceed 0.75mA.

3.2.7 AC Line Dropout

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout less than **10ms**, the power supply must meet dynamic voltage regulation (Table 3.3 Dynamic Tolerance Requirement) over the rated load. An AC line dropout of **1/2** cycle or less shall not cause any tripping of control signals or protection circuits. If the AC dropout lasts longer than **1/2** cycle the power supply should recover and meet all turn on requirements. The power supply must meet the AC dropout requirement over rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply.

3.2.8 Brownout

The power supply should withstand a brownout and recover from it without any damage stated in below table 8:

Table 17. AC Brownout and Recover

0 – 115VAC	Shut Down	Recover
Full Load	80Vac	85Vac

3.2.9 AC Line Fast Transient (EFT) Specification

The power supply shall meet the *EN61000-4-5* directive and any additional requirements in *IEC1000-4-5: 1995* and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.

The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.2.10 Hot Plug

Power supply shall be designed to allow connection into and removal from the system without removing power to the system. During any phase of insertion, start-up, shutdown, or removal, the power supply shall not cause any other like modules in the system to deviate outside of their specifications. When AC power is applied, the auxiliary supply shall turn on providing bias power internal to the supply and the 5VSB standby output.

3.2.11 Susceptability Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria, defined in the SSI document EPS Power Supply Specification. For further information on customer standards please request a copy of the customer Environmental Standards Handbook.

Table 18. Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024: 1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-4:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

Radiated Immunity

The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

Surge Immunity

The power supply shall be tested with the system for immunity to AC Ring wave and AC Unidirectional wave, both up to 2kV, per EN 55024:1998, EN 61000-4-5:1995 and ANSI C62.45: 1992.
The pass criteria include: No unsafe operation is allowed under any condition; All power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.
The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

3.2.12 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 19. AC Line Sag Transient Performance

AC Line Sag				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria.
Continuous	10%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance.
0 – 10ms	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance.
> 1 AC cycle	>10%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable.

Table 20. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.2.13 Power recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.2.14 AC Line Isolation

The power supply shall meet all safety agency requirements for dielectric strength. Transformers’ isolation between primary and secondary windings must comply with the

3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. In addition the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

3.2.15 AC Power Inlet

The AC input connector should be an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250 VAC.

The AC power cord must meet the following specification requirements:

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105º C
Amperage Rating	13 A
Voltage Rating	125 V

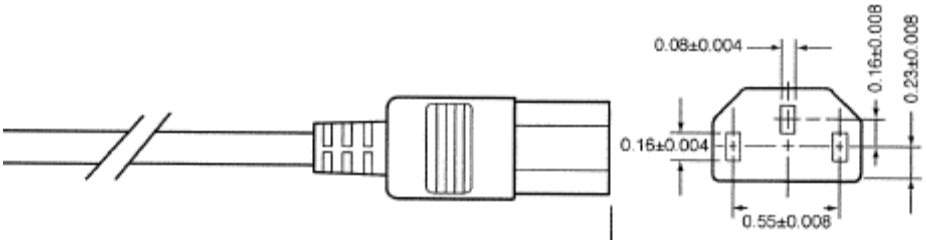


Figure 12. AC Power Cord Specification

3.3 DC Voltage Ouput Specification

3.3.1 Output Power/Currents

The following table defines the output current ratings. The combined output power of all outputs shall not exceed 400W @90V to 264V AC input. Each output has a maximum and minimum current rating shown in table 3.1. The power supply shall meet both static and dynamic voltage regulation requirements for the minimum dynamic load conditions. The power supply must meet only the static load voltage regulation requirements for the minimum static load conditions.

Table 21. Load Rating

	+12V	+5VSB
MAX	33A	3A
MIN DYNAMIC	2A	0.5A
MIN STATIC	0.5A	0.1A

3.3.2 Static Regulation

The power supply output voltages shall stay within the following voltage limits when operating at steady state load conditions. These limits do not include the peak-peak ripple/noise specified in below table.

Table 22. Static Voltage Regulation

Output	Min	Nom	Max	Units	Tolerance
+12V	+11.664	+12.150	+12.636	V_{rms}	+4/-4%
+5VSB	+4.850	+5.000	+5.200	V_{rms}	+4/-3%

3.3.3 Static Regulation

The output voltages shall remain within limits specified in Dynamic Regulation for the step loading and capacitive loading specified in below table. The dynamic tolerance includes the static regulation tolerance. The load transient repetition rate shall be tested between 50 Hz and 5 kHz at duty ranging from 10% to 90%. The load transient repetition rate is only a test specification. The Δstep load may occur anywhere within the Min load to Max load conditions.

Table 23. Dynamic Tolerance Requirements

Output	Min	Max	Tolerance
+12V	11.482 V	12.636 V	+4 / -5.5 %
+5VSB	4.800 V	5.250 V	+5/ -4 %

Table 24. Transient Load Requirements

Output	Step Load Size	Slew Rate	Capacitive Load
+12V	50% load change	0.5 A/ sec	2,200 F
+5VSB	50% load change	0.5 A/ sec	470 F

3.3.4 Capacitive Loading

The power supply must be stable and meet all requirements, with the following capacitive loading conditions.

Table 25. Capacitive Loading Conditions

Output	Min	Max	Units
+12V	2,200	22,000	F
+5VSB	470	1000	F

3.3.5 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in the table below. This is measured over a bandwidth of 0Hz to 20MHz at the power supply output connector. Minimum capacitance as specified within Table 3.4 in parallel with a 10 F tantalum capacitor and also in parallel with a 0.47 F ceramic capacitor are placed at the point of measurement.

Table 26. Ripple and Noise

+12V	+5VSB
120mVp-p	50mVp-p

3.3.6 Timing Requirement

These are the timing requirements for single power supply operation. All outputs shall rise and fall monotonically.

Table 27. Turn On/Off Timing

Item	Description	Min	Max	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	ms
T_{5Vsb_rise}	5Vsb Output voltage rise time	1	50	ms
T_{vout_rise}	DC Output voltage rise time	1	50	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to DC output voltage being within regulation.		2000	ms
T_{vout_holdup}	Time DC output voltage stay within regulation after loss of AC	12		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	11		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to DC output voltage within regulation limits.	5	100	ms
T_{pson_pwok}	Delay from PSON# de-active to PWOK being de-asserted.		50	ms
T_{pwok_on}	Delay from DC output voltage within regulation limits to PWOK asserted at turn on.	100	500	ms
T_{sb_vout}	Delay from 5Vsb being in regulation to DC output voltage being in regulation at AC turn on.	50	1000	ms
T_{5VSB_holdup}	Time the 5Vsb output voltage stays within regulation after loss of AC.	70		ms
$T_{vout\_falling}$	Output falling from 90% regulation to < 0.3V with respect to common return (12V@0.5A, 5VSB @ 0.1A.)		500	ms
$T_{5Vsb\_falling}$	Output falling from 90% regulation to < 0.3V with respect to common return (5VSB @ 0.1A.)		500	ms

3.3.7 Forced Load Sharing

The +12V output shall have forced load sharing. The +12V output load shall be shared between parallel units within 10% (+5%, -5%) from the half load point to full load for a single supply. For purpose of verifying current sharing function, full load value shall be 33A for a single supply for the +12V output. The supplies must be able to load share with up to 2 power supplies in parallel and operate in a hot swap/redundant 1+1 configuration. The 5VSB output is not required to share current between power supplies however these outputs are connected together in the system and a failure or hot swap of a redundant power supply will not cause these outputs to go out of regulation in the system.

Examples of load share accuracy at limits of acceptability (**+5%, -5% sharing**):
2 power supplies and system load equals 33A: PS #1 = 17.325A, PS #2 = 15.675A

3.3.8 Load Sharing, Load Monitoring Signal Characteristic

The load share signal provides both the load sharing function and +12V output current information. The characteristics of the load share signal are defined below in the table below.

3.4 Control And Indicator Functions

Signals that can be defined as low true or high true shall adopt the following conversion: signal# = low true.

3.4.1 PSON#(Power supply enable)

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the +12V output is turned off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Figure 3.6 Turn On/Off Timing diagram. When in off or standby condition, the +12V output shall be less than 50mV with respect to output return.

Table 28. PS ON# Signal Characteristics.

Signal Type(Input Signal to Supply)	Accepts an open collector/drain input from the system. Pull-up internal to the power supply.	
PSON# = Low, PSKILL = Low	ON	
PSON# = Open, PSKILL = Low or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2V	5.25V
Source current, V_{PSON}# = low		4mA

3.4.2 PSKILL

The purpose of the PSKILL pin is to allow for hot swapping of the power supply and to provide a fast shutdown input. The PSKILL pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PSKILL pin shall quickly turn off the power supply and prevent arcing of the DC output contacts. The DC output contacts shall not arc under this condition. T_{PSKILL} (shown in below table) is the minimum time delay from the PSKill pin un-mating to when the power pins un-mate. The power supply shall discharge its output inductor within this time from the un-mating of the PSKill pin. When the PSKILL signal pin is not pulled down or left open (power supply is extracting from the system), the power supply shall shut down regardless of the condition of the PSON# signal. The mating pin of this signal in the system shall be tied to ground. Internal to the power supply, the PSKill pin shall be connected to a standby voltage through a pull-up resistor. Upon receiving a LOW state signal at the PSKill pin, the power supply shall be allowed to turn on via the PSON# signal. A logic LOW on this pin by itself shall not turn on the power outputs.

Table 29. PSKILL# Signal Characteristics

Signal Type (Input Signal to Supply)	Accepts a ground input from the system. Pull-up to VSB located in the power supply.	
PSKILL = Low, PSON# = Low	ON	
PSKILL = Open, PSON# = Low or Open	OFF	
PSKILL = Low, PSON# = Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	0.8V
Logic level high (power supply OFF)	2V	5.25V
Source current, V_{PSKILL} = low		4mA
Delay from PSKILL=High to power supply turned off ($T_{PSKILLI}$) [1]		100 sec

3.4.3 PWOK(power good)

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that the +12V output is within the regulation limits of the power supply. When +12V output voltage falls out of regulation or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK shall be de-asserted to a LOW state. See Figure 3.6 Turn On/Off Timing Diagram for a representation of the timing characteristics of PWOK. This signal shall be pulled up to 5VSB inside the PS.

Table 30. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in power supply.	
DCOK = High	Power Good	
DCOK = Low	Power Not Good	
	MIN	MAX
Logic level low voltage, Isink=4mA	0V	**0.6V**
Logic level high voltage, Isource=200 A	**3.0V**	**3.3V**
Sink current, DCOK = low		4mA
Source current, DCOK = high		2mA
DCOK rise and fall time		100 sec

3.4.4 LED indicators

There is a green POWER LED (PWR). The LED shall be visible on the power supply's exterior face. The LED and its location shall meet ESD requirements required for the power supply. The LED shall be securely mounted in such a way that incidental pressure on the LED will not cause it to become displaced.

Table 31. Power Supply Unit LED Indications

	Power Supply LED
Power Supply Condition	Power LED (green)
No AC power to all PSU	OFF
No AC power to this PSU only	OFF
AC present / Standby Outputs On	OFF
Power supply DC outputs ON and OK	ON
Power supply failure	OFF

3.5 Protection circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. The 5VSB output shall remain powered on if the failure does not involve this outputs. When a protection circuit shuts down the power supply, green LED shall change to unlighted status and the DC OK signal shall be asserted false. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec must be able to reset the power supply.

3.5.1 Current Limit (OCP)

The power supply shall have current limit to prevent the +12V output from exceeding the values shown in the table3.10 as below. The current limiting shall be of the constant current type. The over current limit level shall be maintained for a period of **100 msec** minimum and 3**00 msec** maximum. After this time the power supply shall latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. The 5VSB shall be protected under over current or shorted conditions but are not subject to the same constant current timing followed by requirement to latch off.

Table 32. Over Current Protection

VOLTAGE	OVER CURRENT LIMIT (Iout limit)
+12V	110% minimum; 150% maximum
+5VSB	3.6A minimum, 8A maximum

3.5.2 Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown in a latch off mode after an over voltage condition. This latch can be cleared by toggling the PSON# signal or by an AC power interruption. Table 3.11 contains the minimum and maximum output voltage levels for this condition. The values are measured at the output of the power supply's DC connector.

3.5.3 Over Thermal protection

The power supply shall be protected against over temperature conditions caused by loss of forced air-cooling or excessive ambient temperature. In an over-temperature condition the PS will shutdown. The Standby output may also shutdown or remain powered on. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically. The OTP circuit shall have built in hysteresis such that the power supply will not oscillate on and off due to temperature recovering condition. The power supply shall alert the system of the OTP condition via the power supply DCOK signal changing to false state and the green LED changing to an unlighted condition.

3.5.4 Closed Loop Stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: **45 degrees phase margin** and **-10dB-gain margin** is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.5.5 Common Mode Noise

The Common Mode noise on the output shall not exceed **350mVpk-pk** over the frequency band of 10Hz to 30MHz.
1. The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).
2. The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

3.5.6 Zero Load Stability Requirements

When the power subsystem operates in a no load condition on all outputs including 5VSB in a 1+0 or 1+1 configuration, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

3.5.7 Residual Voltage Immunity

The PS supply shall be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stress of any internal components with this voltage applied to any individual output, and all outputs simultaneously. It also should not trip the power supply protection circuits during turn on.

3.5.8 Hot Swap Requirement

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system in operating under static, dynamic, and zero loading conditions. The power supply can be hot swapped by the following method:
Extraction: The AC power will be disconnected from the power supply before the power supply is being extracted from the system. This could occur in standby mode or powered on mode.
Insertion: The AC power will be connected to the power supply after the power supply is inserted into the system and the power supply will power on into standby mode or powered on mode.
In general, a failed (off by internal latch or external control) power supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby mode or powered on mode once inserted.

3.6 PMBus*

The PMBus* features are requirements for power supply unit for use in server systems. This specification is based on the PMBus* specifications part I and II, revision 1.1. The power supply device address locations are shown below:

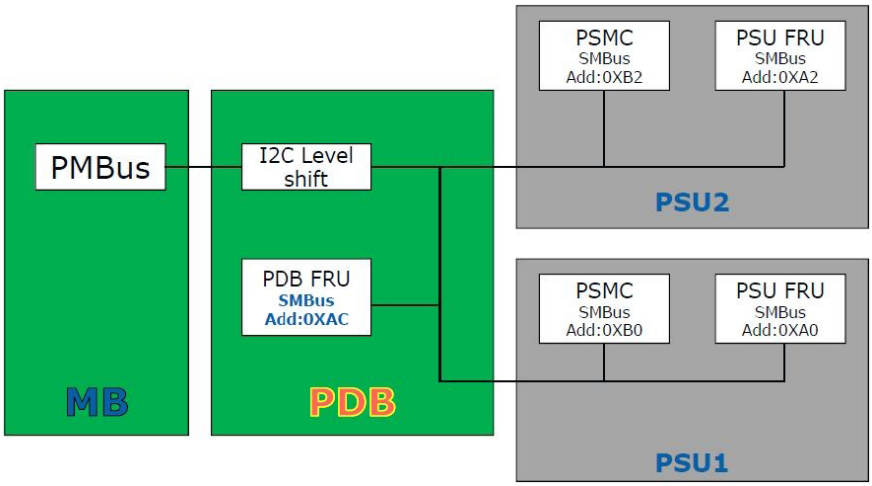


Figure 13. Power Supply Device Address

3.6.1 I2C Data and Clock

I2C data and clock signals shall be used to communicate power supply status with end use system.

3.6.2 PSU Address Lines A0

Address pins A0 is used by end use system to allocate unit address to a power supply in particular slot position.
For redundant systems there are two signals to set the address location of the power supply once it is installed in the system; Address0 and Address1. For non-redundant systems the power supply device address locations should align with the Address0/Address1 location of 0/0.

Table 33. PSU addressing

PDB addressing Address0	0	1
Power supply PMBus™ device	B0h	B2h

Note: Non-redundant power supplies will use the 0 address locations.

3.6.3 IPMI FRU Addressing

If the power supply has a FRU (field replaceable unit) serial EEPROM; it shall be located at the following addresses.

Table 34. PSU FRU addressing

System addressing Address0	0	1
FRU device addresses [2]	A0h/A1h [1]	A2h/A3h

Notes:

1 Non-redundant power supplies will use the 0 address location.
2 The addressing method uses the 7 MSB bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined above use 8 bits including the read/write bit.

4. Cooling Sub-System

Several components and configuration requirements make up the cooling sub-system of the chassis. These include processors, chipsets, VR heatsinks, system fan module, power supply fans, CPU air duct, and drive bay population. All are necessary to provide and regulate the air flow and air pressure needed to maintain the system's thermals when operating at or below the maximum specified thermal limits.

In order to maintain the necessary airflow within the system, you must properly install the air duct and the top cover.

The chassis uses a variable fan speed control engine to provide adequate cooling for the system at various ambient temperature conditions, under various server workloads, and with the least amount of acoustic noise possible. The fans operate at the lowest speed for any given condition to minimize acoustics.

Note: The server system does not support redundant cooling fans. If any of the fans fail, you must power down the system as soon as possible to replace the fan.

4.1 Processor Heatsink

A heatsink is included in the system package. This heatsink is designed for optimal cooling and performance. To achieve better cooling performance, you must properly attach the heatsink bottom base with TIM (thermal interface material). ShinEtsu* G-751 or 7783D or Honeywell* PCM45F TIM is recommended. The mechanical performance of the heatsink must satisfy mechanical requirement of Intel® Xeon® 3400 series and Core™ i3 series processors. To keep chipsets and VR temperature at or below maximum temperature limit, the heatsink is required if necessary.

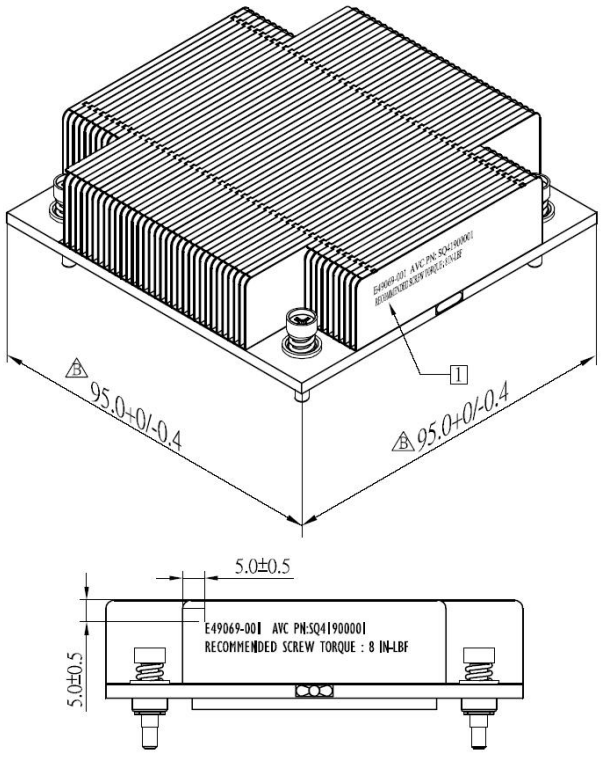


Figure 14. Processor Heatsink Overview

Note: The passive heatsink is Intel® standard thermal solution for 1U/2U rack chassis.

4.2 System cooling Fans

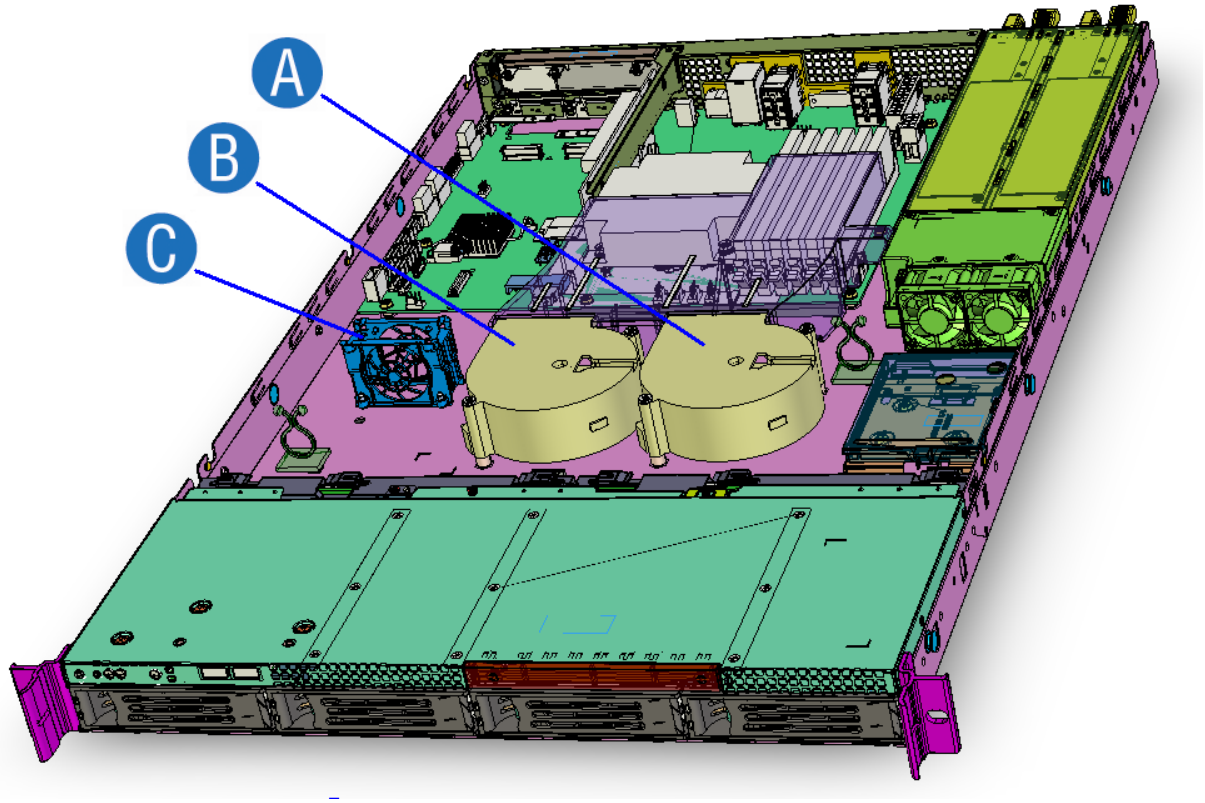
The Intel® Server System SR1695GPRX cooling subsystem consists of two 97 x 94 x 33 blower fans and one 40 x 40 x 15 rotor fan, and CPU air duct. These components provide the necessary cooling and airflow to the system. A fan on the processor heatsink is not needed.

To maintain the necessary airflow within the system, the air duct and the top cover must be properly installed.

Note: The Intel® Server Systems SR1695GPRX does not support redundant cooling. If a fan blower fails, the system should be powered down as soon as possible to replace the failed fan blower. The system fans are not hot-swappable.

Each fan within the module is capable of supporting multiple speeds. Fan speed changes automatically when internal ambient temperature of the system or processor temperature changes. The fan speed control algorithm is programmed into the server board's BIOS.

Each fan connector within the module supplies a tachometer signal that allows the BMC to monitor the status of each fan. If one of the fans should fail, the system fault LED on front panel will light.



A	Memory Cooling Blower
B	Processor Cooling Blower
C	PCI Express* Add-in Cooling Rotor Fan

Figure 15. Blower Fan Module Assembly

The blower fan uses 4-pin connector, which is connected to fan headers on motherboard.

The fan connector pin-out definition is as follows:

Table 35. 4-pin Connector Pin-Out for Blower Cooling Fan

Pin	Signal Name	Description
1	GND	Ground
2	12V	Power Supply +12 V
3	Tach Out	FAN_TACH signal output
4	PWM In	PWM signal input

There is additional rotor fan for cooling the chipset and PCI Express* add-in card. The rotor fan also uses 4-pin connector, which is connected to fan headers on motherboard.

The rotor fan connector pin-out definition is as follows:

Table 36. 8-pin Connector Pin-Out for Chassis Rotor Fan

Pin	Signal Name	Description
1	GND	Ground
2	12V	Power Supply +12 V
3	Tack0	Tach signal output
4	PMW0	PWM control signal input

4.3 Power Supply Fan

Each power supply module supports one non-redundant 40 mm fan. The fans control the cooling of the power supply and some drive bays. These fans are not replaceable. Therefore, if a power supply fan fails, you must replace the power supply module.

4.4 Air Duct Module

The chassis requires the use of an air duct module to direct airflow over critical areas within the system. The following provides a summary and description of Air Duct Module.

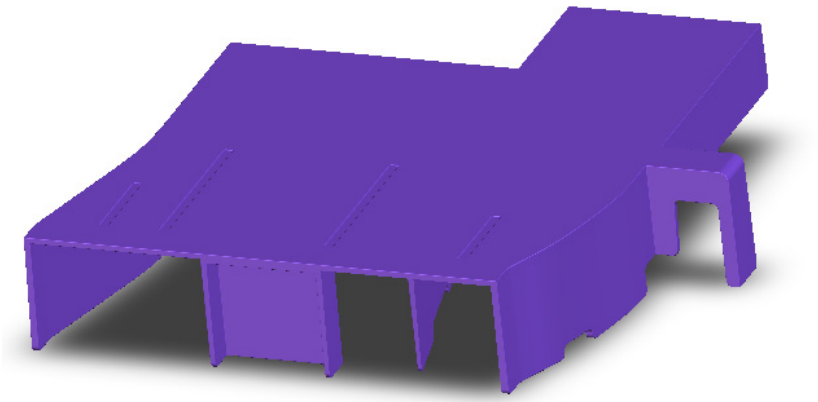


Figure 16. Air Duct Module

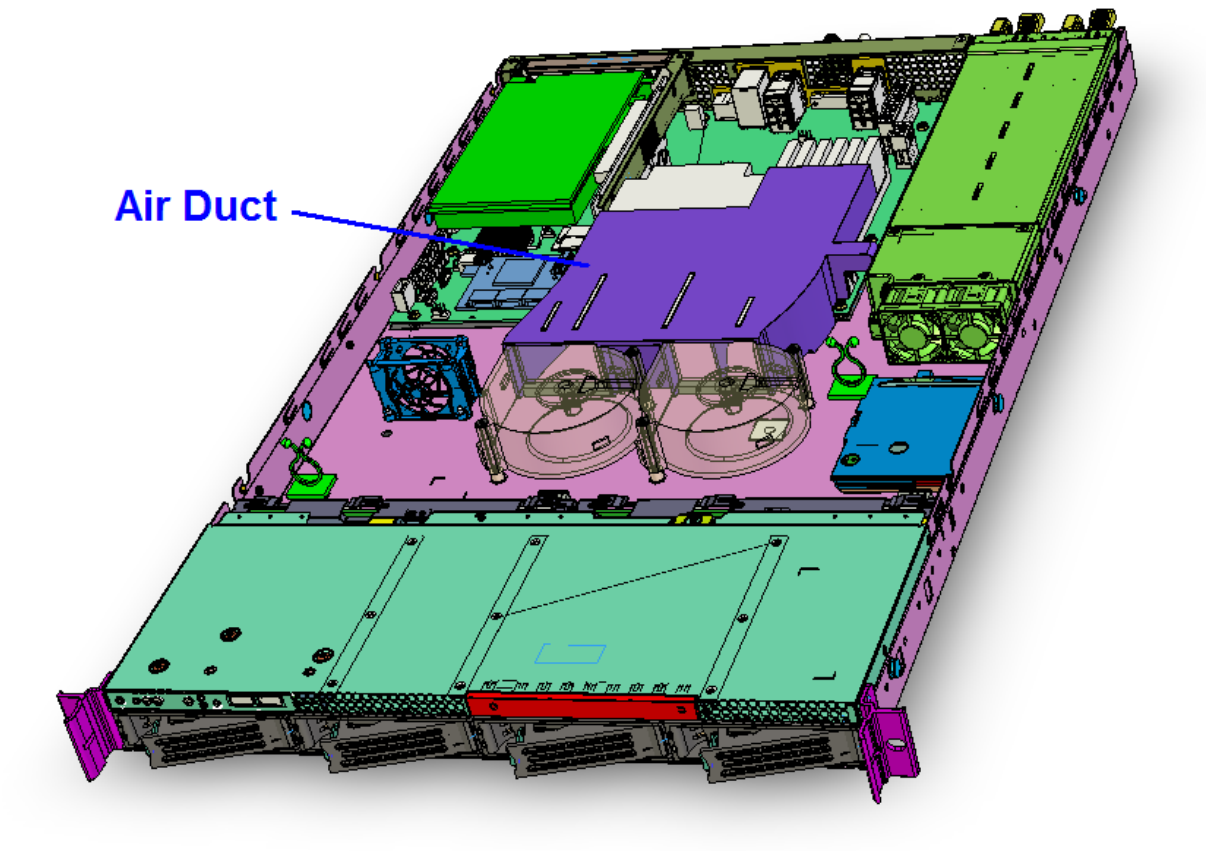


Figure 18. Air Duct Position in System

4.5 Drive Bay Population Requirement

In order to maintain system thermal requirements, you must fully populate all hard drive bays. Hard drive trays used for hot-swap drives must either have a hard drive installed or not have a hard drive installed.

IMPORTANT: If the drive bay is missing or not fully populated, the system will not meet the thermal cooling requirements of the processor, which will most likely result in degraded performance as a result of throttling or thermal shutdown of the system. It is recommended to apply the air block on the blank HDD carrier if the installed HDD quantity is less than four pieces.

5. Peripheral Drive Support

The system provides a slim-line drive bay that can populate with a SATA optical drive (CD-ROM, DVD, and DVD/CD-R). The drive is mounted on a tool-less tray, which allows for easy installation into and removal from the system. The slim-line device is not hot-swappable. It is recommended to use Intel® validated optical drive.

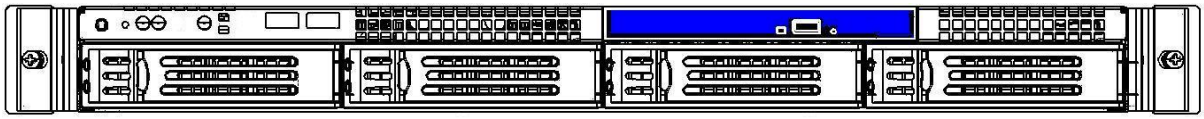


Figure 17. View of Slim-line Optical Drive Bay (in Deep Blue)

The drive is directly connected to a SATA cable and a SATA power cable. The other end of the SATA cable is connected to one SATA port on the server board.

Table 37. Optical Drive SATA Connector Pin-out

Pin	Signal Name	Description
1	GND	Ground
2	SATA_TX_P	Positive side of transmit differential pair
3	SATA_TX_N	Negative side of transmit differential pair
4	GND	Ground
5	SATA_RX_N	Negative side of receive differential pair
6	SATA_RX_P	Positive side of receive differential pair
7	GND	Ground

Table 38. Optical Drive SATA Power Connector Pin-out

Pin	Signal Name	Description
P1	Not Used	-
P2	Not Used	-
P3	Not Used	-
P4	GND	Ground
P5	GND	Ground
P6	GND	Ground
P7	P5V	Power supply 5V
P8	P5V	Power supply 5V
P9	P5V	Power supply 5V
P10	GND	Ground
P11	Reserved	-
P12	GND	Ground
P13	P12V	Power supply 12V
P14	P12V	Power supply 12V
P15	P12V	Power supply 12V

6. Hard Disk Drive Support

The server system provides four hard drive bays at the front of the chassis. You can populate all hard drive bays with a carrier-mounted 3.5-inch or 2.5-inch SATA or SAS hard disk drives.

6.1 Hard Disk Drive Bays

The server system 1U chassis can support up to four carrier-mounted SATA or SAS 3.5-inch or 2.5-inch hard disk drives. The drives may be “electrically” hot-swapped while the system power is applied, but you must take caution before hot-swapping while the system is functioning under operating system/application control or data may be lost.

Note: All drive bays (0 through 3) are controlled by the server board or the RAID controller card.

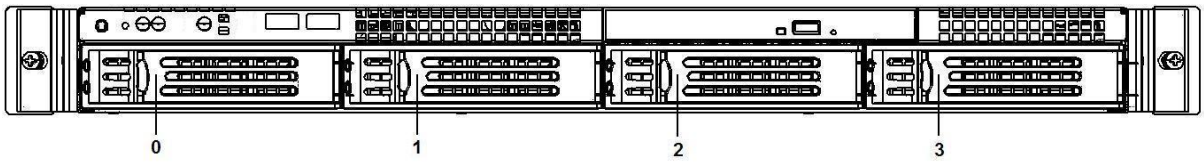


Figure 18. HDD Bays and Numbering

If a failed drive needs replacing, it is recommended you replace it with the same manufacturer, model, and capacity.

6.2 Hard Drive Trays

You can use hard drive trays for 3.5-inches or 2.5-inches hot-swap hard drive configurations.

Hot-swap drive trays make insertion and extraction of the drive from the system very simple. Each drive tray has its own latching mechanism, which is used to both insert and extract drives from the chassis and lock the tray in place. Each drive tray supports two light pipes to direct light from the drive status LEDs on the backplane to the tray’s face allowing it to be viewable from the front of the system.

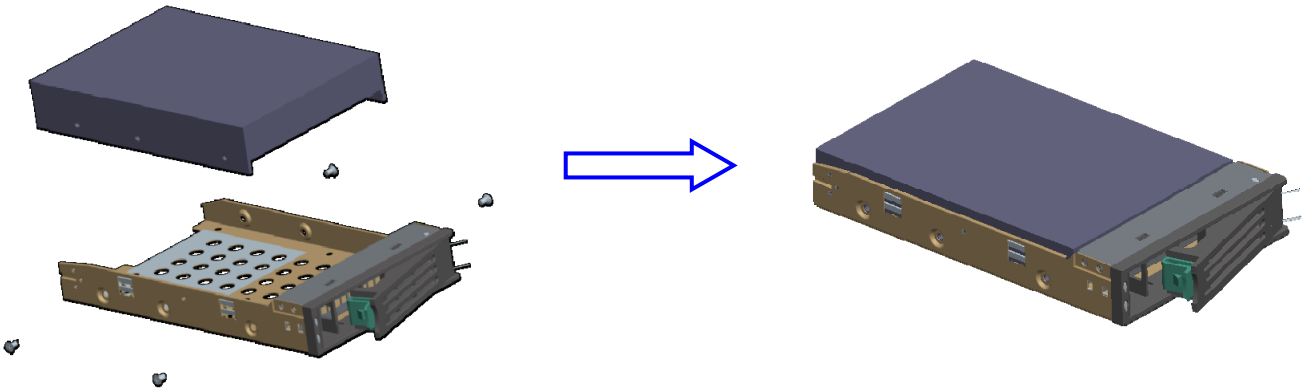


Figure 19. 3.5-inch HDD Assembly Overview

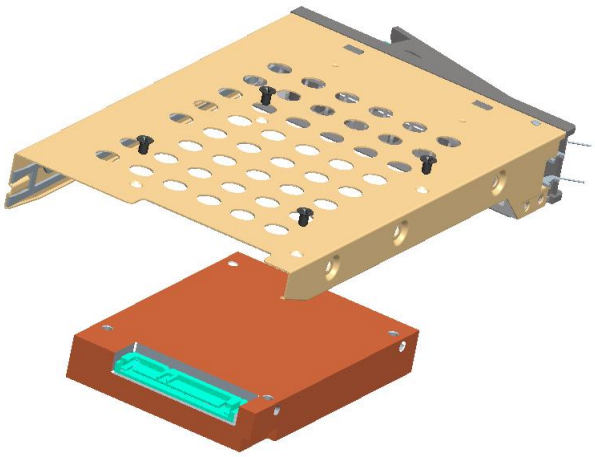


Figure 20. 2.5-inch HDD Assembly Overview

6.3 Hot-Swap Hard Drive Support

The Intel® Server System SR1695GPRX can support up to four hot-swap SATA or SAS hard drives. Hard drives interface with the passive backplane through a blind mate connection when drives are installed into a hard drive bay using hot-swap drive trays.

The passive backplane acts as an intermediate pass-through interface board where SATA ports of the server board or add-in SAS/SATA controller are cabled to the backplane. The on board Intel® 3420 Chipset (PCH) provides the necessary drive interface. You can also connect the passive backplane to an add-in PCI Express* based SAS/SATA RAID card.

The following sections describe the feature and connections between the backplane and server board.

6.3.1 Backplane Feature set:

Vitesse* VSC410 enclosure management controller

- Integrated v3000 32 bit RISC microprocessor core
- External non-volatile Flash ROM
- Four I^2C interfaces
- 44 GPIO pins

Four drive control connectors supporting either SATA ports from the server board or SAS/SATA ports from an add-in RAID card

Support for up to four hot-swap SAS/SATA drives

4x2 hard drive activity/fault LEDs

2x4 pin power connector

One 4-pin IPMB connector

One 4-pin SMBus connector

One 4-pin SGPIO connector
One 3-pin SES connector
Four internal SAS/SATA connectors

6.3.2 Backplane Block Diagram:

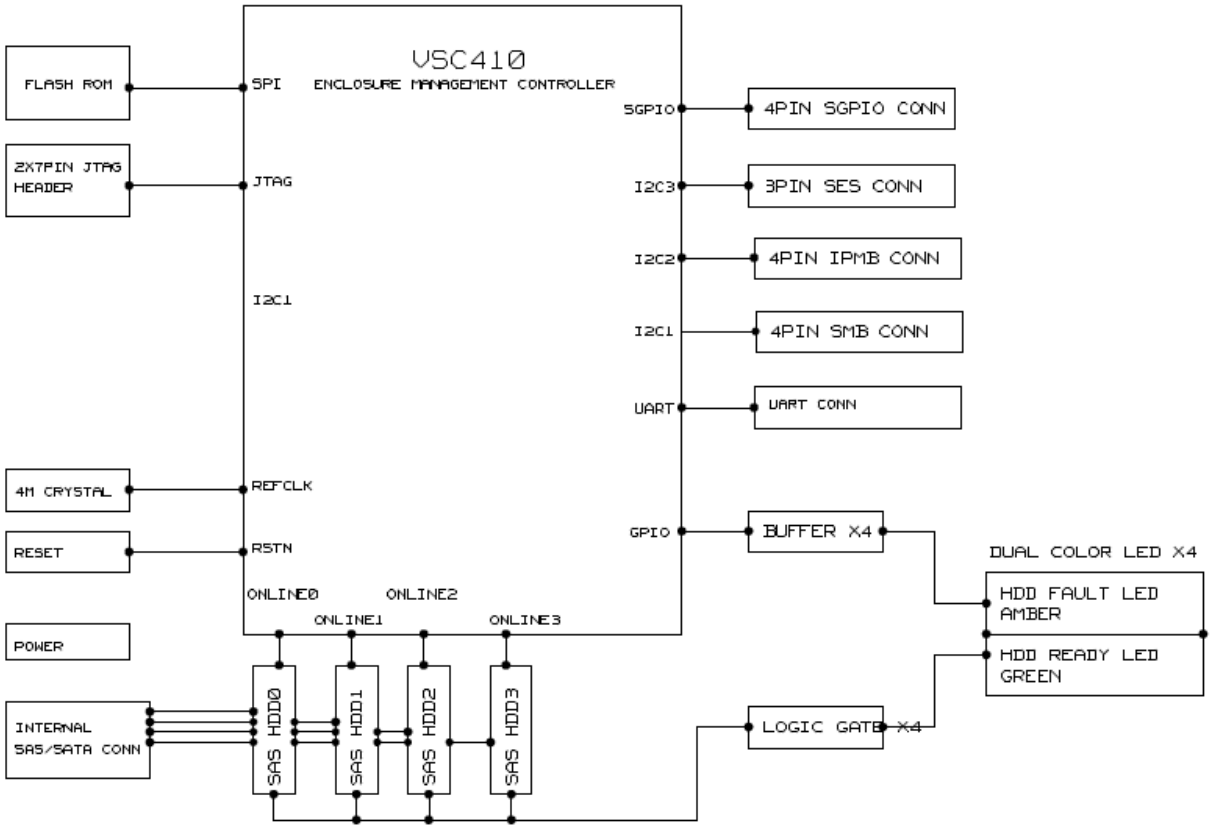
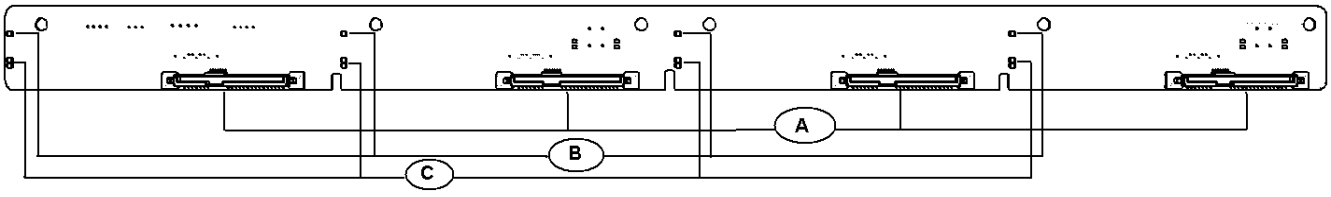


Figure 21. Passive Backplane Block Diagram

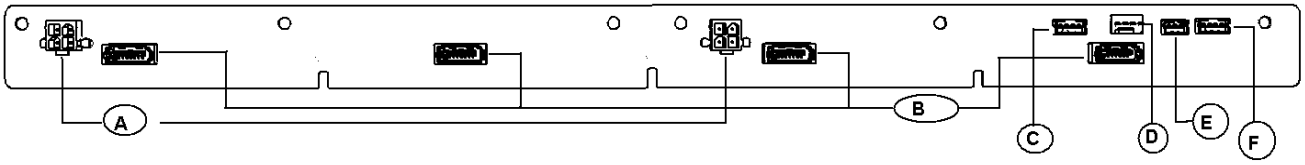
6.3.3 Backplane Connector Definition

The following diagrams show the layout of major components and connectors for backplane.



A	HDD Connectors 0~3 (left to right)
B	HDD On-line LEDs 0~3 (left to right)
C	HDD Act/Fault LEDs 0~3 (left to right)

Figure 22. Backplane Component and Connectors (Front View)



A	4-pin power connectors 1~2 for backplane
B	SATA/SAS connectors 0~3 (right to left)
C	4-pin SGPIO connector
D	4-pin SMBus connector
E	3-pin SES connector
F	4-pin IPMB connector

Figure 23. Backplane Component and Connectors (Back View)

6.3.4 Backplane LED Support

The backplanes support both HDD online and activity/fault LEDs for each of the hard drive connectors. A light duct in HDD tray is used to conduct LED light to front panel. The following lists LED functionality.

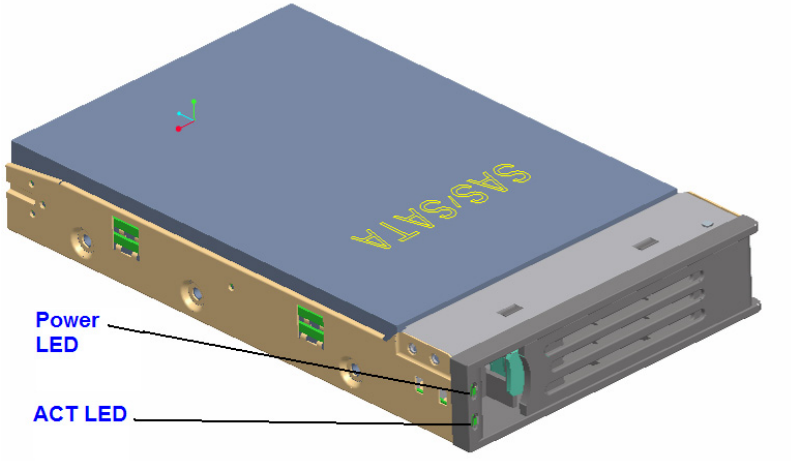


Table 39. Hard Drive Tray LED Functions

	LED color	Condition	Description
Power LED	Blue	ON	HDD On-line
		OFF	HDD Not On-line
Activity LED	Green	OFF	Standby/Stopped
		Flashing(on 0.5s off 0.5s)	Spin-Up/Spin-Down
		Flashing(on 1s, off 1s)/Off	Active/Idle power
		Flashing with high frequency	Formatting
	Amber	ON	Fault
		Flashing(on 0.5s off 0.5s)	Rebuild

6.3.5 Backplane Connector Definition

The backplanes include several different connectors. This section defines the purpose and pin out associated with each.

1) Power Connector(J1A1, J5A1)

The backplane provides power to the three hard drive bays and the slim-line drive bay. An 8-pin power cable is routed from the power supply and plugs into two 4-pin shrouded plastic PC power connector on the backplane. The following table shows the power connector pin-out.

Table 40. Backplane Power Connector Pin-out

Pin	Signal	Pin	Signal
1	COM	3	+5VDC
2	+12VDC	4	+3V3DC

2) Hot-Swap SATA/SAS Drive Connectors(JC2L1, JC4L1, JC6L1, JC9L1)

The backplanes provide four hot-swap SATA/SAS connectors, which provide power and signals using a single docking connector. Each drive attaches to the backplane using one of these connectors.

Table 41. Hot-Swap SATA/SAS Connector Pin-out

Pin#	Signal Description
SI	Ground
S2	SAS#_TX_DP (# = 0…2)
S3	SAS#_TX_DN (# = 0…2)
S4	Ground
S5	SAS#_RX_DN (# = 0…2)
S6	SAS#_RX_DP (# = 0…2)

Pin#	Signal Description
S7	Ground
S8	Not Used
S9	Not Used
S10	Not Used
S11	Not Used
S12	Not Used
S13	Not Used
S14	Not Used
P1	Not Used
P2	Not Used
P3	Not Used
P4	Ground
P5	Ground
P6	P3V3
P7	P5V
P8	P5V
P9	P5V
P10	Ground
P11	LED_SAS#_ACT_L (# = 0…2)
P12	Ground
P13	P12V
P14	P12V
P15	P12V
PTH0	Ground
PTY1	Ground

3) SATA/SAS Drive Control Connectors (J1A2, J4A1, J6A2, and J8A2)

The passive backplane includes four drive control connectors. These are used to attach SATA/SAS cables from the backplane to either the SATA ports on the server board, or to SAS/SATA ports from an add-in card. Each drive control connector has the following pin-out.

Table 42. SATA/SAS Drive Control Connector Pin-out

Pin#	Description
1	GROUND
2	SATA # TX_DP (# = 0,1,2)
3	SATA # TX_DN (# = 0,1,2)
4	GROUND
5	SATA # RX_DN (# = 0,1,2)
6	SATA # RX_DP (# = 0,1,2)
7	GROUND

4) System Management(IPMB) Connector(J9A1)

The backplanes provide connectors to interface with system management buses. The following tables define the pin-out for each of these connectors.

Table 43. IPMB Connector Pin-out

Pin #	Description
1	SMB_5VSB_IPMB_DAT
2	GND
3	SMB_5VSB_IPMB_CLK
4	SMB_PWR_IPMB_CONN

5) System Management Bus (SMBus) Connector (J8A1)

The backplanes provide connectors to interface with System Management Bus. The following tables define the pin-out for each of this connector.

Table 44. SMBus Connector Pin-out

Pin #	Description
1	SMB_5V_DAT
2	GND
3	SMB_5V_CLK
4	GND

6) System General Purpose IO (SGPIO) Connector (J4A2)

The backplanes provide connectors to interface with System General Purpose IO control. The following tables define the pin-out for each of this connector.

Table 45. SGPIO Connector Pin-out

Pin #	Description
1	Data In
2	Data Out
3	End Control
4	Clock

7) SCSI Enclosure Services (SES) Connector (J9A2)

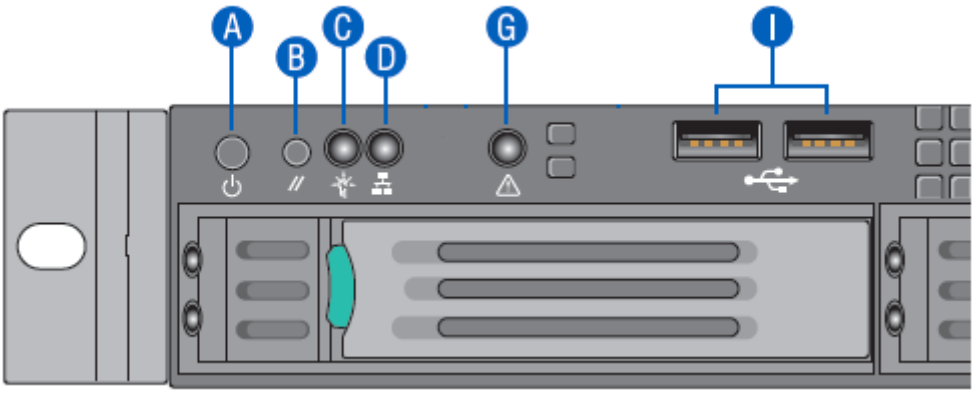
The backplanes provide connectors to interface with SCSI Enclosure Services (SES) signals. The following tables define the pin-out for each of this connector.

Table 46. SES Connector Pin-out

Pin #	Description
1	SMB_HBA_I2C_DAT
2	GND
3	SMB_HBA_I2C_CLK

7. Front Panel Control and Indicators

The Intel® Server System SR1695GPRX Front Control Panel integrates control buttons, LEDs, and USB ports. The control panel assembly is pre-assembled and fixed to the chassis.



A	Power/Sleep Button
B	System Reset Button
C	Power/Sleep LED
D	System NIC 5 Activity LED
G	System Status LED
I	USB 2.0 Connectors

Figure 24. Front Control Panel

7.1 Control Panel Button

The following table lists the control panel features and functions. The control panels features a system power button.

Table 47. Front Control Button Function

Feature	Function
Power/Sleep Button	Toggles the system power on/off. This button also functions as a Sleep Button if enabled by an ACPI-compliant operating system.
System Reset Button	Reset system to reboot

7.2 Control Panel LED Indicators

The control panel houses three LEDs, which are viewable to display the system's operating status.

The following table identifies each LED and describes their functionality.

Table 48. Front LED Indicator Functions

LED Indicator	Color	Condition	What it describes
Power/Sleep	Green	On	Power On/ACPI S0 state
	Green	Blink	Sleep /ACPI S1 state
	-	Off	Power Off /ACPI S5 state
LAN	Green	On	LAN Link no Access
	Green	Blink	LAN Activity
	-	Off	No Link
System Status	Green	On	System Ready/No Alarm
	Green	Blink	System ready, but degraded: redundancy lost such as the power supply or fan failure; non-critical temp/voltage threshold; battery failure; or predictive power supply failure.
	Amber	On	Critical Alarm: Critical power modules failure, critical fans failure, voltage (power supply), critical temperature and voltage
	Amber	Blink	Non-Critical Alarm: Redundant fan failure, redundant power module failure, non-critical temperature and voltage
	-	Off	Power off: System unplugged Power on: System powered off and in standby, no prior degraded\non-critical\critical state

Note:

Blink rate is ~1 Hz at 50% duty cycle.

It is also off when the system is powered off (S5) or in a sleep state (S1).

The power LED sleep indication is maintained on standby by the chipset. If the system is powered down without going through the BIOS, the LED state in effect at the time of power off is restored when the system is powered on until the BIOS clear it.

If the system is not powered down normally, it is possible the Power LED will blink at the same time the system status LED is off due to a failure or configuration change that prevents the BIOS from running.

7.2.1 Power/Sleep LED

Table 49. SSI Power LED Operation

State	Power Mode	LED	Description
Power Off	Non-ACPI	Off	System power is off and the BIOS has not initialized the chipset.
Power On	Non-ACPI	Solid On	System power is on but the BIOS has not yet initialized the chipset.
S5	ACPI	Off	Mechanical is off and the operating system has not saved any context to the hard disk.
S1 Sleep	ACPI	Blink	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Solid On	System and the operating system are up and running.

Note: Blink rate is ~ 1Hz at 50% duty cycle.

7.2.2 System Status LED

Table 50. System Status LED Operation

Color	State	Criticality	Description
Off	N/A	Not ready	Power off or BMC initialization completes if no degraded, non-critical, critical, or non-recoverable conditions exist after power cable plug in
Green/ Amber	Both Solid On	Not ready	Pre DC Power On – 15-20 second BMC Initialization when AC is applied to the server. The system will not POST until BMC initialization completes.
Green	Solid on	Ok	System ready
Green	Blink	Degraded	**BIOS detected** 1. Unable to use all of the installed memory (more than one DIMM installed).[1] 2. In a mirrored configuration, when memory mirroring takes place and system loses memory redundancy. This is not covered by (2). [1] 3. PCI Express* correctable link errors. **Integrated BMC detected** 1. One of redundant power supplies not present. 2. CPU disabled – if there are two CPUs and one CPU is disabled. 3. Fan alarm – Fan failure. Number of operational fans should be more than minimum number needed to cool the system. 4. Non-critical threshold crossed – Temperature, voltage, power nozzle, power gauge, and PROCHOT2 (Therm Ctrl) sensors. 5. Battery failure. 6. Predictive failure when the system has redundant power supplies.
Amber	Blink	Non-critical	Non-fatal alarm – system is likely to fail **BIOS Detected** 1. In non-mirroring mode, if the threshold of ten correctable errors is crossed within the window.[1] 2. PCI Express* uncorrectable link errors. **Integrated BMC Detected** 1. Critical threshold crossed – Voltage, temperature, power nozzle, power gauge, and PROCHOT (Therm Ctrl) sensors. 2. VRD Hot asserted. 3. One of the redundant power supplies failed. 4. Minimum number of fans to cool the system are not present or have failed.
Amber	Solid on	Critical, non-recoverable	Fatal alarm – system has failed or shutdown **BIOS Detected** 1. DIMM failure when there is one DIMM present and no good memory is present.[1] 2. Run-time memory uncorrectable error in non-redundant mode.[1] 3. CPU configuration error (for instance, processor stepping mismatch). **Integrated BMC Detected**

Color	State	Criticality	Description
			1. CPU CATERR signal asserted. 2. CPU 1 is missing. 3. CPU THERMTRIP. 4. System cooling fan failure. 5. No power good – redundant power fault. Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies are present).

Notes:
1. The BIOS detects these conditions and sends a *Set Fault Indication* command to the Integrated BMC to provide the contribution to the system status LED
2. Blink rate is ~ 1Hz at 50% duty cycle.

7.2.3 System Status LED – BMC Initialization

When power is first applied to the system and 5V-STBY is present, the BMC controller on the server board requires 15-20 seconds to initialize. During this time, the system status LED will be solid on, both amber and green. Once BMC initialization has completed, the status LED will stay green solid on. If power button is pressed before BMC initialization completes, the system will not boot to POST.

7.3 Front Panel Connectors

Front Panel uses 2 cables to connect with motherboard, one is 24-pin SSI control panel cable to J1C1 on motherboard, another is 10-pin 2 ports USB cable to J1E3 (USB port 8/9) on motherboard.

The pin-out for SSI control cable is as follows:

Table 51. Front Panel SSI connector pin-out

Pin	Signal Name	Pin	Signal Name
1	P3V3_STBY (Power LED Anode)	2	P3V3_STBY (Front Panel Power)
3	Key	4	P5V_STBY (ID LED Anode)
5	FP_PWR_LED_N	6	FP_ID_LED_BUF_N
7	P3V3 (HDD Activity LED Anode)	8	FP_LED_STATUS_GREEN_N
9	LED_HDD_ACTIVITY_N	10	FP_LED_STATUS_A MBER_N
11	FP_PWR_BTN_N	12	NIC3_LINK_LED_N
13	GND (Power Button GND)	14	NIC1_LINK_LED_N
15	BMC_RST_BTN_N	16	SMB_SENSOR_3V3STB_DATA
17	GND (Reset GND)	18	SMB_SENSOR_3V3STB_CLK
19	FP_ID_BTN_N	20	FP_CHASSIS_INTRU
21	NIC5_LINK_LED_N	22	NIC4_LINK_LED_N
23	FP_NMI_BTN_N	24	NIC2_LINK_LED_N

Front panel USB connector pin-out is as follows:

Table 52. Front Panel USB connector pin-out

Pin	Signal Name	Pin	Signal Name
1	NC	2	Key Pin
3	GND	4	GND
5	USB_P	6	USB_P
7	USB_N	8	USB_N
9	+5V	10	+5V

8. Configuration Jumpers

The following table provides a summary and description of configuration, test, and debug jumpers on the Intel® Server Board S3420GPRX, which is used in Intel® Server System SR1695GPRX.

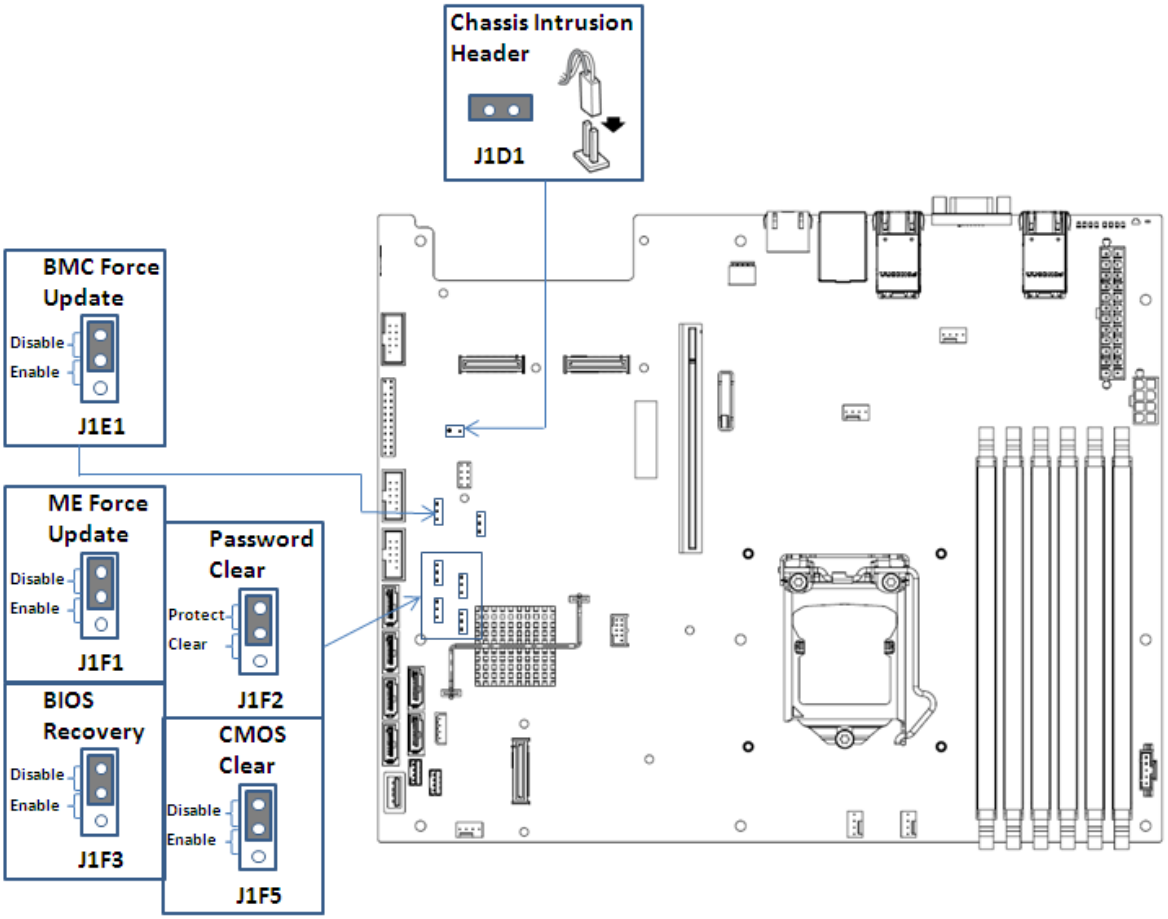


Figure 25.Jumper Locations and Functions

8.1 Force Integrated BMC Update (J1E1)

When performing a standard BMC firmware update procedure, the update utility places the BMC into an update mode, allowing the firmware to load safely onto the flash device. In the unlikely event the BMC firmware update process fails due to the BMC not being in the proper update state, the server board provides a BMC Force Update jumper (J1E1) that forces the BMC into the proper update state. You must complete the following procedure in the event the standard BMC firmware update process fails.

Table 53. Force Integrated BMC Update Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	Integrated BMC GPIO [1] is pulled HIGH. Default position.

Jumper Position	Mode of Operation	Note
2-3	Update	Integrated BMC GPIO [1] is pulled LOW.

1. Power down and remove the power cord.
2. Open the server chassis. Refer to your server chassis documentation for instructions.
3. Move the jumper from the default operating position, covering pins 1 and 2, to the enabled position, covering pins 2 and 3.
4. Close the server chassis.
5. Reconnect the power cord and power up the server.
6. Perform the BMC firmware update procedure as documented in the README.TXT file included in the given BMC firmware update package. After the successful completion of the firmware update process, the firmware update utility may generate an error stating the BMC is still in update mode.
7. Power down and remove the power cord.
8. Open the server chassis.
9. Move the jumper from the enabled position, covering pins 2 and 3 to the disabled position, covering pins 1 and 2.
10. Close the server chassis.
11. Reconnect the power cord and power up the server.

Note: Normal BMC functionality is disabled when the Force BMC Update jumper is set to the enabled position. You should never run the server with the BMC Force Update jumper set in this position. You should only use this jumper setting when the standard firmware update process fails. This jumper should remain in the default/disabled position when the server is running normally.

8.2 ME Force Update (J1F1)

When performing the standard ME force update procedure, the update utility places the ME into an update mode, allowing the ME to load safely onto the flash device. In the unlikely event ME firmware update process fails due to ME not being in the proper update state, the server board provides an Integrated BMC Force Update jumper (J1F1), which forces the ME into the proper update state. The following procedure should be completed in the event the standard ME firmware update process fails.

Table 54. Force ME Update Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	ME Firmware Force Update Mode – Disabled (Default)
2-3	Update	ME Firmware Force Update Mode – Enabled

1. Power down and remove the AC power cord.
2. Open the server chassis. For instructions, see your server chassis documentation.
3. Move jumper from the default operating position (covering pins 1 and 2) to the enabled position (covering pins 2 and 3).
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.

6. Perform the ME firmware update procedure as documented in the README.TXT file that is included in the given ME firmware update package (same package as BIOS).
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move jumper from the enabled position (covering pins 2 and 3) to the disabled position (covering pins 1 and 2).
10. Close the server chassis.

8.3 Password Clear (J1F2)

This 3-pin jumper is used to clear the BIOS password.

Table 55. BIOS Password Clear Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	These pins should have a jumper in place for normal system operation. (Default)
2-3	Clear Password	To clear administrator and user passwords, power on server with pins 2-3 connected. The passwords are cleared within 5-10 seconds. These pins should not be connected for normal operation.

8.3.1 Clearing the BIOS Password

1. Power down server. Do not unplug the power cord.
2. Open the chassis. For instructions, refer to your server chassis documentation.
3. Move the jumper (J1F2) from the default operating position, covering pins 1 and 2, to the password clear position, covering pins 2 and 3.
4. Close the server chassis.
5. Power up the server, wait 10 seconds or until POST completes.
6. Power down the server.
7. Open the chassis and move the jumper back to default position, covering pins 1 and 2.
8. Close the server chassis.
9. Power up the server. The password is now cleared and you can reset it by going into the BIOS setup. The BIOS password is now cleared.

8.4 BIOS Recovery Mode (J1F3)

The Intel® Server Board S3420GPRX uses the BIOS recovery to repair the system BIOS from flash corruption in the main BIOS and Boot Block. This 3-pin jumper is used to reload the BIOS when the image is suspected to be corrupted. For instructions on how to recover the BIOS, refer to the specific BIOS release notes.

Table 56. BIOS Recovery Mode Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	These pins should have a jumper in place for normal system operation. (Default)

Jumper Position	Mode of Operation	Note
2-3	Recovery	The main system BIOS will not boot with these pins connected, system can only boot from EFI-bootable recovery media with the recovery BIOS image.

8.5 CMOS Clear (J1F5)

This jumper used to be the CMOS Clear jumper. The BIOS has moved CMOS data to the NVRAM region of the BIOS flash since the previous generation. The BIOS checks during boot to determine if the data in the NVRAM must be set to default.

Table 57. Reset BIOS Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	These pins should have a jumper in place for normal system operation. (Default)
2-3	Reset BIOS Configuration	If these pins 2-3 are connected with AC power plugged, the CMOS settings are cleared within five seconds. These pins should not be connected for normal operation.

Clearing the CMOS

1. Power down server. Do not unplug the power cord.
2. Open the server chassis. For instructions, refer to your server chassis documentation.
3. Move the jumper (J1F5) from the default operating position, covering pins 1 and 2, to the reset/clear position, covering pins 2 and 3.
4. Wait five seconds.
5. Remove power cable.
6. Move the jumper back to default position, covering pins 1 and 2.
7. Close the server chassis.
8. Power up the server.

The CMOS settings are now cleared.

Note: Removing power before performing the CMOS Clear operation causes the system to automatically power up and immediately power down, after the procedure is followed and power is re-applied. If this happens, remove the power cord again, wait 30 seconds, and re-install the power cord. Power up system and proceed to the <F2> BIOS Setup Utility to reset the preferred settings.

8.6 Chassis Intrusion (J1D1)

This 2-pin connector is used to indicate the status of chassis top cover. In normal status, top cover is closed. These two pins are connected.
If the top cover is opened, these two pins are disconnected. And an intrusion status will be recorded by BMC.

9. PCI Riser Card and Assembly

Each Intel® Server System SR1695GPRX includes one PCI Express* riser slot that accepts one PCI Express* x16 full height or low profile adapter card. The riser also accommodates PCI Express x8, x4, and x1 adapters.

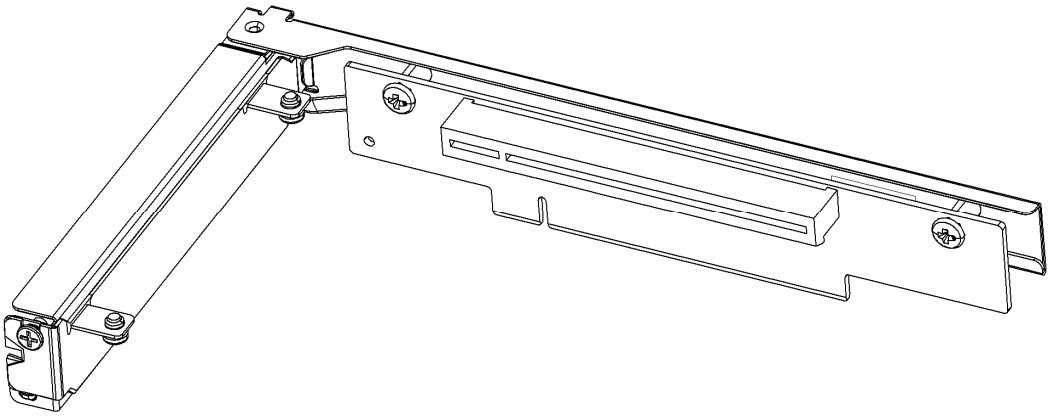


Figure 26. 1U PCI Express* Riser Card Assembly

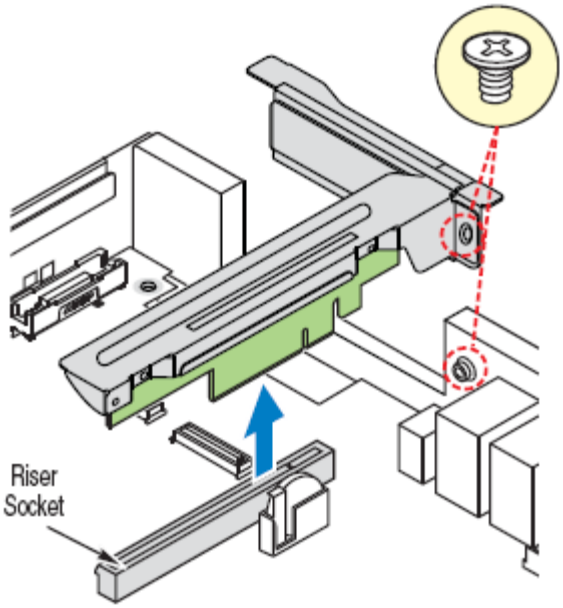


Figure 27. Intel® Server System SR1695GPRX PCI Express* Riser Installation

Note: The PCI Express* riser card is separately orderable as spare.

10. Environmental and Regulatory Specifications

10.1 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 58. System Office Environmental Summary

Parameter	Limits
Operating Temperature	+10 C to +35 C with the maximum rate of change not to exceed 10 C per hour
Non-Operating Temperature	-40 C to +70 C
Non-Operating Humidity	50%- 90%, non-condensing with a maximum wet bulb of 28 C
Acoustic noise	Sound Pressure: 55 dBA (Rackmount) in an idle state at typical office ambient temperature. (23 C +/- 2 C) Sound Power: 7.0 BA in an idle state at typical office ambient temperature. (23 +/- 2 degrees C)
Shock, operating	Half sine, 2 g peak, 11 mSec
Shock, unpackaged	Trapezoidal, 25 g, velocity change 136 inches/sec (≧40 lbs to > 80 lbs)
Shock, packaged	Non-palletized free fall in height 24 inches (≧40 lbs to > 80 lbs)
Vibration, unpackaged	5 Hz to 500 Hz, 2.20 g RMS random
Shock, operating	Half sine, 2 g peak, 11 mSec
ESD	+/-15kV except I/O port +/-8KV per Intel® Environmental test specification
System Cooling Requirement in BTU/Hr	2050 BTU/hour
EMI operating	Required to meet EMI emission requirements, tested as part of system

10.2 Serviceability and Availability

The system is designed to be serviced by qualified technical personnel only.

The desired Mean Time To Repair (MTTR) the system is 30 minutes, which includes diagnosing the system's problem. To meet this goal, the system enclosure and hardware was designed to minimize the MTTR.

The following are the maximum time a trained field service technician should take to perform the listed system maintenance procedures after diagnosing the system and identifying the failed component(s).

Table 59. Maintenance Activity Duration

Activity	Time Estimate
Remove and replace top cover	40 sec
Remove and replace hard disk drive	1 min 40 sec
Remove and replace power supply module(include cable routing)	4 min 35 sec
Remove and replace system blower/fan(each)	45 sec
Remove and replace backplane board(include cable routing)	6 min 15 sec
Remove and replace server board(include cable routing)	6 min 45 sec

10.3 Replacing the Backup Battery

The lithium battery on the server board powers the real time clock (RTC) for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

10.4 Product Regulatory Compliance

The server chassis product, when correctly integrated per this guide, complies with the following safety and electromagnetic compatibility (EMC) regulations.

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as:

medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

Notifications to Users on Product Regulatory Compliance and Maintaining Compliance – To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products/components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC compliance testing. For more information please contact your local Intel Representative. This is an FCC Class A device and its use is intended for a commercial type market place.

10.5 Use of Specified Regulated Components

To maintain the UL listing and compliance to other regulatory certifications and/or declarations, the following regulated components must be used and conditions adhered to. Interchanging or use of other component will void the UL listing and other product certifications and approvals.

Updated product information for configurations can be found on the Intel Server Builder Web site at the following URL:
http://serverconfigurator.intel.com/default.aspx

If you do not have access to Intel's Web address, please contact your local Intel representative.

Server chassis (base chassis is provided with power supply and fans) – NRTL listed.

Server board – you must use an Intel server board – UL recognized.

Add-in boards – must have a printed wiring board flammability rating of minimum UL94V-1. Add-in boards containing external power connectors and/or lithium batteries must be UL recognized or UL listed. Any add-in board containing modem telecommunication circuitry must be UL listed. In addition, the modem must have the appropriate telecommunications, safety, and EMC approvals for the region in which it is sold.

Peripheral Storage Devices – must be UL recognized or UL listed accessory and TUV or VDE licensed. Maximum power rating of any one device or combination of devices can not exceed manufacturer's specifications. Total server configuration is not to exceed the maximum loading conditions of the power supply.

The following table references Server Chassis Compliance and markings that may appear on the product. Markings below are typical markings however, may vary or be different based on how certification is obtained.

Note: Certifications Emissions requirements are to Class A.

Table 60. Product Safety and Electromagnetic (EMC) Compliance

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Australia/New Zealand	AS/NZS CISPR22 (Emissions)	 N232
Argentina	IRAM Certification (Safety)	
Canada/USA	CSA 60950-1 – UL 60950-1 (Safety) Listing	 3178574
	Industry Canada ICES-003 (Emissions)	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A
	FCC CFR 47, Part 15 (Emissions)	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept interference receive, including interference that may cause undesired operation.
CENELEC Europe Germany	Low Voltage Directive 2006/95/EC (Europe – EN60950-1); EMC Directive 2004/108/EEC EN55022 (Emissions) EN55024 (Immunity) EN61000-3-2 (Harmonics) EN61000-3-3 (Voltage Flicker) CE Declaration of Conformity GS Certification – EN60950-1	 
International	CB Certification – IEC60950-1 CISPR 22/CISPR 24	None Required
Japan	VCCI Certification	この装置は、クラスA情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。VCCI-A

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Korea	KCC Certification MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI)	인증번호: CPU-SR1695(A)
Russia	GOST-R 50377-92 Certification GOST R 29216-91 (Emissions) GOST R 50628-95 (Immunity)	MO04
Ukraine	Ukraine Certification	None Required
Taiwan	BSMI CNS13438 BSMI CNS14336	R33025 警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策

10.6 Electromagnetic Compatibility Notices

10.6.1 USA

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.

- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

10.6.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

10.6.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

10.6.4 Japan EMC Compatibility

Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

10.6.5 BSMI (Taiwan)

The BSMI Certification number and the following warning is located on the product safety label which is located on the bottom side (pedestal orientation) or side (rack mount configuration).

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

10.6.6 KCC (Korea)

Following is the KCC certification information for Korea.

인증번호: CPU-SR1695 (A)

10.7 Rack Mount Installation Guidelines

Anchor the equipment rack: The equipment rack must be anchored to an unmovable support to prevent it from falling over when one or more servers are extended in front of the rack on slides. You must also consider the weight of any other device installed in the rack. A crush hazard exists should the rack tilt forward which could cause serious injury.
Temperature: The temperature, in which the server operates when installed in an equipment rack, must not go below 5 °C (41 °F) or rise above 40 °C (104 °F). Extreme fluctuations in temperature can cause a variety of problems in your server.
Ventilation: The equipment rack must provide sufficient airflow to the front of the server to maintain proper cooling. The rack must also include ventilation sufficient to exhaust a maximum of 1023 BTUs (British Thermal Units) per hour for the server. The rack selected and the ventilation provided must be suitable to the environment in which the server will be used.

10.7.1 If AC power supplies are installed:

Mains AC power disconnection: The AC power cord(s) is considered the mains disconnect for the server and must be readily accessible when installed. If the individual server power cord(s) will not be readily accessible for disconnection then you are responsible for installing an AC power disconnect for the entire rack unit. This main disconnect must be readily accessible, and it must be labeled as controlling power to the entire rack, not just to the server(s).
Grounding the rack installation: To avoid the potential for an electrical shock hazard, you must include a third wire safety ground conductor with the rack installation. If the server

power cord is plugged into an AC outlet that is part of the rack, then you must provide proper grounding for the rack itself. If the server power cord is plugged into a wall AC outlet, the safety ground conductor in the power cord provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.
Overcurrent protection: The server is designed for an AC line voltage source with up to 20 amperes of overcurrent protection per cord feed. If the power system for the equipment rack is installed on a branch circuit with more than 20 amperes of protection, you must provide supplemental protection for the server.

10.7.2 If DC power supplies are installed:

Connection with a DC (Direct Current) source should only be performed by trained service personnel. The server with DC input is to be installed in a Restricted Access Location in accordance with articles 110-16, 110-17, and 110-18 of the National Electric Code, ANSI/NFPA 70. The DC source must be electrically isolated by double or reinforced insulation from any hazardous AC source.
Main DC power disconnect: You are responsible for installing a properly rated DC power disconnect for the server system. This mains disconnect must be readily accessible, and it must be labeled as controlling power to the server. The circuit breaker of a centralized DC power system may be used as a disconnect device when easily accessible and should be rated no more than 10 amps.
Grounding the server: To avoid the potential for an electrical shock hazard, you must reliably connect an earth grounding conductor to the server. The earth grounding conductor must be a minimum 18AWG connected to the earth ground stud(s) on the rear of the server. The safety ground conductor should be connected to the chassis stud with a Listed closed two-hole crimp terminal having 5/8 inch pitch. The nuts on the chassis earth ground studs should be installed with a 10 in/lbs torque. The safety ground conductor provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.
Overcurrent protection: Overcurrent protection circuit breakers must be provided as part of each host equipment rack and must be incorporated in the field wiring between the DC source and the server. The branch circuit protection shall be rated minimum 75Vdc, 10 A maximum per feed pair. If the DC power system for the equipment rack is installed with more than 10 amperes of protection, you must provide supplemental protection for the server.

10.8 Power Cord Usage Guidelines

Warning: *Do not attempt to modify or use a power cord set that is not the exact type required. You must use a power cord set that meets the following criteria:*

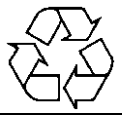
- *Rating: In the U.S. and Canada, cords must be UL (Underwriters Laboratories, Inc.) Listed/CSA (Canadian Standards Organization) Certified type SJT, 18-3 AWG (American Wire Gauge). Outside of the U.S. and Canada, cords must be flexible harmonized (<HAR>) or VDE (Verband Deutscher Electrotechniker, German Institute of Electrical Engineers) certified cord with 3 x 0.75 mm conductors rated 250 VAC (Volts Alternating Current).*
- *Connector, wall outlet end: Cords must be terminated in grounding-type male plug designed for use in your region. The connector must have certification marks showing certification by an agency acceptable in your region and for U.S. must be Listed and rated 125% of overall current rating of the server.*

• Connector, server end: The connectors that plug into the AC receptacle on the server must be an approved IEC (International Electrotechnical Commission) 320, sheet C13, type female connector.
• Cord length and flexibility: Cords must be less than 4.5 meters (14.76 feet) long.

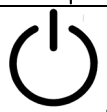
10.9 Product Ecology Compliance

Intel has a system in place to restrict the use of banned substances in accordance with world wide product ecology regulatory requirements. The following is Intel's product ecology compliance criteria.

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
California	**CA. Lithium Perchlorate insert** California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials.	Special handling may apply. See www.dtsc.ca.gov/hazardous waste/perchlorate This notice is required by California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials. This product/part includes a battery which contains Perchlorate material.
China	**China RoHS** China RoHS (MII Measure 39) Product marked with the Environmental Friendly Usage Period (EFUP) label of 20yrs, substance table in Simplified Chinese either placed with the product documentation or separate insert.	
	China Recycling (GB18455-2001) Mark requires to be applied to be retail product only. Marking applied to bulk packaging and single packages. Not applied to internal packaging such as plastics, foams, etc.	
Intel Internal Specification	All materials, parts and subassemblies must not contain restricted materials as defined in *Intel's Environmental Product Content Specification of Suppliers and Outsourced Manufacturers* – http://supplier.intel.com/ehs/environmental.htm	None Required
Europe	**European Directive 2002/95/EC** - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below. Quantity limit of 0.1% by mass (1000 PPM) for: Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE) Quantity limit of 0.01% by mass (100 PPM) for: Cadmium	None Required

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Intel Internal Specification	**ISO11469** - Plastic parts weighing >25gm are intended to be marked with per ISO11469.	>PC/ABS<
International	Recycling Markings – Fiberboard (FB) and Cardboard (CB) are marked with international recycling marks. Applied to outer bulk packaging and single package.	

10.10 Other Markings

Compliance Description	Compliance Reference	Compliance Reference Marking Example
Stand-by Power	60950 Safety Requirement Applied to product is stand-by power switch is used.	
Multiple Power Cords	60950 Safety Requirement Applied to product if more than one power cord is used.	English: This unit has more than one power supply cord. To reduce the risk of electrical shock, disconnect (2) two power supply cords before servicing.
		Simplified Chinese: 注意： 本设备包括多条电源系统电缆。为避免遭受电击，在进行维修之前应断开两（2）条电源系统电缆。
		Traditional Chinese: 注意： 本設備包括多條電源系統電纜。爲避免遭受電擊，在進行維修之前應斷開兩（2）條電源系統電纜。
		German: Dieses Geräte hat mehr als ein Stromkabel. Um eine Gefahr des elektrischen Schlages zu verringern trennen sie beide (2) Stromkabeln bevor Instandhaltung.
Ground Connection	60950 Deviation for Nordic Countries	Line1 : "WARNING:" Swedish on line2: "Apparaten skall anslutas till jordat uttag, när den ansluts till ett nätverk." Finnish on line 3: "Laite on liitettävä suojamaadoituskoskettimilla varustettuun pistorasiaan." English on line 4: "Connect only to a properly earth grounded outlet."

Compliance Description	Compliance Reference	Compliance Reference Marking Example
Country of Origin	Logistic Requirements Applied to products to indicate where product was made.	**Made in China**

Appendix A: Integration and Usage Tips

Before attempting to integrate and configure your system, you should reference this section, which provides a list of useful information.

- After the system is integrated with processors, memory, and peripheral devices, the FRUSDR utility **must** be run to load the proper Sensor Data Record data to the integrated Server Management subsystem. Failure to run this utility may prevent Server Management from accurately monitoring system health and may affect system performance. The FRUSDR utility for this server system can either be run from the Intel Deployment CDROM that came with your system, or can be downloaded from the Intel website referenced at the bottom of this page.

- To ensure the highest system reliability, make sure the latest system software is loaded on the server before deploying the system onto a live networking environment. This includes system BIOS, FRUSDR, BMC firmware, and hot-swap controller firmware. The system software can be updated using the Intel Deployment CDROM that came with your system or can be downloaded from the Intel website referenced at the bottom of this page.

- System fans are not hot-swappable.

- Only supported memory validated by Intel should be used in this server system. A list of supported memory can be found in the Intel® Server System SR1695GPRX Tested Memory List which can be downloaded from the Intel website referenced at the bottom of this page.

- This system supports the Intel® Xeon® processor 3400 and Core™ i3 sequence. You cannot use Intel® Xeon® processors not referenced on the supported processor list in this server system.

- You must use the CPU/memory air duct to maintain system thermals.

- To maintain system thermals, you must populate all hard drive bays with either a hard drive or drive blank.

- You must remove AC power from the system prior to opening the chassis for service

You can download the latest system documentation, drivers, and system software from the Intel Support website:

http://www.intel.com/p/en_US/support/highlights/server/s3420gp

Appendix B: POST Code LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, you can use the diagnostic LEDs to identify the last POST process executed.

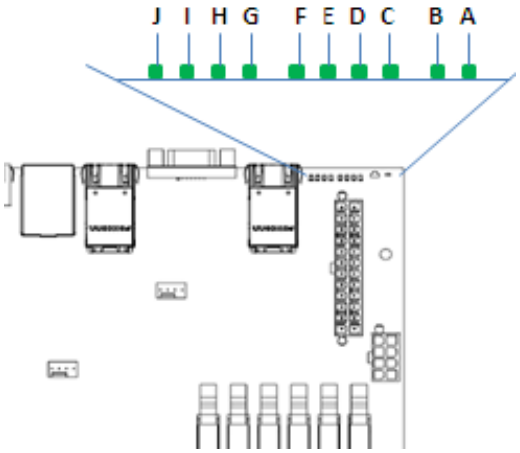


Figure 28. Diagnostic LED location

Table 61. POST Code Diagnostic LED Location

A	ID LED	B	Status LED
C	Diagnostic LED #7 MSB	G	Diagnostic LED #3
D	Diagnostic LED #6	H	Diagnostic LED #2
E	Diagnostic LED #5	I	Diagnostic LED #1
F	Diagnostic LED #4	J	Diagnostic LED #0 LSB

Each POST code is represented by the eight amber diagnostic LEDs. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by diagnostic LEDs #4, #5, #6, and #7. The lower nibble bits are represented by diagnostics LEDs #0, #1, #2, and #3. If the bit is set in the upper and lower nibbles, then the corresponding LED is lit. If the bit is clear, then the corresponding LED is off.

The diagnostic LED #7 is labeled as “MSB” (Most Significant Bit), and the diagnostic LED #0 is labeled as “LSB” (Least Significant Bit).

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 62. POST Progress Code LED Example

LEDs	Upper Nibble LEDs				Lower Nibble LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF

Results	1	0	1	0	1	1	0	0
	Ah				Ch			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 63. Dianostic LED POST Code Decoder

Checkpoint	Diagnostic LED Decoder 0 = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
Host Processor									
0x04h	X	X	X	X	X	O	X	X	Early processor initialization (flat32.asm) where system BSP is selected
0x10h	X	X	X	O	X	X	X	X	Power-on initialization of the host processor (Boot Strap Processor)
0x11h	X	X	X	O	X	X	X	O	Host processor cache initialization (including AP)
0x12h	X	X	X	O	X	X	O	X	Starting application processor initialization
0x13h	X	X	X	O	X	X	O	O	SMM initialization
Chipset									
0x21h	X	X	O	X	X	X	X	O	Initializing a chipset component
Memory									
0x22h	X	X	O	X	X	X	O	X	Reading configuration data from memory (SPD on FBDIMM)
0x23h	X	X	O	X	X	X	O	O	Detecting presence of memory
0x24h	X	X	O	X	X	O	X	X	Programming timing parameters in the memory controller
0x25h	X	X	O	X	X	O	X	O	Configuring memory parameters in the memory controller
0x26h	X	X	O	X	X	O	O	X	Optimizing memory controller settings
0x27h	X	X	O	X	X	O	O	O	Initializing memory, such as ECC init
0x28h	X	X	O	X	O	X	X	X	Testing memory
PCI Bus									
0x50h	X	O	X	O	X	X	X	X	Enumerating PCI buses
0x51h	X	O	X	O	X	X	X	O	Allocating resources to PCI buses
0x52h	X	O	X	O	X	X	O	X	Hot Plug PCI controller initialization
0x53h	X	O	X	O	X	X	O	O	Reserved for PCI bus
0x54h	X	O	X	O	X	O	X	X	Reserved for PCI bus
0x55h	X	O	X	O	X	O	X	O	Reserved for PCI bus
0x56h	X	O	X	O	X	O	O	X	Reserved for PCI bus
0x57h	X	O	X	O	X	O	O	O	Reserved for PCI bus
USB									
0x58h	X	O	X	O	O	X	X	X	Resetting USB bus
0x59h	X	O	X	O	O	X	X	O	Reserved for USB devices
ATA/ATAPI/SATA									
0x5Ah	X	O	X	O	O	X	O	X	Resetting SATA bus and all devices
0x5Bh	X	O	X	O	O	X	O	O	Detecting the presence of ATA device
0x5Ch	X	O	X	O	O	O	X	X	Enable SMART if supported by ATA device
0x5Dh	X	O	X	O	O	O	X	O	Reserved for ATA
SMBUS									
0x5Eh	X	O	X	O	O	O	O	X	Resetting SMBUS
0x5Fh	X	O	X	O	O	O	O	O	Reserved for SMBUS
Local Console									
0x70h	X	O	O	O	X	X	X	X	Resetting the video controller (VGA)
0x71h	X	O	O	O	X	X	X	O	Disabling the video controller (VGA)

Checkpoint	Diagnostic LED Decoder								Description
	0 = On, X=Off								
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0x72h	X	O	O	O	X	X	O	X	Enabling the video controller (VGA)
Remote Console									
0x78h	X	O	O	O	O	X	X	X	Resetting the console controller
0x79h	X	O	O	O	O	X	X	O	Disabling the console controller
0x7Ah	X	O	O	O	O	X	O	X	Enabling the console controller
Keyboard (only USB)									
0x90h	O	X	X	O	X	X	X	X	Resetting the keyboard
0x91h	O	X	X	O	X	X	X	O	Disabling the keyboard
0x92h	O	X	X	O	X	X	O	X	Detecting the presence of the keyboard
0x93h	O	X	X	O	X	X	O	O	Enabling the keyboard
0x94h	O	X	X	O	X	O	X	X	Clearing keyboard input buffer
0x95h	O	X	X	O	X	O	X	O	Reserved for keyboard
Mouse (only USB)									
0x98h	O	X	X	O	X	X	O	X	Resetting the mouse
0x99h	O	X	X	O	X	X	O	O	Detecting the mouse
0x9Ah	O	X	X	O	X	O	O	X	Detecting the presence of mouse
0x9Bh	O	X	X	O	X	O	O	O	Enabling the mouse
Fixed Media									
0xB0h	O	X	O	O	X	X	X	X	Resetting fixed media device
0xB1h	O	X	O	O	X	X	X	O	Disabling fixed media device
0xB2h	O	X	O	O	X	X	O	X	Detecting presence of a fixed media device (SATA hard drive detection, etc.)
0xB3h	O	X	O	O	X	X	O	O	Enabling / configuring a fixed media device
Removable Media									
0xB8h	O	X	O	O	O	X	X	X	Resetting removable media device
0xB9h	O	X	O	O	O	X	X	O	Disabling removable media device
0xBAh	O	X	O	O	O	X	O	X	Detecting presence of a removable media device (SATA CDROM detection, etc.)
0xBCh	O	X	O	O	O	O	X	X	Enabling / configuring a removable media device
Boot Device Selection (BDS)									
0xD0	O	O	X	O	X	X	X	X	Entered the Boot Device Selection phase (BDS)
0xD1	O	O	X	O	X	X	X	O	Return to last good boot device
0xD2	O	O	X	O	X	X	O	X	Setup boot device selection policy
0xD3	O	O	X	O	X	X	O	O	Connect boot device controller
0xD4	O	O	X	O	X	O	X	X	Attempt flash update boot mode
0xD5	O	O	X	O	X	O	X	O	Transfer control to EFI boot
0xD6	O	O	X	O	X	O	O	X	Trying to boot device selection
0xDF	O	O	X	O	O	O	O	O	Reserved for boot device selection
Pre-EFI Initialization (PEI) Core									
0xE0h	O	O	O	X	X	X	X	X	Entered Pre-EFI Initialization phase (PEI)
0xE1h	O	O	O	X	X	X	X	O	Started dispatching early initialization modules (PEIM)
0xE2h	O	O	O	X	X	X	O	X	Initial memory found, configured, and installed correctly
0xE3h	O	O	O	X	X	X	O	O	Transfer control to the DXE Core
Driver eXecution Environment (DXE) Core									

Checkpoint	Diagnostic LED Decoder 0 = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0xE4h	O	O	O	X	X	O	X	X	Entered EFI driver execution phase (DXE)
0xE5h	O	O	O	X	X	O	X	O	Started dispatching drivers
0xE6h	O	O	O	X	X	O	O	X	Started connecting drivers
DXE Drivers									
0xE7h	O	O	O	X	O	O	X	O	Waiting for user input
0xE8h	O	O	O	X	O	X	X	X	Checking password
0xE9h	O	O	O	X	O	X	X	O	Entering BIOS setup
0xEAh	O	O	O	X	O	O	X	X	Flash Update
0xEEh	O	O	O	X	O	O	X	X	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	O	O	O	X	O	O	X	O	Unrecoverable boot failure
Pre-EFI Initialization Module (PEIM) / Recovery									
0x30h	X	X	O	O	X	X	X	X	Crisis recovery has been initiated because of a user request
0x31h	X	X	O	O	X	X	X	O	Crisis recovery has been initiated by software (corrupt flash)
0x34h	X	X	O	O	X	O	X	X	Loading crisis recovery capsule
0x35h	X	X	O	O	X	O	X	O	Handing off control to the crisis recovery capsule
0x3Fh	X	X	O	O	O	O	O	O	Crisis recovery capsule failed integrity check of capsule descriptors
Runtime Phase / EFI Operating System Boot									
0XF2h	O	O	O	O	X	X	O	X	Signal that the OS has switched to virtual memory mode
0XF4h	O	O	O	O	X	O	X	X	Entering the sleep state
0XF5h	O	O	O	O	X	O	X	O	Exiting the sleep state
0XF8h	O	O	O	O	O	X	X	X	Operating system has requested EFI to close boot services has been cancelled.
Progress Code									
0XF9h	O	X	X	O	X	X	X	X	Resetting the keyboard
0xFAh	O	X	X	O	X	X	X	O	Disabling the keyboard

Appendix C: Video POST Code Errors

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

No Pause: The message is displayed on the local Video screen during POST or in the Error Manager. The system continues booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.

Pause: The message is displayed on the Error Manager screen, and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error, where the user can take immediate corrective action or choose to continue booting.

Halt: The message is displayed on the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

Table 64. POST Error Message and Handling

Error Code	Error Message	Response
0012	CMOS date/time not set	Pause
0048	Password check failed	Halt
0108	Keyboard component encountered a locked error	No Pause
0109	Keyboard component encountered a stuck key error	No Pause
0113	Fixed Media The SAS RAID firmware cannot run properly. The user should attempt to re-flash the firmware.	Pause
0140	PCI component encountered a PERR error	Pause
0141	PCI resource conflict	Pause
0146	PCI out of resources error	Pause
0192	L3 cache size mismatch	Halt
0194	CPUID, processor family are different	Halt
0195	Front side bus mismatch	Pause
0196	Processor model mismatch	Pause
0197	Processor speed mismatch	Pause
0198	Processor family is unsupported	Pause
019F	Processor and chipset stepping configuration is unsupported	Pause
5220	CMOS/NVRAM configuration cleared	Pause
5221	Password cleared by jumper	Pause
5224	Password clear jumper is set	Pause
8110	Processor 01 internal error (IERR) on last boot	Pause
8111	Processor 02 internal error (IERR) on last boot	Pause
8120	Processor 01 thermal trip error on last boot	Pause
8121	Processor 02 thermal trip error on last boot	Pause
8130	Processor 01 disabled	Pause
8131	Processor 02 disabled	Pause
8140	Processor 01 Failed FRB-3 Timer.	No Pause

Error Code	Error Message	Response
8141	Processor 02 Failed FRB-3 Timer.	No Pause
8160	Processor 01 unable to apply BIOS update	Pause
8161	Processor 02 unable to apply BIOS update	Pause
8170	Processor 01 failed Self Test (BIST).	Pause
8171	Processor 02 failed Self Test (BIST).	Pause
8180	Processor 01 BIOS does not support the current stepping for processor	No Pause
8181	Processor 02 BIOS does not support the current stepping for processor	No Pause
8190	Watchdog timer failed on last boot	Pause
8198	Operating system boot watchdog timer expired on last boot	Pause
8300	Integrated Baseboard Management Controller failed self-test	Pause
84F2	Integrated Baseboard Management Controller failed to respond	Pause
84F3	Integrated Baseboard Management Controller in update mode	Pause
84F4	Sensor data record empty	Pause
84FF	System event log full	No Pause
8500	Memory component could not be configured in the selected RAS mode.	Pause
8520	DIMM_A1 failed Self Test (BIST).	Pause
8521	DIMM_A2 failed Self Test (BIST).	Pause
8522	DIMM_A3 failed Self Test (BIST).	Pause
8523	DIMM_A4 failed Self Test (BIST).	Pause
8524	DIMM_B1 failed Self Test (BIST).	Pause
8525	DIMM_B2 failed Self Test (BIST).	Pause
8526	DIMM_B3 failed Self Test (BIST).	Pause
8527	DIMM_B4 failed Self Test (BIST).	Pause
8528	DIMM_C1 failed Self Test (BIST).	Pause
8529	DIMM_C2 failed Self Test (BIST).	Pause
852A	DIMM_C3 failed Self Test (BIST).	Pause
852B	DIMM_C4 failed Self Test (BIST).	Pause
852C	DIMM_D1 failed Self Test (BIST).	Pause
852D	DIMM_D2 failed Self Test (BIST).	Pause
852E	DIMM_D3 failed Self Test (BIST).	Pause
852F	DIMM_D4 failed Self Test (BIST).	Pause
8540	DIMM_A1 Disabled.	Pause
8541	DIMM_A2 Disabled.	Pause
8542	DIMM_A3 Disabled.	Pause
8543	DIMM_A4 Disabled.	Pause
8544	DIMM_B1 Disabled.	Pause
8545	DIMM_B2 Disabled.	Pause
8546	DIMM_B3 Disabled.	Pause
8547	DIMM_B4 Disabled.	Pause
8548	DIMM_C1 Disabled.	Pause
8549	DIMM_C2 Disabled.	Pause
854A	DIMM_C3 Disabled.	Pause
854B	DIMM_C4 Disabled.	Pause
854C	DIMM_D1 Disabled.	Pause
854D	DIMM_D2 Disabled.	Pause
854E	DIMM_D3 Disabled.	Pause
854F	DIMM_D4 Disabled.	Pause
8560	DIMM_A1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8561	DIMM_A2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8562	DIMM_A3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8563	DIMM_A4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8564	DIMM_B1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8565	DIMM_B2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8566	DIMM_B3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8567	DIMM_B4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8568	DIMM_C1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8569	DIMM_C2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause

Error Code	Error Message	Response
856A	DIMM_C3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856B	DIMM_C4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856C	DIMM_D1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856D	DIMM_D2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856E	DIMM_D3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856F	DIMM_D4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8580	DIMM_A1 Correctable ECC error encountered.	Pause after 10 Occurrence
8581	DIMM_A2 Correctable ECC error encountered.	Pause after 10 Occurrence
8582	DIMM_A3 Correctable ECC error encountered.	Pause after 10 Occurrence
8583	DIMM_A4 Correctable ECC error encountered.	Pause after 10 Occurrence
8584	DIMM_B1 Correctable ECC error encountered.	Pause after 10 Occurrence
8585	DIMM_B2 Correctable ECC error encountered.	Pause after 10 Occurrence
8586	DIMM_B3 Correctable ECC error encountered.	Pause after 10 Occurrence
8587	DIMM_B4 Correctable ECC error encountered.	Pause after 10 Occurrence
8588	DIMM_C1 Correctable ECC error encountered.	Pause after 10 Occurrence
8589	DIMM_C2 Correctable ECC error encountered.	Pause after 10 Occurrence
858A	DIMM_C3 Correctable ECC error encountered.	Pause after 10 Occurrence
858B	DIMM_C4 Correctable ECC error encountered.	Pause after 10 Occurrence
858C	DIMM_D1 Correctable ECC error encountered.	Pause after 10 Occurrence
858D	DIMM_D2 Correctable ECC error encountered.	Pause after 10 Occurrence
858E	DIMM_D3 Correctable ECC error encountered.	Pause after 10 Occurrence
858F	DIMM_D4 Correctable ECC error encountered.	Pause after 10 Occurrence
85A0	DIMM_A1 Uncorrectable ECC error encountered.	Pause
85A1	DIMM_A2 Uncorrectable ECC error encountered.	Pause
85A2	DIMM_A3 Uncorrectable ECC error encountered.	Pause
85A3	DIMM_A4 Uncorrectable ECC error encountered.	Pause
85A4	DIMM_B1 Uncorrectable ECC error encountered.	Pause
85A5	DIMM_B2 Uncorrectable ECC error encountered.	Pause
85A6	DIMM_B3 Uncorrectable ECC error encountered.	Pause
85A7	DIMM_B4 Uncorrectable ECC error encountered.	Pause
85A8	DIMM_C1 Uncorrectable ECC error encountered.	Pause
85A9	DIMM_C2 Uncorrectable ECC error encountered.	Pause
85AA	DIMM_C3 Uncorrectable ECC error encountered.	Pause
85AB	DIMM_C4 Uncorrectable ECC error encountered.	Pause
85AC	DIMM_D1 Uncorrectable ECC error encountered.	Pause
85AD	DIMM_D2 Uncorrectable ECC error encountered.	Pause
85AE	DIMM_D3 Uncorrectable ECC error encountered.	Pause
85AF	DIMM_D4 Uncorrectable ECC error encountered.	Pause
8601	Override jumper is set to force boot from lower alternate BIOS bank of flash ROM	No Pause
8602	WatchDog timer expired (secondary BIOS may be bad!)	No Pause
8603	Secondary BIOS checksum fail	No Pause
8604	Chipset Reclaim of non critical variables complete.	No Pause

Error Code	Error Message	Response
9000	Unspecified processor component has encountered a non specific error.	Pause
9223	Keyboard component was not detected.	No Pause
9226	Keyboard component encountered a controller error.	No Pause
9243	Mouse component was not detected.	No Pause
9246	Mouse component encountered a controller error.	No Pause
9266	Local Console component encountered a controller error.	No Pause
9268	Local Console component encountered an output error.	No Pause
9269	Local Console component encountered a resource conflict error.	No Pause
9286	Remote Console component encountered a controller error.	No Pause
9287	Remote Console component encountered an input error.	No Pause
9288	Remote Console component encountered an output error.	No Pause
92A3	Serial port component was not detected	Pause
92A9	Serial port component encountered a resource conflict error	Pause
92C6	Serial Port controller error	No Pause
92C7	Serial Port component encountered an input error.	No Pause
92C8	Serial Port component encountered an output error.	No Pause
94C6	LPC component encountered a controller error.	No Pause
94C9	LPC component encountered a resource conflict error.	Pause
9506	ATA/ATPI component encountered a controller error.	No Pause
95A6	PCI component encountered a controller error.	No Pause
95A7	PCI component encountered a read error.	No Pause
95A8	PCI component encountered a write error.	No Pause
9609	Unspecified software component encountered a start error.	No Pause
9641	PEI Core component encountered a load error.	No Pause
9667	PEI module component encountered an illegal software state error.	Halt
9687	DXE core component encountered an illegal software state error.	Halt
96A7	DXE boot services driver component encountered an illegal software state error.	Halt
96AB	DXE boot services driver component encountered invalid configuration.	No Pause
96E7	SMM driver component encountered an illegal software state error.	Halt
0xA022	Processor component encountered a mismatch error.	Pause
0xA027	Processor component encountered a low voltage error.	No Pause
0xA028	Processor component encountered a high voltage error.	No Pause
0xA421	PCI component encountered a SERR error.	Halt
0xA500	ATA/ATPI ATA bus SMART not supported.	No Pause
0xA501	ATA/ATPI ATA SMART is disabled.	No Pause
0xA5A0	PCI Express* component encountered a PERR error.	No Pause
0xA5A1	PCI Express* component encountered a SERR error.	Halt
0xA5A4	PCI Express* IBIST error.	Pause
0xA6A0	DXE boot services driver Not enough memory available to shadow a legacy option ROM.	No Pause

POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on POST Progress LEDs.

Table 65. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error	Multiple	System halted because a fatal error related to the memory was detected.

USB Device Beeps When POST

Intel® Server Boards of the S3420 family are designed to indicate USB readiness by a series of beep codes early during POST, just before video becomes available. These 4-5 beeps mean that USB is powered and initialized, in order for USB devices such as keyboard and mouse to become operational.

If a USB device such as a pen drive or USB CD/DVD ROM drive is attached to any external USB port, a beep code means that the device is recognized, powered and initialized. Each USB port will issue a beep once an external device is ready for use.

These beep codes do not signal any errors, they are by design to advise the user of USB readiness during POST and when attaching external devices.

This USB Beep is OS Independent

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
Byte	8-bit quantity.
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.)
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2-E	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
FMB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I^2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
INTR	Interrupt

Term	Definition
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ms	milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware.)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
RMM3	Remote Management Module – 3rd generation
RMM3 NIC	Remote Management Module – 3rd generation dedicated management NIC
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board.)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory

Term	Definition
SEL	System Event Log
SIO	Server Input/Output
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt.)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
SSI	Server System Infrastructure
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinate
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity
ZIF	Zero Insertion Force

Reference Documents

Refer to the following documents for additional information:

Intel® Server Board S3420GPRX Technical Product Specification

Intel® Server System SR1630GPRX and SR1630HGPRX Technical Product Specification

Intel® Server System SR1695GPRX Service Guide