Intel® Server System R1304BTSSFAN
Intel® Server System R1304BTLSFAN
Intel® Server System R1304BTLSHBN

Technical Product Specification

Intel order number G17455-007

Revision 2.3

April, 2013

Enterprise Platforms and Services Division – Marketing

Revision History

Date	Revision Number	Modifications
September 2010	0.1	Initial release.
November 2010	0.5	Updated the hardware info.
January 2011	0.7	Updated S1200BTS info.
March 2011	1.0	Updated Regulatory info.
May 2011	1.1	▪ Updated Chassis Dimensions info. ▪ Updated Operation Temperature info.
January 2012	2.0	▪ Updated System Feature Set table. ▪ Added a note in chapter 1.
October 2012	2.1	▪ Updated Disclaimers. ▪ Updated description of System Feature Set. ▪ Added the caution for rack rails. ▪ Added the disclaimer note for system level environment limits.
February 2013	2.2	Updated the description of Peripherals.
April, 2013	2.3	Updated the Video part of System Feature Set table.

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1. Introduction

The Intel® Server Systems R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN are 1U server systems.

- The Intel® Server System R1304BTSSFAN supports up to four fixed Serial ATA (SATA) hard disk drives. The Intel® Server System R1304BTSSFAN includes the Intel® Server Board S1200BTS.
- The Intel® Server System R1304BTLSFAN supports up to four fixed Serial ATA (SATA) hard disk drives. The Intel® Server System R1304BTLSFAN includes the Intel® Server Board S1200BTL.
- The Intel® Server System R1304BTLSHBN supports up to four hot-swappable SATA disk drives and includes the Intel® Server Board S1200BTL.
- The server boards and the server systems have features designed to support the high-density server market. This chapter provides a high-level overview of the system features. Subsequent chapters provide greater detail for each major system component or feature.

Note: The products with the product codes of R1304BTLSFAN, R1304BTSSFAN, and R1304BTLSHBN can only support Intel®Xeon® E3-1200 processor, the 2nd Generation Intel® Core™ i3 Processor. The products with the product codes of R1304BTLSFANR and R1304BTSSFANR or R1304BTLSHBNR can only support Intel® Xeon® E3-1200 processor, the 2nd Generation Intel® Core™ i3 Processor, Intel® Xeon® E3-1200 V2 processor, or the 3rd Generation Intel® Core™ i3 Processor.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Product Overview
- Chapter 3 – 250W Power Sub-system
- Chapter 4 – 350W Power Sub-system
- Chapter 5 – Cooling Sub-system
- Chapter 6 – Peripheral and Hard Drive Support
- Chapter 7 – Front Control Panel
- Chapter 8 – PCI Riser Cards and Assembly
- Chapter 9 – Intel® Server System R1304BTLSHBN Passive SAS/SATA Hot-swap Backplane
- Chapter 10 – Supported Intel® Server Boards
- Chapter 11 – Environmental Specifications
- Appendix A – Integration and Usage Tips
- Appendix B – Integrated BMC Sensor Tables
- Appendix C – POST Code Diagnostic LED Decoder
- Appendix D – Post Error Beep Codes

- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards contain a number of high-density VLSI (Very Large Scale Integration) and power delivery components that need adequate airflow to cool. Intel® ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system meets the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel® developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The Intel® Server System R1304BTLSFAN and R1304BTLSHBN are both of 1U server system designed to support the Intel® Server Board S1200BTL. The Intel® Server System R1304BTSSFAN is 1U server system designed to support the Intel® Server Board S1200BTS. Intel® Server Board S1200BTL, Intel® Server Board S1200BTS and the systems have features designed to support the entry-level market. This chapter provides a high-level overview of the system features. The following chapters provide greater detail for each major system component or feature:

Table 1. System Feature Set

Feature	Description
Server Board	Intel® Server System R1304BTLSFAN/R1304BTLSHBN: ▪ Intel® Server Board S1200BTL Intel® Server System R1304BTSSFAN: ▪ Intel® Server Board S1200BTS
Processors	Support for one Intel® Xeon® E3-1200 processor, Intel® Xeon® E3-1200 V2 processor, the 2nd Generation Intel® Core™ i3 Processor or the 3rd Generation Intel® Core™ i3 Processor in FC-LGA 1155 socket package ▪ 5.0 GT/s point-to-point DMI interface to PCH ▪ LGA 1155 pin socket ▪ TDP 95W
Memory	Two memory channels: ▪ Up to two UDIMMs per channel ▪ 32 GB maximum with x8 ECC UDIMM (2 Gb DRAM)
Chipset	Intel® Server Board S1200BTL: ▪ Support for Intel® C204 Platform Controller Hub (PCH) ▪ Server Engines* LLC Pilot III BMC controller (Integrated BMC) Intel® Server Board S1200BTS: ▪ Support for Intel® C202 Platform Controller Hub (PCH)
I/O	Intel® Server System R1304BTLSFAN/R1304BTLSHBN: External connections: ▪ DB-15 video connector ▪ DB-9 serial Port A connector ▪ Four USB ports on two USB/LAN combo connectors at rear of board ▪ Two USB ports on front panel Internal connections: ▪ Two USB 2x5 pin headers, each supporting two USB 2.0 ports ▪ One 2x5 Serial Port B headers ▪ One SATA RAID key connector ▪ Two 6Gb/s SATA ports and four 3Gb/s SATA ports ▪ One SAS mezzanine slot for optional SAS module ▪ One TPM module connector ▪ One RMM4 module connector Intel® Server System R1304BTSSFAN: External connections: ▪ DB-15 video connector

Feature	Description
	▪ DB-9 serial Port A connector ▪ Four USB ports on two USB/LAN combo connectors at rear of board ▪ Two USB ports on front panel Internal connections: ▪ One USB 2x5 pin headers, supporting two USB 2.0 ports ▪ One SATA RAID key connector ▪ Six 3Gb/s SATA ports
Video	Intel® Server System R1304BTLSFAN/R1304BTLSHBN: ▪ Onboard ServerEngines* LLC Pilot II BMC Controller ▪ Integrated 2D Video Controller ▪ External DDR3 800MHz memory which has 8MB (or above) for graphic display Intel® Server System R1304BTSSFAN: ▪ Silicon Motion SM712GX04LF02-BA
LAN	One Gigabit Ethernet device 82574L connect to PCI-E x1 interfaces on the PCH. One Gigabit Ethernet PHY 82579 connected to PCH through PCI-E x1 interface
Expansion Capabilities	One x8 PCI Express* PCI riser slot capable of supporting a low-profile PCI Express* add-in card.
Hard Drive Options	Four SATA drives
Peripherals	Slimline bay for slimline SATA optical drive One PCI Express* x8 Add-in Card slot
Control Panel	Standard control panel
LEDS and displays	LEDs with standard control panel: ▪ NIC1 Activity ▪ NIC2 Activity ▪ Power/Sleep ▪ System Status ▪ Hard Drive Activity
Power supply	Intel® Server System R1304BTLSFAN/R1304BTSSFAN: ▪ Single 250-W power supply Intel® Server System R1304BTLSHBN: ▪ Single 350-W power supply
Fans	Three non-redundant, variable-speed system cooling fans
Server Management	Intel® Server System R1304BTLSFAN/R1304BTLSHBN: Onboard LLC Pilot III Controller (iBMC) ▪ Integrated Baseboard Management Controller (Integrated BMC), IPMI 2.0 compliant ▪ Integrated 2D video controller on PCI-E x1 ▪ Optional Intel® Remote Management Module 4 (RMM4) lite and optional dedicated NIC module.
Security	Intel® TPM module connector

2.1 System Views

Figure 1. Intel® Server System R1304BTSSFAN/R1304BTLSFAN

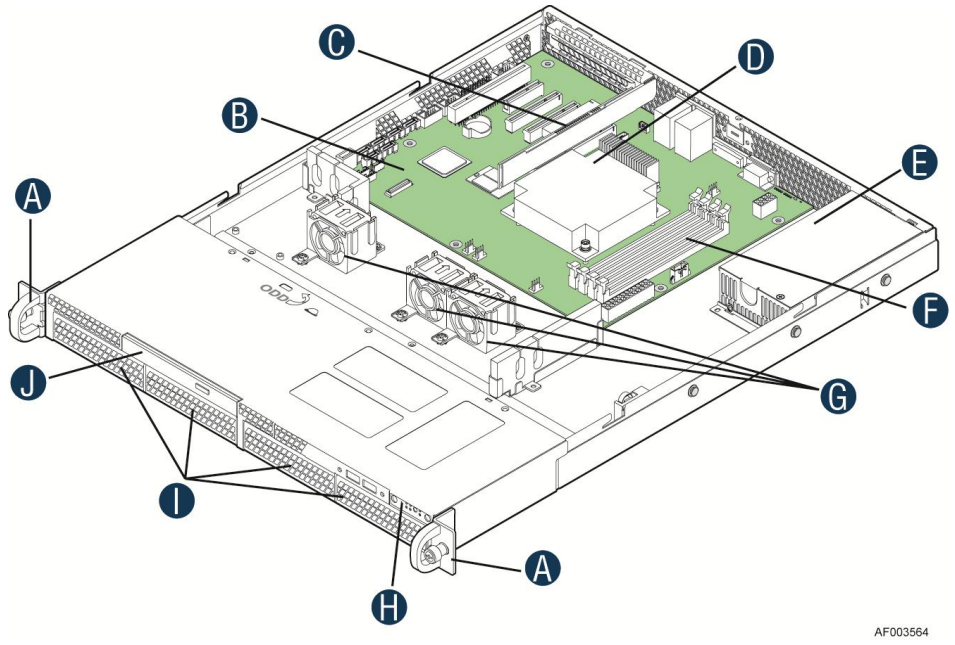
Figure 2. Intel® Server System R1304BTLSHBN

2.2 Chassis Dimensions

Table 2. Intel® Server System R1304BTSSFAN/R1304BTLSFAN/R1304BTLSHBN Dimensions

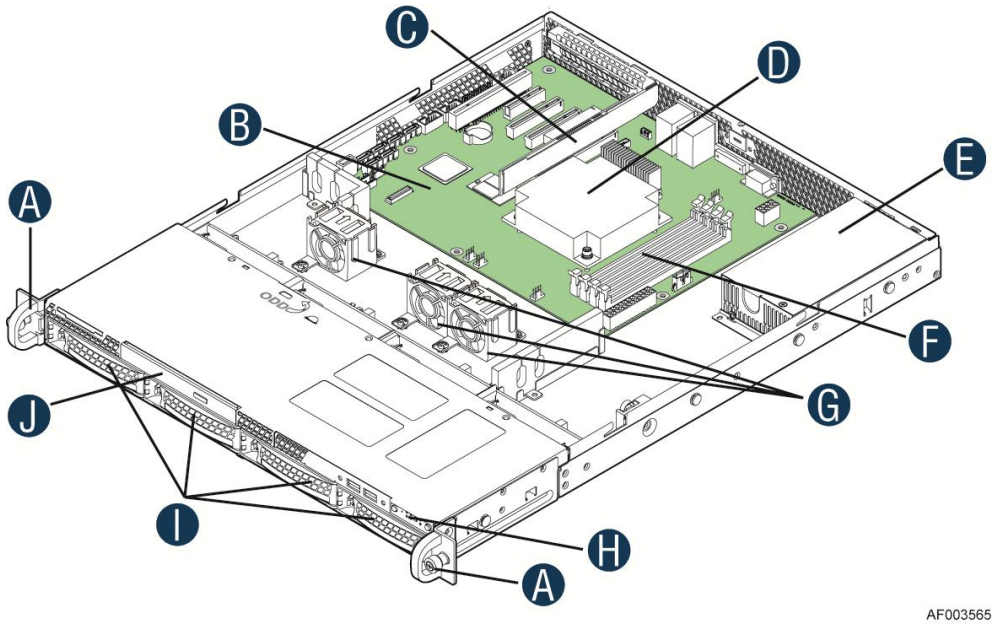
Height	1.67 inches (4.24 centimeters)
Width	17.25inches (43.82 centimeters)
Depth	21.8 inches (55.37 centimeters)

2.3 System Components



A	Rack handles (two)	F	System Memory DIMM slots
B	Server Board	G	Cooling Fans
C	PCIe Riser Assembly	H	Front Panel
D	Processor and heatsink	I	Hard Drive Bays
E	Power supply	J	Front Panel Slimline optical drive

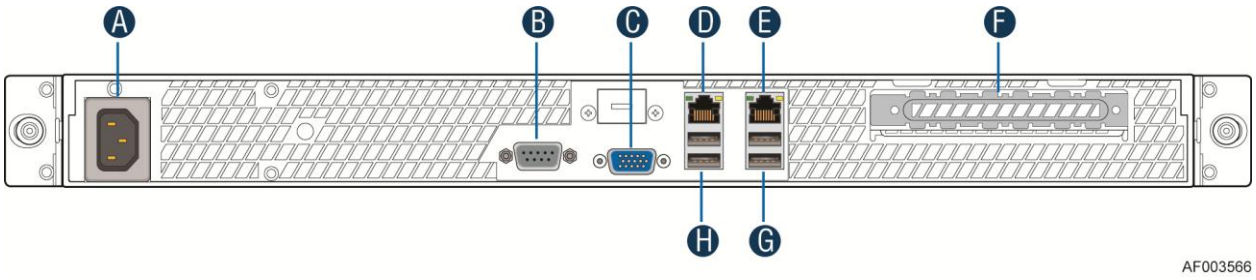
Figure 3. Intel® Server System R1304BTSSFAN/R1304BTLSFAN Major System Components



A	Rack handles (two)	F	System Memory DIMM slots
B	Server Board	G	Cooling Fans
C	PCIe Riser Assembly	H	Front Panel Board
D	Processor and Heatsink	I	Hard Drive Bays
E	Power supply	J	Slimline optical drive

Figure 4. Intel® Server System R1304BTLSHBN Major System Components

The I/O connector locations on the back of the system are pre-cut, so an I/O shield is not required. The EMI gasket is pre-installed to maintain electromagnetic interference (EMI) compliance levels. The layout arrangement is the same for both the fixed and hot-swap systems.



A	AC Power Connector	E	NIC 2 Connector (10/100/1000 Mb)
B	Serial Port A	F	PCI Express* Slot
C	Video Connector	G	USB Ports
D	NIC 1 Connector (10/100/1000 Mb)	H	USB Ports

Figure 5. Intel® Server System R1304BTSSFAN/R1304BTLSFAN/R1304BTLSHBN Back Panel Features

2.4 System Boards

The Intel® Server Systems R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN include system boards used as internal interconnects and provide feature accessibility. The following section provides a brief description for each:

2.4.1 Intel® Server System R1304BTSSFAN

The Intel® Server System R1304BTSSFAN includes an Intel® Server Board S1200BTS. This board supports a PCI Express* riser card.

- PCI Express* Riser Card – Supports a single, low-profile x8 PCI Express* riser card.

2.4.2 Intel® Server System R1304BTLSFAN

The Intel® Server System R1304BTLSFAN includes an Intel® Server Board S1200BTL. This board supports a PCI Express* riser card.

- PCI Express* Riser Card – Supports a single, low-profile x8 PCI Express* riser card.

2.4.3 Intel® Server System R1304BTLSHBN

The Intel® Server System R1304BTLSHBN includes an Intel® Server Board S1200BTL. This board supports one riser card options. The Intel® Server System R1304BTLSHBN supports a hot-swap SATA/SAS back plane with four SATA/SAS drives.

- PCI Express* Riser Card –Supports a single, low-profile x8 PCI Express* riser card.

2.5 System Cooling

The Intel® Server System R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN provide three, non-redundant system cooling fans. When external ambient temperatures remain within specified limits, the cooling system provides sufficient air flow for all drive configurations, processors, supported memory, and add-in cards.

2.6 Rack and Cabinet Mounting Options

The server systems were designed to support 19-inches wide by up to 30-inches deep server cabinets. The server systems support the following rack mount option:

Slide rail kit (Product order code – AXXVRAIL): Designed to mount the chassis into a standard (19-inch by up to 30-inch deep) EIA-310D compatible server cabinet.

CAUTION: THE MAXIMUM RECOMMENDED SERVER WEIGHT FOR THE RACK RAILS CAN BE FOUND at http://www.intel.com/support/motherboards/server/sb/CS-033655.htm. EXCEEDING THE MAXIMUM RECOMMENDED WEIGHT OR MISALIGNMENT OF THE SERVER MAY RESULT IN FAILURE OF THE RACK RAILS HOLDING THE SERVER. Use of a mechanical assist to install and align server into the rack rails is recommended.

3. 250W Power Sub-system

The power subsystem of the server systems consists of a single, non-redundant 250-W power supply with five outputs: 3.3 V, 5 V, 12 V, -12V, and 5 VSB. The form factor fits into a 1U system and provides a wire harness output to the system. An IEC connector is provided on the external face for AC input to the power supply. The power supply provides one; non-redundant 40 mm fan for self -cooling. The power supply fans also provide additional airflow for parts of the system.

The power supply operates within the following voltage ranges and ratings:

Table 3. Input Voltage Range

Parameter	Min	Rated	Max	Max Input AC Current
Line Voltage (110)	90Vrms	100-127 Vrms	140Vrms	6 Arms[1]
Line Voltage (220)	180Vrms	200-240 Vrms	264Vrms	3 Arms[2]
Frequency	47 Hz	50/60Hz	63 Hz	

Notes:

1. Maximum input current at low input voltage range should be measured at 90Vac, at maximum load.
2. Maximum input current at high input voltage range should be measured at 180VAC, at maximum load.

The power supply must operate within all specified limits over the following input voltage ranges shown in the table. Harmonic distortion of up to 10% Total Harmonic Distortion (THD) must not cause the power supply to go out of specified limits.

3.1 Mechanical Specifications

The 1U 250W power supply is designed specifically for use in the Intel® Server Systems R1304BTSSFAN and R1304BTLSFAN. The physical size of the power supply enclosure is intended to accommodate power ranges from 250 W. The power supply size is 40 mm x 81.5 mm x 150 mm and has a wire harness for the DC outputs. The AC input plugs directly into the external face of the power supply; refer to the following figure for more information:

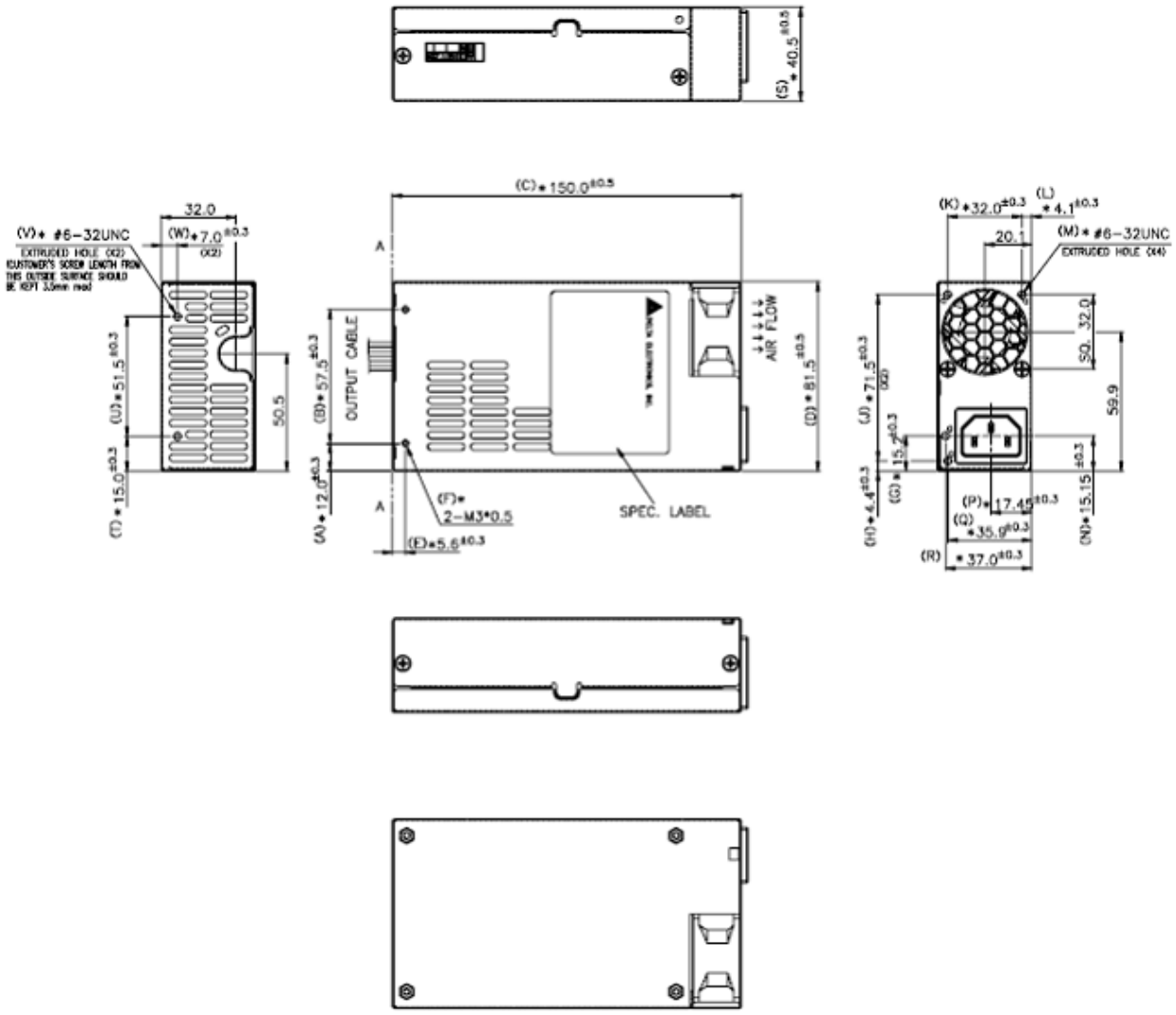


Figure 6. Power Supply Enclosure Drawing

Note: All dimensions are in millimeter.

3.2 Output Connectors

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 80°C, 300 VDC (Volts Direct Current) should be used for all output wiring.

Table 4. Intel® 250W PSU Cable Lengths

From	Length (mm)	To connector #	Description
Power Supply cover exit hole	230	P1	Baseboard Power Connector
Power Supply cover exit hole	220	P2	Processor Power Connector
Power Supply cover exit hole	440	P7	SATA Drive Power Connector
Power Supply cover exit hole	600	P3	Mini SATA Drive Power Connector
P7	185	P6	SATA Drive Power Connector
P6	185	P5	SATA Drive Power Connector
P5	185	P4	SATA Drive Power Connector

3.2.1 Baseboard power connector (P1)

Connector housing: 24-Pin Molex* Mini-Fit Jr. 39-01-2200 or equivalent.
Contact: Molex* Mini-Fit, HCS, female, crimp 44476-1111 or equivalent approved by Intel®.

Table 5. P1 Main Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1*	+3.3VDC	Orange	11	+3.3VDC	Orange
	3.3V S	Orange (24AWG)	12	-12VDC	Blue
2	+3.3VDC	Orange	13	GND	Black
3	GND	Black	14	PSON#	Green (24AWG)
4	+5VDC	Red	15*	GND	Black
5	GND	Black		COMRS	Black (24AWG)
6	+5VDC	Red	16	GND	Black
7	GND	Black	17	GND	Black
8	PWR OK	Gray	18	Reserved	N.C.
9	5 VSB	Purple	19	+5VDC	Red
10*	+12V	Yellow	20*	+5VDC	Red
	12VRS	Yellow/White (24AWG)		5VRS	Red/White (24AWG)

Notes:
1. Remote Sense wire double-crimped.
2. P1 add cable bend requirement at P1.

3.2.2 Processor Power Connector (P2)

Connector housing: 8-Pin Molex* 39-01-2085 or equivalent.
Contact: 44476-1111 or equivalent.

Table 6. P2 Processor Power Connector

Pin	Signal	20 AWG color	Pin	Signal	20 AWG Color
1	COM	Black	5	+12V	Yellow
2	COM	Black	6	+12V	Yellow

Pin	Signal	20 AWG color	Pin	Signal	20 AWG Color
3	COM	Black	7	+12V	Yellow
4	COM	Black	8	+12V	Yellow

3.2.3 SATA Hard Drive Power Connectors (P4, P5, P6, P7)

Connector housing: JWT* A3811H00-5P (94V2) or equivalent.
Contact: JWT* A3811TOP-0D or equivalent.

Table 7. SATA Power Connector

Pin	Signal	18 AWG Color
1	+3.3V	Orange
2	GND	Black
3	+5VDC	Red
4	GND	Black
5	+12V	Yellow

3.2.4 Mini SATA Hard Drive Power Connectors (P3)

Connector housing: AMPHENDOL* SSATA-111-1201-1-3 or equivalent.

Table 8. SATA Power Connector

Pin	Signal	18 AWG Color
1	N/C	N/C
2	+5V	Red
3	+5V	Red
4	N/C	N/C
5	GND	Black
6	GND	Black

3.3 AC Inlet Connector

The AC input connector should be an IEC 320 C-14 power inlet. This inlet is rated for 10A/250 VAC.

3.3.1 AC Power Cord Specification Requirements

The AC power cord must meet the following specification requirements:

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105ºC
Amperage Rating	13 A
Voltage Rating	125 V

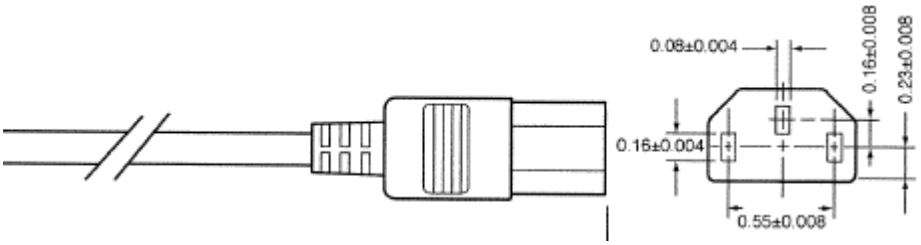


Figure 7. AC Power Cord Specifications

3.4 Marking and Identification

The power supply module marking supports the following requirements: safety agency requirements, government requirements (if required, for example, point of manufacturing), power supply vendor requirements, and Intel® manufacturing and field support requirements.

3.5 Efficiency

The power supply should have a recommended efficiency of 85% at maximum load and over the specified AC voltage.

3.6 AC Input Voltage

The power supply must operate within all specified limits over the following input voltage ranges, shown in the following table:

Table 9. AC Input Rating

Parameter	Min	Rated	Max	Max Input AC Current
Line Voltage (110)	90Vrms	100-127 Vrms	140Vrms	6 Arms1
Line Voltage (220)	180Vrms	200-240 Vrms	264Vrms	3 Arms2
Frequency	47 Hz	50/60Hz	63 Hz	

Notes:
1. Maximum input current at low input voltage range should be measured at 90 VAC at maximum load.
2. Maximum input current at high input voltage range should be measured at 180 VAC at maximum load.

3.7 Output Power/Currents

The following tables define two power and current ratings for this 350-W power supply. The combined output power of all outputs should not exceed the rated output power. The power supply must meet both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 10. Load Ratings

Voltage	Minimum	Maximum	Output Power
+3.3 V	0.1 A	6 A	19.8 W
+5 V	0.1 A	12 A	60 W

Voltage	Minimum	Maximum	Output Power
+12 V	0.75 A	17 A	204 W
-12 V	0 A	0.5 A	6 W
+5 VSB	0.05 A	2.0 A	10 W

Notes:
1. The total output for this PSU is 250W.
2. The total output of +3.3V and +5V will not exceed 60W
3. Peak power shall be 300W for 10sec. The peak 12V current shall be 1sec.

3.8 Protection Circuits

Protection circuits inside the power supply should cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec min (with +5VSB/0.1A) and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

3.8.1 Over Current Protection (OCP)

Each output shall have individual OCP protection circuits. The PSU shall shutdown and latch off after an over current condition occurs. Whereas OCP of +5VSB shall turn the power supply into "hiccup mode" until the OCP condition removed. The values are measured at the PSU harness connectors and shall not be damaged from repeated power cycling in this condition. There shall be current sensors and limit circuits to shut down the entire power supply if the limit is exceeded. The limits are listed in the following table:

Table 11. Over Load Protection (OCP) Limits

Output Voltage	Continuous Load	
	Current Limit MIN	Current Limit MAX
+12V	23A	25A
+5V	14.4 A	25A
+3.3V	15A	30A
-12V		4A
+5VSB		4.5A

3.8.2 Over Voltage Protection (OVP)

Each output shall have individual OVP protection circuits built in and it shall be locally sensed. The PSU shall shutdown and latch off after an over voltage condition occurs. The output voltages are measured at the harness connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the output harness connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the connector.

Table 12. Over Voltage Protection (OVP) Limits

Output Voltage	OVP MIN (V)	OVP MAX (V)
+3.3V	3.7	4.5
+5V	5.6	6.5
+12V	13.3	15.6

Output Voltage	OVP MIN (V)	OVP MAX (V)
-12V	-13.3	-15.6
+5VSB	5.6	6.5

3.8.3 Over Temperature Protection (OTP)

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops within specified limits, the power supply shall restore power automatically, while the +5VSB remains always on. The OTP trip level shall have a minimum of 4°C of ambient temperature hysteresis, so that the power supply will not oscillate on and off due to temperature recovery condition.

4. 350W Power Sub-system

The power subsystem of the server systems consists of a single, non-redundant 350-W power supply with five outputs: 3.3 V, 5 V, 12 V, -12V, and 5 VSB. The form factor fits into a 1U system and provides a wire harness output to the system. An IEC connector is provided on the external face for AC input to the power supply. The power supply provides one; non-redundant 40 mm fan for self-cooling. The power supply fans also provide additional airflow for parts of the system.

The power supply operates within the following voltage ranges and ratings:

Table 13. Input Voltage Range

Parameter	Min	Rated	Max	Max Input AC Current
Line Voltage (110)	$90V_{rms}$	100-127 V_{rms}	$140V_{rms}$	6 A_{rms} [1]
Line Voltage (220)	$180V_{rms}$	200-240 V_{rms}	$264V_{rms}$	3 A_{rms} [2]
Frequency	47 Hz	50/60Hz	63 Hz	

Notes:
1. Maximum input current at low input voltage range shall be measured at 90Vac, at maximum load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at maximum load.

The power supply must operate within all specified limits over the following input voltage ranges shown in the table. Harmonic distortion of up to 10% Total Harmonic Distortion (THD) must not cause the power supply to go out of specified limits.

4.1 Mechanical Specifications

The 1U 350 W power supply is designed specifically for use in the Intel® Server Systems R1304BTLSHBN. The physical size of the power supply enclosure is intended to accommodate power ranges from 350 W. The power supply size is 40 mm x 81.5mm x 150 mm and has a wire harness for the DC outputs. The AC input plugs directly into the external face of the power supply; refer to the following figure for more information.

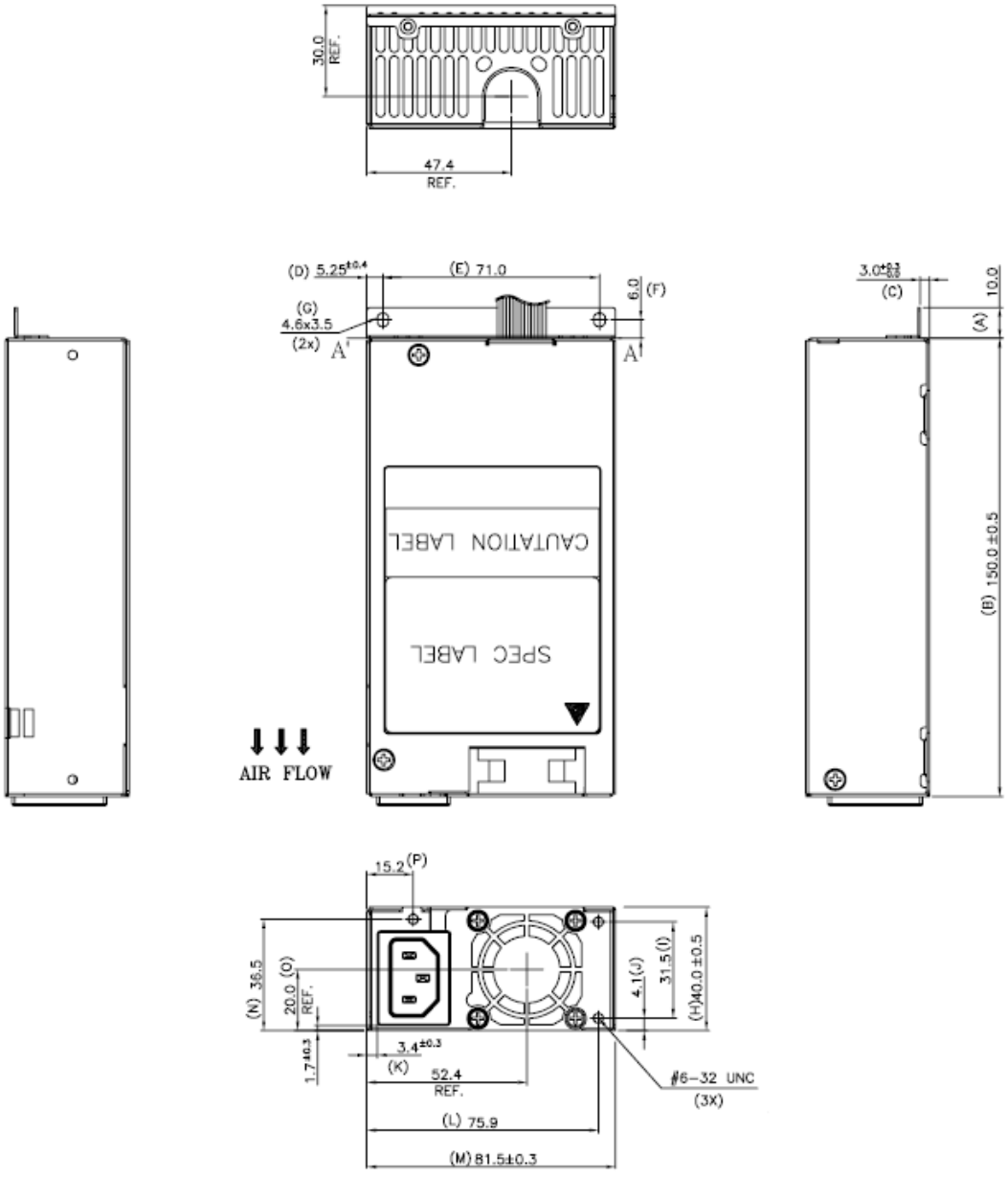


Figure 8. Power Supply Enclosure Drawing

Note: All dimensions are in millimeter.

4.2 Output Connectors

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 80°C, 300 VDC should be used for all output wiring.

Table 14. 350W PSU Cable Lengths

From	Length (mm)	To connector #	Description
Power Supply cover exit hole	230	P1	Baseboard Power Connector
Power Supply cover exit hole	220	P2	Processor Power Connector
Power Supply cover exit hole	150	P3	AUX Power Connector
Power Supply cover exit hole	340	P7	2 x 4 HSBP Power Connector
P7	100	P5	SATA Drive Power Connector
P5	145	P4	SATA Drive Power Connector
Power Supply cover exit hole	600	P8	Mini SATA Drive Power Connector

4.2.1 Baseboard power connector (P1)

Connector housing: 24-Pin Molex* Mini-Fit Jr. 39-01-2200 or equivalent.

Contact: Molex* Mini-Fit, HCS, female, crimp 44476-1111 or equivalent approved by Intel®.

Table 15. P1 Main Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1*	+3.3VDC	Orange	11	+3.3VDC	Orange
	3.3V S	Orange (24AWG)	12	-12VDC	Blue
2	+3.3VDC	Orange	13	GND	Black
3	GND	Black	14	PSON#	Green (24AWG)
4	+5VDC	Red	15*	GND	Black
5	GND	Black		COMRS	Black (24AWG)
6	+5VDC	Red	16	GND	Black
7	GND	Black	17	GND	Black
8	PWR OK	Gray	18	Reserved	N.C.
9	5 VSB	Purple	19	+5VDC	Red
10*	+12V	Yellow	20*	+5VDC	Red
	12VRS	Yellow/White (24AWG)		5VRS	Red/White (24AWG)

Notes:
1. Remote Sense wire double-crimped.
2. P1 add cable bend requirement at P1.

4.2.2 Processor Power Connector (P2)

Connector housing: 8-Pin Molex* 39-01-2085 or equivalent.

Contact: 44476-1111 or equivalent.

Table 16. P2 Processor Power Connector

Pin	Signal	20 AWG color	Pin	Signal	20 AWG Color
1	COM	Black	5	+12V	Yellow
2	COM	Black	6	+12V	Yellow
3	COM	Black	7	+12V	Yellow
4	COM	Black	8	+12V	Yellow

4.2.3 SATA Hard Drive Power Connectors (P4, P5)

Connector housing: JWT* A3811H00-5P (94V2) or equivalent.

Contact: JWT* A3811TOP-0D or equivalent.

Table 17. SATA Power Connector

Pin	Signal	18 AWG Color
1	+3.3V	Orange
2	GND	Black
3	+5VDC	Red
4	GND	Black
5	+12V	Yellow

4.2.4 Mini SATA Hard Drive Power Connectors (P8)

Connector housing: AMPHENDOL* SSATA-111-1201-1-3 or equivalent.

Table 18. SATA Power Connector

Pin	Signal	18 AWG Color
1	N/C	N/C
2	+5V	Red
3	+5V	Red
4	N/C	N/C
5	GND	Black
6	GND	Black

4.2.5 AUX Power Connector (P3)

The AUX Power Connector is used for the Power Management Bus - PMBus*.

Connector housing: Molex* 50-57-9705 or equivalent.

Contact: Molex* 16-02-0087 or equivalent.

Table 19. AUX Power Connector

Pin	Signal	24 AWG Color	Pin	Signal	24 AWG Color
1	SCL	White/Green	4	COM	White/Black
2	SDA	White/Yellow	5	+3.3V	White/Brown
3	N/C	N/C			

4.2.6 Hot-swap Backplane Power Connector (P7)

Connector housing: Molex* 39-01-2085 or equivalent.

Contact: Molex* 39-00-0079 or equivalent.

Table 20. P7 HSBP Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	GND	Black	5	12V	Yellow
2	GND	Black	6	NC	NC
3	+5V	Red	7	NC	NC
4	NC	NC	8	3.3V	Orange

4.3 AC Inlet Connector

The AC input connector should be an IEC 320 C-14 power inlet. This inlet is rated for 10A/250 VAC.

4.3.1 AC Power Cord Specification Requirements

The AC power cord must meet the following specification requirements:

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105ºC
Amperage Rating	13 A
Voltage Rating	125 V

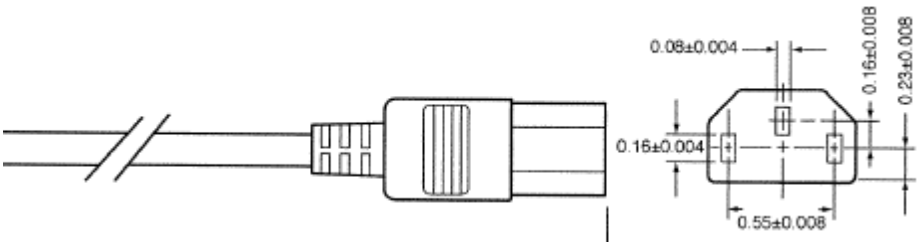


Figure 9. AC Power Cord Specifications

4.4 Marking and Identification

The power supply module marking supports the following requirements: safety agency requirements, government requirements (if required, for example, point of manufacturing), power supply vendor requirements, and Intel® manufacturing and field support requirements.

4.5 Efficiency

The power supply should have a recommended efficiency of 85% at maximum load and over the specified AC voltage.

4.6 AC Input Voltage

The power supply must operate within all specified limits over the following input voltage ranges, shown in the following table:

Table 21. AC Input Rating

Parameter	Min.	Rated	Max.	Max. Input AC Current
Line Voltage (110)	90Vrms	100-127 Vrms	140Vrms	6 Arms1
Line Voltage (220)	180Vrms	200-240 Vrms	264Vrms	3 Arms2
Frequency	47 Hz	50/60Hz	63 Hz	

Notes:

1. Maximum input current at low input voltage range should be measured at 90 VAC at maximum load.
2. Maximum input current at high input voltage range should be measured at 180 VAC at maximum load.

4.7 Output Power/Currents

The following tables define two power and current ratings for this 350W power supply. The combined output power of all outputs should not exceed the rated output power. The power supply must meet both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 22. Load Ratings

Voltage	Minimum	Maximum	Output Power
+3.3 V	0.1 A	10 A	33W
+5 V	0.1 A	16 A	80W
+12 V1	0.75 A	18 A	216W
+12 V2	0.75 A	18 A	216W
-12 V	0 A	0.5 A	6W
+5 VSB	0.05 A	2.5 A	12.5W

Notes:

1. The total current of +12V1/2 will not exceed 28A.
2. The total output for this PSU is 350W.
3. The total output of +3.3V and +5V will not exceed 100W.

4.8 Protection Circuits

Protection circuits inside the power supply should cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec min (with +5VSB/0.1A) and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

4.8.1 Over Current Protection (OCP)

Each output shall have individual OCP protection circuits. The PSU shall shutdown and latch off after an over current condition occurs. Whereas OCP of +5VSB shall turn the power supply into "hiccup mode" until the OCP condition removed. The values are measured at the PSU harness connectors and shall not be damaged from repeated power cycling in this condition. There shall be current sensors and limit circuits to shut down the entire power supply if the limit is exceeded. The limits are listed in the following table:

Table 23. Over Load Protection (OCP) Limits

Output Voltage	Continuous Load	
	Current Limit Min.	Current Limit Max.
+12V1	18.2A	20A
+12V2	18.2A	20A
+5V	19.2A	24A
+3.3V	12A	15A
-12V		4A
+5VSB		4.5A

4.8.2 Over Voltage Protection (OVP)

Each output shall have individual OVP protection circuits built in and it shall be locally sensed. The PSU shall shutdown and latch off after an over voltage condition occurs. The output voltages are measured at the harness connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the output harness connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the connector.

Table 24. Over Voltage Protection (OVP) Limits

Output Voltage	OVP Min. (V)	OVP Max. (V)
+3.3V	3.7	4.5
+5V	5.7	6.5
+12V1/+12V2	13.3	15.6
-12V	-13.3	-15.6
+5VSB	5.7	6.5

4.8.3 Over Temperature Protection (OTP)

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition, the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the +5VSB remains always on. The OTP trip level shall have a minimum of 4°C of ambient temperature hysteresis, so that the power supply will not oscillate on and off due to temperature recovery condition.

4.9 PMBus*

The PMBus* features included in this specification are requirements for ac/dc silver box power supply for use in server systems. This specification is based on the *PMBus* Specifications Parts I and II, revision 1.1X3*.

4.9.1 Related Documents

- *PMBus* Power System Management Protocol Specification Part I – General Requirements, Transport and Electrical Interface, Revision 1.1X3.*
- *PMBus* Power System Management Protocol Specification Part II – Command Language, Revision 1.1X3 SMBus* 2.0.*

4.9.2 Addressing

The power supply device address locations are shown below. For redundant systems, there are two signals to set the address location of the power supply once it is installed in the system; Address0 and Address1. For non-redundant systems, the power supply device address locations should align with the Address0/Address1 location of 0/0.

Table 25. Power Supply Device Address Locations

PDB addressing Address0/Address1	0/0	0/1	1/0	1/1
Power supply PMBus* device	B0h	B2h	B4h	B6h

Note: Non-redundant power supplies use the 0/0 address locations.

5. Cooling Sub-system

The Intel® Server System R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN cooling subsystem consists of three fans, CPU air duct, and PS/electronics bay isolation air baffle. These components provide the necessary cooling and airflow to the system. A fan on the processor heatsink is not needed.

To maintain the necessary airflow within the system, the air duct, and the top cover must be properly installed.

Note: The Intel® Server Systems R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN do not support redundant cooling. If a fan fails, the system should be powered down as soon as possible to replace the failed fan blower. The system fans are not hot-swappable.

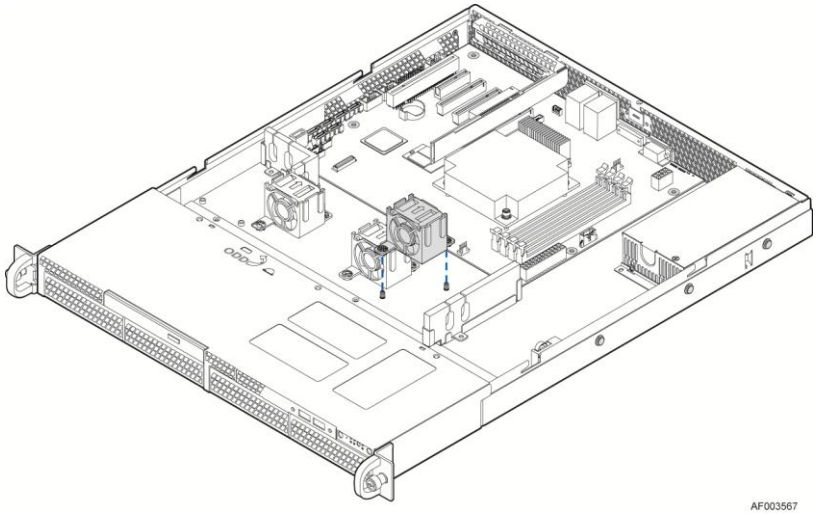


Figure 10. Intel® Server System R1304BTSSFAN/R1304BTLSFAN Fan Module Assembly

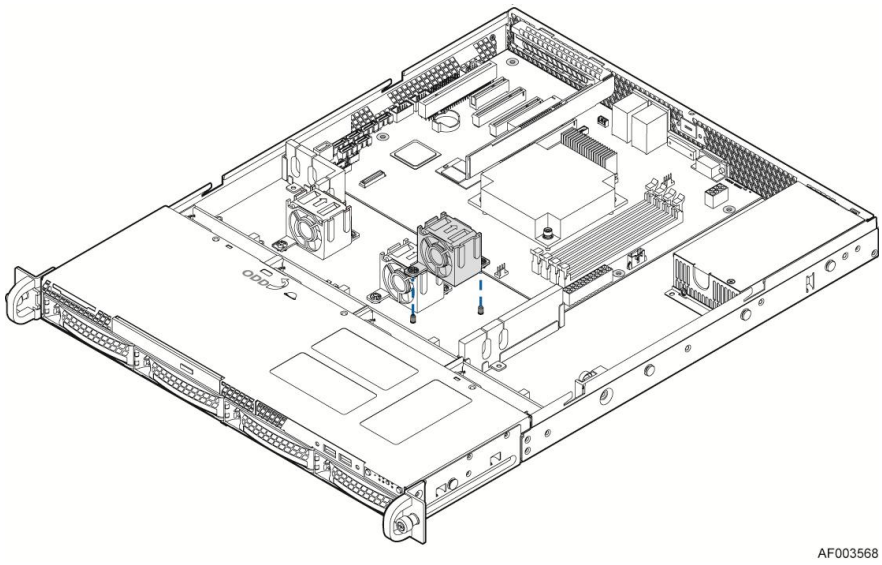


Figure 11. Intel® Server System R1304BTLSHBN Fan Module Assembly

5.1 Power Supply Fans

The power supply supports one, non-redundant 40 mm fans. It is responsible for the cooling of the power supply.

5.2 CPU Air Duct

The chassis requires the use of a CPU air duct to direct airflow through the processor's heatsink and memory area.

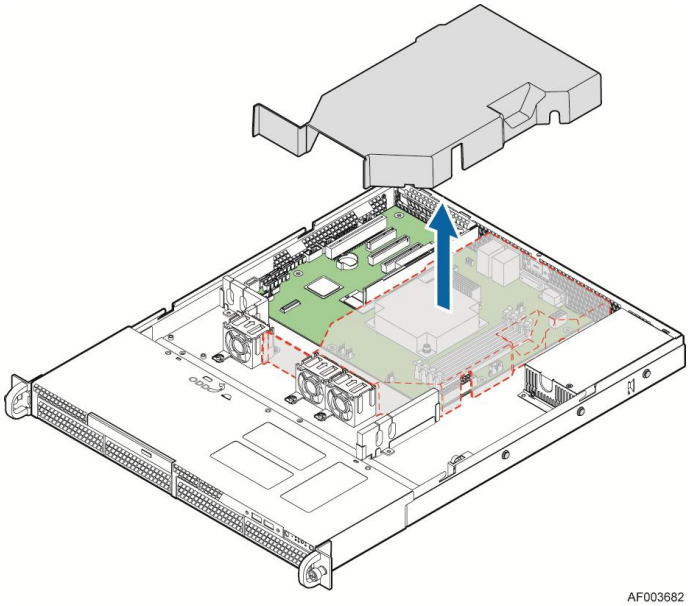


Figure 12. Intel® Server System R1304BTSSFAN/R1304BTLSFAN Air Duct

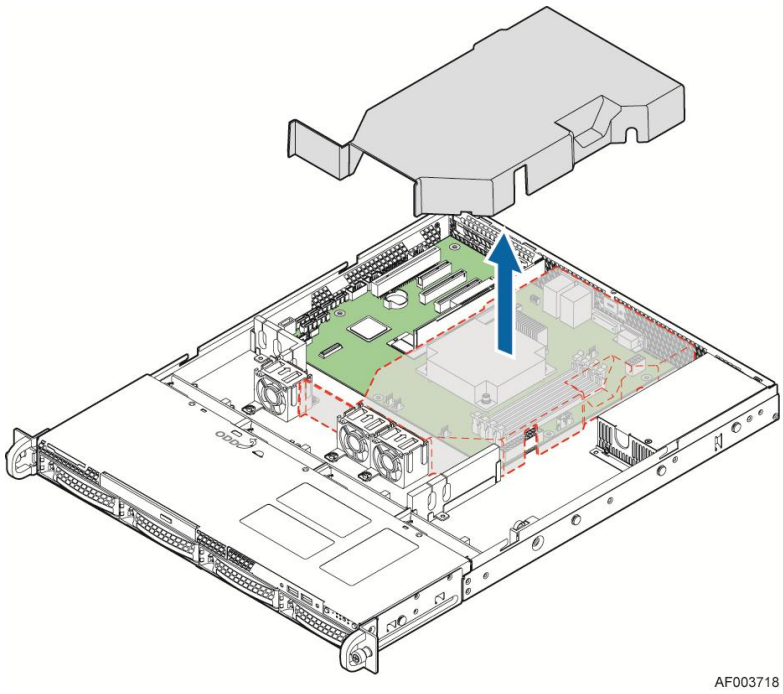
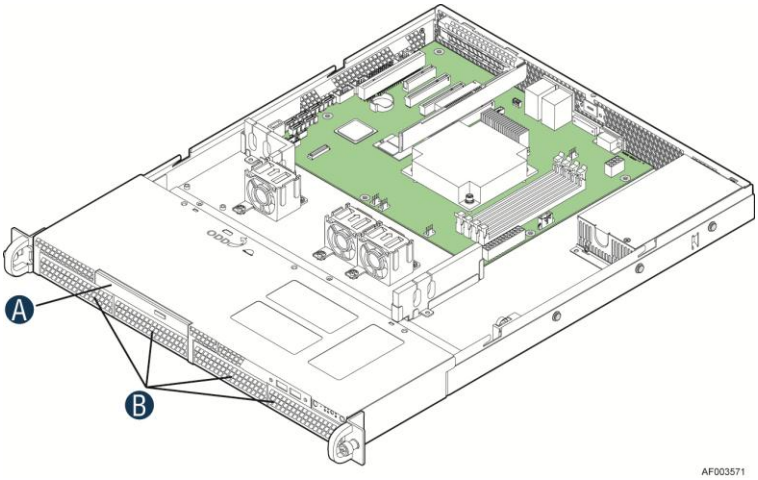


Figure 13. Intel® Server System R1304BTLSHBN Air Duct

6. Peripheral and Hard Drive Support

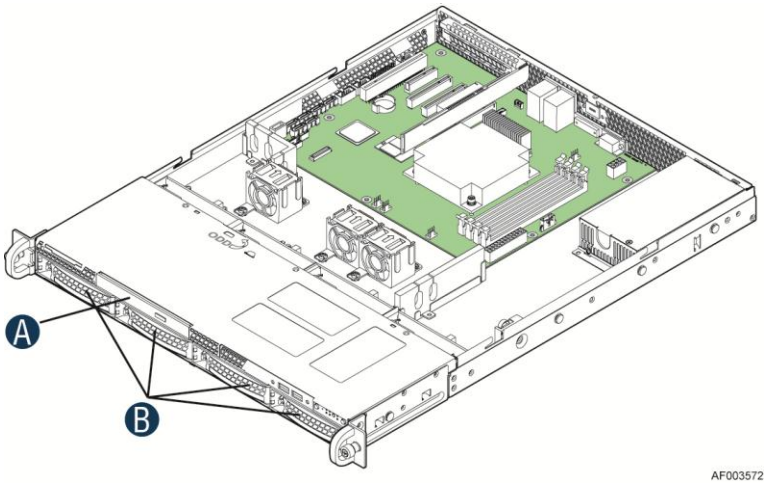
The Intel® Server Systems R1304BTSSFAN/R1304BTLSFAN provides support for four fixed hard drive bays and one slimline peripheral drive bay at the front of the chassis. The fixed hard drive bays are designed to support SATA drives only.



A	Slimline optical drive bay
B	Hard drive bays

Figure 14. Intel® Server Systems R1304BTSSFAN/R1304BTLSFAN Drive Bays

The Intel® Server System R1304BTLSHBN provides support for four hot-swap hard drive bays and one slimline peripheral drive bay at the front of the system. The hot-swap drive bays are designed to support SATA/SAS drives.



A	Slimline optical drive bay
B	Hot-swap Drive Bays

Figure 15. Intel® Server Systems R1304BTLSHBN Drive Bays

6.1 Optical Drive Support

Both the fixed and hot-swap systems provide a slimline drive bay that you can configure for an SATA optical CD-ROM or DVD/CDR drive. The slimline devices are not hot-swappable.

6.1.1 Optical Drive Support

The server systems support a slimline SATA optical drive.

6.2 Hard Disk Drive Support

The Intel® Server System R1304BTSSFAN/R1304BTLSFAN supports up to four, 3.5-inch by 1-inch fixed SATA hard disk drives. The drives are mounted inside the chassis and are not hot-swappable. The Intel® Server System R1304BTLSHBN supports up to four SATA hard disk drives mounted in hot-swappable drive carriers.

6.2.1 System Fan Connectors

The Intel® Server Systems R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN support three system cooling fans. The following table provides the pin-out for each connector:

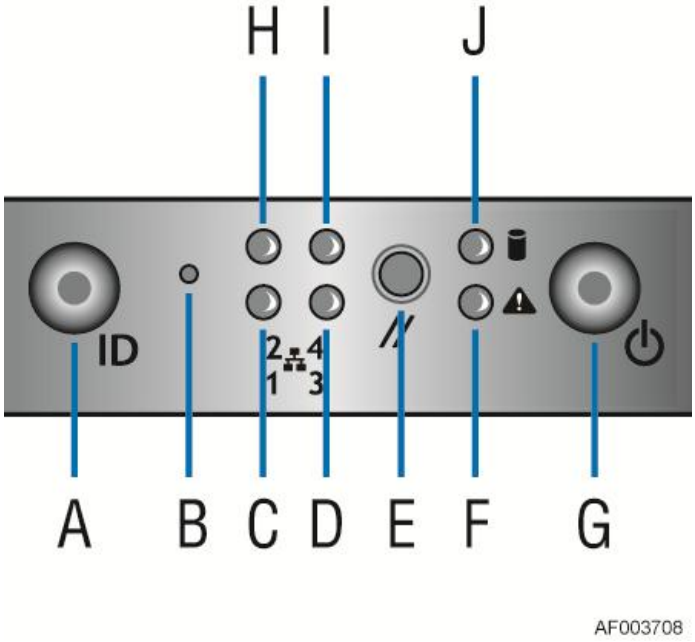
Table 26. System Four-pin Fan Headers Pin-outs

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Fan Power
3	Fan Tach	Out	FAN_TACH signal is connected to the Heceta* to monitor the FAN speed
4	PWM	Control	Pulse Width Modulation – Fan Speed Control signal

7. Front Control Panel

The standard control panel supports a power button, status LED, hard drive activity LED, and NIC 1 and NIC 2 activity LEDs. The control panel assembly comes pre-assembled into the chassis. The control panel assembly module slides into a predefined slot on the front of the chassis. Once installed, communication to the server board is achieved through a standard 24-pin cable connected directly to the server board.

Note: The LAN3/4 LEDs are not used on the Intel® Server Systems R1304BTSSFAN, R1304BTLSFAN, or R1304BTLSHBN. Unstuffable ID Button with ID LED and Status/Fault LED are not used on Intel® Server System R1304BTSSFAN.



A. Unstuffable ID Button with ID LED	F. Status/Fault LED
B. NMI Button	G. Power Button with power LED
C. LAN1 LED	H. LAN2 LED
D. LAN3 LED	I. LAN4 LED
E. Reset Button	J. HDD LED

Figure 16. Intel® Server System R1304BTSSFAN/R1304BTLSFAN/R1304BTLSHBN Front Control Panel

Table 27. Control Panel LED Functions

LED	Color	State	Description
NIC1/NIC2 Activity	Green	On	NIC Link/no access
	Green	Blink	LAN access
Power/Sleep (on standby power)	Green	On	Power on
		Blink	Sleep/ACPI S1 state
	Off	Off	Power Off/ACPI S4 state
System Status (on standby power)	N/A	N/A	N/A
Disk Activity	Green	Random blink	HDD access
	Off	Off	No hard disk activity

7.1.1 Power/Sleep LED

Table 28. SSI Power LED Operation

State	Power Mode	LED	Description
Power Off	Non-ACPI	Off	System power is off, and the BIOS have not initialized the chipset.
Power On	Non-ACPI	On	System power is on, but the BIOS have not yet initialized the chipset.
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off, and the operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink 1	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

Note: The blink rate is ~ 1 Hz at 50% duty cycle.

7.1.2 System Status LED

The system status LED is available on the Intel® Server Systems R1304BTLSFAN and R1304BTLSHBN.

7.1.3 Drive Activity LED

The drive activity LED on the front panel indicates drive activity from the onboard hard disk controllers.

8. PCI Riser Cards and Assembly

The Intel® Server System R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN provides one PCI Express* x8 slot which supports one riser card with one riser card slot. The riser card supports one low-profile PCI Express* x8 add-in card.

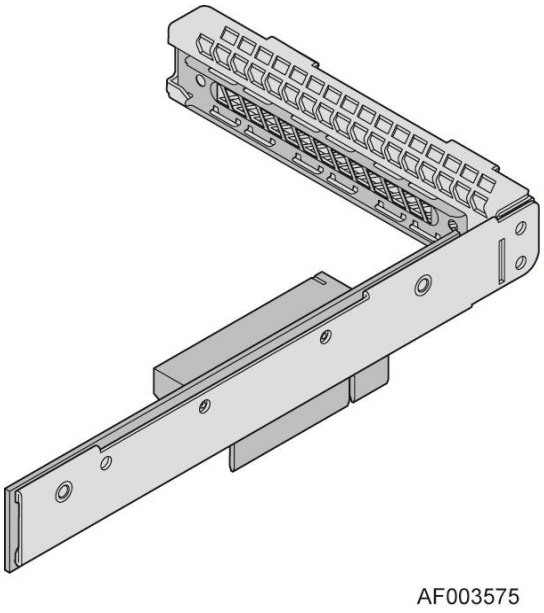


Figure 17. PCI–E Riser Card Assembly for Intel® Server System R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN

9. Intel® Server System R1304BTLSHBN Passive SAS/SATA Hot-swap Backplane

The Intel® Server System R1304BTLSHBN supports a passive backplane designed to be compatible with the Intel® Server Board S1200BTL. The Intel® Server Board S1200BTL is connected directly to the SATA backplane (default) or you can connect the backplane to an add-in SAS or SATA adapter.

The system supports a multi-functional SATA/SAS backplane with the following features:

- Four SATA/SAS compatible hot-swap hard drive connectors
- Four SATA/SAS connectors to the baseboard
- Hard Drive Activity LED for each hard drive connector
- One 2x4-pin power connector

The Intel® Server Board S1200BTL on-board SATA controller supports the following RAID arrays:

- Intel® Embedded Server RAID Technology II – RAID 0, 1, and 10.
- Intel® Matrix Storage Technology - RAID 0, 1, 10, or 5 (Microsoft Windows* only)

This system support drive status LEDs, You can determine a failed drive and drive rebuild activity by observing the drive activity LED.

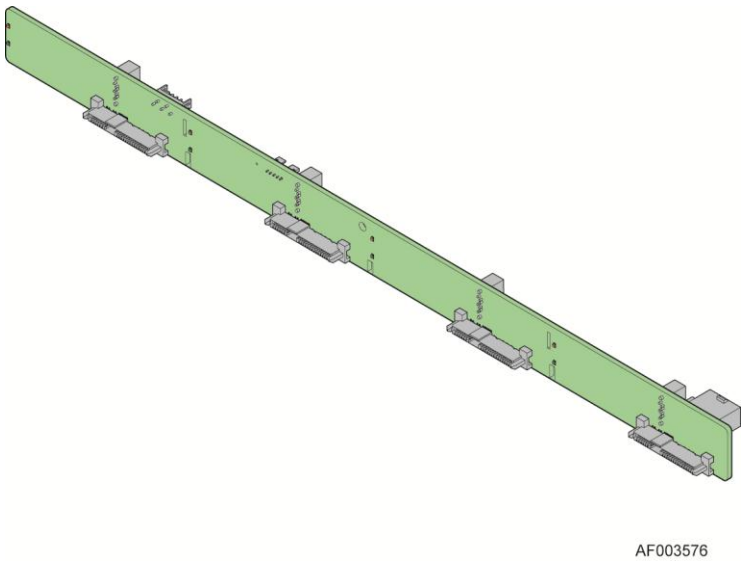


Figure 18. Intel® Server System R1304BTLSHBN Hot-swap Backplane

Table 29. Passive SATA/SAS Backplane Power Connector Pin-out

Pin #	Signal Name
1	Ground
2	Ground
3	P5V
4	P5V
5	P12V
6	P12V
7	No Connection
8	P3V3

Table 30. Passive SATA/SAS Backplane Connector to Hard Drive Pin-out

Pin #	Signal Name
S1	Ground
S2	SAS_DRVxA_RX_P
S3	SAS_DRVxA_RX_N
S4	Ground
S5	SAS_DRVxA_TX_N
S6	SAS_DRVxA_TX_P
S7	Ground
P1	TP
P2	TP
P3	TP
P4	Ground
P5	Ground
P6	Ground
P7	P5V_DRVx_PRECHG
P8	P5V
P9	P5V
P10	Ground
P11	LED_DRVx_READY_N
P12	Ground
P13	P12V_DRVx_PRECHG
P14	P12V
P15	P12V

9.1.1 Hot-swap Drive Trays

You must mount each hard drive to a hot-swap drive tray, making insertion and extraction of the drive from the system very simple. Each drive tray has its own dual-purpose latching mechanism, which is used to both insert/extract drives from the system and lock the tray in place. Each drive tray supports a light pipe providing a drive activity indicator, located on the backplane, which is viewable from the front of the system.

10. Supported Intel® Server Boards

The Intel® Server Systems R1304BTSSFAN, R1304BTLSFAN, and R1304BTLSHBN are mechanically and functionally designed to support the Intel® Server Board S1200BT family. For detailed server board information, refer to the *Intel® Server Board S1200BT Technical Product Specification*.

11. Environmental Specifications

11.1 System Level Environmental Limits

The following table defines the system-level operating and non-operating environmental limits:

Table 31. System Environmental Limits Summary

Parameter	Limits
Operating Temperature	+10°C to +35°C with the maximum rate of change not to exceed 10°C per hour
Non-Operating Temperature	-40°C to +70°C
Non-Operating Humidity	90%, non-condensing at 35°C
Acoustic noise	Sound Power: 7.0 BA in an idle state at typical office ambient temperature. (23 +/- 2°C)
Shock, operating	Half sine, 2g peak, 11 msec
Shock, unpackaged	Trapezoidal, 25g, velocity change 136 inches/sec (≧40 lbs to > 80 lbs)
Shock, packaged	Non-palletized free fall in height 24 inches (≧40 lbs to > 80 lbs)
Vibration, unpackaged	5 Hz to 500 Hz, 2.20 g RMS random
Shock, operating	Half sine, 2 g peak, 11 mSec
ESD	+/-12kV for air discharge and 8K for contact
System Cooling Requirement in BTU/Hr	1660 BTU/hour

Disclaimer Note: Intel® ensures the unpackaged server board and system meet the shock requirement mentioned above through its own chassis development and system configuration. It is the responsibility of the system integrator to determine the proper shock level of the board and system if the system integrator chooses different system configuration or different chassis. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

Appendix A: Integration and Usage Tips

- When adding or removing components or peripherals from the server board, AC power must be removed. With AC power plugged into the server board, 5-Volt standby is still present, even though the server board is powered off.
- When updating BIOS and BMC, AC power must be on.
- Supports only Intel® Xeon® Processor E3-1200 Series with 95W and less Thermal Design Power (TDP). Does not support previous generations of the Intel® Xeon® processor.
- On the back edge of the server board are diagnostic LEDs that display a sequence of amber POST codes during the boot process. If the server board hangs during POST, the LEDs display the last POST event run before the hang.
- Supports only unbuffered DDR3 ECC DIMMs (UDIMMs). Does not support the mixing of RDIMMs and UDIMMs.
- The Intel® Remote Management Module 4 (Intel® RMM4) lite connector is not compatible with the Intel® Remote Management Module (Product Order Code - AXXRMM), Intel® Remote Management Module 2 (Product Order Code - AXXRMM2) or Intel® Remote Management Module 3 (Product Order Code – AXXRMM3).
- Clear the CMOS with the AC power cord plugged in. Removing the AC power before performing the CMOS clear operation causes the system to automatically power up and immediately power down after the CMOS clear procedure is followed and AC power is re-applied. If this happens, remove the AC power cord, wait 30 seconds, and then re-connect the AC power cord. Power up the system and proceed to the <F2> BIOS Setup utility to reset the needed settings.
- Normal Integrated BMC functionality is disabled with the force Integrated BMC update jumper set to the “enabled” position (pins 2-3). The server should never be run with the Integrated BMC force update jumper set in this position and should only be used when the standard firmware update process fails. This jumper should remain in the default (disabled) position (pins 1-2) when the server is running normally.
- When performing a normal BIOS update procedure, the BIOS recovery jumper must be set to its default position (pins 1-2).

Appendix B: Integrated BMC Sensor Tables

Intel® Server Board S1200BTL implements the below sensors:

Sensor Type Codes

Sensor table given below lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion, and de-assertion information, and a brief description of the sensor purpose. Refer to the *Intelligent Platform Management Interface Specification, Version 2.0* for sensor and event/reading-type table information.

- **Sensor Type**

  The sensor type references the values in the Sensor Type Codes table in the *Intelligent Platform Management Interface Specification Second Generation v2.0*. It provides a context to interpret the sensor.

- **Event/Reading Type**

  The event/reading type references values from the Event/Reading Type Code Ranges and the Generic Event/Reading Type Code tables in the *Intelligent Platform Management Interface Specification Second Generation v2.0*. Digital sensors are specific type of discrete sensors that only have two states.

- **Event Thresholds/Triggers**

  The following event thresholds are supported for threshold type sensors:

  [u,l] [nr,c,nc] upper non-recoverable, upper critical, upper non-critical, lower non-recoverable, lower critical, and lower non-critical

  [uc, lc] upper critical and lower critical

  Event triggers are supported event-generating offsets for discrete type sensors. The offsets can be found in the Generic Event/Reading Type Code or Sensor Type Code tables in the *Intelligent Platform Management Interface Specification Second Generation v2.0*, depending on whether the sensor event/reading type is generic or a sensor-specific response.

- **Assertion/De-assertion**

  Assertion and de-assertion indicators reveal the type of events this sensor generates:

  As: Assertion

  De: De-assertion

- **Readable Value/Offsets**

  Readable value indicates the type of value returned for threshold and other non-discrete type sensors.

  Readable offsets indicate the offsets for discrete sensors that are readable by means of the *Get Sensor Reading* command. Unless otherwise indicated, event triggers are readable. Readable offsets consist of the reading type offsets that do not generate events.

- **Event Data**

  Event data is the data that is included in an event message generated by the associated sensor. For threshold-based sensors, these abbreviations are used:

  R: Reading value

  T: Threshold value

- **Rearm Sensors**

  The rearm is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used in the comment column to describe a sensor:

  A: Auto-rearm

  M: Manual rearm

  I: Rearm by init agent

- **Default Hysteresis**

  The hysteresis setting applies to all thresholds of the sensor. This column provides the count of hysteresis for the sensor, which can be 1 or 2 (positive or negative hysteresis).

- **Criticality**

  Criticality is a classification of the severity and nature of the condition. It also controls the behavior of the front panel status LED.

- **Standby**

  Some sensors operate on standby power. These sensors may be accessed and/or generate events when the main (system) power is off, but AC power is present.

Table 32. BMC Core Sensors

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Power Unit Status *(Pwr Unit Status)*	01h	All	Power Unit 09h	Sensor Specific 6Fh	00 - Power down	OK	As and De	–	Trig Offset	A	X
					04 - A/C lost						
					05 - Soft power control failure	Fatal					
					06 - Power unit failure						
Power Unit Redundancy1 *(Pwr Unit Redund)*	02h	Chassis-specific	Power Unit 09h	Generic 0Bh	00 - Fully Redundant	OK	As and De	–	Trig Offset	A	X
					01 - Redundancy lost	Degraded					
					02 - Redundancy degraded	Degraded					
					03 - Non-redundant: sufficient resources. Transition from full redundant state.	Degraded					
					04 – Non-redundant: sufficient resources. Transition from insufficient state.	Degraded					
					05 - Non-redundant: insufficient resources	Fatal					

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
					06 – Redundant: degraded from fully redundant state.	Degraded					
					07 – Redundant: Transition from non-redundant state.	Degraded					
IPMI Watchdog *(IPMI Watchdog)*	03h	All	Watchdog 2 23h	Sensor Specific 6Fh	00 - Timer expired, status only 01 - Hard reset 02 - Power down 03 - Power cycle 08 - Timer interrupt	OK	As	–	Trig Offset	A	X
Physical Security *(Physical Scrty)*	04h	Chassis Intrusion is chassis-specific	Physical Security 05h	Sensor Specific 6Fh	00 - Chassis intrusion 04 - LAN leash lost	OK	As and De	–	Trig Offset	A	X
FP Interrupt *(FP NMI Diag Int)*	05h	Chassis - specific	Critical Interrupt 13h	Sensor Specific 6Fh	00 - Front panel NMI/diagnostic interrupt	OK	As	–	Trig Offset	A	–
SMI Timeout *(SMI Timeout)*	06h	All	SMI Timeout F3h	Digital Discrete 03h	01 – State asserted	Fatal	As and De	–	Trig Offset	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
System Event Log *(System Event Log)*	07h	All	Event Logging Disabled 10h	Sensor Specific 6Fh	02 – Log area reset/cleared	OK	As	–	Trig Offset	A	X
System Event *(System Event)*	08h	All	System Event 12h	Sensor Specific 6Fh	04 – PEF action	OK	As	–	Trig Offset	A	X
Button Sensor *(Button)*	09h	All	Button/Switch 14h	Sensor Specific 6Fh	00 – Power Button 02 – Reset Button	OK	AS	–	Trig Offset	A	X
PCH Thermal Trip *(PCH Therm Trip)*	0Dh	All	Temperature 01h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	X
Baseboard Temperature 1 *(Baseboard Temp)*	20h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Front Panel Temperature *(Front Panel Temp)*	21h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
PCH TemperatureNote1 *(PCH Temp)*	22h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Baseboard Temperature 3 *(Inlet Temp)*	24h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Hot-swap Backplane Temperature *(HSBP Temp)*	29h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Fan Tachometer Sensors *(Chassis specific sensor names)*	30h–34h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	nc = Degraded c = Non-fatal2	As and De	Analog	R, T	M	–
Power Supply 1 Status *(PS1 Status)*	50h	Chassis-specific	Power Supply 08h	Sensor Specific 6Fh	00 – Presence	OK	As and De	–	Trig Offset	A	X
					01 – Failure	Degraded					
					02 – Predictive Failure	Degraded					
					03 – A/C lost	Degraded					
					06 – Configuration error	OK					
Power Supply 2 Status	51h	Chassis-specific	Power Supply 08h	Sensor Specific	00 – Presence	OK	As and De	–	Trig Offset	A	X
					01 – Failure	Degraded					

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
(PS2 Status)				6Fh	02 – Predictive Failure	Degraded					
					03 – A/C lost	Degraded					
					06 – Configuration error	OK					
Power Supply 1 AC Power Input *(PS1 Power In)*	54h	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 2 AC Power Input *(PS2 Power In)*	55h	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 1 +12V % of Maximum Current Output *(PS1 Curr Out %)*	58h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 2 +12V % of Maximum Current Output *(PS2 Curr Out %)*	59h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 1 Temperature *(PS1 Temperature)*	5Ch	Chassis-specific	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Power Supply 2 Temperature *(PS2 Temperature)*	5Dh	Chassis-specific	Temperature	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Processor Status *(P1 Status)*	70h	All	Processor 07h	Sensor Specific 6Fh	01 – Thermal trip	Fatal	As and De	–	Trig Offset	M	X
					07 – Presence	OK					
Processor Thermal Margin *(P1 Therm Margin)*	74h	All	Temperature 01h	Threshold 01h	–	–	–	Analog	R, T	A	–
Processor Thermal Control % *(P1 Therm Ctrl %)*	78h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	Trig Offset	A	–
Catastrophic Error *(CATERR)*	80h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	Non-fatal	As and De	–	Trig Offset	M	–
MSID Mismatch *(MSID Mismatch)*	81h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	Non-fatal	As and De	–	Trig Offset	M	–
Processor Population Fault *(CPU Missing)*	82h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Processor VRD Temperature *(P1 VRD Hot)*	90h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Fatal	As and De	–	Trig Offset	M	–
Power Supply 1 Fan Tachometer 1 *(PS1 Fan Tach 1)*	A0h	Chassis-specific	Fan 04h	Threshold 01h	–	–	–	Analog	–	–	–
Power Supply 1 Fan Tachometer 2 *(PS1 Fan Tach 2)*	A1h	Chassis-specific	Fan 04h	Threshold 01h	–	–	–	Analog	–	–	–
Power Supply 2 Fan Tachometer 1 *(PS2 Fan Tach 1)*	A4h	Chassis-specific	Fan 04h	Threshold 01h	–	–	–	Analog	–	–	–
Power Supply 2 Fan Tachometer 2 *(PS2 Fan Tach 2)*	A5h	Chassis-specific	Fan 04h	Threshold 01h	–	–	–	Analog	–	–	–
Processor DIMM Aggregate Thermal Margin *(Mem P1 Thrm Mrgn)*	B0h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor DIMM Thermal Trip *(Mem P1 Thrm Trip)*	C0h	All	Temperature 01h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	X
Baseboard +12V *(BB +12.0V)*	D0h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Baseboard +5V *(BB +5.0V)*	D1h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +3.3V *(BB +3.3V)*	D2h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +5V Stand-by *(BB +5.0V STBY)*	D3h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard +3.3V Auxiliary *(BB +3.3V AUX)*	D4h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard +1.2V Processor Vccp *(BB P1 Vccp)*	D6h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.5V VDDQ *(BB +1.5V P1 MEM)*	D8h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Baseboard CMOS Battery *(BB +3.3V Vbat)*	DEh	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard Processor Vcc *(BB P1 Vcc)*	E0h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard Processor VccUSA *(BB P1 VccUSA)*	E1h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.05V PCH *(BB +1.05V PCH)*	E2h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.05V Auxiliary *(BB +1.05V AUX)*	E3h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard +1.35V VDDQ *(BB +1.35V P1 MEM)*	E4h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Baseboard +12.0V V1 *(BB +12.0V V1)*	E8h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.5V Auxiliary *(BB +1.5V AUX)*	E9h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Hard Disk Drive 0 Status *(HDD 0 Status)*	F0h	Chassis-specific	Drive Slot 0Dh	Sensor Specific 6Fh	00 – Drive Presence	OK	As and De	–	Trig Offset	A	X
					01 – Drive Fault	Degraded					
					02- Predictive Failure	Degraded					
					07 – Rebuild/Remap in progress	Degraded					
Hard Disk Drive 1 Status *(HDD 1 Status)*	F1h	Chassis-specific	Drive Slot 0Dh	Sensor Specific 6Fh	00 – Drive Presence	OK	As and De	–	Trig Offset	A	X
					01 – Drive Fault	Degraded					
					02 – Predictive Failure	Degraded					
					07 – Rebuild/Remap in progress	Degraded					
Hard Disk Drive 2 Status *(HDD 2 Status)*	F2h	Chassis-specific	Drive Slot 0Dh	Sensor Specific 6Fh	00 – Drive Presence	OK	As and De	–	Trig Offset	A	X
					01 – Drive Fault	Degraded					

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
					02 – Predictive Failure	Degraded					
					07 – Rebuild/Remap in progress	Degraded					
Hard Disk Drive 3 Status *(HDD 3 Status)*	F3h	Chassis-specific	Drive Slot 0Dh	Sensor Specific 6Fh	00 – Drive Presence	OK	As and De	–	Trig Offset	A	
					01 – Drive Fault	Degraded					
					02 – Predictive Failure	Degraded					
					07 – Rebuild/Remap in progress	Degraded					

Appendix C: POST Code Diagnostic LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, you can use the diagnostic LEDs to identify the last POST process executed.

Later in POST, the BIOS displays POST Error Codes on the video monitor in the Error Manager display. Any POST Error Codes are automatically logged in the event log.

The Diagnostic LEDs are a set of LEDs found on the back edge of the server board. The exact implementation may differ for some boards, but in general there are eight Diagnostic LEDs which form a two hex digit (8 bit) code read left-to-right as facing the rear of the server.

An LED which is ON represents a 1 bit value, and an LED which is OFF represents a 0 bit value. The LED bit values are read as Most Significant Bit to the left, Least Significant Bit to the right.

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 33. POST Progress Code LED Example

LEDs	Upper Nibble LEDs				Lower Nibble LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	OFF	ON	OFF
Results	1	0	1	0	1	1	0	0
	Ah				Ch			

Note:

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 34. POST Progress Codes

Progress Code	Diagnostic LED Decoder O = On, X=Off Upper Nibble MSB 8h 4h 2h 1h #7 #6 #5 #4 Lower Nibble 8h 4h 2h 1h LSB #3 #2 #1 #0	Description
SEC Phase		
0x01	X X X X X X X O	First POST code after CPU reset
0x02	X X X X X X O X	CPU Microcode load begin
0x03	X X X X X X O O	Cache As RAM initialization begin
0x04	X X X X X O X X	PCI Cache when Disabled
0x05	X X X X X O X O	SEC Core at Power On Begin

Progress Code	Diagnostic LED Decoder O = On, X=Off Upper Nibble MSB 8h 4h 2h 1h #7 #6 #5 #4 Lower Nibble 8h 4h 2h 1h LSB #3 #2 #1 #0	Description
0x06	X X X X X O O X	Early CPU initialization during Sec Phase
0x07	X X X X X O O O	Early South Bridge initialization
0x08	X X X X O X X X	Early North Bridge initialization
0x09	X X X X O X X O	End Of Sec Phase
0x0E	X X X X O O O X	CPU Microcode Not Found.
0x0F	X X X X O O O O	CPU Microcode Not Loaded
PEI Phase		
0x10	X X X O X X X X	PEI Core Starts
0x11	X X X O X X X O	CPU PEI Module Starts
0x15	X X X O X O X O	North Bridge PEI Module Starts
0x19	X X X O O X X O	South Bridge PEI Module Starts
0x31	X X O O X X X O	Memory Installed
0x32	X X O O X X O X	CPU PEI Module for CPU initialization
0x33	X X O O X X O O	CPU PEI Module for Cache initialization
0x34	X X O O X O X X	CPU PEI Module for Boot Strap Processor Select
0x35	X X O O X O X O	CPU PEI Module for Application Processor initialization
0x36	X X O O X O O X	CPU PEI Module for CPU SMM initialization
0x4F	X O X X O O O O	Dxe IPL started
DXE Phase		
0x60	X O O X X X X X	DXE Core started
0x61	X O O X X X X O	DXE NVRAM initialization
0x62	X O O X X X O X	SB RUN initialization
0x63	X O O X X X O O	Dxe CPU initialization
0x68	X O O X O X X X	DXE PCI Host Bridge initialization
0x69	X O O X O X X O	DXE NB initialization
0x6A	X O O X O X O X	DXE NB SMM initialization
0x70	X O O O X X X X	DXE SB initialization
0x71	X O O O X X X O	DXE SB SMM initialization
0x72	X O O O X X O X	DXE SB devices initialization
0x78	X O O O O X X X	DXE ACPI initialization
0x79	X O O O O X X O	DXE CSM initialization

Progress Code	Diagnostic LED Decoder O = On, X=Off Upper Nibble MSB 8h 4h 2h 1h #7 #6 #5 #4 Lower Nibble 8h 4h 2h 1h LSB #3 #2 #1 #0	Description
0x90	O X X O X X X X	DXE BDS Started
0x91	O X X O X X X O	DXE BDS connect drivers
0x92	O X X O X X O X	DXE PCI Bus begin
0x93	O X X O X X O O	DXE PCI Bus HPC initialization
0x94	O X X O X O X X	DXE PCI Bus enumeration
0x95	O X X O X O X O	DXE PCI Bus resource requested
0x96	O X X O X O O X	DXE PCI Bus assign resource
0x97	O X X O X O O O	DXE CON_OUT connect
0x98	O X X O O X X X	DXE CON_IN connect
0x99	O X X O O X X O	DXE SIO initialization
0x9A	O X X O O X O X	DXE USB start
0x9B	O X X O O X O O	DXE USB reset
0x9C	O X X O O O X X	DXE USB detect
0x9D	O X X O O O X O	DXE USB enable
0xA1	O X O X X X X O	DXE IDE begin
0xA2	O X O X X X O X	DXE IDE reset
0xA3	O X O X X X O O	DXE IDE detect
0xA4	O X O X X O X X	DXE IDE enable
0xA9	O X O X O X X O	DXE verifying SETUP password
0xAB	O X O X O X O O	DXE SETUP start
0xAC	O X O X O O X X	DXE SETUP input wait
0xAD	O X O X O O X O	DXE Ready to Boot
0xAE	O X O X O O O X	DXE Legacy Boot
0xAF	O X O X O O O O	DXE Exit Boot Services
0xB0	O X O O X X X X	RT Set Virtual Address Map Begin
0xB1	O X O O X X X O	RT Set Virtual Address Map End
0xB2	O X O O X X O X	DXE Legacy Option ROM init
0xB3	O X O O X X O O	DXE Reset system
0xB4	O X O O X O X X	DXE USB Hot plug
0xB5	O X O O X O X O	DXE PCI BUS Hot plug
0xB6	O X O O X O O X	DXE NVRAM cleanup
0xB7	O X O O O O O O	DXE Configuration Reset
0x00	X X X X X X X X	INT19

Progress Code	Diagnostic LED Decoder O = On, X=Off Upper Nibble Lower Nibble MSB 8h 4h 2h 1h 8h 4h 2h 1h LSB #7 #6 #5 #4 #3 #2 #1 #0	Description
BIOS Recovery		
0xF0	O O O O X X X X	PEIM which detected forced Recovery condition
0xF1	O O O O X X X O	PEIM which detected User Recovery condition
0xF2	O O O O X X O X	Recovery PEIM (Recovery started)
0xF3	O O O O X X O O	Recovery PEIM (Capsule found)
0xF4	O O O O X O X X	Recovery PEIM (Capsule loaded)

Appendix D: POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users of error conditions. The beep code is followed by a user-visible code on POST Progress LEDs:

Table 35. POST Error Messages and Handling

Error Code	Error Message	Response
0012	CMOS date/time not set	Major
0048	Password check failed	Major
0140	PCI component encountered a PERR error	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
5220	CMOS/NVRAM configuration cleared	Major
5221	Passwords cleared by jumper	Major
5224	Password clear jumper is Set	Major
8160	Processor 01 unable to apply microcode update	Major
8180	Processor 01 microcode update not found	Minor
8190	Watchdog timer failed on last boot	Major
8198	OS boot watchdog timer failure	Major
8300	Baseboard management controller failed self-test	Major
8305	Hot Swap Controller failure	Major
83A0	Management Engine (ME) failed Selftest	Major
83A1	Management Engine (ME) Failed to respond	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode	Major
8501	DIMM Population Error	Major
8520	DIMM_A1 failed test/initialization	Major
8521	DIMM_A2 failed test/initialization	Major
8523	DIMM_B1 failed test/initialization	Major
8524	DIMM_B2 failed test/initialization	Major
8540	DIMM_A1 disabled	Major
8541	DIMM_A2 disabled	Major
8543	DIMM_B1 disabled	Major
8544	DIMM_B2 disabled	Major

Error Code	Error Message	Response
9667	PEI module component encountered an illegal software state error	Fatal
9687	PEI module component encountered an illegal software state error	Fatal
96A7	PEI module component encountered an illegal software state error	Fatal
A000	TPM device not detected	Minor
A001	TPM device missing or not responding	Minor
A002	TPM device failure	Minor
A003	TPM device failed self-test	Minor
A100	BIOS ACM Error	Major
A421	PCI component encountered a SERR error	Fatal
A5A0	PCI Express* component encountered a PERR error	Minor
A5A1	PCI Express* component encountered a SERR error	Fatal

POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on POST Progress LEDs:

Table 36. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error	Multiple	System halted because a fatal error related to the memory was detected.
The following Beep Codes are from the BMC, and are controlled by the Firmware team. They are listed here for convenience.			
1-5-2-1	CPU socket population error	N/A	CPU1 socket is empty.
1-5-2-4	MSID Mismatch	N/A	MSID mismatch occurs if a processor is installed into a system board that has incompatible power capabilities.
1-5-4-2	Power fault	N/A	DC power unexpectedly lost (power good dropout) – Power unit sensors report power unit failure offset.
1-5-4-4	Power control fault	N/A	Power good assertion timeout – Power unit sensors report soft power control failure offset.

Glossary

This section contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (for example, 82460GX) with alpha entries following (for example, AGP 4x). Acronyms are then entered in their respective place, with non-acronyms following:

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ARP	Address Resolution Protocal
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
Byte	8-bit quantity
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis)
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	Complementary Metal-oxide-semiconductor In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board
DHCP	Dynamic Host Configuration Protocal
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMI	Electromagnetic Interference
EMP	Emergency Management Port
EPS	External Product Specification
ESB2	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
F MB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024 MB
GPA	Guest Physical Address
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HPA	Host Physical Address
HSC	Hot-swap Controller
Hz	Hertz (1 cycle/second)
I^2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture

Term	Definition
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
ILM	Independent Loading Mechanism
IMC	Integrated Memory Controller
INTR	Interrupt
I/OAT	I/O Acceleration Technology
IOH	I/O Hub
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
KVM	Keyboard, Video, Mouse
LAN	Local Area Network
LCD	Liquid Crystal Display
LDAP	Local Directory Authentication Protocol
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024 KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ME	Management Engine
MMU	Memory Management Unit
ms	Milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
OVP	Over-voltage Protection
PECI	Platform Environment Control Interface
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt

Term	Definition
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
QPI	QuickPath Interconnect
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
RMII	Reduced Media-Independent Interface
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SIO	Server Input/Output
SMBus*	System Management BUS
SMI	Server Management Interrupt (SMI is the highest priority non-maskable interrupt)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
SPS	Server Platform Services
SSE2	Streaming SIMD Extensions 2
SSE3	Streaming SIMD Extensions 3
SSE4	Streaming SIMD Extensions 4
TBD	To Be Determined
TDP	Thermal Design Power
THD	Total Harmonic Distortion
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
URS	Unified Retention System
UTC	Universal time coordinare
VDC	Voltage Direct Current
VID	Voltage Identification
VLSI	Very Large Scale Integration
VRD	Voltage Regulator Down
VT	Virtualization Technology
Word	16-bit quantity
WS-MAN	Web Services for Management
ZIF	Zero Insertion Force

Reference Documents

Refer to the following documents for additional information:

- *Intel® Server Board S1200BT BIOS External Product Specification*
- *Intel® Server Board S1200BT Common Core Integrated BMC External Product Specification*