Intel® SBT2 Server Board

Technical Product Specification

Revision 1.00

August 2000

Enterprise Products Group

Revision History

Date	Revision Number	Modifications
July 2000	0.95	Preliminary release of SBT2 Baseboard Technical Specification
August 2000	1.00	Production release

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The SBT2 system may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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1. Introduction

This document provides an overview of the SBT2 server board, showing the board layout of major components and connectors, and describing the functional blocks of the boards and their relationships.

1.1 Audience

This document is written for technical personnel who want a technical overview of the SBT2 server board. Familiarity with the personal computer, Intel server architecture, and the PCI local bus is assumed.

1.2 Features

Major features of the SBT2 Server Board include:

- Support for one or two Intel® Pentium® III Xeon™ Processors with an On-Cartidge Voltage Regulator (OCVR)
- 133Mhz system bus design
- Support for 64MB to 4GB of PC133-compliant ECC, registered SDRAM memory
- ServerWorks ServerSet* III LE chipset
- Integrated Adaptec* 7899 PCI dual-port SCSI controller providing separate Ultra160 and Ultra wide SCSI channels
- Integrated Intel® EtherExpress™ PRO100+ 10/100Mbit PCI Ethernet controller (Intel® 82559)
- ATI Rage* IIC video controller with 4 MB of SGRAM on-board
- A PCI IDE controller that provides a single Enhanced IDE interface
- Four PCI 33 MHz, 32-bit, 5 Volt, expansion slots
- Two PCI 66 MHz, 64-bit, 3.3 Volt expansion slots
- One PCI 33 Mhz, 64-bit, 3.3 Volt expansion slot (all 64-bit slots run at 33 Mhz if used)
- Dual Universal Serial Bus (USB) ports
- A compatibility I/O device, integrating floppy, serial and parallel ports
- Integration of server management features, including thermal, voltage, fan, and chassis monitoring into one controller
- Flash BIOS support for all of the above

1.3 Component and Connector Placement

The following diagram shows the placement of major components and connectors on the SBT2 server board.

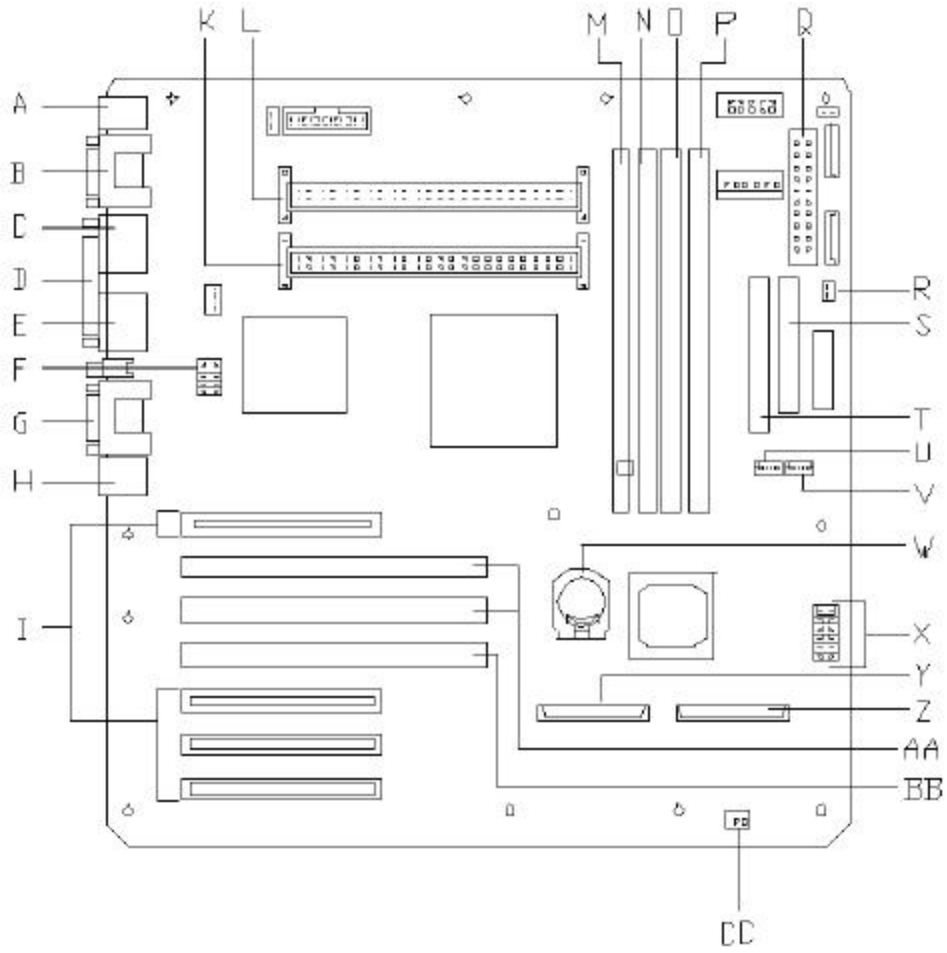

Figure 1-1. SBT2 Server Board Layout

Code	Description	Code	Description
A	USB connectors (top USB 1, bottom USB 2)	**P**	DIMM module slot 1 connector
B	Serial port connectors (top COM1, bottom COM2)	**Q**	Power connector
C	Keyboard connector, PS/2 compatible	**R**	Speaker connector
D	Parallel port connector	**S**	Diskette drive connector
E	Mouse connector, PS/2 compatible	**T**	IDE connector
F	Processor Frequency Jumper Block	**U**	Front fan connector (P20)
G	SVGA monitor port connector	**V**	Lower rear fan connector (P21)
H	LAN RJ-45 network controller connector	**W**	CMOS battery
I	32-Bit/33-MHz PCI slots (4)	**X**	Jumper block
K	Secondary processor SC330.1 connector	**Y**	Ultra-160 (SCSI-A/LVD) SCSI connector
L	Primary processor SC330.1 connector	**Z**	Ultra Wide (SCSI-B/SE) SCSI connector
M	DIMM module slot 4 connector	**AA**	64-Bit/66-MHz PCI slots (2)
N	DIMM module sot 3 connector	**BB**	64-Bit/33-MHz PCI slot (1)
O	DIMM module slot 2 connector	**CC**	Reset switch connector

2. Architectural Overview

The following diagram shows the functional blocks of the SBT2 server board and the plug-in modules that it supports.

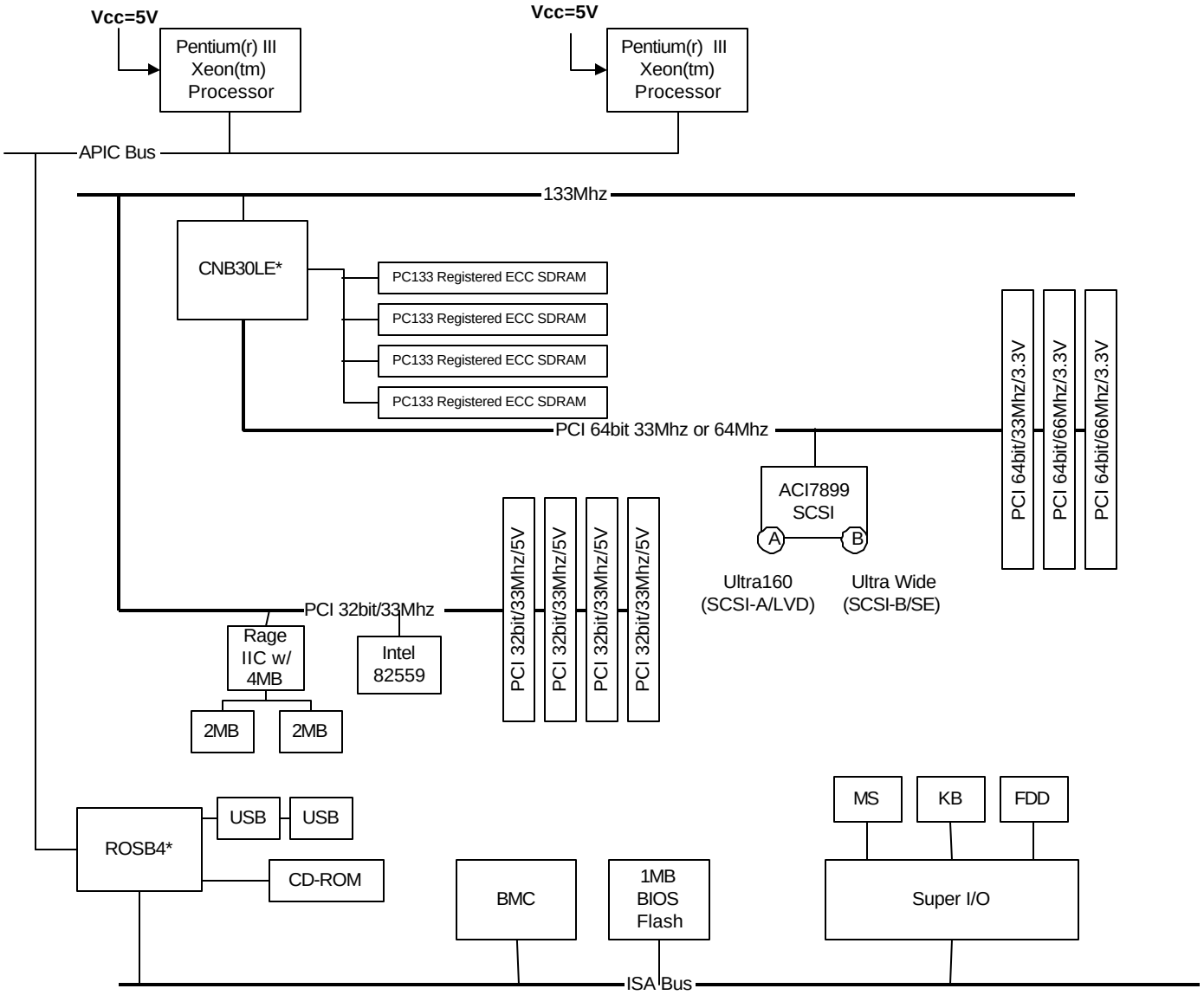

Figure 2-1. SBT2 Block Diagram

The architecture of the SBT2 server board is based on a design that supports dual-processor operation with Intel Pentium® III Xeon™ processors and the ServerWorks ServerSet* III LE.

The SBT2 contains embedded devices for video, NIC, SCSI, and IDE. The server board also provides support for server management and monitoring hardware, and interrupt control that supports dual-processor and PC/AT compatible operation.

This section provides an overview of the following SBT2 sub-systems:

- Support for Pentium® III Xeon™ processors
- ServerWorks ServerSet* III LE
- Memory
- PCI support
- BMC server management controller (See Section 3)

2.1 Intel® Pentium® III Xeon™ Processor Support

The SBT2 server board supports only Pentium III Xeon processors that contain an On-Cartidge Voltage Regulator (OCVR). The system bus functions at 133Mhz and thus supports all SC330.1 processors that can run at 133Mhz. The Pentium III Xeon processors with OCVRs are available only with the Advanced Transfer Cache (ATC).

The Advanced Transfer Cache operates at the core processor frequency and is also “on-chip”, reducing latency. This cache is available on 600+ MHz Pentium III Xeon processors.

2.2 ServerWorks ServerSet* III LE

The SBT2 server board architecture utilizes the ServerWorks ServerSet* III LE chipset. The ServerWorks ServerSet III LE chipset provides an integrated I/O bridge and memory controller, and a flexible I/O subsystem core (PCI), targeted for multiprocessor systems and standard high-volume servers based on the Intel Pentium III processor. The ServerWorks ServerSet III LE chipset consists of two components:

- **NB6635 North Bridge 3.0LE**
  The NB6635 North Bridge 3.0LE is responsible for accepting access requests from the host (processor) bus and for directing those accesses to memory or to one of the PCI busses. The NB6635 North Bridge 3.0LE monitors the host bus, examing addresses for each request. Accesses may be directed to a memory request queue, for subsequent forwarding to the memory subsystem, or to an outbound request queue, for subsequent forwarding to one of the PCI buses. The NB6635 North Bridge 3.0LE is reponsible for controlling data transfer to and from the memory. The NB6635 North Bridge 3.0LE provides the interface for both the 64-bit/66Mhz revision 2.2 compliant PCI bus and the 32-bit/33Mhz Revision 2.2 compliant PCI bus. The NB6635 North Bridge 3.0LE is both a master and target on both PCI buses.
- **IB6566 South Bridge**
  The IB6566 South Bridge controller has several components. It can be both a master and a target on the 32-bit/33Mhz PCI bus. The IB6566 South Bridge also includes a USB controller and an IDE controller. The IB6566 South Bridge is also responsible for much of the power management functions, with ACPI control registers built in. The IB6566 South Bridge also provides a number of GPIO pins.

2.3 Memory

The SBT2 server board supports only 3.3V, 133MHz, PC133-compliant registered ECC SDRAM DIMMs.

Note: PC100 DIMMs cannot be used.

Four DIMM slots are provided for DIMM population. The minimum supported memory configuration is 64 MB using one DIMM. The maximum configurable memory size is 4 GB using 4 DIMMs.

Memory can be installed in one, two, three, or four sockets and must be populated starting with the lowest numbered slot first and filling slots in consecutive order. Empty memory slots between DIMMs are not supported. The user can mix various sizes of DIMMs.

2.4 PCI I/O Sub-system

The I/O bus for the SBT2 is PCI, compliant with revision 2.2 of the PCI specification. The 33Mhz, 5V PCI bus has network control, video and a multi-function PCI device embeded on the board. The multi-function PCI device provides a PCI-to-ISA bridge, bus master IDE controller, Universal Serial Bus (USB) controller, and power management controller. The 33Mhz PCI bus also supports four slots for PCI add-in cards.

Note: Full length cards will not fit in slot 1 (which is a 32-bit/33Mhz expansion slot).

The SBT2 also has a 66Mhz, 3.3V PCI Bus that supports two 66Mhz, 64/32-bit cards or three 33Mhz, 64/32-bit cards. The embeded SCSI Adaptec controller is also located on the 66Mhz bus. 5V cards will not fit into the keyed 3.3V PCI connector.

Three 64-bit slots are on on the SBT2 board. If PCI slot 4 (64-bit/33Mhz) is used, all 64-bit expansion slots will funciton at 33Mhz. Likewise, if a 33Mhz card is place in any of the 64-bit expansion slots, all 64-bit slots will function at 33Mhz, including the SCSI controller.

2.4.1 SCSI Sub-system

The embedded SCSI controller on the SBT2 is the Adaptec AIC-7899 dual function controller. This is located on the 64-bit/66Mhz bus and provides both LVD Ultra160 and SE Ultra wide SCSI interfaces as two independent PCI functions. Both devices have a 68-pin wide SCSI connector. The SBT2 server board provides the ability to disable the embedded Ultra160M SCSI Controller in the BIOS Setup option. When disabled, it will not be visible to the operating system.

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. SCSI control signals are the same for either bus width. To accommodate 8-bit devices on the 16-bit Wide SCSI connector, the AIC-7899 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and does not need to be connected. During chip power down, all inputs are disabled to reduce power consumption.

Refer to the *AIC-7899 PCI-Dual Channel SCSI Multi-Function Controller Data Manual* for more information on the internal operation of this device and for descriptions of SCSI I/O registers.

2.4.2 PCI Network Interface Sub-system

The network interface on the SBT2 is implemented with an Intel 82559 network controller, which provides a 10/100Mbit Ethernet interface supporting 10BaseT and 100BaseTX, integrated with an RJ45 physical interface. The 82559 network controller also provides Wake-on-LAN functionality if the power supply supports a minimum of 720mA of 5V standby current (configurable via baseboard jumper). NIC features supported on SBT2 server boards include Adapter Fault Tolerance and Adapter Load Balancing when integrated with an additional Intel server NIC.

The 82559 is a highly integrated PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. As a PCI bus master, the 82559 can burst data at up to 132 MB/s. This high-performance bus master interface can eliminate the intermediate copy step in RX/TX frame copies, resulting in faster frame processing. The network OS communicates with the 82559 using a memory-mapped I/O interface, PCI interrupt connected directly to the PIC, and two large transmit and receive FIFOs.

The receive and transmit FIFOs prevent data overruns or underruns while waiting for access to the PCI bus, and also enable back-to-back frame transmission within the minimum 960ns inter-frame spacing. The figure below shows the PCI signals supported by the 82559:

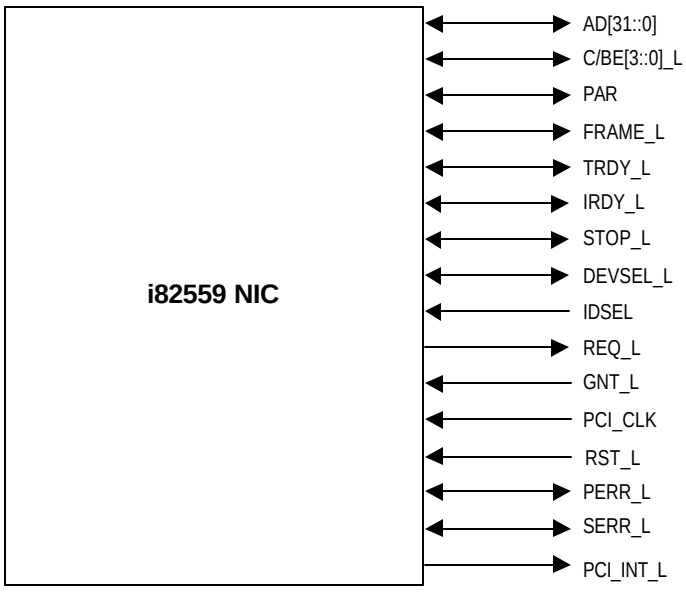

Figure 2-2. Embedded NIC PCI Signals

The 82559 contains an IEEE MII compliant interface to the components necessary to implement an IEEE 802.3 100BASE-TX network connection. The SBT2 supports the following features of the 82559 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- Chained memory structure, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization

- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management
- Autodetect and autoswitching for 10 or 100 Mbps network speeds
- Support for both 10 Mbps and 100 Mbps networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps
- The magnetics component terminates the 100BASE-TX connector interface. A flash device stores the network ID.
- Suport for Wake-on-LAN (WOL).

2.4.3 PCI Video Sub-system

The embedded SVGA-compatible video controller on the SBT2 is the ATI Rage IIC* video controller with 4MB of SGRAM. The Rage IIC is a 64-bit VGA Graphics Accelerator containing a SVGA video controller, clock generator, BitBLT engine, and RAMDAC. Two 512K x 32 SGRAM chips make up the 4 MB of 10ns video memory.

The SVGA subsystem supports a variety of modes: up to 1280 X 1024 resolution, and up to 16.7 Million colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100 Hz vertical retrace frequency. The SBT2 server board provides a standard 15-pin VGA connector, and external video blanking logic for server management console redirection support.

The Rage IIC supports a subset of 32-bit PCI signals because it never acts as a PCI master. As a PCI slave, the device requires no arbitration or interrupts.

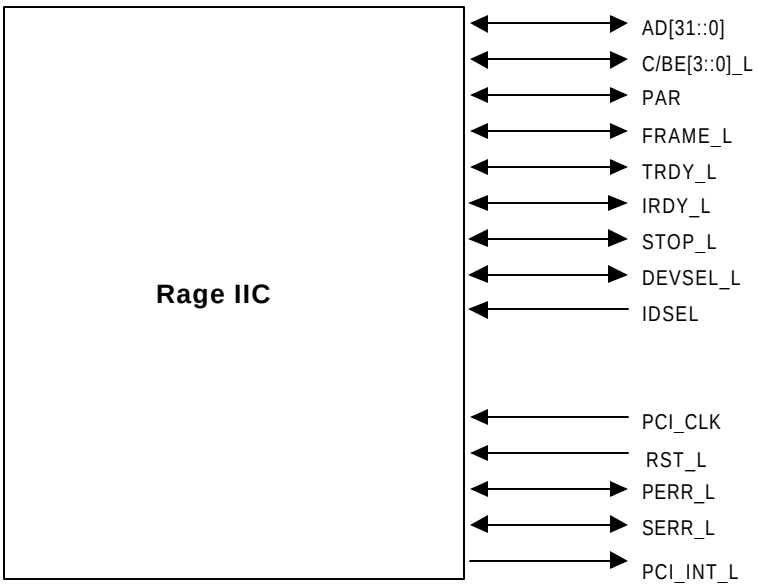

Figure 2-3. Video Controller PCI Signals

2.4.4 IB6566 South Bridge Controller

The IB6566 South Bridge is a PCI device that provides multiple PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the IB6566 South Bridge has its own set of configuration registers; once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

On the SBT2 baseboard, the primary role of the IB6566 South Bridge is to provide the gateway to all PC-compatible I/O devices and features. The SBT2 server board uses the following IB6566 South Bridge features:

- PCI interface
- PCI Bus Master IDE interface
- USB interface
- PC-compatible timer/counters and DMA controllers
- Baseboard Plug-and-Play support
- General purpose I/O
- Power management
- APIC and 82C59 interrupt controller
- Host interface for AT compatible signaling
- Internal only ISA bus (no ISA expansion connectors) bridge for communication with Super I/O, BIOS flash and BMC

The following sections describe each supported feature as used on the SBT2 server board.

2.4.4.1 PCI Interface

The IB6566 South Bridge implements a complete 32-bit PCI master/slave interface, in accordance with the PCI Local Bus Specification, Revision 2.1. On the SBT2 server board, the PCI interface operates at 33 MHz, using the 5V-signaling environment.

2.4.4.2 PCI Bus Master IDE Interface

The IB6566 South Bridge contains a PCI-based enhanced IDE 32-bit interface controller for intelligent disk drives that have disk controller electronics onboard. The server board includes a single IDE connector, featuring 40 pins (2 x 20) that support a master and a slave device. The IDE controller provides support for an internally mounted CD-ROM.

The IDE controller has the following features:

- PIO and DMA transfer modes
- Mode 4 timings
- Transfer rates up to 33 MB/s
- Buffering for PCI/IDE burst transfers
- Master/slave IDE mode.
- Supports up to two devices.

2.4.4.3 USB Interface

The IB6566 South Bridge contains a USB controller and USB hub. The USB controller moves data between main memory and the two USB connectors provided.

The SBT2 server board provides a dual external USB connector interface. Both ports function identically and with the same bandwidth. The external connector is defined by the *USB Specification, Revision 1.0.*

2.4.4.4 Compatibility Interrupt Control

The IB6566 South Bridge provides the functionality of two 82C59 PIC devices, for ISA-compatible interrupt handling.

2.4.4.5 APIC

The IB6566 South Bridge integrates a 16-entry I/O APIC that is used to distribute 16 PCI interrupts. It also includes an additional 16-entry I/O APIC for distribution of legacy ISA interrupts.

2.4.4.6 Power Management

One of the embedded functions of IB6566 South Bridge is power management control. The SBT2 server board uses this controller to implement ACPI-compliant power management. SBT2 supports sleep states s0, s1, s4, and s5.

2.5 ISA I/O Sub-system

The SBT2 contains a full-featured ISA I/O sub-system with a local ISA bus interface to embedded Super I/O, I/O APIC, Flash BIOS and server management features. **The SBT2 does not have an ISA expansion slot.**

2.5.1 National Semiconductor* PC97317 Super I/O Device

Compatibility I/O on the SBT2 is implemented with a National Semiconductor* PC97317 component. This is a super I/O device that integrates a floppy disk controller, keyboard and mouse controller, two enhanced UARTs, full IEEE 1284 parallel port, and support for power management. The chip provides separate configuration register sets for each supported function. Connectors are provided for all compatible I/O devices.

The National PC97317VUL Super I/O Plug-and-Play Compatible with ACPI-Compliant Controller/Extender is used on the SBT2 server board. This device provides the system with:

- Two serial ports
- One parallel port
- Floppy disk controller
- PS/2-compatible keyboard and mouse controller
- RTC
- General purpose I/O pins
- Plug-and-Play functions
- A power management controller

The SBT2 server board provides the connector interface for the floppy, dual serial ports, parallel port, PS/2 mouse and the PS/2 keyboard. Upon reset, the PC97317 reads the values on strapping pins to determine the boot-up address configuration. These are discussed in the following sections.

2.5.1.1 Serial Ports

Two 9-pin connectors in D-Sub housing are provided for serial port A and serial port B. Both ports are compatible with 16550A and 16450 modes, and both can be relocated. Each serial port can be set to one of four different COM-x ports, and each can be enabled separately. When enabled, each port can be programmed to generate edge- or level-sensitive interrupts. When disabled, serial port interrupts are available to add-in cards.

2.5.1.2 Parallel Port

The SBT2 baseboard provides a IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS enables the parallel port and determines the port address and interrupt. When disabled, its resources are available to other devices.

2.5.1.3 Floppy Port

The FDC in the PC97317 is functionally compatible with floppy disk controllers CMOS 765B and 82077AA. The baseboard provides the 24-MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the PC97317, including the analog data separator and 16-byte FIFO.

2.5.1.4 Keyboard and Mouse Connectors

The keyboard controller is functionally compatible with the 8042A. The keyboard and mouse connectors are PS/2-compatible.

2.5.1.5 Real-time Clock

The PC97317VUL contains a MC146818-compatible real-time clock with an external battery backup. The device also contains 242 bytes of general purpose battery-backed CMOS RAM. The real-time clock provides system clock/calendar information stored in non-volatile memory.

2.5.1.6 Plug-and-Play Functions / ISA Data Transfers

The PC97317VUL contains all signals for ISA compatible interrupts and DMA channels. It also provides ISA control, data, and address signals to transfer data to/from the BMC and the BIOS flash device. This ISA subsystem transfers all Super IO peripheral control data to the IB6566 south bridge as well.

2.5.1.7 Power Management Controller

The PC97317VUL contains functionality that allows various events to allow the power-on and power-off of the system. This can be from PCI Power Management Events or from the BMC or front panel. This circuitry is powered with stand-by voltage present anytime the system is plugged into the AC outlet.

2.5.2 BIOS Flash

The SBT2 baseboard incorporates an 8-Mbit (1-MByte) flash chip for nonvolatile storage of the BIOS and settings.

2.5.3 External Device Connectors

The external I/O connectors provide support for a PS/2 compatible mouse and keyboard, an SVGA monitor, two serial port connectors, a parallel port connector, a LAN port, and two USB connections.

2.6 Interrupt Routing

The SBT2 server board interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the IB6566 South Bridge component.

2.6.1 IB6566 South Bridge Interrupt Routing

For PC-compatible PIC mode, the IB6566 South Bridge provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The IB6566 South Bridge contains configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

Both PCI and IRQ interrupt types are handled by the IB6566 South Bridge. IB6566 South Bridge translates these to the APIC bus.

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3. Server Management

This section describes the features of the server management subsystem for the SBT2 server board. The server management subsystem consists of the BIOS, hardware, and firmware features built into the server board. These features provide hardware monitoring, control, and logging to improve the reliability, availability, and serviceability of the server system.

The server management subsystem conforms to the IPMI (Intelligent Platform Management Interface) v1.0 specification. IPMI defines a standardized, abstracted, message-based interface between system management software and the platform management hardware.

The major elements of the server management architecture for the SBT2 server board include:

- Baseboard Management Controller (BMC)
- Hardware Sensors
- Sensor Data Record (SDR) Repository & System Event Log (SEL)
- FRU Information

3.1 Baseboard Management Controller

The SBT2 server management functionality is concentrated in the Baseboard Management Controller (BMC). The BMC is comprised of a Dallas* Semiconductor DS80CH11 (or equivalent) microcontroller and associated circuitry located on the SBT2 server board. The BMC and associated circuits are powered from a 5V DC standby voltage, which remains active when system power is switched off, as long as the AC power source is still on and connected.

A major function of the BMC is to autonomously monitor system management events, and log their occurrence in the nonvolatile System Event Log (SEL). The events being monitored include over/under temperature and over/under voltage conditions, fan failure, or chassis intrusion. To enable accurate monitoring, the BMC maintains the nonvolatile Sensor Data Record (SDR) from which sensor information can be retrieved. The BMC provides an ISA host interface to SDR sensor information, so that software running on the server can poll and retrieve the server's current status. The BMC also provides the interface to the monitored information and SEL that System Management Software, such as Intel Server Control, uses to poll and retrieve the platform status.

The BMC performs the following functions:

- Monitors server boad termperature and voltage
- Monitores processor presence and controls Fault Resilient Boot (FRB)
- Detects and indicates baseboard fan failure
- Manges the SEL interface
- Manages the SDR Repository interface
- Monitors the SDR/SEL timestamp clock
- Monitors the system mangment watchdog time

- Monitors the periodic SMI timer
- Monitors the event receiver
- Controls secure mode, inlucdin video blanding, diskett write-protect monitoring, and front panel lock/unlock initiation
- Controls Wake-on-Lan via Magic Packet support

3.2 Hardware Sensors

The following table lists the hardware sensors on the SBT2 server board.

Table 3-1. SBT2 Hardware Sensors

Type	Sensor	Hardware Connection
CPU	Internal Error (IERR)	BMC P10-0-0, P10-1-0
	Thermal Trip (THERMTRIP)	BMC P10-0-1, P10-1-1
	Bus Error (BERR)	Not monitored
	Numeric Co-processor Error (FERR)	Not monitored
	BINIT	Not monitored
	CPU Missing	BMC P8-2
	CPU Presence	BMC P10-0-2, P10-1-2
	CPU Disable (CPU StopCLK)	BMC P8-7, P9-0
	SMALERT(from MAX1617)	BMC polling
Memory	ECC1bit Error	CNB30LE - OSB4
	ECC2bit Error	CNB30LE - OSB4
PCI	32-bit PCI Device System Error	CNB30LE - OSB4
	32-bit PCI Device Parity Error	
	64-bit PCI Device System Error	
	64-bit PCI Device Parity Error	
Other	Watch-dog Timer Timeout	BMC
	ISA IO Check (IOCHK)	OSB4
	DUMP	BMC P4-2 (NMI Thorough) - HAL (OS)
Voltage	CPU #1 VCCP (VRM) monitor	ADM1024 Vccp1
	CPU #2 VCCP (VRM) monitor	ADM1024 +5Vin
	+3.3V monitor	BMC P5-4
	+5.0V monitor	BMC P5-2
	+12.0V monitor	ADM1024 +12Vin
	+1.5V monitor	BMC P5-5
	+1.8V monitor	Not monitored
	+2.5V monitor	BMC P5-6
	-5.0V monitor	Not monitored
	-12.0V monitor	Not monitored
	SCSI-A +2.85V	BMC P5-0-0
	SCSI-A Vref0	BMC P5-0-1
	SCSI-A Vref1	BMC P5-0-2
	SCSI-A Vref2	BMC P5-0-3
	SCSI-B +2.85V	BMC P5-1-0
	SCSI-B Vref0	BMC P5-1-1
	SCSI-B Vref1	BMC P5-1-2
	SCSI-B Vref2	BMC P5-1-3

Type	Sensor	Hardware Connection
Fans	Three System Fans	BMC P3-5-0
	FAN Speed Control	None
	FAN Stop Control	None
	CPU FAN #1	ADM1024 FAN1
	CPU FAN #2	BMC P3-5-1
	FAN Speed Control	BMC P4-7
	FAN Stop Control	None
Thermal Sensor	CPU Thermal Sensor #1,#2	MAX1617 #1,#2
	MB Temperature	ADM1024 Internal Temperature
	HDD Temp Alarm	SCSI_LM80(monitors external temperature)
	PW Temperature	PW_ADM1024
Cover Sensor	Side Cover	BMC P7-7(Shuts down power from BMC)
	Front Cover	BMC P5-7

The following table lists the sensor numbers associated with the hardware sensors on the SBT2 server board.

Table 3-2. SBT2 Sensor Numbers

Hardware Sensor	Sensor Number
Ambient Temp (SCSI-BP/MB)	01h
Primary Processor Temperature	02h
Secondary Processor Temperature	03h
Board Temperature (SIO/B)	04h
+3.3V	20h
+5V	21h
+12V	22h
+3.3Vs	23h
VCCP0(CPU#1 VRM)	24h
VCCP1(CPU#2 VRM)	25h
+1.5V	29h
+2.5V	2Ah
SCSI A +2.85V	2Ch
SCSI B +2.85V	2Dh
SCSI A Vref0	2Eh
SCSI A Vref1	2Fh
SCSI A Vref2	30h
SCSI B Vref0	31h
SCSI B Vref1	32h
SCSI B Vref2	33h
CPU Rear FAN	40h
CPU Front FAN	41h
Chassis(HDD) FAN	42h
Front Cover	90h (Offset:01h)
Side Cover	90h (Offset:03h)

The following table provides a list of System Event Log (SEL) events supported by the SBT2 server board.

Table 3-3. SBT2 Supported SEL Events

Sensor Type	Sensor Type Code	Sensor-Specific Offset	Event	Remarks
Reserved	00h	–	Reserved	
Temperature	01h	–	Temperature	An error occurred at thermal sensors.
Voltage	02h	–	Voltage	An error occurred at voltage sensors.
		01h	Performance Lags	When in the single-end event mode, even if SCSI is available for a different mode event.
Fan	04h	–	Fan	An error occurred at fan sensors.
Physical Security	05h	01h	Drive Bay Intrusion	The Front Cover has been opened or closed
		03h	Processor area intrusion	The Side (Chassis) Cover has been opened or closed.
		04h	LAN Connection Lost (System has been unplugged from LAN)	The LAN cable is plugged in or unplugged.
Platform Security Violation Attempt	06h	00h	Secured Mode Violation Attempt	The power / sleep switch is activated in the Secure Mode
		03h	Pre-boot Password Violation (network boot Password)	Bad Password at PXE Boot
Processor	07h	00h	IERR	A CPU IERR has occurred
		01h	Thermal Trip	A CPU Thermal Trip has occurred
		02h	FRB1/BIST Failure	A BIST Error has occurred
		04h	FRB3/Processor Startup/Initialization failure (CPU didn't start)	When a FRB3 Timeout is detected
		08h	Processor disabled	When a CPU is Disabled
Memory	0Ch	00h	Correctable ECC	An ECC 1bit Error has occurred
		01h	Uncorrectable ECC	An ECC 2bit Error has occurred
POST Memory Resize	0Eh		POST Memory Resize	Displays the total amount of memory after memory failure
POST Error	0Fh		POST Error	A POST Error has occurred
Event Logging Disabled	10h	00h	Correctable Memory Error Logging Disabled	Displays ECC single bit error monitoring disabled
		01h	Event 'Type' Logging Disabled	Monitoring of a certain event type is disabled
		02h	Log Area Reset/Cleared	Displays the SEL area cleared.
		03h	All Event Logging Disabled	The monitor for the entire BMC is disabled.
System Event	12h	00h	System Reconfigured	A setup change has occurred
		01h	OEM System Boot Event (Hard Reset)	If a cold reset is issued
Critical Interrupt	13h	00h	Front Panel NMI Dump Switch	The dump switch has been activated
		02h	I/O channel check NMI	An ISA I/O Check has occurred.
		04h	PCI SERR	A PCI SERR has occurred
		05h	PCI PERR	A PCI PERR has occurred

Sensor Type	Sensor Type Code	Sensor-Specific Offset	Event	Remarks
Button	14h	00h	Power Button	The power switch has been activated
		01h	Sleep Button	The sleep switch has been activated
		02h	Reset Button	The reset switch has been activated
Module / Board	15h		CPU / Terminator Missing	The CPU/Terminator is not mounted correctly
System Boot Initiated	1Dh	03h	User requested PXE boot	The PXE (Network) has been booted
		04h	Automatic boot to diagnostic	The maintenance utility has been booted
Boot Error	1Eh	00h	No bootable media	The boot media does not exist.
		02h	PXE Server not found	The PXE Server could not be found
		00h	C: boot completed	The ESM Pro installed OS has been booted
		02h	PXE boot completed	he PXE boot has finished (not supported)
		03h	Diagnostic boot completed	The maintenance utility has been booted (not supported)
		04h	CD-ROM boot completed	The server has been booted (not supported)
OS Critical Stop	20h	00h	Stop during OS load / Initialization	The OS stalled during startup
		01h	Run-time Stop	The OS stalled during startup
System ACPI Power State	22h	00h	S0 / G0 Working	DC is ON
		01h	S1 “sleeping with system H/W & processor context Maintained”	S1 Sleep State
		04h	S4 “non-volatile sleep / suspend-to disk”	S4 Sleep State
		05h	S5 / G2 “soft-off”	DC is OFF
		07h	G3 / Mechanical Off	AC is OFF
		08h	Sleeping (cannot differentiate between S1-S3)	The SUSC# OS has been asserted without the instruction to sleep
Watchdog 2	23h	01h	Hard Reset	POST / boot monitor timed out.
		02h	Power Down	The OS WDT shut down after the monitor timeout.
		08h	Timer Interrupt	The OS WDT monitor timed out
SMI Timeout	F3h		SMI Timeout	The SMI# stayed asserted for more than ten seconds.
EMP	F5h	00h	Communication Error	Communication is unavailable even though the BMC is in communication status
Sensor Failure	F6h	00h	I^2C Bus Device Address Not Acknowledged	If the SMBus Device does not answer.
		01h	I^2C Bus Device Error Detected	Other access errors
		02h	I^2C Bus Timeout	SMBus Timeout error
OEM Reserved	F7h - FFh			

3.3 ACPI

An Advance Configuration and Power Interface (ACPI)-aware operating system can place the system into a sleep state. In this state, the hard drives spin down, the system fans stop, and all processing is halted. The power supply is still on and the processors still dissipate a minimal amount of power, such that the power supply fan and processor fans continue to run.

Note: ACPI requires an operating system that supports it.

The sleep states discussed below are defined as:

- s0: Normal running state
- s1: Processor sleep state. No content is lost in this state and the processor cashes maintain coherency.
- s4: Hibernate or Save to Disk. The memory and machine state are saved to disk. Pressing the power button or another wakeup event restores the system state from the disk and resumes normal operation. This assumes that no hardware changes were made to the system while it was off.
- s5: Soft off. Only the RTC section of the chip set and the BMC are running in this state.

The SBT2 server board supports sleep states s0, s1, s4, and s5. When the server board is operating in ACPI mode, the OS retains control of the system and the OS policy determines the entry methods and wake up sources for each sleep state – sleep entry and wake up event capabilities are provided by the hardware but are enabled by the OS.

3.4 AC Link Mode

The AC link mode allows the system to monitor its AC input power so that if AC input power is lost and then restored, the system returns to one of the following preselected settings:

- Power On
- Last State (Factory Default Setting)
- Stay Off

The AC link mode settings can be changed by running the BIOS Setup Utility (F2).

3.5 Wake On LAN Function

The remote power-on function turns on the system power by way of a network or modem. If the sytem power is set to off, it can be turned on remotely by sending a specific packet from the main computer to the remote system.

Note: The standard default value of the remote power-on function is “Disabled”. The Wake-on-LAN / Ring function can be by changing the setting to “Enabled” in the BIOS Setup Utility (F2).

4. Basic Input Output System (BIOS)

The term BIOS, as used in the context of this document, refers to the system BIOS, BIOS Setup, and option ROMs for onboard peripheral devices that are contained in the system flash. The system BIOS controls basic system functionality using stored configuration values. The terms flash ROM, system flash and BIOS flash may be used interchangeably in this document.

BIOS Setup refers to the flash ROM-resident setup utility that provides the user with control of configuration values stored in battery-backed CMOS configuration RAM. The System Setup Utility (SSU) is discussed in a separate document. BIOS Setup is closely tied with the system BIOS and is considered a part of BIOS.

The PHLASH utility is used to load predefined areas of flash ROM with setup, BIOS, and other code/data.

The SBT2 BIOS supports the following features:

- Plug-and-Play (complies with Plug-and-Play BIOS Specifciaton 1.0a)
- Multi-Boot II (includes disk array)
- DMI specification v2.0
- SMBIOS v2.3
- ATAPI CD-ROM boot
- Quick start
- Memory remapping
- CPU Degeneration
- Security (keyboard password protection, security floppy, write-protect, chassis intrusion detection)
- Dump Hook
- Miser
- ACPI v1.0
- SPM BIOS (Only APM Shutdown)
- Server Hardware Design Guide (SHDG) v2.0 Compliance
- Monitoring functions (fan alarm, memory single-bit error, temperature sensing, voltage monitoring)

4.1 BIOS Setup Utility

The BIOS Setup Utility is used to configure the system and option boards that might be added to the system. The utility is resident in the system FLASH memory and does not require a diskette or an operating system present to run.

4.1.1 Using the BIOS Setup Utility

The BIOS Setup utility can be accessed when the user powers on or reboots the system. The following steps are used to run the BIOS Setup Utility.

1. Power-on or reboot the system.

2. Press the **F2** key at the "Press <F2> to enter SETUP" message. The BIOS Setup Utility starts and the Main Menu is displayed. The menu bar at the top of the Main Menu lists the following selections.

Table 4-1. Main Menu Bar

Menu	Use
Main	Use for basic system configuration.
Advanced	Use for setting system Advanced Features.
Security	Use to set User and Supervisor Passwords and the Backup and Virus-Check reminders.
System	Use for configuring unique server features.
Boot	Use this menu to configure Boot Device priority.
Exit	Exits the current menu.

3. Use the arrow keys to select a menu or an item on a displayed menu. Press the value keys (see the following table) to cycle through the allowable values for the selected field. Use the Exit menu's "Save Values" selection to save the current values on all the menus.

4. To display a submenu, position the cursor on a selection that has a submenu and press Enter. An arrow precedes selections with submenus.

See the following table for information on the keys to use with BIOS Setup. The keys are also listed at the bottom of the Setup menu.

Key	Function in Setup Menu
F1 or Alt-H	Get Help about an item.
ESC	Exit the current menu and return to the previous menu.
Left or right arrow keys	Move between menus.
Up or down arrow keys	Move cursor up and down. The cursor moves only to the settings that can be changed
HOME or END	Move cursor to top or bottom of window.
PAGE UP or PAGE DOWN	Move cursor to next or previous page.
F5 or -	Select the previous value for the field.
F6 or + or SPACE	Select the next value for the field.
F9	Load default configuration values for this menu.
F10	Save configuration values and exit.
ENTER	Execute command or Select a submenu.

4.1.2 BIOS Setup Configuration Settings

The BIOS Setup configuration tables below provide the default BIOS Setup settings and provide a place for the user to record any changes made to these settings. Recommended (default) values are bold in the following tables.

4.1.3 BIOS Setup Main Menu

The following table describes the features of the Main Menu.

4.1.3.1 Table 4-2. Main Menu

Feature	Choices or Display Only	Description	Your Setting
System Time	HH:MM:SS	Sets the system time (hour, minutes, seconds, on 24 hour clock).	
System Date	MM/DD/YYYY	Sets the system date (month, day, year).	
Diskette A	**1.44/1.25 MB 3.5"/** Disabled	Selects the diskette type. Note: 1.25 MB, 3.5 inch references a 1024 byte/sector Japanese media format. To support this type of media format requires a 3.5 inch, 3-mode diskette drive.	
Diskette B	1.44/1.25 MB 3.5"/ **Disabled**	Selects the diskette type. Note: 1.25 MB, 3.5 inch references a 1024 byte/sector Japanese media format. To support this type of media format requires a 3.5 inch, 3-mode diskette drive.	
Hard Disk Pre-Delay	**Disabled** 3 Seconds 6 Seconds 9 Seconds 12 Seconds 15 Seconds 21 Seconds 30 Seconds	Delays first access to disk to ensure the disk is initialized by the BIOS before any accesses.	
Primary Master		Displays IDE device selection. Enters submenu if selected.	
Primary Slave		Displays IDE device selection. Enters submenu if selected.	
Processor		Enters Processor Settings submenu if selected.	
Language	**English (US)** French German Spanish Italian	Selects which language BIOS displays. Note: This feature immediately changes to the language BIOS selected.	

4.1.3.2 Primary Master/Slave Submenus

The following table describes the features of the primary master/slave submenus.

Table 4-3. Advanced Submenu

Feature	Choices or Display Only	Description	User Setting
Type	**Auto** None CD-ROM ATAPI Removable IDE Removable Other ATAPI User	Select the type of device that is attached to the IDE channel If ***User*** is selected, the user will need to enter the parameters of the IDE device (cylinders, heads and sectors).	
Multi-Sector Transfers	**Disable** 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Specifies the number of sectors that are transferred per block during multiple sector transfers.	
LBA Mode Control	**Disabled** Enabled	Enable/Disable Logical Block Addressing instead of cylinder, head, sector addressing.	
32-Bit I/O	**Disabled** Enabled	Enable/Disable 32Bit IDE data transfers	
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3/ DMA 1 FPIO 4 / DMA 2	Select the method of moving data to and from the hard drive. (If Type: Auto is selected above, the optimum transfer mode will be selected)	
Ultra DMA Mode	**Disabled** Enabled	Enable/Disable Ultra DMA mode (If Type: Auto is select, optimum transfer mode will be selected)	

4.1.3.3 Processor Settings Submenu

The following table describes the features of the primary master/slave submenus.

Table 4-4: Processor Settings Submenu Selections

Feature	Choices or Display Only	Description	Your Setting
Processor Speed	XXX	(Display Only). Indicates the processor speed.	
Processor 1 Type	XXX	(Display Only). Indicates the CPUID of the installed processor.	
Cache Ram	XXXKB	(Display Only). Indicates the cache RAM size.	
Processor 2 Type	XXX	(Display Only). Indicates the CPUID of the installed processor.	
Cache Ram	XXXKB	(Display Only). Indicates the cache RAM size.	
Processor #1 Status	Normal[1]	(Display Only)	
Processor #2 Status	Normal[1]	(Display Only)	
Clear Processor Errors	Press Enter	Clears the processor error information.	
Processor Error Pause	**Enabled** Disabled	If enabled, the POST operation pauses if a processor error occurs.	
Processor Serial Number	Disabled **Enabled**	Disables/Enables Processor Serial Number.	

Note:

1. Possible Values: Normal, None, or Error.

4.1.4 Advanced Menu

The following table describes the features of the Advanced Menu.

Table 4-4. Advanced Menu

Feature	Choices or Display Only	Description	User Setting
Memory Reconfiguration		Refer to Memory Reconfiguration Submenu.	
CPU Reconfiguration		Refer to CPU Reconfiguration Submenu.	
Peripheral Configuration		Refer to Peripheral Reconfiguration Submenu.	
PCI Device		Refer to PCI Device Submenu.	
Option ROM		Refer to Option ROM Submenu. It Disables/Enables the Option ROM BIOS on the PCI Bus.	
Numlock		Refer to Numlock Submenu.	
Reset Configuration Data	**No** Yes	Clears the Extended System Configuration Data if selected.	
Installed O/S	**Other** PnP O/S	Selects the type of operating system that will be used most.	

4.1.4.1 Memory Reconfiguration Submenu

The following table describes the features of the Memory Reconfiguration Submenu.

Table 4-5. Memory Reconfiguration Submenu

Feature	Choices or Display Only	Description	Your Setting
System Memory	XXX KB	(Display Only). Indicates the total capacity of the basic memory.	
Extended Memory	XXXXXX KB	(Display Only). Indicates the total capacity of the extended memory.	
DIMM #1 Status	Normal[1]	(Display Only)	
DIMM #2 Status	Normal[1]	(Display Only)	
DIMM #3 Status	Normal[1]	(Display Only)	
DIMM #4 Status	Normal[1]	(Display Only)	
Clear DIMM Errors	Press Enter	Clears the DIMM group error status information.	
DIMM Error Pause	**Enabled** Disabled	If enabled, the POST operation pauses if a DIMM error occurs.	

Note:

1. Possible Values: Normal, None, or Error (DIMM Row Error).

4.1.4.2 Peripheral Configuration Submenu

The following table describes the features of the Peripheral Configuration Submenu.

Table 4-6. Peripheral Configuration Submenu

Feature	Choices or Display Only	Description	User Setting
Serial Port 1: (COM 1)	Disabled 3F8, IRQ3 **3F8, IRQ4** 2F8, IRQ3 2F8, IRQ4 3E8, IRQ3 3E8, IRQ4 2E8, IRQ3 2E8, IRQ4 Auto	Disables serial port 1 or selects the base address and interrupt (IRQ) for serial port 1.	
Serial Port 2: (COM 2)	Disabled 3F8, IRQ3 3F8, IRQ4 **2F8, IRQ3** 2F8, IRQ4 3E8, IRQ3 3E8, IRQ4 2E8, IRQ3 2E8, IRQ4 Auto	Disables serial port 2 or selects the base address and interrupt (IRQ) for serial port 2.	

Feature	Choices or Display Only	Description	User Setting
Parallel Port	Disabled 378, IRQ5 **378, IRQ7** 278, IRQ5 278, IRQ7 3BC, IRQ5 3BC, IRQ7 Auto	Disables the parallel port or selects the base address and interrupt (IRQ) for the Parallel port.	
Parallel Mode	Output only Bi-directional EPP ECP, DMA1 **ECP, DMA3**	Selects the parallel port operation mode.	
Diskette Controller	Disabled **Enabled**	Disables/Enables the floppy disk controller.	
Mouse	Disabled Enabled **Auto Detect**	*Disabled* prevents any installed PS/2 mouse from functioning, but frees up IRQ12. *Enabled* forces the PS/2 mouse port to be enabled regardless if a mouse is present. *Auto Detect* enables the PS/2 mouse only if present. *OS Controlled* is displayed if the OS controls the mouse.	
SCSI Controller	Disabled **Enabled**	Disables/Enables on-board SCSI controller. Frees resources.	
LAN Controller	Disabled **Enabled**	Disables/Enables on-board LAN controller. Frees resources.	
VGA Controller	**Enabled** Disabled	Disables/Enables on-board Video controller. Frees resources.	
USB Controller	**Disabled** Enabled	Enables/Disables on-board USB controller. Frees resources.	

4.1.4.3 PCI Device Submenu

The following table describes the features of the PCI Device Submenu.

Table 4-7. PCI Device Submenu

Feature	Choices or Display Only	Description	User Setting
PCI IRQ1 thru PCI IRQ14	Disabled **Auto Select** IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12	Specify which PIC IRQ a certain PCI IRQ maps to.	

4.1.4.4 Option ROM Submenu

The following table describes the features of the Option ROM Submenu.

Table 4-8. Option ROM Submenu

Feature	Choices or Display Only	Description	User Setting
Onboard SCSI	**Enabled** Disabled	Disables/Enables option ROM expansion for the on-board SCSI option ROM. This must be enable if a boot device is connected to the on-board device.	
Onboard LAN	**Enabled** Disabled	Disables/Enables option ROM expansion for the on-board LAN option ROM.	
PCI Slot 1	**Enabled** Disabled	Disables/Enables the expansion of the option ROM for devices in PCI slot 1	
PCI Slot 2	**Enabled** Disabled	Disables/Enables the expansion of the option ROM for devices in PCI slot 2	
PCI Slot 3	**Enabled** Disabled	Disables/Enables the expansion of the option ROM for devices in PCI slot 3	
PCI Slot 4	**Enabled** Disabled	Disables/Enables the expansion of the option ROM for devices in PCI slot 4	
PCI Slot 5	**Enabled** Disabled	Disables/Enables the expansion of the option ROM for devices in PCI slot 5	
PCI Slot 6	**Enabled** Disabled	Disables/Enables the expansion of the option ROM for devices in PCI slot 6	
PCI Slot 7	**Enabled** Disabled	Disables/Enables the expansion of the option ROM for devices in PCI slot 7	

4.1.4.5 Numlock Submenu

The following table describes the features of the Numlock Submenu.

Table 4-9. Numlock Submenu

Feature	Choices or Display Only	Description	User Setting
Numlock	Auto **On** OFF	Selects the power-on state for Numlock.	
Key Click	**Disabled** Enabled	Disables or enables keyclick.	
Keyboard Auto-repeat Rate	2/sec 6/sec **10/sec** 13.3/sec 18.5/sec 21.8/sec 26.7/sec 30/sec	Selects key repeat rate.	
Keyboard Auto-repeat Delay	0.25 sec 0.5 sec 0.75 sec **1 sec**	Selects delay before key repeat.	

4.1.5 Security Menu

The following table describes the features of the Security Menu

Note: Enabling the Supervisor Password field requires a password for entering Setup. The passwords are not case sensitive.

Table 4-10. Security Menu

Feature	Choices or Display Only	Description	User Setting
Supervisor Password is	Clear	(Display only). Once set, this can be disabled by setting it to a null string, or by clearing password jumper on system board.	
User Password is	Clear	(Display only). Once set, this can be disabled by setting it to a null string, or by clearing password jumper on system board	
Set Supervisor Password	Press Enter	Supervisor password controls access to the setup utility. When the <Enter> key is pressed, the user is prompted for a password; press ESC key to abort. Once set, this can be disabled by setting it to a null string, or by clearing password jumper on system board.	
Set User Password	Press Enter	When the <Enter> key is pressed, the user is prompted for a password; press ESC key to abort. Once set, this can be disabled by setting it to a null string, or by clearing password jumper on system board.	
Password on Boot	**Disabled** Enabled	Disables or enables password entry on boot.	
Diskette Access	**User** Supervisor	Controls access to diskette drives.	
Secure Mode		See Secure Mode Submenu. Submenu can only be entered if supervisor and user password is set.	
Power Switch Mask	Masked **Unmasked**	Determines whether power switch will function from front panel	
Option ROM Menu Mask	**Unmasked** Masked	Determines whether on-board SCSI Option ROM will allow the user to enter adapter configuration with <CTRL>-A	
Processor Serial Number	Disabled **Enabled**	Disables/Enables Processor Serial Number.	

4.1.5.1 Secure Mode Submenu

The following table describes the features of the Thermal Sensor Submenu.

Table 4-11. Secure Mode Submenu

Feature	Choices or Display Only	Description	User Setting
Secure Mode Timer	**Disabled** 1 Min 2 Min 5 Min 10 min	Period of keyboard and mouse inactivity before secure mode is activated and a password is required gain access.	

	30 min 1 hr 2 hr		
Secure Mode HotKey	**Disabled** Enabled	Enables/Disables the ability to lock the system with a <CTRL>+<ALT> + <key> combination. The key can be selected and submenu appears when enabled. A password is required to gain access.	
Secure Mode Boot	**Disabled** Enabled	Enables/Disables secure boot. The system will boot as normal, but a password is required to access the system using any PS/2 device	
Floppy Write Protect	**Disabled** Enable	Enables/Disables floppy drive write protection. If enabled, a password is required to write to a floppy.	

4.1.6 System Hardware Menu

The following table describes the features of the System Hardware Menu.

Table 4-12. System Hardware Menu

Feature	Choices or Display Only	Description	User Setting
Wake On Events		See Wake On Events submenu.	
AC Link	Power On **Last State** Stay Off	Selects power retention mode if AC power is lost a regained.	
Error Log Initialization	Press Enter	Select to clear the system Error Log. If Clear OK, then display "System Event Log Cleared!" If Clear failed, then display “System Event Log Not Cleared!”	
Console Redirection		See Console Redirection Submenu.	
Assert NMI on PERR	**Disabled** Enabled	Enables PCI PERR support.	

4.1.6.1 Wake On Events Submenu

The following table describes the features of the Wake On Events Submenu.

Table 4-13. Wake On Events Submenu

Feature	Choices or Display Only	Description	User Setting
Wake On LAN	Enabled **Disabled**	Enables/Disables Wake-on-LAN support.	
Wake On Ring	Enabled **Disabled**	Enables/Disables Wake-on-Ring support.	

4.1.6.2 Console Redirection Submenu

The following table describes the features of the Console Redirection Submenu.

Table 4-14. Console Redirection Submenu

Feature	Choices or Display Only	Description	User Setting
Serial Port Address	**Disabled** Serial Port 2 (3F8h/IRQ4) Serial Port 2 (2F8h/IRQ3)	If enabled, the console will be redirected to this port. If console redirection is enabled, this address must match the settings of serial port 2.	
Baud Rate	57.6K **19.2K**	Enables the specified baud rate.	
Flow Control	No Flow Control **XON/OFF**	Selects flow control.	

Feature	Choices or Display Only	Description	User Setting
Console Connection	**Direct** Via Modem	Indicate whether the console is connected directly to the system or if a modem is used to connect.	

4.1.7 Boot Menu

The following table describes the features of the Boot Menu.

Table 4-15. Boot Menu

Feature	Choices or Display Only	Description	User Setting
Boot-Time Diagnostic Screen	**Disabled** Enabled	Enable/Disable boot-time diagnostic screen. Splash screen is displayed over the diagnostic screen when is option is Disabled.	
Boot Device Priority		See Boot Device Priority Submenu	
Hard Drive		See Hard Drive Submenu	
Removable Devices		See Removable Devices Submenu	

4.1.7.1 Boot Device Priority Submenu

Use the up or down arrow keys to select a device, then press the <+> or <-> keys to move the device higher or lower in the boot priority list.

Table 4-16. Boot Device Priority Submenu

Boot Priority	Device	Description	User Setting
1	ATAPI CD-ROM Drive	Attempts to boot from an ATAPI CD-ROM drive.	
2	Removable Devices	Attempts to boot from a removable device.	
3	Hard Drive	Attempts to boot from a hard drive device.	
4	Intel UNDI, PXE-2.0 (Build 071)	Attempts to boot from a PXE server.	

4.1.7.2 Hard Drive Submenu

The following table describes the features of the Hard Drive Submenu.

Table 4-17. Hard Drive Submenu

Boot Priority	Device	Description	User Setting
1	AIC-7899,CH B ID 1**	Select the order in which each drive is attempted to be used as the boot device. **These selections will change depending on the system configuration	
2	AIC-7899, CH A, ID 9**		
3	AIC-7899, CH B, ID 4**		
4	Bootable Add-in Cards		

4.1.7.3 Removable Devices Submenu

The following table describes the features of the Removable Devices Submenu.

Table 4-18. Removable Devices Submenu

Boot Priority	Device	Description	User Setting
1	Legacy Floppy Drives	Select the order in which each removable device is attempted to be used as the boot device. These selections will change depending on the system configuration	

4.1.8 Exit Menu

The following selections can be made from the Exit Menu. Select an option using the up or down arrow keys, then press <Enter> to execute the option. Pressing <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Table 4-19. Exit Menu

Choices	Description
Save Changes & Exit	Exits System Setup after saving all changes to CMOS.
Exit Discarding Changes	Exits System Setup without saving setup data to CMOS.
Load Setup Defaults	Loads default values for all Setup items.
Discard Changes	Loads previous values of all Setup items.
Save Changes	Writes all Setup item values to CMOS.

4.2 Updating the BIOS

The BIOS update utility (PHLASH) loads a new copy of the BIOS into Flash ROM. The loaded code and data include the following:

- On-board Video BIOS and SCSI BIOS
- BIOS Setup Utility
- Diagnostic boot loader binary
- Language file
- Quiet Boot Logo Area

When running PHLASH in interactive mode, the user may choose to update a particular Flash area. Updating a flash area takes a file or series of files from a hard or floppy disk, and loads it in the specified area of Flash ROM.

To manually load a portion of the BIOS, the user must specificy which data file(s) to load. The choices include PLATCBLU.BIN, PLATCXLU.BIN, PLATCXXX.BIN, PLATCXLX.BIN or PLATCXXU.BIN. The last three letters specify the functions to perform during the flash process.

- C = Rewrite BIOS
- B = Rewrite Bootblock
- L = Clear LOGO area
- U = Clear user binary
- X = place hold

This file is loaded into the PHLASH program with the /b=<bin file>.

The disk created by the BIOS.EXE program will automatically run “phlash /s /b=PLATCXLU.BIN command” in non-interactive mode. For a complete list of phlash switches, run phlash /h.

4.3 Quiet Boot Logo Screen

During POST, with the POST Diagnostic Screen Disabled (Default), a Manufacturer’s Logo Splash screen is displayed instead of system POST information. The splash screen can be user defined and loaded to into system Flash. When the BIOS is updated, a default “Intel” splash screen is loaded. Any user defined splash screen must be re-loaded to flash.

4.4 Recovery Mode

In the case of a corrupt or an unsuccessful update of the system BIOS, the SBT2 can boot in recovery mode. To place SBT2 into recovery mode, move the boot option jumper (jumper block 3N7 pins 9-10) to the recovery boot position. By default and for normal operation, pins 9 and 10 are not jumpered.

Recovery mode requires at least 8 MB of RAM in the first DIMM socket (NOTE: the system requires 64MB to boot), and drive A: must be set up to support a 3.5” 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, PHLASH (in non-interactive mode only) automatically updates only the main system BIOS. PHLASH senses that SBT2 is in recovery mode and automatically attempts to update the system BIOS

Before powering up the system, the user must obtain a bootable diskette that contains a copy of the BIOS recovery files. This is created by running the "crisdisk.bat" from the compressed recovery file distributed with the BIOS.

Note: During recovery mode, video will not be initialized and many high-pitched beep tones will be heard. The entire process takes two to four minutes. When the process is completed, the tones will stop. The user may see a "Checksum error" on the first boot after updating the BIOS. This is normal and should correct itself after the first boot.

If a failure occurs, it is most likely that of the system BIOS .ROM file is corrupt or missing.

After a successful update, power down the system and remove the jumper from pins 9-10. Power up the system. Verify that the BIOS version number matches the version of the entire BIOS used in the original attempt to update.

4.5 Error Messages and Error Codes

This section describes the various screen messages and beep codes of the system BIOS. The BIOS indicates errors by writing an error code to the PS/2-standard logging area in the Extended BIOS Data Area, and by displaying a message on the screen, which is sometimes preceded by the POST Error Code. The error code also logs to the event log area.

4.5.1 POST Error Codes and Messages

Whenever a recoverable error occurs during POST, BIOS displays a message on the monitor screen and causes the speaker to beep as the message appears. BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails or if an external ROM module does not show a checksum of zero. The following "POST Error Codes and Messages" table is a list of the error codes and messages written at the start of each POST test. The "POST Error Beep Codes" table is a list of beep codes issued for each POST test.

Table 4-20. POST Error Codes and Messages

Code	Error Message
0200	Failure Fixed Disk
0210	Stuck Key
0211	Keyboard error
0212	Keyboard Controller Failed
0213	Keyboard locked - Unlock key switch
0220	Monitor type does not match CMOS - Run SETUP
0230	System RAM Failed at offset
0231	Shadow RAM Failed at offset
0232	Extended RAM Failed at address line
0233	Memory type mixing detected
0234	Single-bit ECC error
0235	Multiple-bit ECC error occurred
0250	System battery is dead - Replace and run SETUP
0251	System CMOS checksum bad - Default configuration used

Code	Error Message
0260	System timer error
0270	Real time clock error
0271	Check date and time
02B0	Diskette drive A error
02B2	Incorrect Drive A type - run SETUP
02D0	System cache error - Cache disabled
0B1B	PCI System Error on Bus/Device/Function
0B1C	PCI Parity Error on Bus/Device/Function
0B30	CPU 1 Fan Alarm occurred
0B31	CPU 2 Fan Alarm occurred
0B32	Chassis Fan Alarm occurred
0B33	Power Unit Fan 1 Alarm occurred
0B34	Power Unit Fan 2 Alarm occurred
0B46	ESMINT not configured
0B50	CPU #1 with error taken off line
0B51	CPU #2 with error taken off line
0B5F	Forced to use CPU with error
0B60	DIMM group #1 has been disabled
0B61	DIMM group #2 has been disabled
0B62	DIMM group #3 has been disabled
0B63	DIMM group #4 has been disabled
0B6F	DIMM group with error is enabled
0B70	The error occurred during temperature sensor reading
0B71	System Temperature out of range
0B74	The error occurred during voltage sensor reading
0B75	System Voltage out of range
0B7C	The error occurred during fan sensor reading
0B80	BMC Memory Test Failed
0B81	BMC Firmware Code Area CRC check failed
0B82	BMC core hardware failure
0B83	BMC IBF or OBF check failed
0B90	BMC Platform Information Area Corrupted
0B91	BMC update firmware corrupted
0B92	Internal Use Area of BMC FRU corrupted
0B93	BMC SDR Repository empty
0B94	IPMB signal lines do not respond
0B95	BMC FRU device failure
0B96	BMC SDR Repository failure
0B97	BMC SEL device failure
0BB0	SMBIOS - SROM data read error
0BB1	SMBIOS - SROM data checksum bad
0BD0	1st SMBus device address not acknowledged
0BD1	1st SMBus device Error detected
0BD2	1st SMBus timeout
0C00	RomPilot reports error number xx
None	Expansion ROM not initialized
None	Invalid System Configuration Data
None	System Configuration Data Read error

Code	Error Message
None	Resource Conflict
None	System Configuration Data Write Source
None	NOTICE: Your System Redundant Power Supply is not configured
None	WARNING:IRQ not configured

Table 4-21. Post Error Beep Codes

Beeps	Error	Cause	Recommended Action
1-2-2-3	ROM Checksum Error	—	Change system board
1-3-1-1	DRAM Refresh Test Error	—	Change memory DIMM's
1-3-1-3	Keyboard Controller Test Error	—	Change system board
1-3-3-1	Memory Not Detected	No memory. Can not write to memory	Verify DIMM installation. Change memory DIMM's
	Memory Capacity Check Error	No memory. Can not write to memory	Verify DIMM installation. Change memory DIMM's
1-3-4-1	DRAM Address Test Error	Memory address signal failure	Change DIMM or M/B
1-3-4-3	DRAM Test low byte Error	Memory data signal failure (low)	Change DIMM or M/B
1-4-1-1	DRAM Test high byte Error	Memory data signal failure (high)	Change DIMM or M/B
1-4-3-3	All Memory Group Errors	—	—
2-1-2-3	BIOS ROM Copy-Write Test Error	Error with Shadow RAM	Change system board
2-2-3-1	Unexpected Interrupt Test Error	Unexpected interrupt	Change CPU or system board
2-3-1-3	All Memory Group Errors	Memory address signal failure	Change DIMM or M/B
3-3-1-4	Memory Not Detected	—	—
1-2	Option ROM Initialization Error	Failure to initialize Option ROM BIOS	Change system board or option board
1-2	Video configuration fails	Failure to initialize VGA BIOS	Change option video board or system board
1-2	OPTION ROM Checksum Error	Failure to initialize Option BIOS	Change M/B or option board

4.6 Identifying BIOS and BMC Revision Levels

The following sections provide information to help identify a system's current BIOS and BMC revision levels.

4.6.1 BIOS Revision Level Identification

During system POST, which runs automatically when the system is powered on, the monitor displays several messages, one of which identifies the BIOS revision level currently loaded on the system (see the following example).

```
Phoenix BIOS 4.0 Release 6.0.250A
```

In the example above, BIOS 6.0.250A is the current BIOS revision level loaded on the system.

Note: Press the **Esc** key to see the diagnostic messages.

Note: The BIOS Revision Level stated in the example might not reflect the actual BIOS setting in any particular system.

4.6.2 BMC Revision Level Identification

During system POST, which runs automatically when the system is powered on, system diagnostics are run. Following the memory test diagnostic, several messages appear to inform the user that the mouse was detected and system configuration data updated. The BMC messages follow these.

To identify the system's current BMC revision level, see the following example.

```
Base Board Management Controller
Device ID  :01  Device Revision :00
IPMI Version    :1.0 Firmware Revision    :01.14
Self Test Result:
```

In the example above, Firmware Revision 01.14 is the current BMC revision level loaded on the system.

Note: Press the **Esc** key to see the diagnostic messages. The Firmware Revision level in the example might not reflect the actual BMC revision level in any particular system.

4.7 Adaptec SCSI Utility

The Adaptec SCSI Utility detects the SCSI host adapters on the server board. The Adaptec SCSI Utility is used to:

- Change default values
- Check and/or change SCSI device settings that may conflict with those of other devices in the server.

4.7.1 Running the SCSI Utility

The user can access the Adaptec SCSI Utility when the system is powered on or rebooted. To run the Adaptec SCSI utility, perform the following procedure.

1. Power-on or reboot the system.
2. At the message to “Press Ctrl-A to run SCSI Utility”, press Ctrl+A.
3. Choose the host adapter that needs to be configured.
4. The SCSI utility starts. When the Adaptec SCSI Utility detects more than one AIC-78xx host adapter, it displays a selection menu listing the bus and device number of each adapter. When the selection menu appears, select the channel that should be configured as follows.

Bus : Device : Channel	Selected SCSI Adapter
01 : 04 : A[1]	AIC7899
01 : 04 : B	AIC7899

Note:

1. Internal SCSI connector.

When the adapter is selected, the following options display.

Menu	Description
Configure/View Host Adapter Settings	Configure host adapter and device settings.
SCSI Disk Utilities	The utility scans the SCSI bus for SCSI devices and reports a description of each device. Run these utilities before configuring SCSI devices.

To format a disk, verify disk media, or display a list of devices and their SCSI IDs, select "SCSI Disk Utilities". To configure the adapter or a device, select "Configure/View Host Adapter Settings."

4.7.2 Adaptec SCSI Utility Configuration Settings

The following keys are active for all Adaptec SCSI Utility screens.

Key	Action
Arrows	Up and down arrows move from one parameter to another within a screen.
ENTER	Displays options for a configurable parameter. Selects an option.
ESC	Moves back to previous screen or parameter or EXIT if at the Main menu.
F5	Switches between color and monochrome.
F6	Resets to host adapter defaults.

The following table shows the normal settings for the Adaptec SCSI Utility and provides a place to record any changes made to these settings.

Table 4-22. Adaptec SCSI Utility Setup Configurations

Option	Recommended Setting or Display Only	User Setting
SCSI Bus Interface Definitions		
Host Adapter SCSI ID	7	
SCSI Parity Checking	Enabled	
Host Adapter SCSI Termination	Enabled	
Additional Options		
Boot Device Options	Press Enter for menu	
Boot Channel	A First	
Boot SCSI ID	0	
Boot LUN Number	0	
SCSI Device Configuration	Press Enter for menu	
Sync Transfer Rate (MB/Sec)	160	
Initiate Wide Negotiation	Yes	
Enable Disconnection	Yes	
Send Start Unit Command	Yes	
Enable Write Back Cache	No	
BIOS Multiple LUN Support	No [1]	
Include in BIOS Scan	Yes [1]	
Advanced Configuration Options	Press Enter for menu.	
Plug-and-Play SCAM Support	Disabled	
Reset SCSI Bus at IC Initialization	Enabled	

Option	Recommended Setting or Display Only	User Setting
SCSI Bus Interface Definitions		
Display <Ctrl-A> Messages During BIOS Initialization	Enabled	
Extended BIOS Translation for DOS Drives >1 Gbyte	Enabled	
Verbose/Silent Mode	Verbose	
Host Adapter BIOS (Configuration Utility Reserves BIOS Space)	Enabled[1]	
Domain Validation	Enabled	
Support Removable Disks Under BIOS as Fixed Disks	Disabled[1, 2]	
BIOS Support for Int13 Extensions	Enabled[1]	

Notes:

1. No effect if BIOS is disabled.
2. Do not remove media from a removable media drive if it is under BIOS control.

4.7.3 Exiting Adaptec SCSI Utility

To exit the Adaptec SCSI Utility, press **Esc** until a message prompts you to exit. If changes have been made, the user is prompted to them before exiting.

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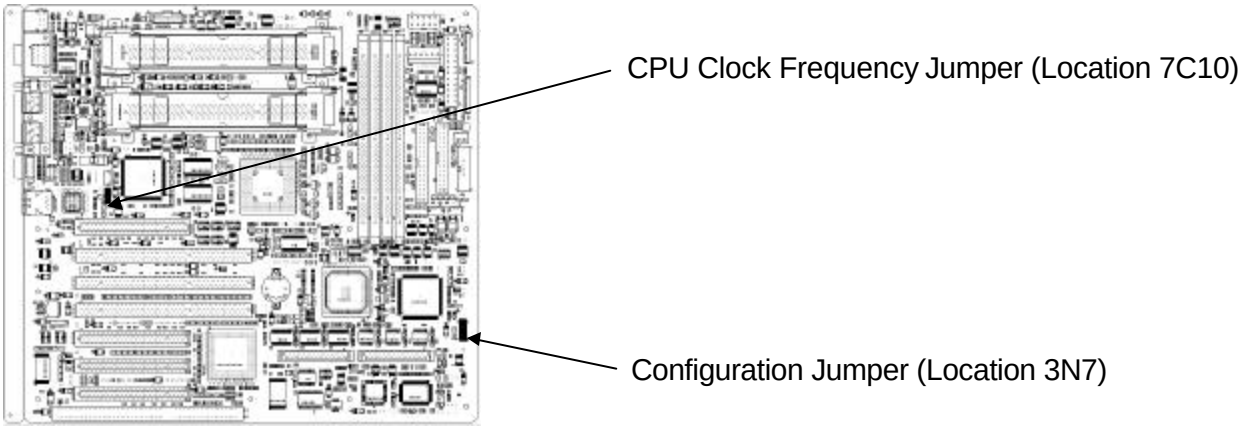
5. Jumpers and Connectors

5.1 Jumpers



5.1.1 Setting Configuration Jumper Block 3N7

Setting a jumper on system board jumper block 3N7 enables the user to clear CMOS or clear a password if it is forgotten. (see the above figure for jumper block location). The following table lists the factory default settings for jumper block TBD. Procedures for setting the jumper on the block follow the table.

Table 5-1. Jumper Block 3N7 Settings

Jumper Pin Numbers	Function	Jumper On/Off	What it does at system reset
1 - 2	CMOS clear	Off, Protect On, Erase	Preserves the contents of CMOS. Clears CMOS.
3 - 4	Password disable	Off, Normal On, Disable	Preserves the password. Disables the password.
5 - 6	Reserved	Off, Not Used	Required. Do Not Change.
7 - 8	Reserved	Off, Not Used	Required. Do Not Change.
9 - 10	BIOS Recovery	Off, Normal On, Recover from Floppy	Required for normal usage. Load BIOS from floppy to recover corrupted image
11 - 12	Spare	Off, in use or lost On, place holder	Jumper is being used or is lost Provides a place to hold jumper.

5.1.1.1 Clearing and Changing a Password

Clear and change a password as follows.

1. Power off the system, unplug the power cord(s), and remove the left panel as described in Section 4 of this guide.
2. Use needle nose pliers or your fingers to remove the spare jumper from pins 11-12 on jumper block 3N7.
3. Reinstall the jumper on pins 3-4 (Password Disable) of jumper block 3N7.

4. Reinstall the left panel, plug in the power cord(s), and power on the system.
5. While waiting for POST to complete, press the **F2** key to enter BIOS setup.
6. This automatically clears all passwords, provided you save and exit the BIOS setup.
7. Power off the system, unplug the power cord(s), and remove the left panel.
8. Remove the Password Disable jumper from pins 3-4 and store the jumper on pins 11-12.
9. Replace the left panel, plug in the power cord(s), and power on the system.
10. To specify a new password run the BIOS Setup Utility as described earlier in this section.

5.1.1.2 Clearing CMOS

Clear CMOS as follows.

1. Power off the system, unplug the power cord(s), and remove the left panel as described in Section 0 of this document.
2. Use needle-nose pliers or your fingers to remove the spare jumper from pins 11-12 on jumper block 3N7.
3. Position the jumper over pins 1-2 on jumper block 3N7.
4. Replace the left panel, plug in the power cable(s), and power on the system.
5. After POST completes, power down the system, unplug the power cable(s), and remove the left panel.
6. Remove the jumper from pins 1-2 and store the jumper on pins 11-12.
7. Replace the left panel and connect system cables.
8. Power on the system, press **F2** at the prompt to run the BIOS Setup utility, and select “Get Default Values” at the Exit menu.

5.1.2 Setting Processor Frequency Jumper Block 7C10

The jumpers on block 7C10 set the processor speed for the installed processor(s). The following table lists the settings for jumper block 7C10. Procedures for setting the jumpers follow the table.

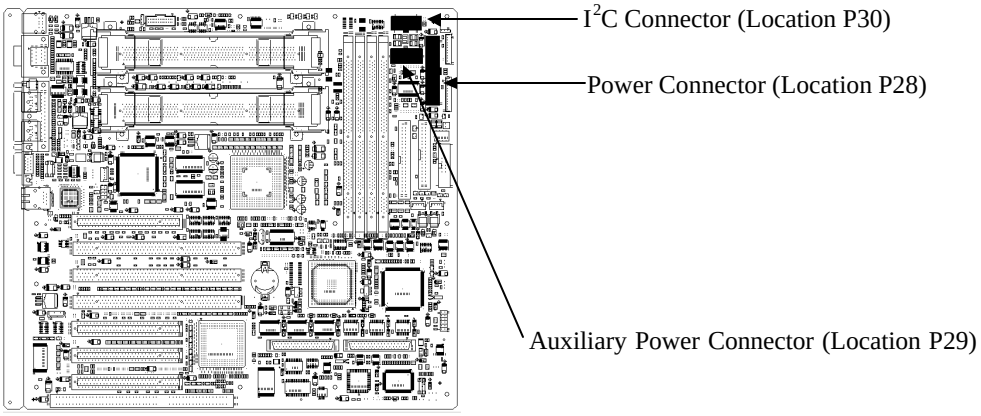
Table 5-2. Jumper Block 7C10 Settings

Processor Frequency (MHz)	Jumper Settings			
	1-2	3-4	5-6	7-8
600	Not Jumpered	Jumpered	Jumpered	Not Jumpered
667	Not Jumpered	Not Jumpered	Jumpered	Jumpered
733	Not Jumpered	Not Jumpered	Jumpered	Not Jumpered
800	Jumpered	Jumpered	Not Jumpered	Jumpered
867	Jumpered	Jumpered	Not Jumpered	Not Jumpered
933	Jumpered	Not Jumpered	Not Jumpered	Jumpered
1000	Jumpered	Not Jumpered	Not Jumpered	Not Jumpered
1067	Not Jumpered	Jumpered	Not Jumpered	Jumpered

Set the processor frequency jumpers as follows.

1. Power off the system, unplug the power cord(s), and remove the left panel as described in Section 4 of this document.
2. From the “Jumper Block 7C10 Settings” table, select the processor frequency matching the installed processor.
3. Use needle nose pliers or your fingers to move the jumpers to the settings shown in the “Jumper Block 7C10 Settings” table.
4. Reinstall the left panel, plug in the power cord(s), and power on the system.

5.1.3 Power Connections



5.1.4 Main Power Connector (P28)

Table 5-3. Main Power Connector Pinout

Pin	Signal	Wire color	Pin	Signal	Wire Color
1	+3.3 VDC	Orange	13	+3.3 VDC	Orange
2	+3.3 VDC	Orange	14	-12 VDC	Blue
3	COM	Black	15	COM	Black
4	+5 VDC	Red	16	PS-ON_L	Green
5	COM	Black	17	COM	Black
6	+5 VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR-GD	Grey	20	N.C.	N.C.
9	5 VSB	Purple	21	+5 VDC	Red
10	+12 VDC	Yellow	22	+5 VDC	Red
11	+12 VDC	Yellow	23	+5 VDC	Red
12	+3.3 VDC	Orange	24	COM	Black

5.1.5 Auxilary Power Connector (P29)

Table 5-4. Auxiliary Power Connector Pinout

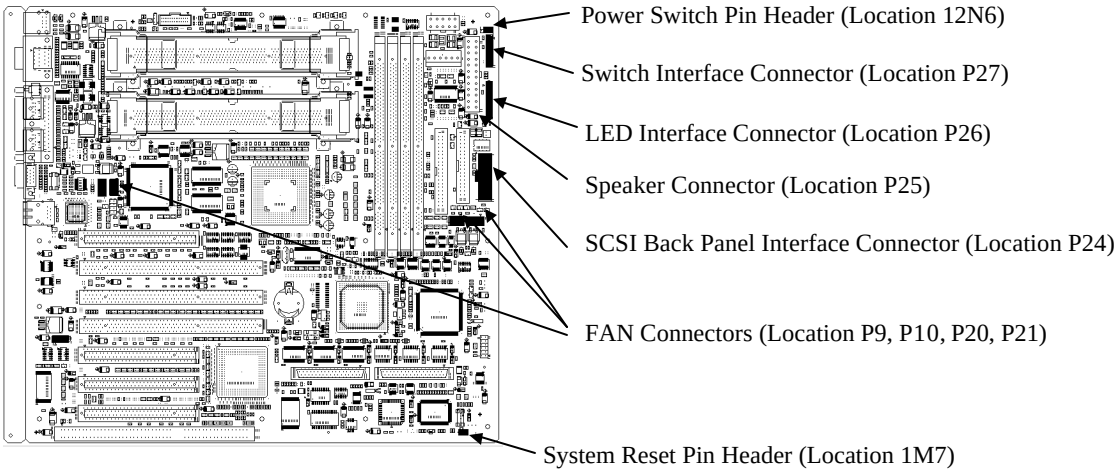
Pin	Signal	Wire Color
1	+5 VDC	Red
2	+3.3 VDC	Orange
3	+3.3 VDC	Orange
4	COM	Black
5	COM	Black
6	COM	Black

5.1.6 I^2C Power Connector (P30)

Table 5-5. I^2C Power Connector Pinout

Pin	Signal	Pin	Signal
1	N.C.	6	N.C.
2	N.C.	7	N.C.
3	+3.3 VDC	8	N.C.
4	N.C.	9	I^2C Data
5	N.C.	10	I^2C Clock

5.1.7 Other Connectors



5.1.8 Power ON/Off Switch Connector (12N6)

Table 5-6. Power On/Off Switch Connector Pinout

Pin	Signal
1	STANDBY +5 VDC
2	GND

5.1.9 Reset Switch Connector (1M7)

Table 5-7. Reset Switch Connector Pinout

Pin	Signal
1	GND
2	RESET BUTTON

5.1.10 LED Interface Connector (P26)

Table 5-8. LED Interface Connector Pinout

Pin	Signal	Pin	Signal
1	Power LED+	7	Status LED (Green) +
2	COM	8	COM
3	150 Ω pulldown	9	Status LED (Red) +
4	SCSI LED (Green) + output	10	Sleep LED (Green)
5	COM	11	COM
6	SCSI LED (Red) + output	12	Sleep LED (Red)

5.1.11 Switch Interface Connector (P27)

Table 5-9. Switch Interface Connector Pinout

Pin	Signal	Pin	Signal
1	Power Switch	6	COM
2	COM	7	Chassis Side Panel Intrusion Switch
3	Sleep Switch	8	COM
4	COM	9	N.C.
5	Chassis Front Panel Intrusion Switch	10	COM

5.1.12 Intelligent Fan Connectors (P9, P10, P20, P21)

Table 5-10. Intelligent Fan Connector Pinout

Pin	Signal
1	+ 12 VDC
2	COM
3	IPMB CLK
4	N.C.

5.1.13 Speaker Connector (P25)

Table 5-11. Speaker Connector Pinout

Pin	Signal
1	SPEAKER
2	GND

5.1.14 Diskette Drive Connector

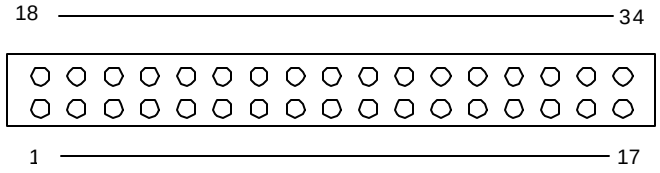


Figure 5-1. Diskette Drive Connector Pin Diagram

Table 5-12. Diskette Drive Connector Pinout

Pin	Signal	Pin	Signal
1	GND	18	FD_DENSEL
2	GND	19	No Connection
3	GND	20	FD_MDAID
4	GND	21	FD_INDEX_L
5	GND	22	FD_MON0_L
6	GND	23	FD_SEL1_L
7	GND	24	FD_SEL0_L
8	GND	25	FD_MON1_L
9	GND	26	FD_DIR_L
10	GND	27	FD_STEP_L
11	GND	28	FD_WDATA_L
12	GND	29	FD_WGATE_L
13	GND	30	FD_TRK0_L
14	GND	31	FD_WPT_L
15	GND	32	FD_RDATA_L
16	GND	33	FD_SIDE_L
17	GND	34	FD_DCHG_L

5.1.15 SVGA Video Port

Table 5-13. Video Port Connector Pinout

Pin	Signal	Pin	Signal
1	Red	9	NC
2	Green	10	GND
3	Blue	11	NC
4	NC	12	DDCDAT
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDCCLK
8	GND		

5.1.16 Keyboard and Mouse Connectors

The keyboard and mouse connectors are functionally equivalent.

Table 5-14. Keyboard and Mouse Connector Pinouts

Pin	Keyboard signal	Pin	Mouse signal
1	KEYDAT	1	MSEDAT
2	NC	2	NC
3	GND	3	GND
4	FUSED_VCC (+5 V)	4	FUSED_VCC (+5 V)
5	KEYCLK	5	MSECLK
6	NC	6	NC

5.1.17 Parallel Port

Table 5-15. Parallel Port Connector Pinout

Pin	Signal	Pin	Signal
1	STROBE_L	10	ACK_L
2	Data bit 0	11	Busy
3	Data bit 1	12	PE
4	Data bit 2	13	SLCT
5	Data bit 3	14	AUTO_L
6	Data bit 4	15	ERROR_L
7	Data bit 5	16	INIT_L
8	Data bit 6	17	SLCTIN_L
9	Data bit 7	18–25	GND

5.1.18 Serial Ports COM1 and COM2

Table 5-16. Serial Ports COM1 and COM2 Connector Pinout

Pin	Signal	Description
1	DCD	Data carrier detected
2	RXD	Receive data
3	TXD	Transmit data
4	DTR	Data terminal ready
5	GND	Ground
6	DSR	Data set ready
7	RTS	Return to send
8	CTS	Clear to send
9	RIA	Ring indication active

5.1.19 RJ-45 LAN Connector

Table 5-17. RJ-45 LAN Connector Pinout

Pin	Signal	Description
1	TX+	Transmit data plus—the positive signal for the TD differential pair contains the serial output data stream transmitted onto the network
2	TX-	Transmit data minus—the negative signal for the TD differential pair contains the same output as pin 1
3	RX+	Receive data plus—the positive signal for the RD differential pair contains the serial input data stream received from the network
4	NC	
5	NC	
6	RX-	Receive data minus—the negative signal for the RD differential pair contains the same input as pin 3
7	NC	
8	NC	

5.1.20 USB Connectors

Table 5-18. USB 1 and USB 2 Connector Pinout

USB 1 Pin	Signal	USB 2 Pin	Signal
1	+5 VDC	1	+5 VDC
2	USB_P1_N	2	USB_P0_N
3	USB_P1_P	3	USB_P0_P
4	GND	4	GND

5.1.21 Ultra SCSI Connector

Table 5-19. Ultra SCSI Connector Pinout

Pin	Signal	Pin	Signal
1-16	GND	49-50	GND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	NC	53	NC
20-34	GND	54	GND
35	SCD12_L	55	SATN_L
36	SCD13_L	56	GND
37	SCD14_L	57	SBSY_L
38	SCD15_L	58	SACK_L
39	SCDPH_L	59	RESET_L
40	SCD0_L	60	SMSG_L
41	SCD1_L	61	SSEL_L
42	SCD2_L	62	SCD_L
43	SCD3_L	63	SREQ_L
44	SCD4_L	64	SI/O_L
45	SCD5_L	65	SCD8_L
46	SCD6_L	66	SCD9_L
47	SCD7_L	67	SCD10_L
48	SCDP_L	68	SCD11_L

5.1.22 Ultra-160/m SCSI Connector

Table 5-20. Ultra-160/m SCSI Connector Pinout

Pin	Signal	Pin	Signal
1	SCDAP12	35	SCDAN12_L
2	SCDAP13	36	SCDAN13_L
3	SCDAP14	37	SCDAN14_L
4	SCDAP15	38	SCDAN15_L
5	SCDAPHP	39	SCDAPHN_L
6	SCDAP0	40	SCDAN0_L
7	SCDAP1	41	SCDAN1_L
8	SCDAP2	42	SCDAN2_L
9	SCDAP3	43	SCDAN3_L
10	SCDAP4	44	SCDAN4_L
11	SCDAP5	45	SCDAN5_L
12	SCDAP6	46	SCDAN6_L
13	SCDAP7	47	SCDAN7_L
14	SCDAPLP	48	SCDAPLN
15	GND	49	GND
16	DIFFSENSA	50	GND
17	TRMPWRA	51	TRMPWRA

Pin	Signal	Pin	Signal
18	TRMPWRA	52	TRMPWRA
19	No Connection	53	No Connection
20	GND	54	GND
21	ATNAP	55	ATNAN_L
22	GND	56	GND
23	BSY	57	BSYAN_L
24	ACK	58	ACKAN_L
25	RSTAP	59	RSTAN_L
26	MSGAP	60	MSGAN_L
27	SELAP	61	SELAN_L
28	CDAP	62	CDAN
29	REQAP	63	REQAN_L
30	IOAP	64	IOAN_L
31	SCDAP8	65	SCDAN8_L
32	SCDAP9	66	SCDAN9_L
33	SCDAP10	67	SCDAN10_L
34	SCDAP11	68	SCDAN11_L

5.1.23 IDE Connector

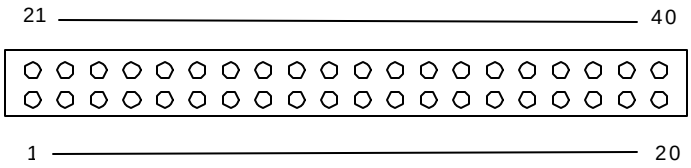


Figure 5-2. IDE Connector Pin Diagram

If no IDE drives are present, no IDE cable should be connected. If a single IDE drive is installed, it must be connected at the end of the cable.

Table 5-21. IDE Connector Pinout

Pin	Signal	Pin	Signal
1	RESET_L	21	GND
2	DD7	22	DD8
3	DD6	23	DD9
4	DD5	24	DD10
5	DD4	25	DD11
6	DD3	26	DD12
7	DD2	27	DD13
8	DD1	28	DD14
9	DD0	29	DD15
10	GND	30	No Connection
11	IDEDRQ	31	GND
12	DIOW_L	32	GND
13	DIOR_L	33	GND

Pin	Signal	Pin	Signal
14	IORDY	34	GND
15	IDEDAK_L	35	GND
16	IDEIRQ	36	No Connection
17	IDESA1	37	No Connection
18	IDESA0	38	IDESA2
19	IDECS0_L	39	IDECS1_L
20	Keyed	40	GND

5.1.24 32-Bit PCI Connector

Table 5-22. 32-Bit PCI Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST_L	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	TCK	A33	+3.3 V	B33	CBE2_L
A3	TMS	B3	GND	A34	FRAME_L	B34	GND
A4	TDI	B4	TD0 (NC)	A35	GND	B35	IRDY_L
A5	+5 V	B5	+5 V	A36	TRDY_L	B36	+3.3 V
A6	INTA_L	B6	+5 V	A37	GND	B37	DEVSEL_L
A7	INTC_L	B7	INTB_L	A38	STOP_L	B38	GND
A8	+5 V	B8	INTD_L	A39	+3.3 V	B39	LOCK_L
A9	Reserved	B9	PRSNT1_L	A40	SDONE	B40	PERR_L
A10	+5 V	B10	Reserved	A41	SBO_L	B41	+3.3 V
A11	Reserved	B11	PRSNT2_L	A42	GND	B42	SERR_L
A12	GND	B12	GND	A43	PARITY	B43	+3.3 V
A13	GND	B13	GND	A44	AD15	B44	CBE1_L
A14	Reserved	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST_L	B15	GND	A46	AD13	B46	GND
A16	+5 V	B16	PCICLK	A47	AD11	B47	AD12
A17	GNT_L	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ_L	A49	AD9	B49	GND
A19	PME_L	B19	+5 V	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	+3.3 V	B21	AD29	A52	CBE0_L	B52	AD8
A22	AD28	B22	GND	A53	+3.3 V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	+3.3 V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	+3.3 V	A56	GND	B56	AD3
A26	IDSEL	B26	CBE3_L	A57	AD2	B57	GND
A27	+3.3 V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	+5 V	B59	+5 V
A29	AD20	B29	AD21	A60	REQ64_L	B60	ACK64_L
A30	GND	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

5.1.25 64-Bit PCI Connector

Table 5-23. 64-Bit PCI Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST_L	B1	-12 V	A48	GND	B48	AD10
A2	+12 V	B2	TCK	A49	AD9	B49	M66EN
A3	TMS	B3	GND	A50	KEY	B50	KEY
A4	TDI	B4	TD0 (NC)	A51	KEY	B51	KEY
A5	+5 V	B5	+5 V	A52	CBE0_L	B52	AD8
A6	INTA_L	B6	+5 V	A53	+3.3 V	B53	AD7
A7	INTC_L	B7	INTB_L	A54	AD6	B54	+3.3 V
A8	+5 V	B8	INTD_L	A55	AD4	B55	AD5
A9	Reserved	B9	PRSNT1_L	A56	GND	B56	AD3
A10	+5 V	B10	Reserved	A57	AD2	B57	GND
A11	Reserved	B11	PRSNT2_L	A58	AD0	B58	AD1
A12	GND	B12	GND	A59	+5 V	B59	+5 V
A13	GND	B13	GND	A60	REQ64_L	B60	ACK64_L
A14	Reserved	B14	Reserved	A61	+5 V	B61	+5 V
A15	RST_L	B15	GND	A62	+5 V	B62	+5 V
A16	+5 V	B16	PCICLK	A63	GND	B63	Reserved
A17	GNT_L	B17	GND	A64	CBE7_L	B64	GND
A18	GND	B18	REQ_L	A65	CBE5_L	B65	CBE6_L
A19	PME_L	B19	+5 V	A66	+3.3 V	B66	CBE4_L
A20	AD30	B20	AD31	A67	Parity	B67	GND
A21	+3.3 V	B21	AD29	A68	AD62	B68	AD63
A22	AD28	B22	GND	A69	GND	B69	AD61
A23	AD26	B23	AD27	A70	AD60	B70	+3.3 V
A24	GND	B24	AD25	A71	AD58	B71	AD59
A25	AD24	B25	+3.3 V	A72	GND	B72	AD57
A26	IDSEL	B26	CBE3_L	A73	AD56	B73	GND
A27	+3.3 V	B27	AD23	A74	AD54	B74	AD55
A28	AD22	B28	GND	A75	+3.3 V	B75	AD53
A29	AD20	B29	AD21	A76	AD52	B76	GND
A30	GND	B30	AD19	A77	AD50	B77	AD51
A31	AD18	B31	+3.3 V	A78	GND	B78	AD49
A32	AD16	B32	AD17	A79	AD48	B79	+3.3 V
A33	+3.3 V	B33	CBE2_L	A80	AD46	B80	AD47
A34	FRAME_L	B34	GND	A81	GND	B81	AD45
A35	GND	B35	IRDY_L	A82	AD44	B82	GND
A36	TRDY_L	B36	+3.3 V	A83	AD42	B83	AD43
A37	GND	B37	DEVSEL_L	A84	+3.3 V	B84	AD41
A38	STOP_L	B38	GND	A85	AD40	B85	GND
A39	+3.3 V	B39	LOCK_L	A86	AD38	B86	AD39
A40	SDONE	B40	PERR_L	A87	GND	B87	AD37
A41	SBO_L	B41	+3.3 V	A88	AD36	B88	+3.3 V
A42	GND	B42	SERR_L	A89	AD34	B89	AD35

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A43	PARITY	B43	+3.3 V	A90	GND	B90	AD33
A44	AD15	B44	CBE1_L	A91	AD32	B91	GND
A45	+3.3 V	B45	AD14	A92	Reserved	B92	Reserved
A46	AD13	B46	GND	A93	GND	B93	Reserved
A47	AD11	B47	AD12	A94	Reserved	B94	GND

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6. Electrical, Environmental, & Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the SBT2 server board. This is a board-level specification only. System specifications are beyond the scope of this document.

6.1 Absolute Maximum Ratings

Operation of SBT2 at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 6-1. Absolute Maximum Ratings

Operating Temperature	0°C to +55°C[1]
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V[2]
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

Notes:

1. Chassis design must provide proper airflow to avoid exceeding SEC Pentium III Xeon Processor maximum case temperature.
2. V_{DD} means supply voltage for the device.

Further topics in this section specify normal operating conditions for SBT2.

6.2 Electrical Specifications

DC specifications for SBT2 power connectors and module power budgets are summarized here. Electrical characteristics for major connector interfaces, including DC and AC specifications, can be obtained from the *PCI Local Bus Specification* Revision 2.1.

6.2.1 Power Connection

The main power supply connection is obtained using the 24-pin SSI connector. The following table defines the pin-outs and wire gauge/color for this connector.

Table 6-2. 24-pin Main Power Connector Pin-out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	COM	Black	15	COM	Black
4	+5Vdc	Red	16	PS-ON	Green
5	COM	Black	17	COM	Black
6	+5Vdc	Red	18	COM	Black
7	COM	Black	19	COM	Black

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
8	PWR OK	Gray	20	-5V	White
9	5VSB	Purple	21	+5Vdc	Red
10	+12Vdc	Yellow	22	+5Vdc	Red
11	+12Vdc	Yellow	23	+5Vdc	Red
12	+3.3Vdc	Orange	24	COM	Black

The following table defines the pin-outs and wire gauge/color for the auxiliary power connector.

Table 6-3. 6-pin Auxiliary Power Connector Pin-out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	COM	Black	4	+3.3Vdc	Orange
2	COM	Black	5	+3.3Vdc	Orange
3	COM	Black	6	+5Vdc	Red

6.2.2 Power Consumption

The following table shows the required power for the SBT2 server board. This is for the board only and does not include other components that may be necessary in a funcitonal system.

Table 6-4. SBT2 Power Supply Voltage Specification

Voltage	Current		Nom	Max	Units	Tolerance
+5V	7.96A	maximum continuous current (includes 1.5A for mouse, keyboard, and USB / does not include processor or memory power requirements)	3.30	3.46	V	-3/+5%
+5Vstby	.5A	maximum continuous current	5.00	5.25	V	-4/+5%
+12V	0	maximum continuous current	12.00	12.60	V	+/-5%
+3.3V	4.24A	maximum continuous current	-12.00	-12.60	V	+10%
-5V	0	maximum continuous current	-5.00	-5.25	V	+10%
-12V	0	maximum continuous current	+5.00	+5.25	V	+/-5%

7. Regulatory and Integration Information

7.1 Product Regulatory Compliance

The SBT2 complies with the following safety regulations, and has been verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible host Intel product.

7.1.1 Product Safety Compliance

- UL 1950 – CSA 950 (US/Canada)
- EN 60 950 – (European Union)
- IEC60 950 – (International)
- CE – Low Voltage Directive (73/23/EEC) (European Union)
- EMKO-TSE – (74-SEC) 207/94 (Nordics)

7.1.2 Product EMC Compliance

To ensure EMC product regulation compliance, the end system must be used with a shield LAN cable.

- FCC (Class A Verification) – Radiated & Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated & Conducted Emissions (Canada)
- CISPR 22 (Class A) – Radiated & Conducted Emissions (International)
- EN55022 (Class A) – Radiated & Conducted Emissions (European Union)
- EN55024 (Immunity) (European Union)
- EN61000-3-2 & -3 (Power Harmonics & Fluctuation and Flicker)
- CE – EMC Directive (89/336/EEC) (European Union)
- VCCI (Class A) – Radiated & Conducted Emissions (Japan)
- AS/NZS 3548 (Class A) – Radiated & Conducted Emissions (Australia / New Zealand)
- RRL (Class A) (Korea)
- BSMI (Class A) (Taiwan)

7.1.3 Product Regulatory Compliance Markings

This product is provided with the following Product Certification Markings.

- UL / cUL Listing Mark
- CE Mark
- German GS Mark
- Russian GOST Mark
- FCC, Class A Verification Marking
- ICES-003 (Canada EMC Compliance Marking)
- VCCI, Class A Mark
- Australian C-Tick Mark
- Taiwan BSMI Class A Certification Marking

7.2 Electromagnetic Compatibility Notices

7.2.1 USA

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124

Telephone: 1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals, that are not shielded and grounded may result in interference to radio and TV reception.

7.2.2 FCC Verification Statement

Product Type: 133-659719; SBT2
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497

Telephone: 1 (800)-INTEL4U or 1 (800) 628-8686

7.2.3 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadian des Communications.

English translation:

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

7.2.4 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

7.2.5 Japan EMC Compatibility

Electromagnetic Compatibility Notices (International)

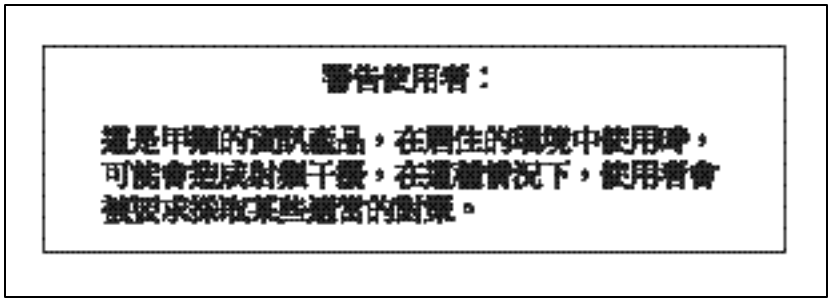
この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation:

This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

7.2.6 BSMI (Taiwan)

The BSMI Certification number and the following warning is located on the product safety label which is located on the bottom side (pedestal orientation) or side (rack mount configuration).



7.3 Replacing the Back up Battery

The lithium battery on the server board powers the real time clock (RTC) for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

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