Intel® Server Board S870BN4 Board Set

Technical Product Specification

Revision 2.5

June, 2003

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
June, 2003	2.5	Initial release to external users.

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1. Introduction

The Intel® Server Board S870BN4 Board Set Technical Product Specification (TPS) provides the specifications for the Intel® Server System SR870BN4 board set. This system is designed to utilize the first microprocessor based on the Intel® Itanium® Processor Family architecture, known as the Itanium® 2 processor. The Itanium 2 processor expands the Intel® Architecture (IA) with new levels of performance and features. The Server System SR870BN4 design is based on the Intel® E8870 chip set.

This document is a combination of the processor board, memory board, midplane board, I/O board, and I/O riser specifications that define the firmware components of the Server System SR870BN4. The purpose of this document is to pull together pertinent information about all of the components.

This document is subject to change. Every effort has been made to ensure that the information contained in this document is correct. Some of the reference documents that were used to create this document have planned revisions that will require this document to be updated.

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2. Processor Baseboard

This chapter describes the architecture of the Intel® Itanium® 2/Intel® E8870 processor baseboard. The baseboard contains the Itanium 2 processors, the Intel E8870 Scalabale Node Controller-McKinley (SNC-M) chip, two memory board connectors, and support circuits. The two memory boards plug into the processor baseboard via two high-density MegArray* connectors. The processor baseboard plugs into the midplane of an Server System SR870BN4 through a 6-row X 60-column, 360-pin, very high density metric (VHDM) connector for connection to the I/O subsystem of an Itanium 2-based server.

2.1 Features

The processor baseboard has the following features:

- Four Itanium 2 processor sockets
- 48-V DC-to-DC (D2D) converter power pod for each Itanium 2 processor
- D2D voltage converters for 2.5 V, 3.3 V
  - Two 48 V to 2.5 V plug-in D2D for DDR memory support
  - One 48 V to 3.3 V plug-in D2D
- Embedded Regulators for 1.2 V, 1.5 V, 1.8 V and 1.3 V
  - 3.3 V to 1.2 V
  - 3.3 V to 1.5 V
  - 3.3 V to 1.8 V
  - 1.8 V to 1.3 V linear regulator
- One SNC-M component of the Intel E8870 chip set
- Three Firmware Hubs (FWH) for BIOS and system configuration utility (SCU) software
- Two memory board connectors supporting 2 Rambus channels each
- One VHDM 360-pin connector for I/O connections
- Debug port for use with an In-Target Probe (ITP) (debug only)
- Two I^2C system management buses (SMBus)

2.2 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. Information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized below:

Section 2.3: Introduction
Provides an overview of the processor baseboard showing functional blocks and board layout.

Section 2.4: Functional Architecture
Describes the way each functional block of the processor baseboard works.

Section 2.5: Signal Descriptions
Summarizes the processor baseboard connector interface signal pin

names and their meanings. Their mnemonics appear throughout this chapter.

Section 2.6: Electrical, Mechanical, and Environmental Specifications
Specifies operational parameters and considerations, and connector pinouts.

2.3 Introduction

The Server Board S870BN4 Itanium 2/E8870 processor baseboard is designed for use as a building block for 4-way, and greater, processor systems. The Itanium 2 processor baseboard provides the support for one to four Itanium 2 processors, each with a dedicated power pod. The system controller is provided via the Intel® E8870 SNC-M chip that interfaces with the Itanium 2 processor system bus, DDR (Double Data Rate) memory via Rambus interface and I/O subsystem via the scalability port. The LPC (Low Pin Count) interface allows for localized FWH support. The processor baseboard design is partitioned according to the following functional blocks:

- Itanium 2 processors
- E8870 SNC-M chip for the Itanium 2-based system bus, memory, and scalability port interface
- Rambus memory interface and connector
- Scalability port/system power interface and connector
- Clock distribution
- Voltage regulators/Itanium 2 power pod
- Processor/system reset
- Server management
- Debug port for ITP

The following figure shows a physical representation of the processor baseboard without memory boards or Itanium 2 processors installed.

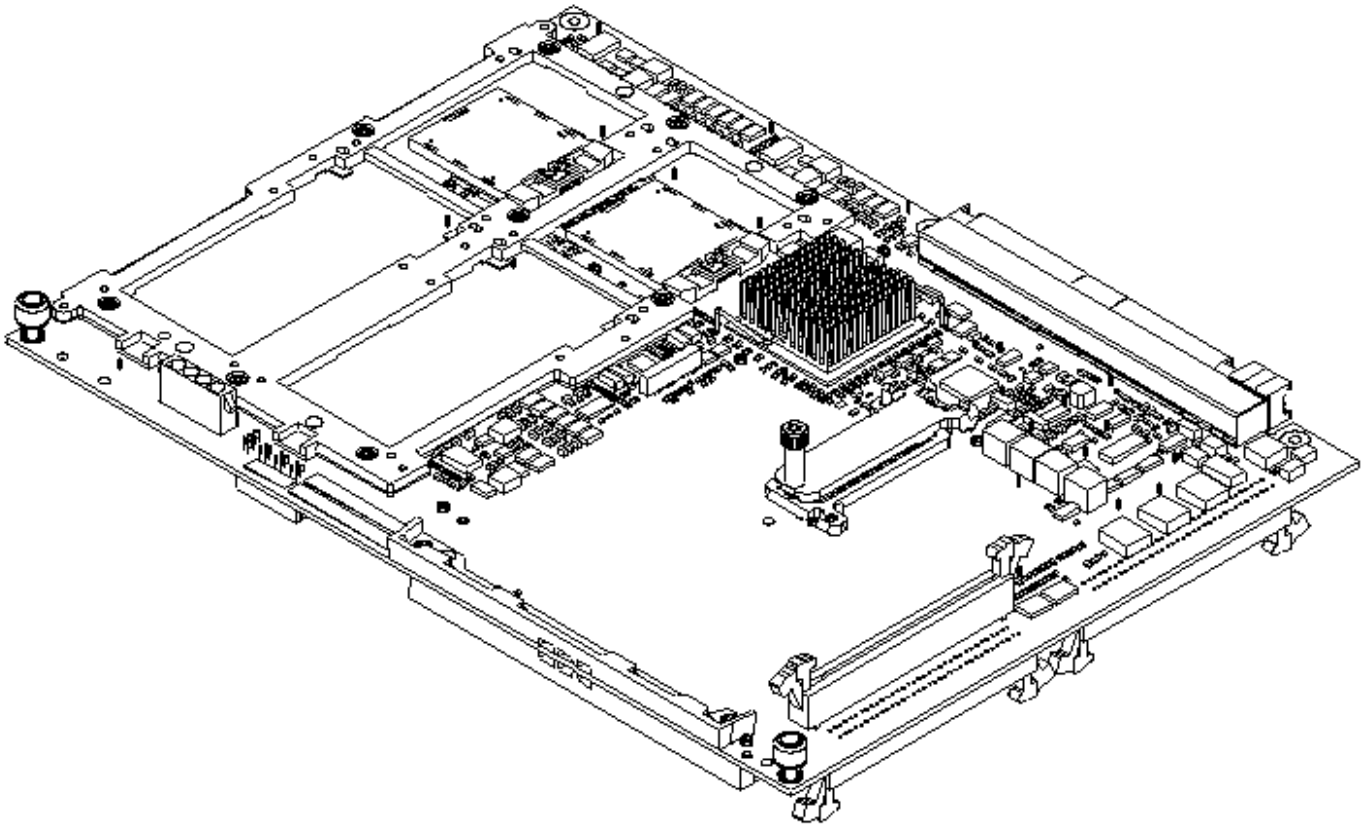


Figure 2-1. Processor Board Complex without Memory Board

2.3.1 Block Diagram

The following figure illustrates the general architecture of the processor baseboard.

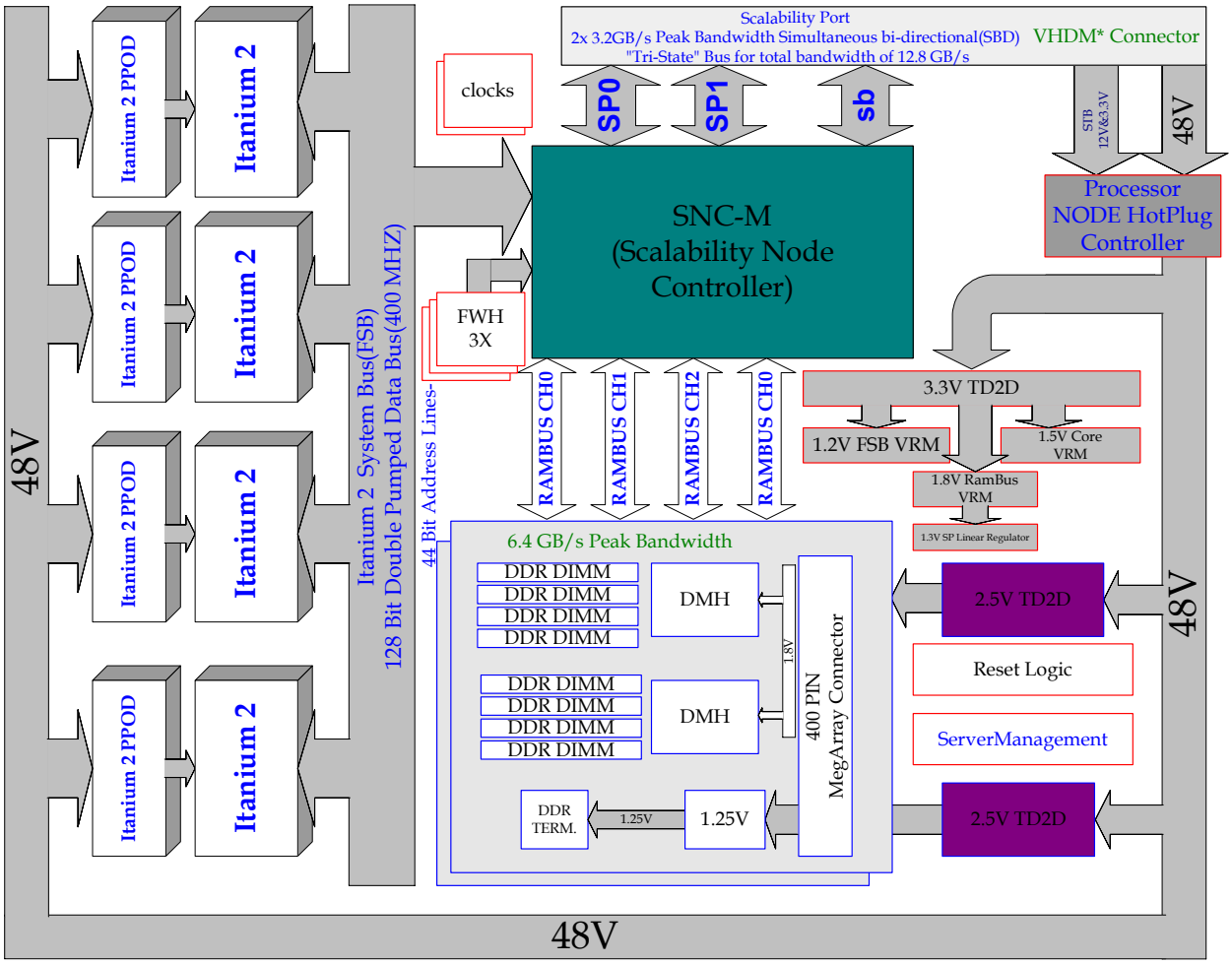


Figure 2-2. Processor Baseboard Block Diagram

2.3.2 Placement Diagram

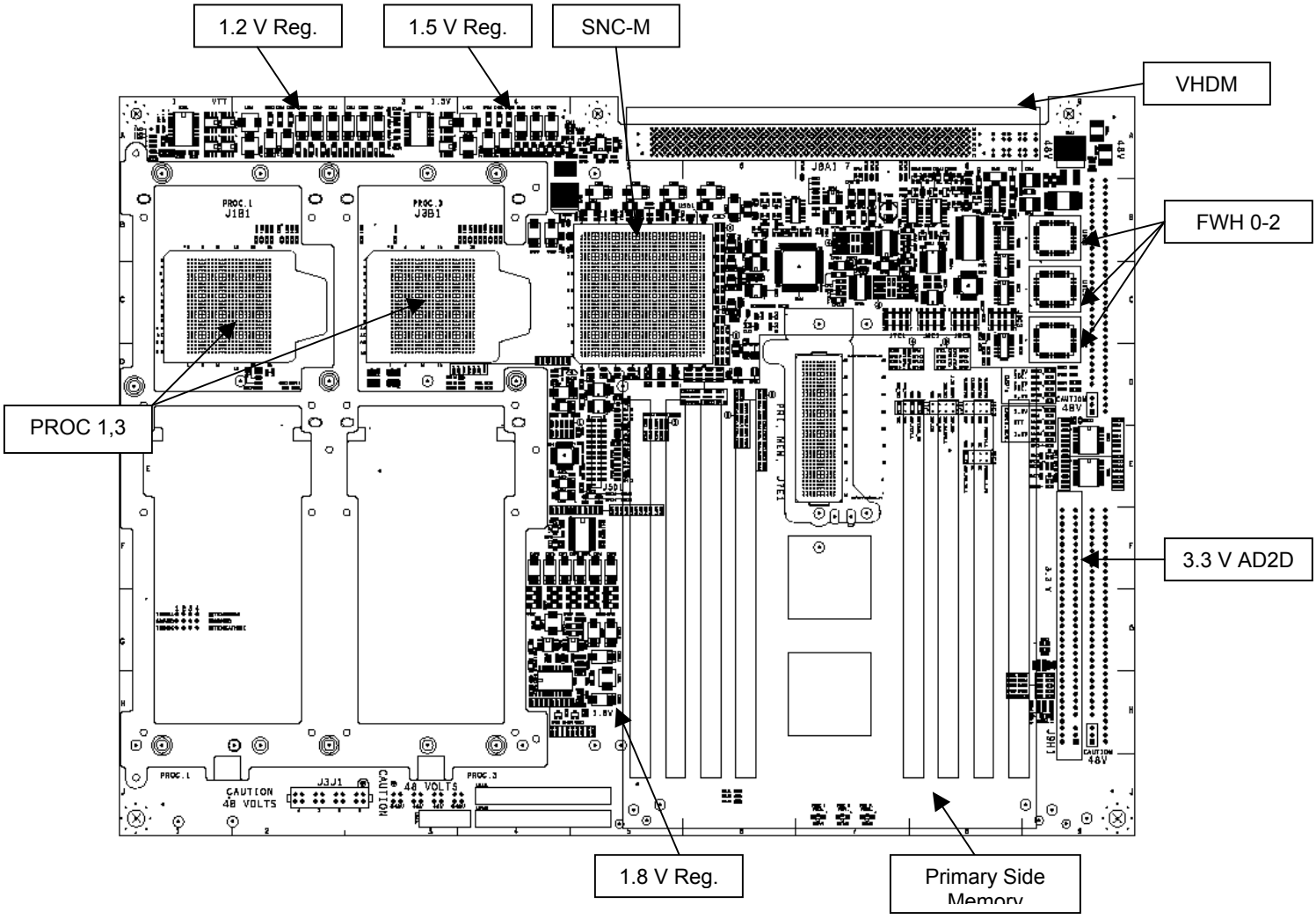


Figure 2-3. Processor Baseboard Component Location (Primary Side)

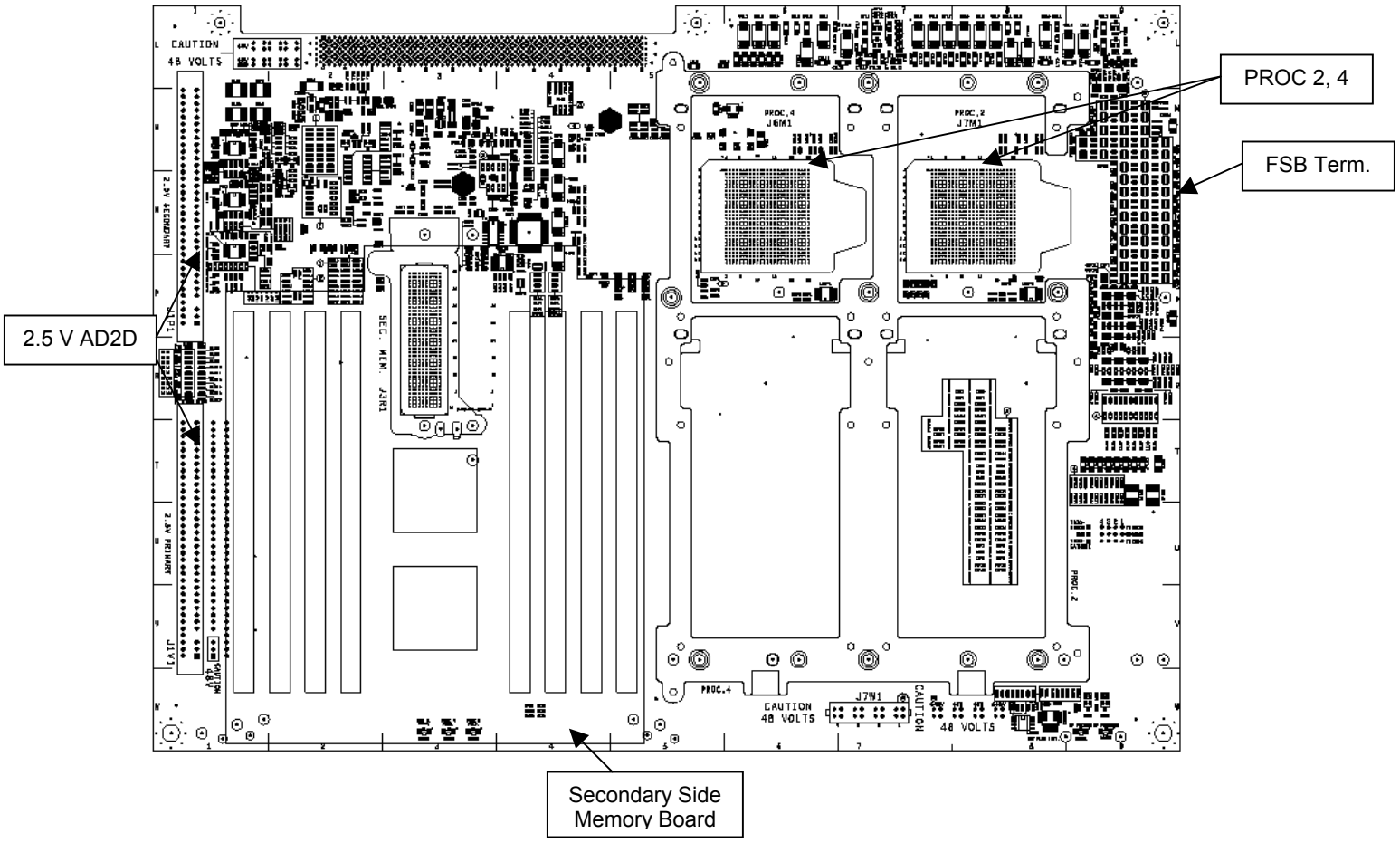


Figure 2-4. Processor Baseboard Component Location (Secondary Side)

Figure 2-3 and Figure 2-4 show the placement of the major components and connectors on the processor baseboard.

2.4 Functional Architecture

This section provides a more detailed architectural description of the processor baseboard functional blocks.

2.4.1 Itanium 2 Front Side Bus (FSB)

All four Itanium 2 processors are connected to the E8870/SNC-M through the system (Front Side) bus. The system bus consists of a 44-bit address bus and a 128-bit data bus. The address and control signals have parity protection. The data bus has Error Correcting Code (ECC) protection on each 64-bit half of the 128-bit data bus. The bus signals use Assisted Gunning Transceiver Logic (AGTL+) technology and are functionally compatible with the Itanium processor bus. The system bus strobes data on both the rising and falling edges of the 200-MHz clock to achieve an effective source synchronous transfer rate of 400 MT/s. The bus structure can support a load limit of five devices: four processors and one SNC-M. The processors are mounted on both sides of the processor baseboard to limit the length of the bus.

The system bus signals are daisy chained with termination resistors at both ends of the bus (the SNC-M termination is on-die). This eliminates the need for a termination card when a processor is absent. The processor baseboard supports up to four processors.

The features of the system bus are:

- Full support for 4-way multiprocessing
- 200 MHz with 2x strobes for equivalent 400-Mhz operation
- 6.4 GB/s peak bandwidth
- 128-bit data bus
- 128-byte cache line size
- Utilization of 44 bits of the 50-bit processor address bus
- Parity protection on address and control signals; ECC protection on the data signals
- AGTL+ bus driver technology
- Enhanced defer feature for out-of-order data delivery
- System bus interrupt delivery (SAPIC architecture)
- Supports Itanium 2 processor special cycles

2.4.2 Memory Interface

The Itanium 2/E8870 memory subsystem consists of two memory boards that connect to the processor baseboard through a 400-pin MegArray connector. Each memory board contains two memory repeater (DMH) chips, one per RDRAM channel, that support up to four 72-bit wide DIMM modules. The DMH translates Rambus memory transactions to SDRAM DDR. The DIMM modules can be 64, 128, 256, 512 Mbit, 1 and 2 Gbit technology. Each memory board can support up to 16 GB of system memory.

Note: The DIMMs off each DMH must be symetrical with the DIMMs of all the other DMHs. That is, each DMH must hold the same type of DIMM on DMH 1, 2, 3, and 4. The memory upgrade granularity is the row of four DIMMs, one on each main channel, which collectively provide a cache line.

The SNC-M and DMH incorporate a 400 MHz Rambus interface. Data is transferred on each edge of the clock giving an equivalent 800 MHz bus, 16-bit data and 2-bit ECC running at 1.6 GT/s per port. Each of the four Rambus ports on the SNC-M is connected to one DMH.

The second memory port is located on the secondary side of the processor baseboard, in order to minimize the baseboard dimension and to shorten the address/control bus to the memory module. As a result, the DIMMs of the first memory board face upward while the DIMMs of the second memory module face downward. Note that both memory boards must be populated with a minimum of two DIMMs on each board.

Note: Both primary and secondary side memory boards must be installed for the processor node to function properly.

2.4.3 Scalability Port I/O Bus Interface

The primary interface between the I/O baseboard and the processor baseboard is the scalability port (SP) bus provided by the SNC-M. The scalablity port is a simultaneous bidirectional (SBD) trilevel bus, which provides a high-speed point-to-point link between a processor baseboard and a target (IO board or SPS). Each port is a 4 byte, quad-pumped (4x) 200MHz bus. This gives a raw throughput of 3.2 GT/s per direction for each bus off the SNC-M. The SNC-M has two SP ports that, combined, have a total bandwidth of 6.4 GB/s per direction, or a total bidirectional bandwidth of 12.8 GB/s.

Note: The scalability port bus has a maximum signal routing length of 20 inches plus two VHDM connectors between the SNC-M and SIOH/SPS. Approximately 3.5 inches is used on the Itanium 2 processor baseboard.

For bus specifications, refer to the *Intel® E8870 External Design Specification* and the *Electrical, Mechanical, and Thermal Specification*.

Along with the SP bus, there are other signals shared between the processor baseboard and the I/O baseboard to support error handling, reset and power control, and system configuration and monitoring (BIOS and server management). Refer to Table 2-26 for a list of non-SP bus signals.

2.4.4 Clock Distribution

Figure 2-5 shows the clock distribution architecture for the Itanium 2/E8870 processor baseboard. In the Server System SR870BN4, the 200-MHz clock is provided by the I/O board. The processor baseboard provides the clock buffers/drivers for clock distribution.

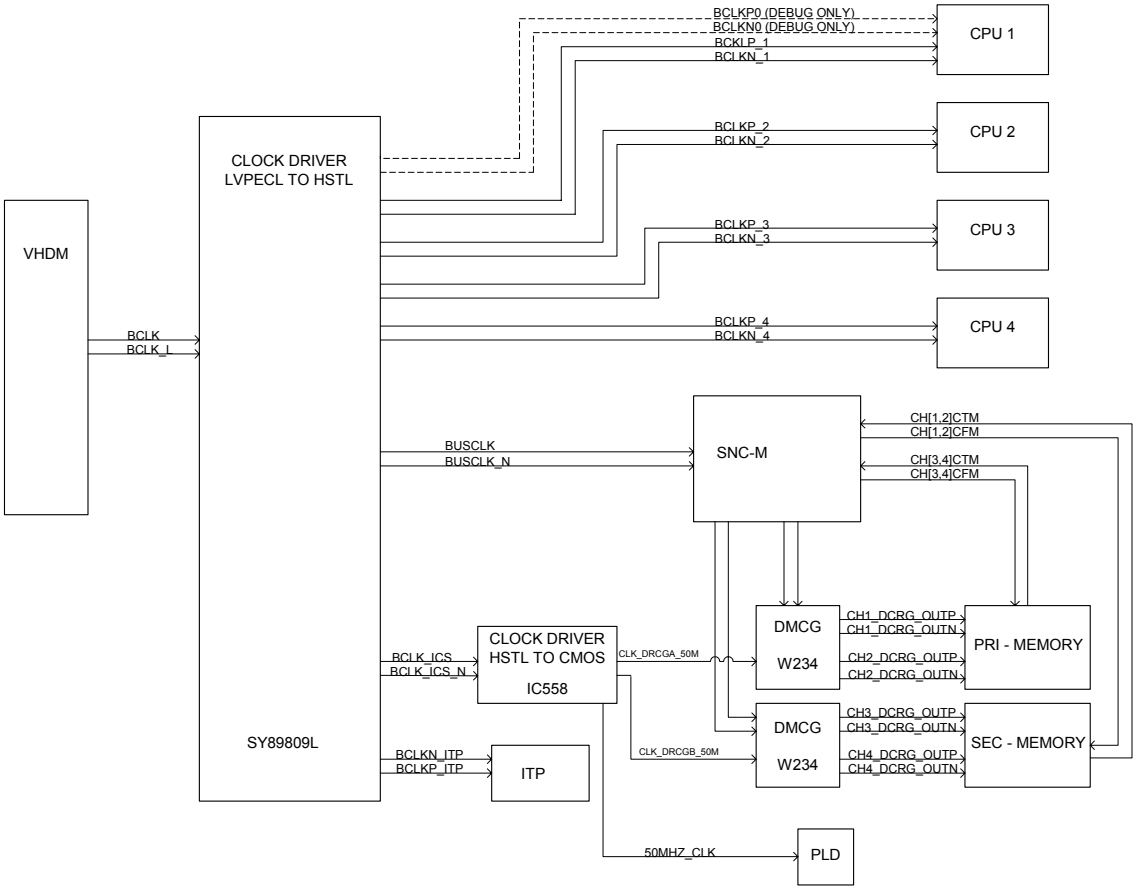


Figure 2-5. Processor Baseboard Clock Distribution

Table 2-1. Clock Frequency Chart

Clock	Description	Logic Family	Frequency
BCLK/BCLK_L	Main Bus Clock from I/O board	HSTL	200 Mhz
BCLKP_1/BCLKN_1	Processor 1 Clock	HSTL	200 Mhz
BCLKP_1/BCLKN_1	Processor 1 Clock	HSTL	200 Mhz
BCLKP_1/BCLKN_1	Processor 1 Clock	HSTL	200 Mhz
BCLKP_1/BCLKN_1	Processor 1 Clock	HSTL	200 Mhz
BUSCLK/BUSCLK_L	SNC-M Clock	HSTL	200 Mhz
BCLK_ICS/BCLK_ICS_N	ICS558 Clock	HSTL	200 Mhz
BCLKN_ITP/BCLKP_ITP	ITP input Clock	HSTL	200 Mhz
CLK_DRCGA_50M	Input Clock for DRCG (Direct Rambus Clock Generator)	CMOS	50 Mhz
CLK_DRCGB_50M	Input Clock for DRCG	CMOS	50 Mhz
50Mhz_Clk	PLD input clock	CMOS	50 Mhz
Ch1_DRCG_OUTP/ Ch1_DRCG_OUTN	Channel 1 Rambus Clock	RSL (Rambus Signal Level)	400 Mhz

Ch2_DRCG_OUTP/ Ch2_DRCG_OUTN	Channel 2 Rambus Clock	RSL (Rambus Signal Level)	400 Mhz
Ch3_DRCG_OUTP/ Ch3_DRCG_OUTN	Channel 3 Rambus Clock	RSL (Rambus Signal Level)	400 Mhz
Ch4_DRCG_OUTP/ Ch4_DRCG_OUTN	Channel 4 Rambus Clock	RSL (Rambus Signal Level)	400 Mhz
CH[1,2]_CTM	Clock To Memory	RSL	400 Mhz
CH[3,4]_CTM	Clock To Memory	RSL	400 Mhz
CH[1,2]_CFM	Clock From Memory	RSL	400 Mhz
CH[3,4]_CFM	Clock From Memory	RSL	400 Mhz

2.4.5 Voltage Regulators

The processor board contains three plug-in D2D regulators to generate two primary voltages, 2.5 V and 3.3 V from 48 V. The 2.5 V D2Ds supply voltage for the DIMM interface of the DMH chip, the DDR DRAM devices, and drive the 1.25 V regulator (for DDR termination). The 3.3 V D2D is the primary voltage used for miscellaneous logic, FWH interface, clock drivers, and drives the input voltage for the 1.2 V, 1.5 V, and 1.8V embedded regulators.

The processor board has three embedded switching regulators, one for the AGTL+ termination voltage (1.2 V) required by the FSB, one 1.8V regulator for the Clocks and Rambus Signaling Level (RSL) logic between the SNC-M and DMH, and one for the SNC-M core (1.5 V) power. There is also one linear regulator to supply the Scalability Port Power (1.3 V). The switching regulators convert 3.3 V from the +3.3 V supply rail into their respective supply outputs. The Scalability Port linear regulator converts 1.8 V into 1.3 V. In addition to the on-board regulators, the Itanium 2 processor requires a separate power pod that supplies the voltage necessary to power the core and cache for each processor. The power pod connects directly to the Itanium 2 processor and runs off of +48 V.

2.4.5.1 Embedded Regulator Voltage ID (VID) table

Table 2-2. Embedded Regulator VID table

VID Pin Name						VID Pin Name					
VID25 mV	VID3	VID2	VID1	VID0	**Vout**	VID25 mV	VID3	VID2	VID1	VID0	**Vout**
0	0	1	0	0	1.050	0	1	1	0	0	1.450
1	0	1	0	0	1.075	1	1	1	0	0	1.475
0	0	0	1	1	1.100	**0**	**1**	**0**	**1**	**1**	**1.500***
1	0	0	1	1	1.125	1	1	0	1	1	1.525
0	0	0	1	0	1.150	0	1	0	1	0	1.550
1	0	0	1	0	1.175	1	1	0	1	0	1.575
0	**0**	**0**	**0**	**1**	**1.200***	0	1	0	0	1	1.600
1	0	0	0	1	1.225	1	1	0	0	1	1.625
0	0	0	0	0	1.250	0	1	0	0	0	1.650
1	0	0	0	0	1.275	1	1	0	0	0	1.675
0	1	1	1	1	1.300	0	0	1	1	1	1.700
1	1	1	1	1	1.325	1	0	1	1	1	1.725
0	1	1	1	0	1.350	0	0	1	1	0	1.750
1	1	1	1	0	1.375	1	0	1	1	0	1.775
0	1	1	0	1	1.400	**0**	**0**	**1**	**0**	**1**	**1.800***
1	1	1	0	1	1.425	1	0	1	0	1	1.825

Note: 0 = stuffed 0 ohm resistor
1 = unstuffed
* VID configuration for current regulators being used.

2.4.5.2 AD2D VID Specification

Table 2-3. AD2D VID table

VID Pin Name[1]						VID Pin Name					
VID4	VID3[2]	VID2	VID1	VID0	**Vout**	VID4	VID3	VID2	VID1	VID0	**Vout**
1	1	1	1	1	2.0	0	1	1	1	1	1.30
1	1	1	1	0	2.1	0	1	1	1	0	1.35
1	1	1	0	1	2.2	0	1	1	0	1	1.40
1	1	1	0	0	2.3	0	1	1	0	0	1.45
1	1	0	1	1	2.4	0	1	0	1	1	1.50
1	**1**	**0**	**1**	**0**	**2.5***	0	1	0	1	0	1.55
1	1	0	0	1	2.6	0	1	0	0	1	1.60
1	1	0	0	0	2.7	0	1	0	0	0	1.65
1	0	1	1	1	2.8	0	0	1	1	1	1.70
1	0	1	1	0	2.9	0	0	1	1	0	1.75
1	0	1	0	1	3.0	0	0	1	0	1	1.80
1	0	1	0	0	3.1	0	0	1	0	0	1.85
1	0	0	1	1	3.2	0	0	0	1	1	1.90
1	**0**	**0**	**1**	**0**	**3.3***	0	0	0	1	0	1.95
1	0	0	0	1	3.4	0	0	0	0	1	2.00
1	0	0	0	0	3.5	0	0	0	0	0	2.05

Note: (1): 0 = 0 ohm resistor stuffed (GND)
1 = resistor unstuffed (Open)
(2): TD2D support uses pin 9 which selects between 2.5V and 3.3V. Please note that TD2D is a subset of the AD2D specification.
*Current Configuration for processor board D2Ds.

2.4.5.3 Processor Power Pod

The voltage supply for each of the four processors is supplied independently by a power pod. Each power pod will provide the processor and cache with the voltages they require from the +48 V power rail provided to it from the processor board. The 48 volts will be supplied to the processor power pods via a Y-cable from a four-pin connector on the processor board to each power pod.

The following list shows the features of the power pod regulator:

- 48 V input @ 3.85 A +/- 10%
- 48 V ground return
- Output: 0.95 V to 1.70 V @ 130 W
- Efficiency at 130 W is 77%

2.4.5.4 +3.3 V Regulator

The 3.3 V converter on the processor baseboard provides power for the SNC-M core regulator, the FSB regulator, the 1.8 V regulator for the Rambus termination, the firmware hubs, and the clock buffer/driver circuits and other miscellaneous logic.

The following list shows the features of the 3.3 V DC to DC regulator (Source: *A-D2D Server Distributed Power 48 V Input (Advanced) DC-to-DC Converter Design Specification*)

- 48 V input @ 2.37 A +/- 10%
- 48 V ground return
- Output: 3.3 V @ 30 Amps (Max)

2.4.5.5 +2.5 V Regulator

The 2.5 V regulator on the processor baseboard provides power for the DIMM interface pins of the DMH, 1.25 V regulator on the memory boards, and DDR DRAMs. There are two 2.5 V D2D which are configured for current sharing.

The following list shows the features of the 3.3 V D2D regulator (source: *A-D2D Server Distributed Power 48 V Input (Advanced) DC-to-DC Converter Design Specification*).

- 48 V input @ 2.37 A +/- 10%
- 48 V ground return
- Output: 2.5 V @ 32 Amps (Max)

2.4.5.6 +1.2 V (Vtt) Embedded Regulator

The 1.2 V voltage regulator circuit utilizes a HIP4006E* controller, which provides an accurate, high drive programmable supply voltage to the processor bus. The following list shows the features of the onboard V_{tt} voltage regulator.

- 0 A to 16 A maximum output current
- 85% efficiency at maximum load
- Active-High PWRGD open collector output

- Active-Low output disable input
- Short circuit protection

Table 2-4. 1.2 V and Vref Typical Voltage and Tolerance

Voltage	Description	Min	Type	Max	Tolerance
3.3 V	Input voltage	3.003 V	3.3 V	3.597 V	3.3 V +/-9%
12 V Stdby	Input Bias Voltage	10.8 V	12 V	13.2 V	12 V +/-10%10%
1.2 V	Output buffer and termination voltage for GTL+ drivers	1.182 V	1.2 V	1.218 V	1.2 V +/-1.5%
Vref	Reference voltage for GTL+ receivers		(2/3)*(1.2 V) V		

2.4.5.7 +1.5 V Embedded Regulator

The 1.5 V voltage regulator circuit utilizes a HIP4006E controller, which provides accurate, high drive, programmable supply voltage to the E8870 SNC-M component on the processor baseboard. The following list shows the features of the onboard VCC 1.5 voltage regulator:

- 0 A to 16 A maximum output current
- 85% efficiency at maximum load
- Active-High PWRGD open collector output
- Active-Low output disable input
- Short circuit protection

Table 2-5. 1.5 V Tolerance

Voltage	Description	Min	Type	Max	Tolerance
3.3 V	Input voltage	3.003 V	3.3 V	3.597 V	3.3 V +/-9%
12 V Stdby	Input Bias Voltage	10.8 V	12 V	13.2 V	12 V +/-10%
1.5 V	Provides core voltage to Intel® E8870 SNC-M component	1.45 V	1.5 V	1.53 V	1.5 V +/-3%

2.4.5.8 +1.8 V Embedded Regulator

The 1.8 V voltage regulator circuit utilizes a HIP4006E controller which provides accurate, high drive, programmable supply voltage to the Intel E8870 SNC-M component on the processor baseboard, and defines the RSL logic. The following list shows the features of the onboard VCC 1.8 voltage regulator:

- 0 A to 16 A maximum output current
- 85% efficiency at maximum load
- Active-High PWRGD open collector output
- Active-Low output disable input

- Short circuit protection

Table 2-6. 1.8 V Tolerance

Voltage	Description	Min	Type	Max	Tolerance
3.3 V	Input voltage	3.003 V	3.3 V	3.597 V	3.3 V +/-9%
12 V Stdby	Input Bias Voltage	10.8 V	12 V	13.2 V	12 V +/-10%
1.8 V	Provides core voltage to Intel® E8870 SNC-M component	1.74 V	1.8 V	1.85 V	1.8 V +/-3%
Vref(RSL)	Reference voltage for RSL Logic Receivers		(77% 1.8 V) V		

2.4.5.9 +1.3V Linear Regulator

The 1.3 V voltage regulator circuit utilizes a EZ1581 linear regulator, which provides accurate voltage to the E8870 SNC-M SP bus drivers on the processor baseboard. The following list shows the features of the onboard 1.3 V voltage regulator.

- 2.0 A maximum output current
- 70% efficiency at maximum load
- Thermal shutdown short circuit protection
- Active-High output disable input (3.3 V enables circuit, 0 V disables output)
- Output protection Schottky to input

Table 2-7. 1.3 V Tolerance

Voltage	Description	Min	Type	Max	Tolerance
1.8 V	Input Voltage	1.74 V	1.8 V	1.85 V	1.8 V +/-3%
1.3 V	SP bus driver bias voltage	1.235 V	1.3 V	1.365 V	1.3 V +/-5%

2.4.6 Power Good/Reset Control

Reset and power good information is communicated between the I/O and processor board using several different signals. The processor board uses the input signals to control the order that power rails and board components are enabled. The I/O board uses the processor board outputs to control the system power sequencing. Table 2-8 describes the power good and reset signals shared between the processor and I/O baseboard. The sections that follow the table describe the power sequencing events on the processor board and the types of resets that are supported.

Processor board and I/O board Power Good/Reset Interface signal details are as follows (see the VHDM Connector section for more information).

Buffer Signal Directions

Buffer Type	Direction
I	Input
O	Output

Signal Descriptors

Buffer Type	Description
CMOS	Push/Pull CMOS
OD	Open drain

Table 2-8. Processor Board and I/O Board Power Good/Reset Interface Signals

Signal	Type	Description
SYS_PWRGOOD	I 3.3V STDBY CMOS	**System Power Good:** I/O board output that notifies the processor board that all power rails in the system are valid.
CD2D33EN	I 3.3V STDBY CMOS	**3.3 V D2D Enable:** I/O board output that is asserted when the I/O portion of the system is ready for the processor board to enable the 3.3V D2D.
PPODOE	I 3.3V STDBY CMOS	**Power Pod Output Enable:** I/O board output that is asserted when the I/O portion of the system is ready for the processor board to enable the processor power pods.
RESETI_L	I 3.3V STDBY CMOS	**RESET Input:** I/O board output that is asserted when the I/O portion of the system wants to reset the processors and Intel® E8870 SNC-M.
AIPPODGD	O 3.3VSTDBY OD	**All Installed Power Pod Good:** Asserted when at least one of the installed processors has asserted processor power pod power good.
PROCESSOR_PRES_L	O 1.5V OD	**Processor Present:** This signal is asserted when there is at least one processor present in the system. This signal is located only on the processor board.
NODE_PG	O 3.3VSTDBY CMOS	**Node Power Good:** Tells the I/O portion of the system that all power rails on the processor board are valid.
RESETO_L	O 3.3VSTDBY CMOS	**Reset Output:** This signal is asserted to notify the I/O portion of the system of SNC-M hard resets and ITP resets (defined in Section 2.4.6.2, “Reset”).

2.4.6.1 Power Sequencing

When a system is first powered-up, there is a specific order in which the power rails need to be brought up. Several events occur to ensure this order and notify the rest of the system when the power rails are valid. The following list describes the sequence of these events.

Power-Up Sequence

1. By default, the 12 Vstndby and 3.3 Vstndby rails should be enabled when the system is plugged in. These rails are enabled on the processor board when the I/O board asserts STDBYEN to the processor board standby hot-plug switches.
2. The I/O board drives 48VEN to enable +48 V on the processor board.
3. The 3.3 V D2D is enabled if both memory boards are in the system and the I/O board asserts CD2D33EN.
4. The 3.3 V D2D power good signal drives the enable for the 1.5 V regulator.
5. The power good signal from the 1.5 V embedded regulator drives the enable for the 1.2 V regulator.
6. The power good signal from the 1.5 V regulator drives the enable for the 1.8 V regulator.
7. The power good signal from the 1.2 V regulator drives the output enables for the installed processor power pods.
8. The power good signal from the 1.5 V regulator drives the enable to the 1.3 V linear regulator.
9. The enable for the 2.5 V D2Ds is driven by the power good signal from the 1.8 V regulator and the 3.3v D2D power good. If either one of the D2Ds is not present on the board, the 2.5 V rail will not be brought up.
10. Node power good (Node_PG) is asserted back to the I/O board when all embedded regulators, D2Ds, memory board 1.25 V rails, and installed power pods are good. The I/O baseboard uses NODE_PG to determine when it tells the processor board that the power rails for the entire system are good.
11. The clocks are enabled (ALLCLKSEN) when Node_pg is asserted.
12. The processor board drives the installed power pod power good signal (AIPPODGD) back to the I/O board when any one of the installed processors asserts power pod power good (PPODGD).
13. The processor board enables the processors on the board as soon as SYS_PWRGOOD is received from the I/O board and each installed processor power pod indicates that power is good (PROC[4:1]_PPODGD is asserted).
14. SYS_PWRGOOD from the I/O board drives the enable for the SNC-M, DMH, and memory DIMMS.

Figure 2-6 shows the order in which the processor board power rails are enabled.

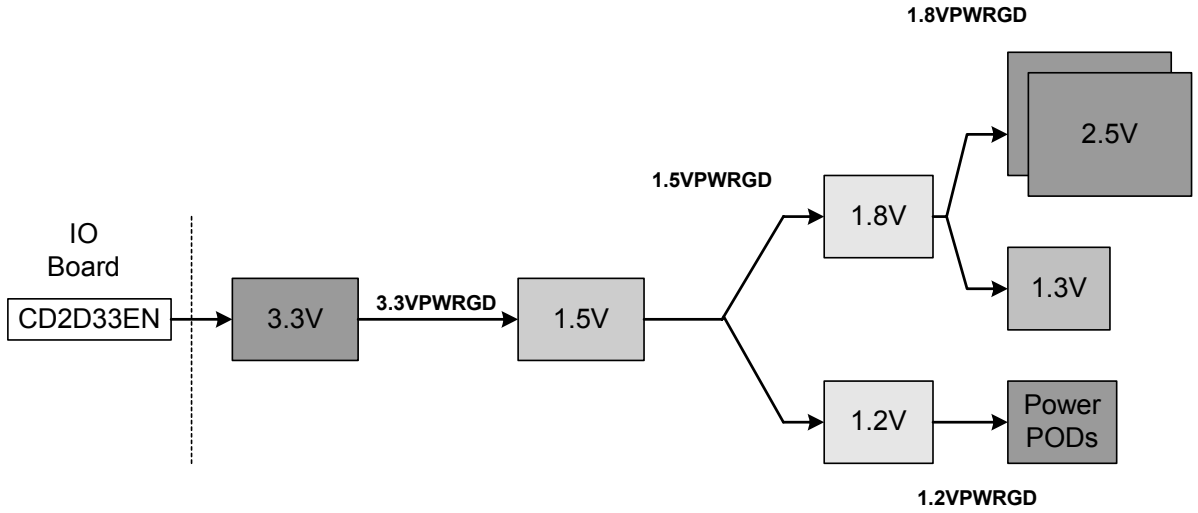


Figure 2-6. Rail Power-up Sequence.

Figure 2-7 shows a block diagram of the processor board's power sequencing control system.

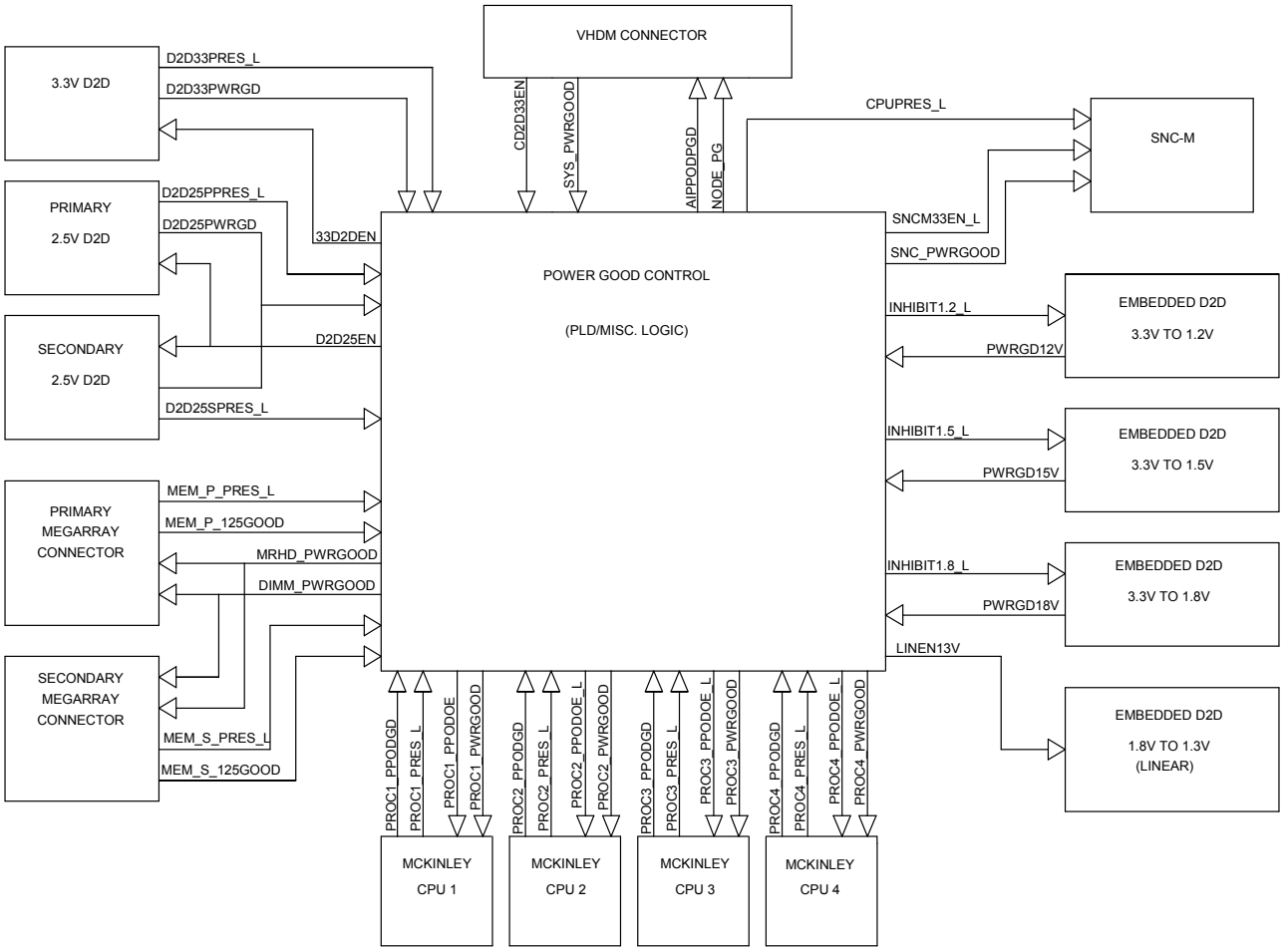


Figure 2-7. The Processor Board's Power Sequencing Control System

2.4.6.2 Reset

There are six types of system resets supported by the processor baseboard. These resets are described in Table 2-9.

Table 2-9. Different Resets Supported by the Procesor Board

Reset Type	Description
Power-Good Reset	Occurs when the system power logic causes a power good assertion. This resets the SNC-M configuration and transaction states, as well as the processors. Whenever the system is powered on, it goes through a power good reset.

Reset Type	Description
Hard Reset	A system reset caused by the assertion of RESETI_L. As a result of a hard reset, the processors, SNC-M, and memory bus are reset to a known state.
Processor-Only Hard Reset	A system reset that only resets the processors. This reset can be triggered by setting the SAVCFG, SAVMEM, and SNC RESET command bits in the SNC System Reset register (SYRE).
SNC-M Local Hard Reset	This is a type of warm reset that resets only the processors, DMH, and LPC-related components. This reset can be performed by setting the SNCReset configuration bit in the SNC-M System Reset Register (SYRE).
Processor Bus BINIT_L	This reset only resets the SNC-M and forces the Processors to the BINIT vector. The reset occurs when the processor bus drives BINIT_L low. Only local memory will be accessible after BINIT_L has been driven low.
Soft Reset	This reset forces the processors to begin executing code at the boot vector. Soft resets are triggered when INIT_L is driven on the processor bus. INIT_L can be driven by either the SNC-M (when the SoftReset configuration bit is set in the System Reset Register [SYRE]) or the ICHX (as a result of an I/O event).

For further information on these resets, please refer to the *Intel® E8870 System Architecture Specification*.

2.4.7 Programmable Logic Devices

There are two programmable logic devices (PLD) on the processor board. The first PLD is the Power Good/Reset PLD. This device's primary responsibility is managing the power sequencing described in Section 2.4.6.1. However, the PLD also provides logic that performs reset, server management, and JTAG functions.

The second PLD is called the Legacy Synchronization PLD and it supports synchronizing the legacy interrupt signals and RESETI_L so that they deterministically arrive at the processors. As an additional feature, this PLD also controls firmware hub initialization. The Power Good/Reset and Legacy Synchronization PLD's are described in Sections 2.4.7.1 and 2.4.7.2. The following conventions are used to help describe the PLDs.

Buffer Signal Directions

Buffer Type	Direction
I	Input
O	Output

Signal Descriptors

Buffer Type	Description
CMOS	Push/Pull CMOS
OD	Open drain
OC	Open Collector

2.4.7.1 Power Good/Reset PLD

The Power Good/Reset PLD implements most of the power sequencing and reset-related logic on the processor board. This PLD also contains logic to enable/disable the SP ports and drive TRST_L to the processors and SNC-M.

A Lattice* ISPLSI2064VE part is used for the Power Good/Reset PLD. This component can be powered off of 3.3 V standby and supports in-system programming. The ISPLSI2064VE has 64 I/O pins, 64 registers, and the ability to define open-drain outputs. The processor board uses the 100-pin TQFP version of the part. Refer to the Lattice Data sheet for further information on the ISPLSI2064VE. Table 2-10 defines the PLD signals, their pin numbers, and pin names. The PLD is powered off of 3.3v standby. However, the device can be configured with Open Drain outputs and, thus, requires external circuitry for the voltage.

Table 2-10. Power Good/Reset PLD Signals

Signal	Type	Description	Pin #	Pin Name
ALLCLKSEN	O 3.3V OD	**Enable All Clocks :** This signal enables the processor board clocks. It is asserted when all of the processor and memory boards rails are valid.	48	IO23
AIPPODGD	O 3.3VSTDBY CMOS	**All installed Power Pod Power Good:** Asserted when at least one processor sends a power pod good signal.	22	IO4
CD2D33EN	I 3.3VSTDBY CMOS	**3.3 V D2D Enable:** I/O board output that is asserted when the I/O portion of the system is ready for the processor board to enable the 3.3 V D2D.	34	IO14
CPUPRES_L	O 1.5V OD	**PROCESSOR Present:** This signal is asserted when there is at least one processor present in the system.	24	IO6
D2D25EN	O 3.3VSTDBY CMOS	**2.5 V Enable:** Enables the 2.5 V rail.	2	IO58
D2D33EN	O 3.3VSTDBY CMOS	**3.3 V Enable:** Enables the 3.3 V rail.	91	IO49
D2D25PWRGD	I 3.3VSTDBY OC	**2.5 V Power Good:** Asserted when the 2.5 V primary and secondary D2D output is valid.	57	IO30
D2D33PWRGD	I 3.3VSTDBY OC	**3.3 V Power Good:** Asserted when the 3.3 V rail is valid.	55	IO28
D2D33PRES_L	I 3.3VSTDBY CMOS	**3.3 V D2D Enable:** Asserted when the D2D is present.	5	IO60
D2D25PPRES_L	I 3.3VSTDBY CMOS	**2.5 V Primary Side D2D Present:** Asserted when the D2D is present.	53	IO27

Signal	Type	Description	Pin #	Pin Name
D2D25SPRES_L	I 3.3VSTDBY CMOS	**2.5 V Secondary Side D2D Present:** Asserted when the D2D is present.	27	IO8
EMBEN12V	O 3.3VSTDBY CMOS	**1.2 V Embedded Regulator Enable:** Enables the 1.2 V regulator.	56	IO29
EMBEN15V	O 3.3VSTDBY CMOS	**1.5 V Embedded Regulator Enable:** Enables the 1.5 V regulator.	96	IO53
EMBEN18V	O 3.3VSTDBY CMOS	**1.8 V Embedded Regulator Enable:** Enables the 1.8 V regulator.	93	IO51
FWH_ID_L	O 3.3VSTDBY OD	**Firmware Hub ID:** This signal is asserted to swap the ID bits of FWH 0 and 2. The signal must be held for as long as the IDs need to be swapped.	46	IO21
ITPRESET_L	I 3.3V CMOS	**In Target Probe (ITP) Reset:** This signal is asserted to perform an ITP initiated hard reset.	84	IO46
JMP_FWH_ID_L	I 3.3V CMOS	**Jumper FWH ID:** This signal is asserted when the FWH ID jumper is installed. When this signal is active, the system will change firmware hub 0 to firmware hub 2 and firmware hub 2 to firmware hub 0.	49	IO24
JMP_TRST_L	I 3.3VSTDBY CMOS	**Jumper TRST_L:** Asserted when the TRST jumper is put in place.	98	IO55
LINEN13V	O 3.3VSTDBY CMOS	**1.3 V Embedded Regulator Enable:** Enable for the 1.3V Embedded Regulator.	52	IO26
LPC_CTRL_L	O 3.3VSTDBY CMOS	**LPC Control Signal:** When asserted, this signal enables the LPC bus.	99	IO56
MEM_P_PRES_L	I 3.3VSTDBY CMOS	**Primary-side Memory Board Present:** Asserted when the primary-side memory board is connected to the processor board.	85	IO47
MEM_S_PRES_L	I 3.3VSTDBY CMOS	**Secondary-side Memory Board Present:** Asserted when the secondary-side memory board is connected to the processor board.	23	IO5
MEM_P_125GOOD	I 3.3VSTDBY CMOS	**Primary Memory 1.25 V Power Good:** Asserted when the primary-side memory board 1.25 V rail is good.	83	IO45
MEM_S_125GOOD	I 3.3VSTDBY CMOS	**Secondary Memory 1.25 V Power Good:** Asserted when the secondary-side memory board 1.25 V rail is good.	90	IO48
MRHD_PWRGD_L	O 3.3VSTDBY CMOS	**MRHD Power Good:** This signal is asserted when the power rails, that the DMH needs, are good.	70	IO35

Signal	Type	Description	Pin #	Pin Name
NODE_PG	O 3.3VSTDBY CMOS	**Node Power Good:** Processor board output that is asserted to indicate that all power rails on the processor board are valid.	33	IO13
PPODOE	I 3.3VSTDBY CMOS	**Power Pod Output Enable:** I/O board output that is asserted when the I/O portion of the system is ready for the processor board to enable the processor power pods.	42	IO18
PWRGD12V	I 3.3V CMOS	**Power Good 1.2 V:** Asserted when the 1.2 V rail is valid.	18	IO1
PWRGD15V	I 3.3V CMOS	**Power Good 1.5 V:** Asserted when the 1.5 V rail is valid.	26	IO7
PWRGD18V	I 3.3V CMOS	**Power Good 1.8 V:** Asserted when the 1.8V rail is valid.	68	IO33
PROC1_PPODGD	I 3.3VSTDBY CMOS	**Processor Power Pod Good:** Asserted when power pod 1 is producing valid output.	43	IO19
PROC2_PPODGD	I 3.3VSTDBY CMOS	**Processor Power Pod Good:** Asserted when power pod 2 is producing valid output.	51	IO25
PROC3_PPODGD	I 3.3VSTDBY CMOS	**Processor Power Pod Good:** Asserted when power pod 3 is producing valid output.	35	IO15
PROC4_PPODGD	I 3.3VSTDBY CMOS	**Processor Power Pod Good:** Asserted when power pod 4 is producing valid output.	47	IO22
PROC1_PPODOE	O 3.3VSTDBY CMOS	**Processor 1 Power Pod Output Enable:** Enables the power pod for processor 1.	20	IO3
PROC2_PPODOE	O 3.3VSTDBY CMOS	**Processor 2 Power Pod Output Enable:** Enables the power pod for processor 2.	19	IO2
PROC3_PPODOE	O 3.3VSTDBY CMOS	**Processor 3 Power Pod Output Enable:** Enables the power pod for processor 3.	28	IO9
PROC4_PPODOE	O 3.3VSTDBY CMOS	**Processor 4 Power Pod Output Enable:** Enables the power pod for processor 4.	17	IO0
PROC1_PRES_L	I 3.3V CMOS	**Processor 1 Present:** This signal is asserted when processor 1 is connected to the processor board.	79	IO42
PROC2_PRES_L	I 3.3V CMOS	**Processor 2 Present:** This signal is asserted when processor 2 is connected to the processor board.	95	IO52
PROC3_PRES_L	I 3.3V CMOS	**Processor 3 Present:** This signal is asserted when processor 3 is connected to the processor board.	92	IO50
PROC4_PRES_L	I 3.3V CMOS	**Processor 4 Present:** This signal is asserted when processor 4 is connected to the processor board.	74	IO38

Signal	Type	Description	Pin #	Pin Name
PROC1_PWRGD_L	O 3.3VSTDBY CMOS	**Processor 1 Power Good:** This signal is asserted to processor 1 when the processor's power is good.	73	IO37
PROC2_PWRGD_L	O 3.3VSTDBY CMOS	**Processor 2 Power Good:** This signal is asserted to processor 2 when the processor's power is good.	41	IO17
PROC3_PWRGD_L	O 3.3VSTDBY CMOS	**Processor 3 Power Good:** This signal is asserted to processor 3 when the processor's power is good.	67	IO32
PROC4_PWRGD_L	O 3.3VSTDBY CMOS	**Processor 4 Power Good:** This signal is asserted to processor 4 when the processor's power is good.	69	IO34
PROC_TRST_L	O 1.5V OD	**Processor TRST:** JTAG TRST input to the processors.	7	IO62
RAMTRM_PWRGD_L	O 3.3VSTDBY CMOS	**Memory Power Good:** This signal is asserted when the power needed for the memory termination is valid.	80	IO43
RESETO_L	O 3.3VSTDBY CMOS	**Reset Output:** This signal is asserted to notify the I/O portion of the system when the SNC-M has performed a hard reset or ITP has peformed a hard reset (defined in Section 2.4.6.2 Reset) .	40	IO16
RESETOTTL_L	I 3.3VSTDBY CMOS	**Reset Output TTL:** RESETO output from the SNC-M level shifted to 3.3 V voltage levels. This signal is asserted to indicate that the SNC-M has undergone a hard reset.	3	IO59
SM_FWH_ID_L	I 3.3VSTDBY CMOS	**Server Management Firmware ID Control:** Asserted by server management to swap the ID's for firmware hub 0 and firmware hub 2. This signal must be held as long as the ID swap is required. .	97	IO54
SM_RSVD2	N/A	**Server Management Reserved:** Currently unused.	45	IO20
SNCM_PWRGD_L	O 3.3VSTDBY CMOS	**SNC-M Power Good:** This signal is asserted when all of the SNC-M power rails are good.	76	IO39
SNCM_TRST_L	O 1.5V OD	**SNCM_TRST_L:** JTAG TRST_L input to the SNC-M.	32	IO12
SNCM33EN	O 3.3VSTDBY OD	**SNC-M 3.3V Rail Enable:** Enables the SNC-M 3.3 V rail and the SMC-M part of the I2C* bus.	29	IO10
SP0_PORT_ENABLE	I 3.3VSTDBY CMOS	**SP0 Port Enable:** This signal is asserted when server management wants to enable SP port 0.	58	IO31
SP1_PORT_ENABLE	I 3.3VSTDBY CMOS	**SP1 Port Enable:** This signal is asserted when server management wants to enable SP port 1.	6	IO61

Signal	Type	Description	Pin #	Pin Name
SP0PRES_CTRL_L	O 3.3VSTDBY CMOS	**SP0 Present Control:** This signal enables SP port 0.	82	IO44
SP1PRES_CTRL_L	O 3.3VSTDBY CMOS	**SP1 Present Control:** This signal enables SP port 1.	78	IO41
SYS_PWRGD	I 3.3VSTDBY CMOS	**System Power Good:** Buffered version of the I/O board's SYS_PWRGOOD output that notifies the processor board that all power rails in the system are valid.	8	IO63
TIME_EN_L	O 3.3VSTDBY OD	**Timer Enable:** Enables the glitch protection timer, when pulsed low. The glitch timer times when this is high, however this signal must be driven low for a short time in order to start the glitch timer.	72	IO36
TIME_EXP_L	I 3.3VSTDBY CMOS	**Timer Expire:** Tells when the glitch protection timer, enabled with TIMER_EN_L, has expired.	77	IO40
TRST_TTL_L	I 3.3VSTDBY CMOS	**TRST_L TTL:** JTAG TRST_L signal level shifted to TTL voltage levels.	1	IO57
50MHZ_CLK	I 3.3VSTDBY CMOS	**PLD CLOCK:** 50 MHz clock**.** Currently unused on the processor board.	10	Y0

2.4.7.1.1 Power Sequencing Logic

The power sequencing block of the PLD is composed of asynchronous logic that implements the power-up sequence described in Section 2.4.6.1. Please refer to Section 2.4.6.1 for further details.

2.4.7.1.2 Reset Logic

The reset block of the PLD is responsible for driving RESETO_L to the I/O board. The logic in the PLD drives RESETO_L when the system receives an ITP reset or when the SNC-M drives RESETOTTL_L low. Only one logic gate is required to do this. Refer to the following diagram.

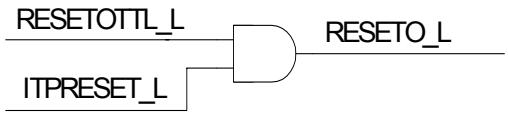


Figure 2-8. Logic Diagram of RESETO_L

2.4.7.1.3 JTAG TRST_L to the Processors and SNC-M

The PLD drives TRST_L to the processors and SNC-M when specific conditions are met. This section discusses what these conditions are and the logic implemented inside the PLD. Refer to Section 2.4.11 for more specific information on the processor board's debug chain.

TRST_L to the Processors

TRST_L is asserted to the processors if the system power rails are valid and TRST_ L is asserted. This means that PROC_TRST_L is only asserted if SYS_PWRGD is asserted and TRST_TTL_L is asserted. Figure 2-9 shows logic that asserts PROC_TRST_L at the correct time.

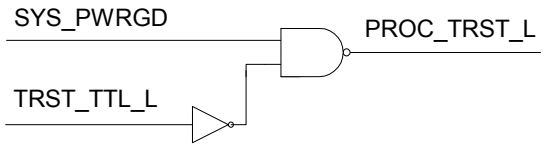


Figure 2-9. Processor TRST Logic diagram

TRST_L to the SNC-M

The way TRST_L is driven to the SNC-M is slightly different from the way it is driven to the processors. There is a TRST jumper on the processor board that can be installed to assert SNCM_TRST_L regardless of whether the TRST_L input to the PLD is asserted or not. Note that the power rails in the system must be valid for SNC_TRST_L to be asserted; however, if the jumper is set, TRST_TTL_L will be ignored as long as the jumper is in place. When the jumper is not installed, SNCM_TRST_L will be asserted in the same way that PROC_TRST_L is asserted. Figure 2-10 shows a logic diagram of SNCM_TRST_L.

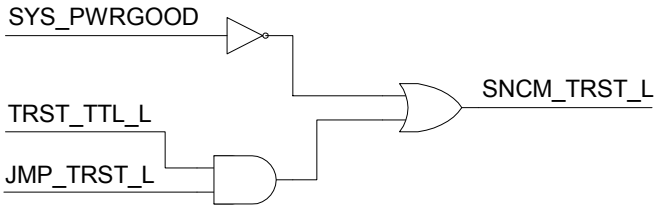


Figure 2-10. SNC-M TRST Logic diagram

2.4.7.1.4 Firmware Hub ID Select

The processor board uses a third firmware hub to provide a backup of the boot block in the event the boot block is corrupted in FWH ID 0. The firmware hub ID select, of the PLD, controls when the processor board will try to use the boot block firmware in FWH ID 2 and allow for normal boot or normal recovery.

The firmware ID select process can be initiated by server management or by setting a jumper on the processor baseboard. Server management can control the process by asserting SM_FWH_ID_L. When installed, the jumper asserts JMP_FWH_ID_L, which can also control the process.

The ID select works in the following manner. The PLD asserts FWH_ID_L whenever JMP_FWH_ID_L or SM_FWH_ID_L is asserted. When FWH_ID_L is asserted, FWH ID 2

becomes the master (ID 0) FWH and FWH ID 0 becomes FWH ID 2. When FWH ID 2 becomes the master, it can contain the boot block firmware that allows for a normal recovery or normal boot. Note that the SM_FWH_ID_L and JMP_FWH_ID_L signals are held asserted until the user has recovered the original boot block information or wants to switch the FWH IDs back to their default settings. The following diagram shows the logic on the processor board associated with firmware hub ID select.

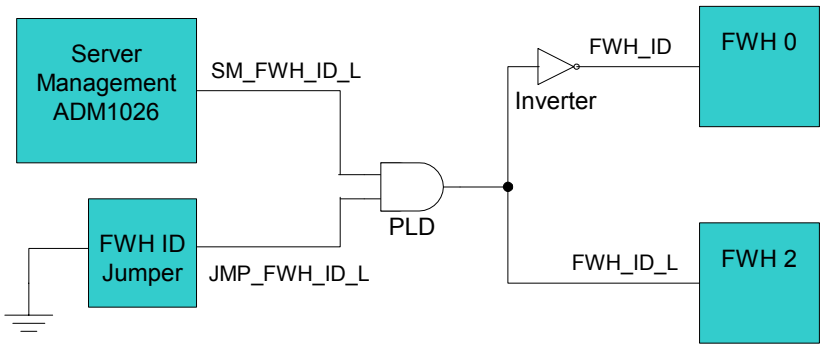


Figure 2-11. Firmware ID Select Logic

2.4.7.1.5 Enabling the SP Ports

The power good/reset PLD enables and disables the SP ports on the SNC-M for normal operation and hot-plug events. When the system is first powered up, the SP ports on the SNC-M are disabled until the system power rails are valid. Once the rails are valid, if server management does not need the ports disabled, the PLD will assert SP0_PRES_CTRL_L and SP1_PRES_CTRL_L to enable the SP ports. During normal operation, this is what should happen. However, there may be times when server management would like to disable the SP ports while SYS_PWRGD is still being asserted. This can be done by deasserting SP0_PORT_ENABLE or SP1_PORT_ENABLE. When either port enable signal is inactive, the corresponding SP port will be disabled. This means that server management can shut down either of the SP ports by driving the corresponding SP_PORT_ENABLE low. The following figure shows the logic implemented in the PLD.

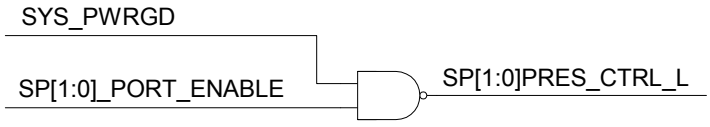


Figure 2-12. SP Port Enable

2.4.7.1.6 Glitch Protection

A special glitch protection circuit is implemented inside the PLD to prevent glitching logic in the event of a slow edge rate or external signal that glitches. The glitch protection uses a timer to

control when data is sampled on slow rise inputs, so that indeterminate logic values don't cause spurious output levels. The following section discribes how the glitch protection timer functions.

Glitch Protection Timer

The glitch protection circuit uses a glitch timer to determine when to sample slow edge inputs and when to propogate changes to PLD outputs. The glitch timer is really just a simple RC timer that asserts TIME_EXP_L (to the PLD) when it expires. Holding TIME_EN_L low for a short period of time, then deasserting it will enable the glitch timer. Figure 2-13 shows a diagram of what the timer looks like.

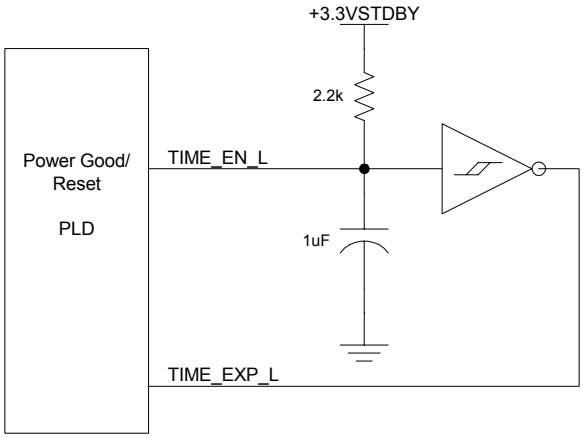


Figure 2-13. Glitch Timer connections.

2.4.7.2 Legacy Synchronization PLD

The Legacy Synchronization PLD is responsible for driving the legacy interrupt signals to the processors and RESETI_L to the SNC-M. A Lattice* ISPLSI2032VE PLD is used to implement the logic for these functions. The ISPLSI2032VE is a 300-MHz component that can be powered off of 3.3 V standby and supports in-system programming. This part has 32 I/O pins, 32 registers, the ability to define open-drain outputs, and comes in several different packages. The processor board uses the 44-pin TQFP package version of the component. Refer to the Lattice Data sheet for further information on the ISPLSI2032VE. Table 2-11 defines the signals used in the PLD, and a more detailed explanation of the PLD follows after the table.

Table 2-11. Legacy Synchronization PLD Inputs and Outputs

Signal	Type	Description
A20M_L	I 3.3VSTDBY CMOS	**A20M_L:** A20 Mask.
A20MGTL_L	O 1.2V OD	**A20M_L GTL Level:** A20 Mask translated into a GTL signal.

Signal	Type	Description
IGNNE_L	I 3.3VSTDBY CMOS	**IGNNE_L:** Ignore Numerical error.
IGNNEGTL_L	O 1.2V OD	**IGNNE_L GTL Level:** IGNNE translated into a GTL signal.
INTR	I 3.3VSTDBY CMOS	**INTR:** Interrupt request.
INIT_L	I 3.3VSTDBY CMOS	**INIT_L:** Processor Init signal.
NMI	I 3.3VSTDBY CMOS	**NMI:** Non-maskable interrupt.
PMI_L	I 3.3VSTDBY CMOS	**PMI:** Processor management interrupt.
PMIGTL_L	O 1.2V OD	**PMI_L GTL Level:** PMI_L translated into a GTL signal.
INITGTL_L	O 1.2V OD	**INIT_L GTL Level:** INIT_L translated into a GTL signal.
LINT0GTL	O 1.2V OD	**LINIT0 GTL:** INTR translated into a GTL signal.
LINT1GTL	O 1.2V OD	**LINIT1 GTL:** NMI translated into a GTL signal.
RESETI_L	I 3.3VSTDBY CMOS	**RESETI_L:** Asserted when the I/O board wants to hard reset the SNC-M and processors.
SNC_RESETI_L	O 1.5V OD	**SNC-M RESETI_L:** RESETI_L translated into a 1.5 V signal.
SYNC_CLK	I 3.3VSTDBY CMOS	**Synchronization Clock:** Clock used only when the legacy signals and RESETI_L need to be synchronized.
SYNCEN_L	I 3.3VSTDBY CMOS	**Synchronization Enable:** When this signal is asserted, the legacy signals and RESETI_L are synchronized to SYNC_CLK.

Synchronization

Usually the Legacy signals and RESETI_L are asynchronous and the PLD serves as a level translator that drives these signals to the processors and SNC-M. A weak pull-up on the processor board sets this as the default mode of operation. However, if SYNCEN_L is driven low, the PLD will go into synchrononized mode and synchronize the Legacy and RESETI_L signals with SYNC_CLK. When SYNCEN_L is asserted, the PLD will sample each synchronizable input on the rising edge of SYNC_CLK and then drive the captured values to the outputs on the next rising edge of SYNC_CLK. This makes the Legacy and RESETI_L outputs

synchronous and deterministic. The following figure illustrates a generic input waveform and the resulting output when in the default and synchronized modes of operation.

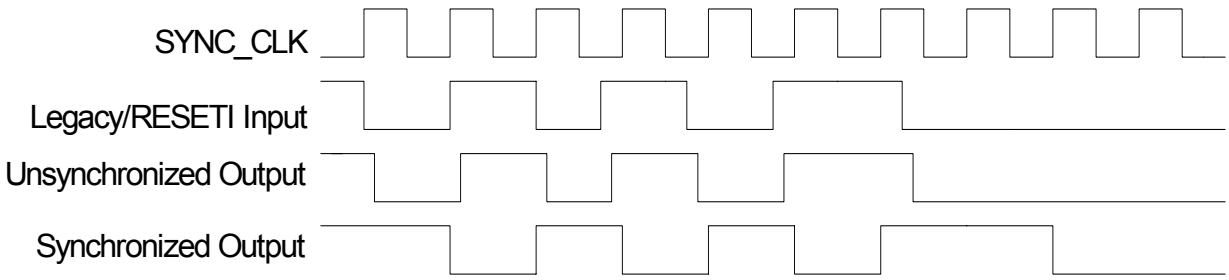


Figure 2-14. Example of Synchronized and Unsynchronized Outputs

2.4.8 Configuring Baseboard Jumpers

There are four jumper blocks on the processor baseboard. The primary functions of these jumper blocks are described in the following tables.

Table 2-12. Miscellaneous Jumper Definitions

Signal	Description
J7C1	
TDI	TDI to SNC_TDI configuration (pins 1 – 2) Jumper stuffed (default)= Shorts TDI to SNC_TDI (pins 3 – 4 should not have a jumper) No Jumper = Nothing (expected pins 3 – 4 to be stuffed)
TDI	TDI to SNC_TDO configuration. (Bypass SNC) (pin 3 – 4) Jumper Stuffed = Shorts TDI to PROC4_TDI (pins 1 – 2 should not be stuffed) No Jumper (default) = Nothing (expects pins 1 – 2 to be stuffed)
JMP_TRST_L	Drives JMP_TRST_L low (pins 5 – 6) Jumper stuffed = JMP_TRST_L is asserted (active position) Jumper not stuffed (default) = JMP_TRST_L is pulled high See PLD section (Section 2.4.7) for description of different assertion levels and what they mean
EXTERNAL_EN	Determines the level of EXTERNAL_EN. Jumper stuffed (default) = EXTERNAL_EN is low, which will add the processor board to the global ISP chain and prevent local programming of the PLDs (active state). Jumper unstuffed = EXTERNAL_EN is high, which will remove the processor board from the global ISP chain and allow local programming of the PLDs.
J8C2	
PROCESSOR_RATIO2	Bit 2 of PROCESSOR Core Ratio (active state is to stuff jumper) (pins 1 – 2)Default Unstuffed
PROCESSOR_RATI	Bit 3 of PROCESSOR Core Ratio (active state is to stuff jumper)

Signal	Description
O3	(pins 3 – 4) Default Unstuffed
PROCESSOR_RATIO4	Bit 4 of PROCESSOR Core Ratio (active state is to stuff jumper) (pins 5 – 6) Default Unstuffed
PROCESSOR_RATIO5	Bit 5 of PROCESSOR Core Ratio (active state is to stuff jumper) (pins 7 – 8) Default Unstuffed
J8C3	
JMP_FWH_ID_L	Swaps addresses between FWHs 0 and 1 (pins 1 – 2) Stuffed jumper = FWH IDs swapped (active state) No Jumper (default) = Normal operation
N/C	(3 – 4, 5 – 6)
FWH0TBL_L	Write protects the boot block of FWH0. Jumper stuffed (default) = FWH0TBL_L is high, which allows the 64k boot block of FWH0 to be written to. Jumper unstuffed = FWH0TBL_L is deasserted, which write protects the 64k bootblock of FWH0 (active position).

Note: Pins 6 and 8 of J7C1 are ground. Pin 1, 3, 5, and 7 of J8C2 are ground. Pin 2 of J8C3 is ground.

Table 2-13. ISP Header (J8C1) Connector Interface Signals

Signal name	Pin	Pin	Signal name
ISP_TCK	1	2	Ground
ISP_TMS	3	4	NC
ISP_EN_L	5	6	ISP_TDI
ISP_SDO	7	8	Ground

2.4.9 Server Management Block

Figure 2-15 shows the system management logic for the Server System SR870BN4 Itanium 2/E8870 processor baseboard. The processor baseboard has one system management bus. The I^2C_PROCESSOR bus connects all server management devices as well as the SNC, memory, and the four Itanium 2 processors. This bus is used to gather different types of information (such as voltage, temperature, and device information) from the various devices. The I^2C_PROCESSOR bus is accessed through the Baseboard Management Controller (BMC) via server management software such as Intel® Server Control (ISC).

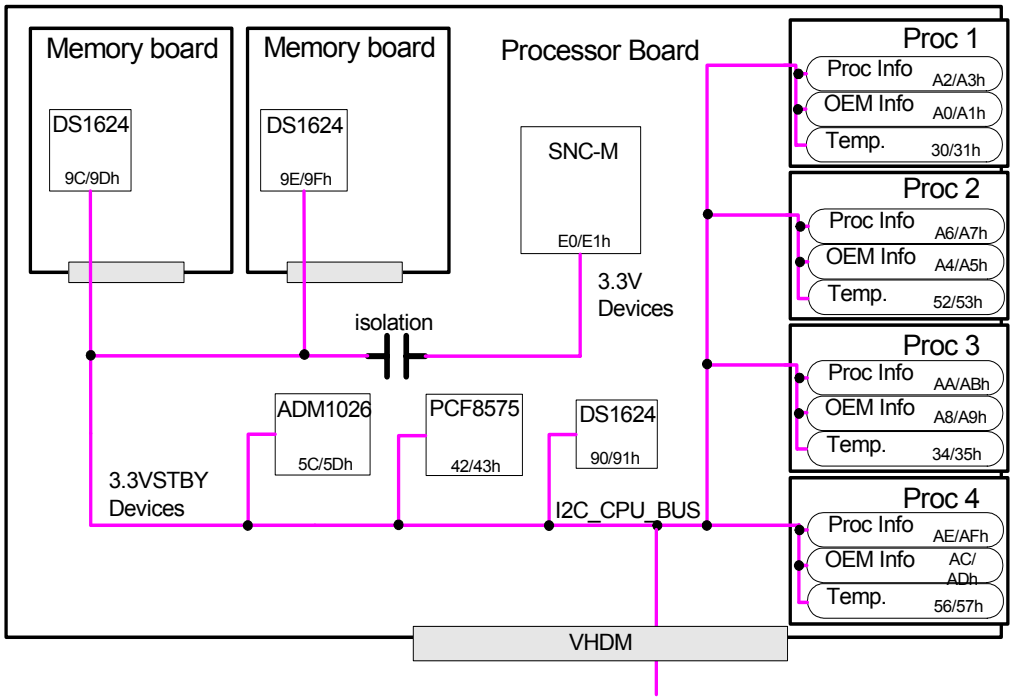


Figure 2-15. Intel® Server System SR870BN4 Intel® Itanium® 2/E8870 Server Management Diagram

2.4.10 I²C Address Map

Table 2-14. Device List on System I²C Bus

Device	Function	I²C Address	Supply Voltage
DS1624*	Temp. sensor & FRU Info	90h, 91h	3.3V STANDBY
PCF8575*	16-bit General purpose IO	42h, 43h	3.3V STANDBY
ADM1026*	Voltage monitor and General Purpose IO.	5Ch, 5Dh	3.3V STANDBY
SNC-M	Register access	E0h, E1h[1]	3.3V (Switched in after power up)
PROCESSOR 1	Proc Info	A2h, A3h	3.3V STANDBY
	OEM scratch EEPROM	A0h, A1h	3.3V STANDBY
	Processor Core Thermal Diode	30h,31h	3.3V STANDBY
PROCESSOR 2	Proc Info	A6h, A7h	3.3V STANDBY
	OEM scratch EEPROM	A4h, A5h	3.3V STANDBY
	Processor Core Thermal Diode	52h,53h	3.3V STANDBY
PROCESSOR 3	Proc Info	AAh, Abh	3.3V STANDBY
	OEM scratch EEPROM	A8h, A9h	3.3V STANDBY
	Processor Core Thermal Diode	34h,35h	3.3V STANDBY
PROCESSOR 4	Proc Info	AEh, Afh	3.3V STANDBY
	OEM scratch EEPROM	ACh, Adh	3.3V STANDBY
	Processor Core Thermal Diode	56h,57h	3.3V STANDBY

Device	Function	I²C Address	Supply Voltage
Primary Mem Brd DS1624	Temp. sensor and FRU info	9Ch, 9Dh[2]	3.3V STANDBY
SecondaryMem Brd DS1624	Temp. sensor and FRU info	9E,h 9Fh[2]	3.3V STANDBY

Note: 1. The SNC-M SMBus device ID is set through NODEID[3:0].
2. Bit 1 of the memory board DS1624 device ID is set on the processor board.

2.4.10.1 DS1624* Temperature Sensor and FRU Information

The DS1624*, when accessed via the I²C bus, will provide the temperature of the module, as measured at the DS1624, as well as the FRU information noted in Table 2-16. The FD1624* SEEPROM has 256 bytes of programmable space, which is broken into four areas. Table 2-15 lists and describes these areas.

Table 2-15. DS1624* SEEPROM Programming Areas

Area	Size	Description
Common Header	8 bytes	Programming offsets to the other areas below.
Internal Use	48 bytes	This area is reserved for general purpose use by the Intel® Server Management Firmware/Controllers.
Board Info	80 bytes	Contains the board FRU information listed in Table 2-16.
Product Info	120 bytes	Available for OEM use.[1]

1. The Intel-provided FRU and SDR load utility allows OEMs to program any of the FRU SEEPROM on the Intel® Server Board SR870BN4 board set. Refer to the *FRU & SDR Load Utility EPS* for more details.

In addition to being used as a SEEPROM to store the FRU information for the Server System SR870BN4 processor board, the DS1624 is a temperature sensor as well. The temperature data is a 13-bit value which gives a range of –55C to +125C in 0.03125C increments. For more information regarding the DS1624, see the vendor's datasheet.

Table 2-16. Example of Subset of FRU Information for Intel® Server Board SR870BN4 Processor Baseboard

Information	Description	Example	Notes
Mfg. Date/Time	Time and date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96	01ff593h (Date and time translation shown below) f593 = 2094483 min = 3 yr 358 Days & 1116 min = Dec 23, 1999, 6:36pm	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	SR870BN4 Processor/Memory Module	2
Board Serial Number	Intel® Board Serial Number	INBR42385906	2
Board Part Number	Intel Board Part Number	A55955-200	2

Notes: 1. Actual Value programmed into the board.

2. Example value. Actual value to be determined at the time the board is manufactured.

2.4.10.2 PCF8575* 16-bit I/O Expander

The PCF8575*, when accessed via the I^2C_PROCESSOR_bus, can read/write information to specific signals hooked up to these devices. Table 2-17 describes a list of signals and their interface to server management.

Table 2-17. I^2C_PROCESSOR Signals and their Interface to Server Management

Signal	I^2C Interface	Comments/Description
PCF8575* @ I^2C Address 42h		
PROC1_PRES_L	Input	Processor 1 Present signal
PROC2_PRES_L	Input	Processor 2 Present signal
PROC3_PRES_L	Input	Processor 3 Present signal
PROC4_PRES_L	Input	Processor 4 Present signal
PROC1_PPODGD_L	Input	Processor 1 Power POD Power Good
PROC2_PPODGD_L	Input	Processor 2 Power POD Power Good
PROC3_PPODGD_L	Input	Processor 3 Power POD Power Good
PROC4_PPODGD_L	Input	Processor 4 Power POD Power Good
NODE_PG	Input	Node Power Good
12V_HP_FAULT_L	Input	Hot plug fault on 12v
12V_STDBY_PWRGD	Input	12v standby Power Good
MEM_P_PRES_L	Input	Primary Side Memory Board Present
MEM_S_PRES_L	Input	Secondary Side Memory Board Present
PROGRESS_LED	Output	Hot-Plug Progress LED
FAILURE_LED	Output	Hot-Plug Failure LED

2.4.10.3 ADM1026* Hardware Monitor

The ADM1026* is a complete system hardware monitor for providing measurement and limit comparison of various system parameters. There are five voltage sensing inputs, two temperature sensing inputs and four digital signal inputs that are monitored using the ADM1026*. Table 2-18 shows the voltage sensors, temperature sensors, and data signals configured with the ADM1024. The ADM1024 resides on the I^2C_PROCESSOR bus.

Table 2-18: Signals Monitored by the ADM1026*

Signal	I^2C Interface	Comments/Description
+3.3V (Standby)	Input	Server Management and PLD primary voltage sensor
+3.3V	Input	D2D regulator output and embedded input voltage sensor
+1.8V	Input	RSL voltage sensor
+1.5V	Input	Intel® E8870 chipset core voltage sensor

Signal	I^2C Interface	Comments/Description
+1.2V	Input	FSB Termination voltage sensor
+1.3V	Input	SP Bus voltage sensor
SSENSE_125	Input	Monitors 1.25 V from Secondary Memory Board
PSENSE_125	Input	Monitors 1.25 V from Primary Memory Board
SNC-M Thermal Diode	Input (Cathode and Anode)	Temp. diode #1. Monitoring temperature of SNCM Core
FAULT48_L	Input	Monitors 48 V Hot-Plug Controller Fault
MEM_S_125GOOD	Input	Secondary Side memory board 1.25 V power good
MEM_P_125GOOD	Input	Primary Side Memory board 1.25 V power good
25SD2DOK_L	Input	Secondary 2.5 V Plug in D2D OK
D2D25SPRES_L	Input	Secondary 2.5 V Plug in D2D Present signal
25PD2DOK_L	Input	Primary 2.5 V Plug in D2D OK
D2D25PPRES_L	Input	Primary 2.5 V Plug in D2D Present signal
33D2DOK_L	Input	3.3 V Plug in D2D OK
D2D33PRES_L	Input	3.3 V Plug in D2D Present signal
SP0_PORT_ENABLE	Output	SP0 Port Enable
SP1_PORT_ENABLE	Output	SP1 Port Enable
SM_FWH_ID_L	Output	Server Management FWH ID change signal
SM_RSVD2	Input/Output	Server Management Reserved signal to PLD
THERMTRIP0_L	Input	Processor 1 Thermal Trip
THERMTRIP1_L	Input	Processor 2 Thermal Trip
THERMTRIP2_L	Input	Processor 3 Thermal Trip
THERMTRIP3_L	Input	Processor 4 Thermal Trip

2.4.10.4 Intel® E8870 Chip Set I^2C Interface

The SNC-M component of the Intel E8870 set includes an I^2C slave port to accept commands from a server management controller. This I^2C slave port interfaces with the SNC-M configuration unit, which gives a server management controller visibility into all configuration registers in the chip set.

2.4.10.5 Intel® Itanium® 2 Processor Server Management Features

The Itanium 2 processor cartridge includes a system management bus interface, which allows access to several processor features. The system management components on the cartridge include two memory components (EEPROMs) and a thermal sensing device (digital thermometer). The processor information EEPROM provides information about the processor. This information is permanently write-protected. The other EEPROM is a scratch EEPROM that is available for other data at the system vendor's discretion.

The thermal sensing device on the cartridge provides an accurate means of acquiring the relative junction temperature of the processor core die. The thermal sensing device is connected to the on-die thermal diode. THRMALERT# is a signal that is asserted when the processor thermal diode equals or exceeds the temperature threshold data programmed in the high-temp register on the sensor.

For more information, please refer to the *Intel® Itanium® 2 Electrical, Mechanical and Thermal Specification (EMTS)*.

2.4.11 Debug Port/In-Target Probe (ITP)

This ITP port provides an interface for system and component level debug. During system test and debug, all events and commands use the Joint Test Action Group (JTAG) protocol to access registers and memory.

In system debug, this port is controlled by the ITP, which is a PCI card driven by an application running on a PC. JTAG runs asynchronous to the system clocks at no more than 1/12.5 of the bus clock frequency, or 16 MHz. There are two ways to access the processor board JTAG chain. One method is through the ITP header on the processor board. The other method is through the assertion of the IS_JTAGEN_L signal (see the following figure).

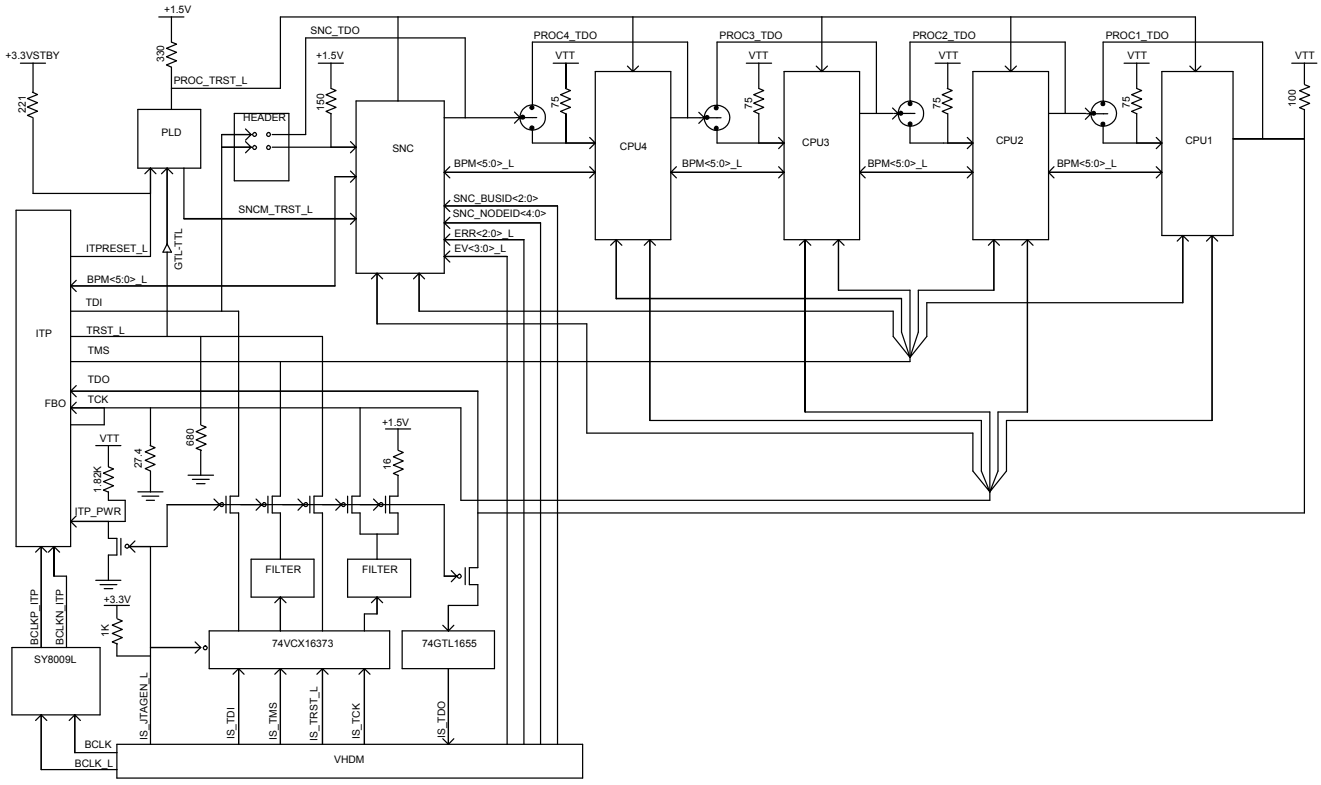


Figure 2-16. Implementation of JTAG on the Processor/Memory Node.

2.4.11.1 ITP Connector Description

Signal	Input/Output	Comments/Description
PWR	Input	PWR is derived from target system GTL+ termination level. This signal is used to reference the BPM[5:0]_L, RESET_L, TDO and FBO signals. This signal is deasserted when target

Signal	Input/Output	Comments/Description
		power is off or when the IS_JTAGEN_L is asserted from the I/O subsystem.
BCLK(n/p)	Input	Differential clocks from target system. Used to sample execution signals and phase align signals driven from the debug port.
DBA_L	Output	This signal is the debug tool's active signal which is output from the ITP to the system TAP port interface. This signal is not used by the processor/memory node.
FBI	Output	This signal is a copy of TCK without the passive edge rate control.
FBO	Input	This signal is used to register TDO into the ITP tool. FBO is connected to TCK through one of the legs of the star topology (see figure above).
DBR_L	Output	Reset signal driven to system to generate a system hard reset.
TCK	Output	TAP master clock. Debug port drives at up to 16 MHz if so enabled.
TDI	Output	Tap data input signal to the target. This signal is to be driven to the input of the first device in the scan chain.
TDO	Input	Tap data output from the target. This signal is received and registered with FBO. This signal is from the last device in the scan chain.
TMS	Output	TAP state management signal. This signal determines what mode the TAP state machines are in. TMS is also used as a method to reset the TAP internal to the chipset and processors.
TRST_L	Output	This signal transitions asynchronous to TCK. This signal is low during normal operation. This signal is used to asynchronously reset the TAP controller for the chipset and processors.
BPM[5:0]_L	Input	The debug port senses these signals along with RESET_L relative to BCLK. They are GTL+ level input break points from the Itanium® 2 processors. In the event of that BPM[5:0]_L is asserted by the processors, certain applications can make use of these signals to trigger other events in the ITP software.
RESET_L	Input	The debug port senses this signal relative to BCLK. This is a GTL+ level input from the Intel® E8870 SNC-M. In the event that Reset_L is asserted by the chipset, the ITP software can perform a break or function and/or inform the user that a reset has occurred.
BPM5DR_L	Output	This is the Debug Port Break at reset. This signal is connected to BPM5_L and is driven asynchronously from 50 ns after Reset_L is asserted until at least 25 ns after Reset_L is deasserted.

2.4.11.2 JTAG Scan ChainTarget Selection

The processor/memory node board is designed to provide an auto-detect configuration for JTAG. For each processor that is on the chain, there is a bypass function that routes TDO to TDI of the next device when the processor is either missing or defective (see the following figure).

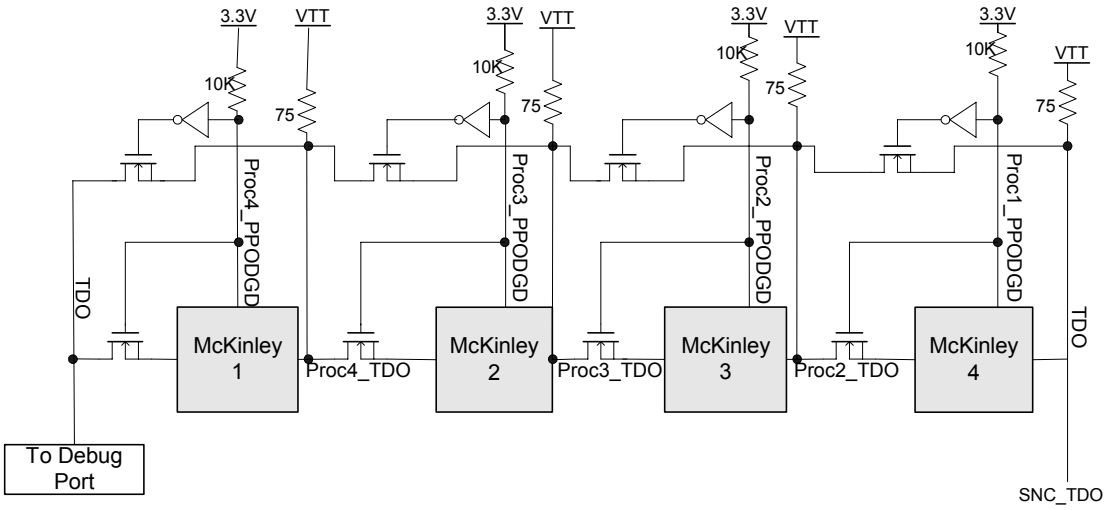


Figure 2-17. Intel® Itanium® 2 Processor Bypass Scheme

2.4.12 ISP interface

The two Lattice* PLD's on the processor board support In-System Programming (ISP). The parts are programmed using a JTAG ISP chain that is separate from the system debug JTAG chain. Figure 2-18 shows a block diagram of the ISP chain on the processor board.

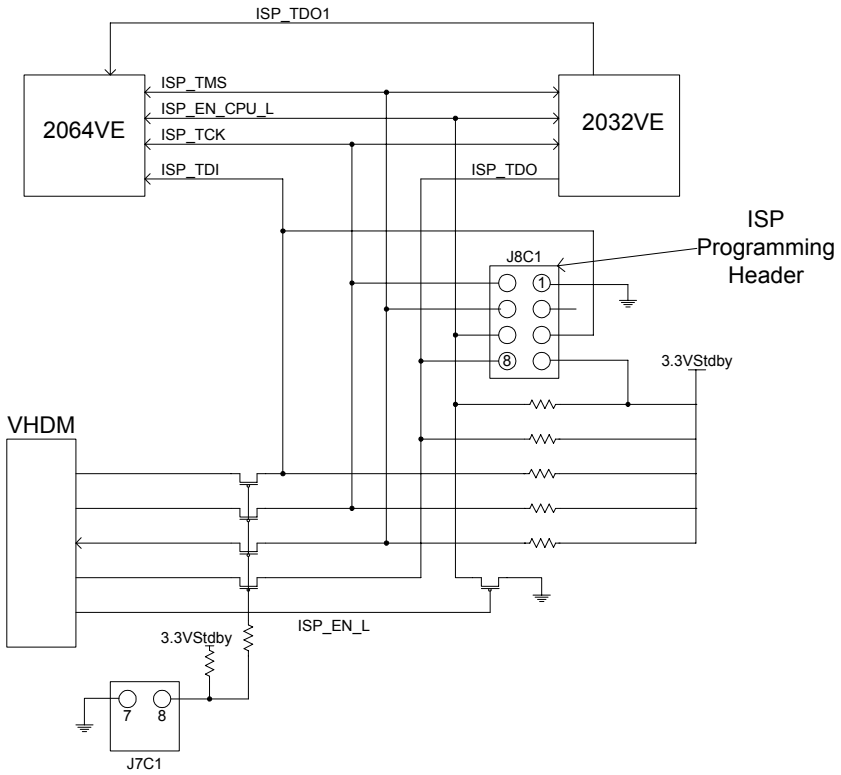


Figure 2-18. ISP Programming Chain Block Diagram

As the preceeding diagram shows, the processor board can be connected to the global ISP chain by installing the External Enable jumper on the processor board (refer to Section 2.4.8, “Configuring Baseboard Jumpers”). When the jumper is not installed, the processor board PLD’s can be programmed locally using the ISP header J8C1. Note that when the board is being programmed locally, the ISP_EN_L signal from the I/O baseboard must be kept inactive. The pinout for the local programing header is shown in Section 2.4.8, “Configuring Baseboard Jumpers”.

2.4.13 Firmware Hub

The Firmware Hub (FWH) interfaces to the system through the LPC/FWH interface of the SNC. The support of the FWH protocol enables the attachment of FWH-compatible devices to the SNC-M for storing processor-specific firmware.

There are three Intel® 82802AC FWHs in 32-pin PLCC packages. Each FWH is an 8 megabit device for a total of 24 megabits on the processor board. To program the FWHs, the SNCFWHWP_L must be deasserted through the I/O riser.

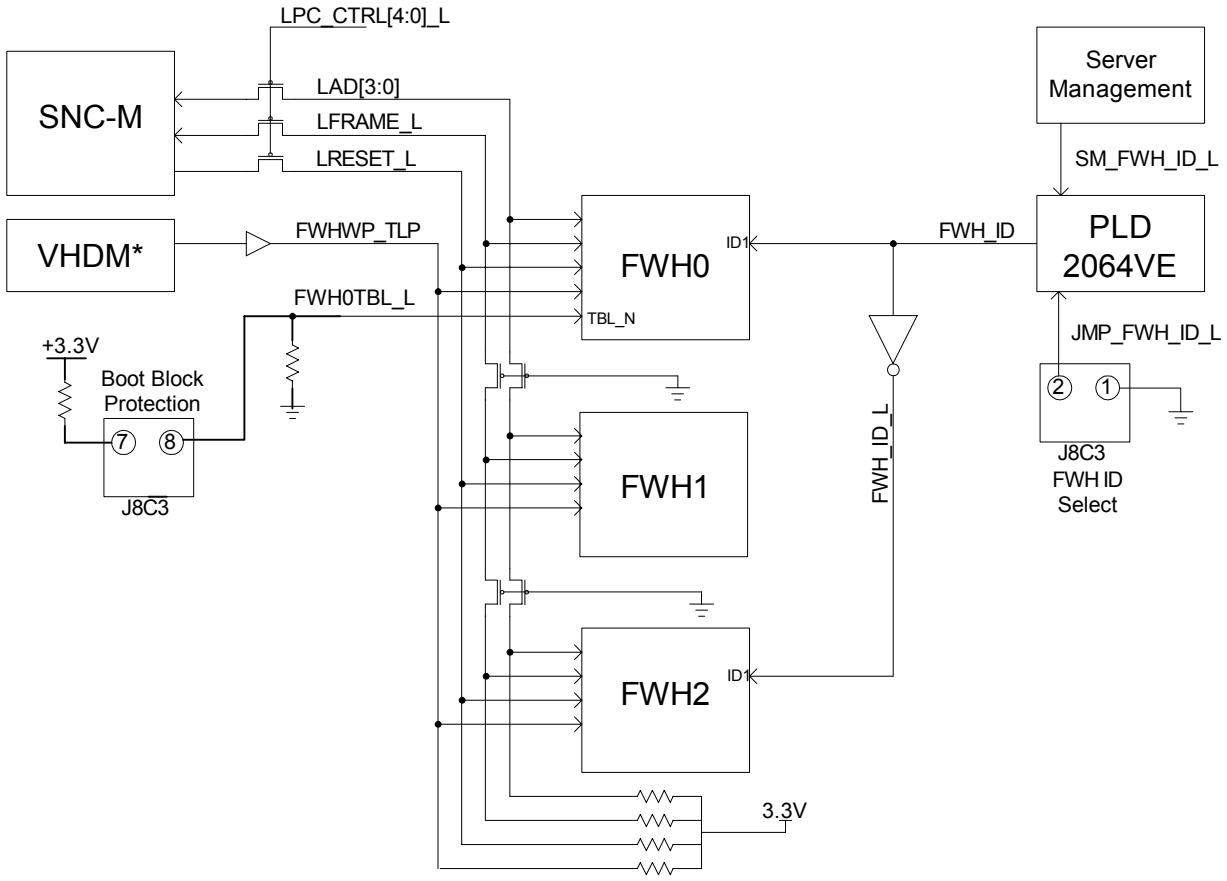


Figure 2-19. LPC Block Diagram

2.5 Signal Descriptions

The following notations are used to describe signal types:

Buffer Signal Directions

I	Input pin
O	Output pin
I/O	Bidirectional (input/output) pin
SBD	Simultaneous bidirectional pin

The signal description also includes the type of buffer used for the particular signal.

Buffer Technology Types

Buffer Type	Description
GTL+	Open drain GTL+ interface
SBD	Simultaneous bidirectional
Differential	A differential input that requires a voltage reference or the signal compliment
CMOS	CMOS type I/O with Schmitt trigger input

LPC	LPC I/O with Schmitt trigger input with a voltage level of 1.3 V, 3.3 V tolerant and max. frequency of 25 MHz
JTAG	1.5 V JTAG I/O
Analog	Typically, a voltage reference or specialty power supply

2.5.1 Intel® Itanium® 2 Processor System Bus Signals

All the signals on the system bus are driven by either the Itanium 2 processor or the SNC-M of the E8870 chip set. All of these signals are GTL+ signal levels. A detailed description of the Itanium 2 processor signals is provided in the *Intel® Itanium® 2 EMTS*.

2.5.2 Scalability Port (SP) Bus Signals

The scalability port (SP) is an internode interface that enables implementation of scalable shared memory multiprocessor systems. It is a point-to-point coherent interface for interconnection of processor nodes with local memory, I/O nodes, and network switches. A detailed description of the Intel E8870 SP bus signals is included in the *Intel® E8870 EMTS*.

2.5.3 Memory Interface Signals

Table 2-19 defines the signals according to functional groups: address/control, scan, and power. These tables provide a summary of memory signal pins, including the signal mnemonic, electrical type, full name, and a brief description. The electrical types are described in the beginning of this section.

Table 2-19. Memory Interface Signals Including RAMBUS Channels 0, 1, 2, 3

Signal	Type	Description
R{0/1/2/3}DQA[8:0]	I/O RSL 400 MHz [x2]	**Rambus Data(A):** Data signals used for read and write operations on Rambus data bus A.
R{0/1/2/3}DQB[8:0]	I/O RSL 400 MHz [x2]	**Rambus Data(B):** Data signals used for read and write operations on Rambus data bus B.
R{0/1/2/3}RQ[7:0]	O RSL 400 MHz [x2]	**Request Control Signals:** R{0/1/2/3}RQ[7:0] are used for sending control packets on Rambus channel. The Rambus specification defines the mapping of Rambus packets to these lines for RDRAM. The DMH component specification defines the mapping for DDR.
R{0/1/2/3}ExRC	O RSL 400 MHz [x2]	**Row Expansion Signal:** These select one of the two possible DMHs on each main channel to receive a row packet.
R{0/1/2/3}ExCC	O RSL 400 MHz [x2]	**Column Expansion Signal:** These select one of the two possible DMHs on each main channel to receive a column packet.
R{0/1/2/3}CTM	I RSL 400 MHz	**Clock to Master:** One of the two differential transmit clock signals used for RDRAM operations on the corresponding Rambus channel. It is input to SNC-M and is generated by an external clock generator.
R{0/1/2/3}CTMN	I RSL 400 MHz	**Clock To Rambus Master Complement:** One of the two differential transmit clock signals used for RDRAM operations on the corresponding Rambus channel. It is complement of clock signal R{0/1/2/3}CTM.

Signal	Type	Description
R{0/1/2/3}CFM	O RSL 400 MHz	**Clock from Master:** One of the two differential signals used to clock Rambus packets driven by the SNC.
R{0/1/2/3}CFMN	O RSL 400 MHz	**Clock from Master Complement:** One of the two differential signals used to clock Rambus packets driven by the SNC.
R{0/1/2/3}SYNCLK	O CMOS 100 MHz	**Phase Detect Signal:** This signal is sent to the DRCG for generating 400-MHz clock. This signal is generated from SYNCLK of the corresponding RAC. This signal trace must be delay matched with R{0/1/2/3}PCLKN trace.
R{0/1/2/3}PCLKN	O CMOS 100 MHz	**Phase Detect Signal:** This signal is sent to the DRCG for generating the 400-MHz clock. This signal is generated from the SNC-M core clock.
R{0/1/2/3}SCK	O CMOS 1 MHz **or** 100 MHz	**Serial Clock:** This signal provides clocking for register accesses (1 MHz) and selecting RDRAM devices on the corresponding Rambus channel for power management (100 MHz).
R{0/1/2/3}SIO	I/O CMOS 1 MHz **or** 100 MHz	**Serial Input/Output:** Bidirectional serial data signal used for device initialization, register operations, power mode control and device reset, etc.
R{0/1/2/3}CMD	O CMOS 1 MHz **or** 100 MHz	**Serial Command:** Serial command to the RDRAM devices used for power mode control, configuring SIO* daisy chain, and framing SIO operations.
VREF{0/1/2/3}[1:0]	I	**DC Signal Voltage Reference:** Supplies Vref for input buffers.

2.5.4 Server Management Interface Signals

The processor board interface with Server Management (the BMC) is performed through an I^2C bus. Table 2-20 describes each interface signal. Note that the two I^2C signals, listed in the table, fan out through zero Ohm resistors to target devices and form several different signals. The resistors are present to provide the ability to isolate devices from the bus, so the fan-out signals are not included in the table.

Table 2-20. System Server Management Interface

Signals(s)	Type	Name and Description
I2C_PROCESSOR_SCL	3.3V CMOS	**Server Management Clock:** Clock signal for the system management bus between the baseboard management controller, processor board, and memory board.
I2C_PROCESSOR_SDA	3.3V CMOS	**Server Management Serial Data:** Data line for the system management bus between baseboard management controller, processor board, and memory board.

2.5.5 Power Connection

The power connection to the Itanium 2 base power is provided via the VHDM connector. 48V and 48V Return are provided through the power blades, while the rest of the power signals are

provided through the VHDM connector itself. Table 2-21 is a summary of power connector pins, including the signal name, the type, and a brief description of each.

Table 2-21. Power Connection

Signals(s)	Type	Name and Description
GND	Analog	Ground.
+48 Return	Analog	48 V Ground Return
+3.3V	Analog	+3.3 V Standby
+12V	Analog	+12 V Standby
+48V	Analog	+48 V

2.6 Electrical, Mechanical, and Environmental Specifications

This section specifies the operational parameters and physical characteristics for the processor baseboard. This is a board-level specification only. System specifications are beyond the scope of this chapter.

Further topics in this section specify normal operating conditions for the processor baseboard and mechanical specifications for the module and connector interfaces to the board.

2.6.1 Electrical Specifications

The absolute maximum temperature and voltage ratings, power budget for the processor baseboard, and pinouts for the external interface connectors are defined in the following sections. Table 2-22 describes the absolute maximum temperature and voltage ratings for the processor.

Table 2-22. Processor Baseboard Maximum Ratings

Feature	Absolute Maximum Rating
Operating Temperature	10°C to 35°C

2.6.1.1 Power Requirements

Table 2-23 shows the power required by the Itanium 2 processor baseboard populated with maximum configurations, as defined below:

- Maximum Configuration:
  4 x 130-W processors with power pods and two fully populated memory cards

Note: The numbers are provided only to show design limits. Actual power consumption will vary depending on the exact configuration.

Table 2-23. Maximum Power Requirements

			Power (W)	Current (A)
1.45V - Primary Supply - Itanium 2 Power Pod			117.0	89.7
		Each	**Extended**	

Device	Qty	Power (W)	Current (A)	Power (W)	Current (A)
Itanium 2 Core	4	130	89.66	468.0	358.8
Total 1.45V				468.0	358.8

2.5V - Primary Supply				111.7	60.1
		Each		**Extended**	
Device	**Qty**	**Power (W)**	**Current (A)**	**Power (W)**	**Current (A)**
Memory Mezzanine	2	55.85	30.05	111.7	60.1
Total 2.5V				111.7	60.1

3.3V - Primary Supply				56.8	17.2
		Each		**Extended**	
Device	**Qty**	**Power (W)**	**Current (A)**	**Power (W)**	**Current (A)**
1.2 V FSB Regulator	1	14.12	4.28	14.1	4.3
1.5 V SNC-M Regulator	1	13.55	4.11	13.6	4.1
1.8 V Regulator	1	17.82	5.40	17.8	5.4
SY89809L Bus Driver	1	0.3795	0.115	0.38	0.12
ICS558 PECL to CMOS	1	0.495	0.15	0.50	0.15
FWH	3	0.22	0.07	0.66	0.21
PECL Termination (50 Ohm)	10	0.066	0.02	0.7	0.2
W234 Clock Generator	2	0.33	0.1	0.7	0.2
74GTL1655 Bus transceiver	1	0.4125	0.125	0.4	0.1
SN74CBT3125 Bus Switch	7	0.5016	0.152	3.5	1.06
TL1431CDR Prog. Ref for regs	1	0.4653	0.141	0.46	0.14
74ACT125 quad tri state	1	0.2508	0.076	0.3	0.1
Other Loads	1	3.3	1	3.3	1.0
Total 3.3 V				56.4	17.08

Power Supply Requirements

The power supply must meet the following requirements:

- Delay of 10 ms (minimum) from valid power to power good.
- All voltage rails (+48 V, +3.3 VSB, +12 VSB,) must reach their minimum regulation level within ± 50 ms of each other. See Section 2.4.5 for acceptable tolerances for each rail.

2.6.1.2 Connector Specifications

Table 2-24 shows the reference designators, quantity, manufacturer, and part number for connectors on the baseboard. Refer to the manufacturer's documentation for more information.

Table 2-24. Baseboard Connector Specifications

Item	Reference Designator(s)	Quantity	Manufacturer and Part Number	Description
	J8A1	1	Molex* 0740300448	6 Row X 60 Column VHDM and power blade
	J7E1, J3R1	2	FCI* 74220-001	MegArray* Recpt. 10X40 400 pins on processor board
	J1B1, J3B1, J6M1, J7M1	4	Foxconn* PZ70003-003-S	Itanium 2 processor socket

2.6.1.3 VHDM* (I/O) Connector Pinout and Non-SP Signal Descriptions

The processor baseboard interfaces to the midplane through the VHDM connector, a 6 row X 60 column, 360-pin VHDM style connector and a three-blade VHDM power connector.

Table 2-25. SP Signals and Non-SP Signals Pinout

Pin	F	E	D	C	B	A
1	RSVD	GND	GND	RSVD	GND	RSVD
2	GND	RSVD	GND	GND	RSVD	GND
3	RSVD	GND	RSVD	RSVD	GND	RSVD
4	RSVD	RSVD	RSVD	GND	RSVD	RSVD
5	RSVD	RSVD	RSVD	RSVD	GND	RSVD
6	RSVD	RSVD	RSVD	RSVD	RSVD	GND
7	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
11	12V_ STDBY	12V_STDBY	RSVD	3.3V_STDBY	3.3V_STDBY	PROCESSOR_INTERLOCK0_L
12	RSVD	RSVD	BUSID2	BUSID1	I2C_PROCESSOR_SDA	I2C_PROCESSOR_SCL
13	STPCLK_L	PROCHOT_L	BUSID0	NODEID4	SP1GPIO	PPODOE
14	EV3_L	EV2_L	NODEID3	EV1_L	EV0_L	SP0GPIO
15	RSVD	RSVD	NODEID2	RSVD	HP_INT_L	THERMALERT_L
16	INT_OUT_L	BERROUT_L	NODEID1	ERR2_L	ERR1_L	ERR0_L
17	BERRIN_L	RSVD	RSVD	BINITIN_L	RSVD	RSVD
18	IS_TMS	IS_TRST_L	NODEID0	BINITOUT_L	CD2D33EN	AIPPODPG
19	IS_TDO	IS_TDI	IS_TCK	RSVD	FERR_L	PMI_L
20	NMI	INTR	RSVD	INIT_L	IGNNE_L	A20M_L
21	RESETO_L	RSVD	RESETI_L	RSVD	NODE_PG	SYS_PWRGOOD
22	SP1PRES	SP0PRES	GND	SP1SYNC	GND	SP0SYNC
23	SP1BD13	GND	SP1BD14	SP1BD6	GND	SP1BD5
24	SP1BD12	SP1BD15	GND	SP1BD4	SP1BD7	GND
25	GND	SP1BVREFH3	SP1BVREFL3	GND	SP1BVREFH1	SP1BVREFL1
26	SP1BD11	GND	SP1BSSO	SP1BD3	GND	SP1BEP0

27	SP1BRSVD	SP1BD10	GND	SP1BSTBN0	SP1BD2	GND
28	GND	SP1BSTBP1	SP1BSTBN1	GND	SP1BEP2	SP1BSTBP0
29	SP1BLLC	GND	SP1BD9	SP1BEP1	GND	SP1BD1
30	SP1BVREFL2	SP1BVREFH2	GND	SP1BVREFL0	SP1BVREFH0	GND
31	GND	SP1BD8	IS_JTAGEN_L	GND	SP1BD0	SNCFWHWP_L
32	IA64_IA32*	GND	SP1AD8	SNCFWHDIS_L	GND	SP1AD0
33	GND	SP1AVREFH2	SP1AVREFL2	GND	SP1AVREFH0	SP1AVREFL0
34	SP1AD9	SP1ALLC	GND	SP1AD1	SP1AEP2	GND
35	GND	SP1ASTBN1	SP1ASTBP1	GND	SP1ASTBN0	SP1ASTBP0
36	SP1AD10	GND	SP1ARSVD	SP1AD2	GND	SP1AEP1
37	SP1ASSO	SP1AD11	GND	SP1AEP0	SP1AD3	GND
38	GND	SP1AVREFL3	SP1AVREFH3	GND	SP1AVREFL1	SP1AVREFH1
39	SP1AD15	GND	SP1AD12	SP1AD7	GND	SP1AD4
40	SP1AD14	SP1AD13	GND	SP1AD5	SP1AD6	GND
41	SP0BD13	GND	SP0BD14	SP0BD6	GND	SP0BD5
42	SP0BD12	SP0BD15	GND	SP0BD4	SP0BD7	GND
43	GND	SP0BVREFH3	SP0BVREFL3	GND	SP0BVREFH1	SP0BVREFL1
44	SP0BD11	GND	SP0BSSO	SP0BD3	GND	SP0BEP0
45	SP0BRSVD	SP0BD10	GND	SP0BEP1	SP0BD2	GND
46	GND	SP0BSTBP1	SP0BSTBN1	GND	SP0BSTBP0	SP0BSTBN0
47	SP0BLLC	GND	SP0BD9	SP0BEP2	GND	SP0BD1
48	SP0BVREFL2	SP0BVREFH2	GND	SP0BVREFL0	SP0BVREFH0	GND
49	GND	SP0BD8	STDBYEN_L	GND	SP0BD0	RSVD
50	V48EN	GND	SP0AD8	33STDBY_GD	GND	SP0AD0
51	GND	SP0AVREFH2	SP0AVREFL2	GND	SP0AVREFH0	SP0AVREFL0
52	SP0AD9	SP0ALLC	GND	SP0AD1	SP0AEP2	GND
53	GND	SP0ASTBN1	SP0ASTBP1	GND	SP0ASTBP0	SP0AEP1
54	SP0AD10	GND	SP0ARSVD	SP0AD2	GND	SP0ASTBN0
55	SP0ASSO	SP0AD11	GND	SP0AEP0	SP0AD3	GND
56	GND	SP0AVREFL3	SP0AVREFH3	GND	SP0AVREFL1	SP0AVREFH1
57	SP0AD15	GND	SP0AD12	SP0AD7	GND	SP0AD4
58	SP0AD14	SP0AD13	GND	SP0AD5	SP0AD6	GND
59	ISP_SCLK	ISP_MODE	GND	GND	BCLK_L	BCLK
60	PROCESSOR_INTERLOCK1_L	ISP_EN_L	ISP_SDO	ISP_SDI	GND	GND

* - Pulled up to 3.3v – always in IA64 mode.

Table 2-26. Non-SP Signal List

Name	Description	Pins	I/O	Source	Target	Tech
Non-SP Signals		**80**				
Clocks		**2**				
BCLK	200 MHz System Clock	1	I	IO	Processor	LVPECL

BCLK_L	200 MHz System Clock#	1	I	IO	Processor	LVPECL
Resets		**6**				
RESETI_L	Hard Reset from IO subsystem	1	I	IO	SNCM	3.3V
RESETO_L	From the PLD to reset the IO subsystem	1	O	PLD	IO	3.3V
NODE_PG	Power good from processor board	1	O	Processor	IO	3.3V TTL
SYS_PWRGOOD	Global power good from IO board	1	I	IO (PLD)	Processor (PLD)	3.3V
SP{0/1}GPIO	Scalability Port General Purpose I/O	2	I/O	Processor / IO	IO / Processor	1.5V CMOS OD
Legacy		**7**				
A20M_L	A20 Mask	1	I	IO (ICH2)	Processor	3.3V
IGNNE_L	Ignore Numerical Error	1	I	IO (ICH2)	Processor	3.3V
INIT_L	Processor Init	1	I	IO (ICH2)	Processor	3.3V
INTR	Interrupt Request	1	I	IO (ICH2)	Processor	3.3V
NMI	Non-maskable interrupt	1	I	IO (ICH2)	Processor	3.3V
FERR_L	Floating point error	1	O	Processor	IO (ICH2)	3.3V
PMI_L	Processor Management Interrupt (SMI_L)	1	I	IO (ICH2)	Processor	3.3V TTL
JTAG		**5**				
IS_TCK	In System JTAG Clock to processor board	1	I	IO	Processor	3.3V
IS_TDI	In System JTAG Data In from processor board	1	O	Processor	IO	3.3V
IS_TDO	Test Data Out to processor board	1	I	IO	Processor	3.3V
IS_TMS	Test Mode Select to processor board	1	I	IO	Processor	3.3V
IS_TRST_L	Test Reset to I/O board	1	I	IO	Processor	3.3V

IS_JTAGEN_L	Enables the In-System JTAG master	1	I	IO	Processor	3.3V
ISP for processor board PLDs		**5**				
ISP_SDI	In-System Programming Data In	1	I	IO	Processor	3.3V CMOS
ISP_SDO	In-System Programming Data out	1	O	Processor	IO	3.3V CMOS
ISP_EN_L	In-System Programming Enable	1	I	IO	Processor	3.3V CMOS
ISP_MODE	In-System Programming Mode	1	I	IO	Processor	3.3V CMOS
ISP_SCLK	In-System Programming Clock	1	I	IO	Processor	3.3V CMOS
MISC		**31**				
IA64_IA32	Indicates processor type to the IO	1	O	Processor	IO	3.3V TTL or pulled to ground
BINITIN_L	BINIT from PLD to SNC-M	1	I	IO	SNC-M	1.5V
BERRIN_L	To SNC-M to generate machine check on FSB	1	I	IO	SNC-M	1.5V
BINITOUT_L	From SNC-M Only used in 8way	1	O	SNC-M0	SNC-M1	3.3V
BERROUT_L	From SNC-M Only used in 8way	1	O	SNC-M0	SNC-M1	3.3V
ERR[2:0]_L	Error Code Signals	3	I/O	SNC-M	IO(PLD)	1.5V CMOS OD
INT_OUT_L	Generated by SNC-M	1	O	SNC-M	IO (PLD)	3.3V
HP_INT_L	Node hot plug interrupt	1	O	Processor	IO	3.3V
BUSID[2:0]	Strap bits that indicate the configuration bus number of the SNC-M	3	IO	Midplane	SNC-M	1.5V CMOS OD
NODEID[4:0]	Strap bits that indicate node ID to SNC-M	5	IO	Midplane	SNC-M	1.5V CMOS OD
EV[3:0]_L	Event logic interconnect	4	I/O	SNCM/ SPS/SIOH /Processor	SIOH/SPS/ SNC-M/ IO	1.5V CMOS OD

THERMALERT_L	Indicates processor temp out of range	1	O	Processor (proc's)	IO (PLD)	OD 3.3V
PPODOE	Enable processor PPODs	1	I	IO (PLD)	Processor (PLD)	3.3V
AIPPODPG	All installed PPOD powergood.	1	O	Processor	IO	3.3V
CD2D33EN	Enables 3.3V D2D on processor board	1	I	IO	Processor	3.3V
V48EN	Enable 48V FETs for hot plug	1	I	IO (Sahalee/ PLD)	Processor (to FETs)	3.3V
STDBYEN	Enable STDY FETs for hot plug	1	I	IO	Processor	3.3V
INTERLOCK0_L	VHDM Connector interlocking detection	1	I	IO	Processor	3.3V
INTERLOCK1_L	VHDM Connector interlocking detection	1	O	Processor	IO	3.3V
SNCFWHDIS_L	Disables access to the north FWH behind the SNC	1	I	IO	Processor (SNC-M)	1.5V
SNCFWHWP_L	Unlocks the SNC-M FWH to allow updates	1	I	IO	Processor (SNC-M)	1.5V
33STDBY_GD	Indicates the state of the 3.3VSTDBY on the Processor board	1	O	Processor	IO	3.3V
SM		**2**				
I2C_PROCESSOR_SDA	I2C Data connected to proc and mem boards	1	I/O	IO, Processor	Processor, IO	3.3V CMOS
I2C_PROCESSOR_SCL	I2C clock connected to proc and mem boards	1	I	IO	Processor	3.3V CMOS
ACPI		**1**				
STPCLK_L	Stop clock for IA32 support	1	I	IO (ICH2)	Processor	3.3V
Reserved		**60**				
Power/Ground		**4**				

48V	18 A	3 blades	I	IO	Processor	Analog
48VGND	18 A	3 blades	I	Processor	IO	Analog
12V_STDBY	1 A	2	I	IO	Processor	Analog
3.3V_STDBY	1 A	2	I	IO	Processor	Analog
GND			I	IO	Processor	Analog

2.6.1.4 Memory Board Pinout

The processor baseboard interfaces to the memory board through the Megarray* connector, a 10 row X 40 column 400 BGA style connector. There is one connector on the primary side and one on the secondary side to support four Rambus channels and miscellaneous signals between the processor board and memory board. Table 2-27 shows the pinout of this connector.

Table 2-27. Processor Baseboard Memory Connector Pinout (MegArray*) – Pins A1-F40

Col	Row A	B	C	D	E	F	G	H	J	K
1	CH1_DQA8	GND	MRHD_PWRGOOD	MEMRST0_L	+1.8V	+1.8V	I2C_MEM_SCL	I2C_MEM_SDA	GND	CH2_DQA8
2	GND	CH1_DQA7	GND(mem Interlock)	+1.8V	+1.8V	+1.8V	+1.8V	GND	CH2_DQA7	GND
3	CH1_DQA6	GND	+1.8V	CH1_VREF_TM	GND	GND	CH2_VREF_TM	+1.8V	GND	CH2_DQA6
4	GND	CH1_DQA5	+1.8V	+1.8V	GND	GND	+1.8V	+1.8V	CH2_DQA5	GND
5	CH1_DQA4	GND	GND	CH1_VREF_FM	+1.8V	+1.8V	CH2_VREF_FM	GND	GND	CH2_DQA4
6	GND	CH1_DQA2	GND	+1.8V	+1.8V	+1.8V	+1.8V	GND	CH2_DQA2	GND
7	CH1_DQA3	GND	+1.8V	DIMM_PWRGOOD	GND	GND	GND	+1.8V	GND	CH2_DQA3
8	GND	CH1_DQA1	GND	GND	+2.5V	+2.5V	GND	GND	CH2_DQA1	GND
9	CH1_DQA0	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_DQA0
10	GND	CH1_CFMN	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	CH2_CFMN	GND
11	CH1_CFMP	GND	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	GND	CH2_CFMP
12	GND	CH1_CTMN	GND	GND	+2.5V	+2.5V	GND	GND	CH2_CTMN	GND
13	CH1_CTMP	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_CTMP
14	GND	CH1_DRCG_OUTP	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	CH2_DRCG_OUTP	GND

15	CH1_DRCG_OUTN	GND	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	GND	CH2_DRCG_OUTN
16	GND	CH1_RQ7	GND	GND	+2.5V	+2.5V	GND	GND	CH2_RQ7	GND
17	CH1_RQ6	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_RQ6
18	GND	CH1_EXRC	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	CH2_EXRC	GND
19	CH1_RQ5	GND	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	GND	CH2_RQ5
20	GND	CH1_RQ4	GND	GND	+2.5V	+2.5V	GND	GND	CH2_RQ4	GND
21	CH1_EXCC	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_EXCC
22	GND	CH1_RQ3	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	CH2_RQ3	GND
23	CH1_RQ2	GND	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	GND	CH2_RQ2
24	GND	CH1_RQ1	GND	GND	+2.5V	+2.5V	GND	GND	CH2_RQ1	GND
25	CH1_DQB0	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_DQB0
26	GND	CH1_RQ0	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	CH2_RQ0	GND
27	CH1_DQB1	GND	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	GND	CH2_DQB1
28	GND	CH1_DQB2	GND	GND	+2.5V	+2.5V	GND	GND	CH2_DQB2	GND
29	CH1_DQB3	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_DQB3
30	GND	CH1_DQB4	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	CH2_DQB4	GND
31	CH1_DQB5	GND	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	GND	CH2_DQB5
32	GND	CH1_DQB6	GND	GND	+2.5V	+2.5V	GND	GND	CH2_DQB6	GND
33	CH1_DQB7	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_DQB7
34	GND	CH1_DQB8	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	CH2_DQB8	GND
35	CH1_CMD	GND	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	GND	CH2_CMD
36	GND	CH1_SCK	GND	GND	+2.5V	+2.5V	GND	GND	CH2_SCK	GND
37	CH1_SIO	GND	GND	GND	+2.5V	+2.5V	GND	GND	GND	CH2_SIO

38	GND	+3.3VSTDBY	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	+2.5V	GND
39	+12VSTDBY	MEM_P_125GOOD	+2.5V	+2.5V	GND	GND	+2.5V	+2.5V	MEM_P_PRES_L	+3.3V
40	+12VSTDBY	I2C_MRHD_SDA	I2C_MRHD_SCL	PSENSE_25_RTN	PSENSE_25	PSENSE_125	+2.5V	+2.5V	FRU1_SA0	+3.3V

2.6.1.5 Processor Board Power Connection

The processor baseboard draws the 48 V DC power from the midplane through the blades of the VHDM connectors. See Table 2-28 for pinout. The 3.3 V and the 12 V standby voltages are provided to the processor baseboard through the midplane VHDM connector via two pins for each voltage. Each of the power blades is rated at 10 A, and each signal pin is rated at 1 A.

Table 2-28. Processor Baseboard Power Connection (VHDM*)

Signal	Current	Pin #	# of Pins
+48 V	18 A	PA1 – PA4 PC1 – PC4 PE1 – PE4	3 blades
48V Return	18 A	PB1 – PB4 PD1 – PD4 PF1 – PF4	3 blades
+12 V Standby	1 A	E11, F11	2 pins
3.3 V Standby	1 A	B11, C11	2 pins
GND		See VHDM Pin List	GND blades + misc pins

2.6.1.6 Itanium® 2 Processor Socket Pinout

A detailed description of the Itanium 2 processor signals and their pinouts are described in the *Intel® Itanium® 2 EMTS*.

2.6.2 Mechanical Specifications

Figure 2-20 and Figure 2-21 show the mechanical specifications and the connector positions for the processor baseboard. The board outline dimensions are 14.6” x 10.7”.

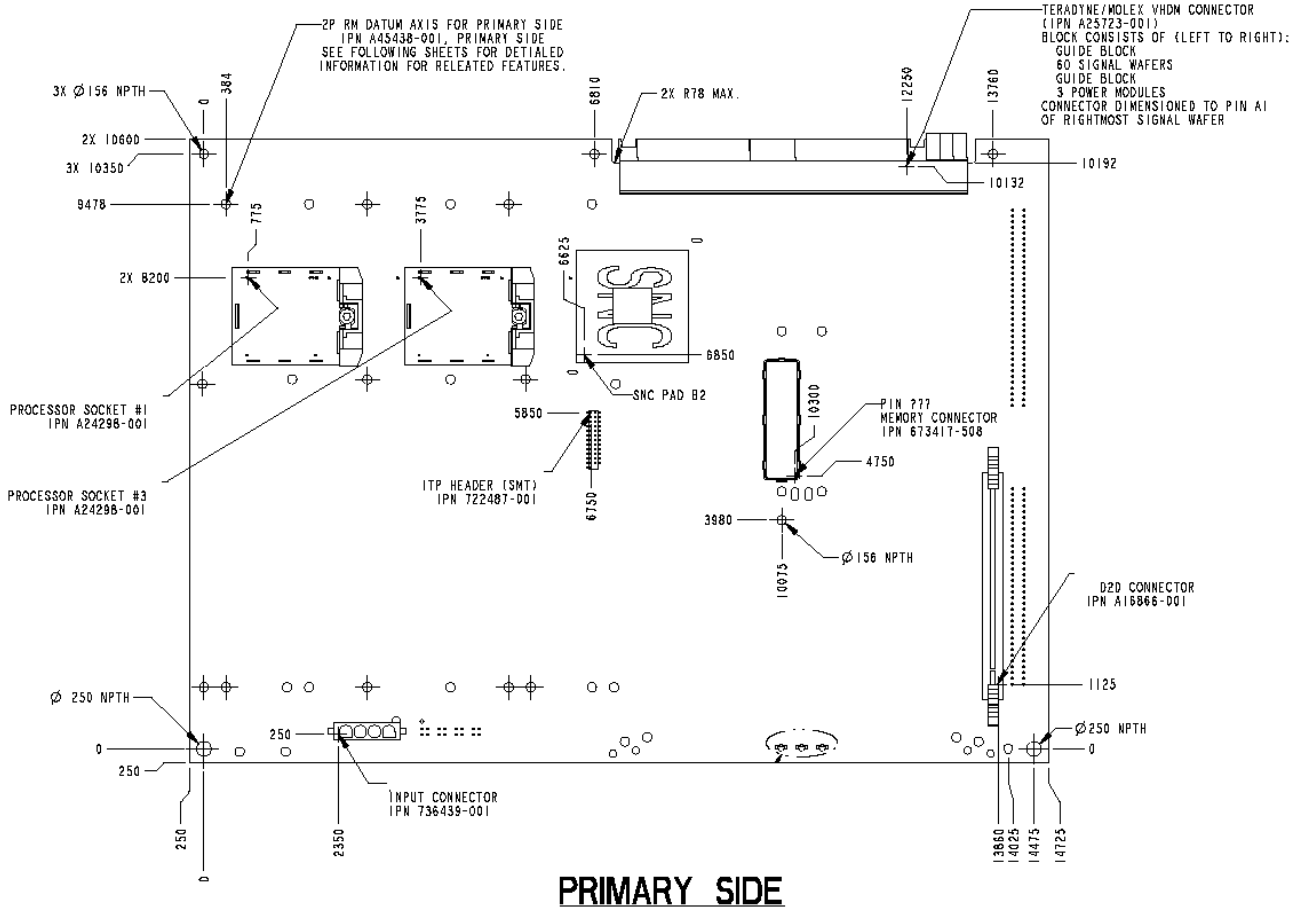


Figure 2-20. Processor Baseboard Mechanical Drawing (Primary)

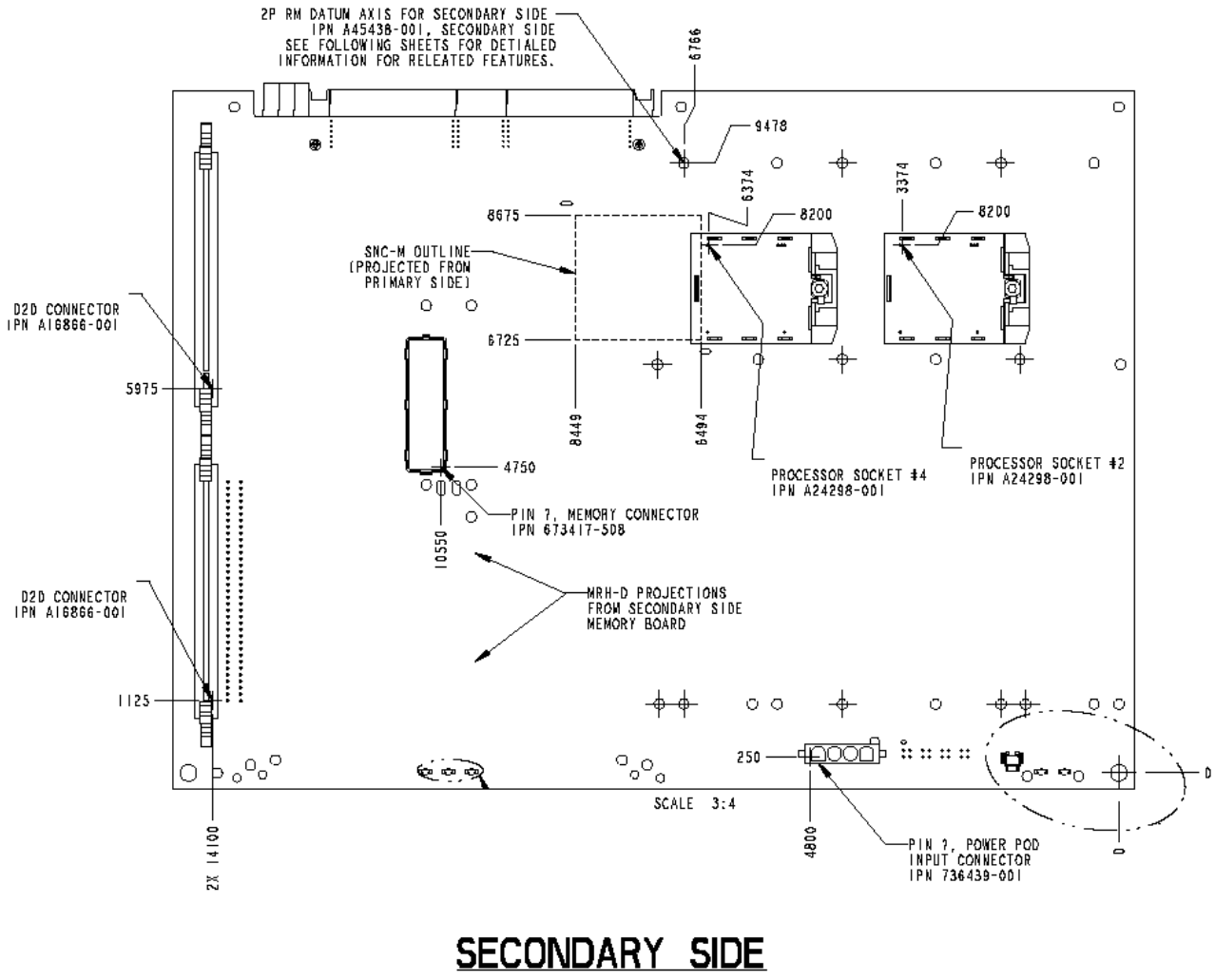


Figure 2-21. Processor Baseboard Mechanical Drawing (Secondary)

2.6.3 Processor Retention Mechanism

The processor retention mechanism is shown in Figure 2-22. There are two used for the S870BN4 processor board: one to support the two processors on the primary side and one for the two processors on the secondary side. The primary purpose of the retention mechanism is to provide a secure base to fasten the processor and power pod assembly to the processor board.

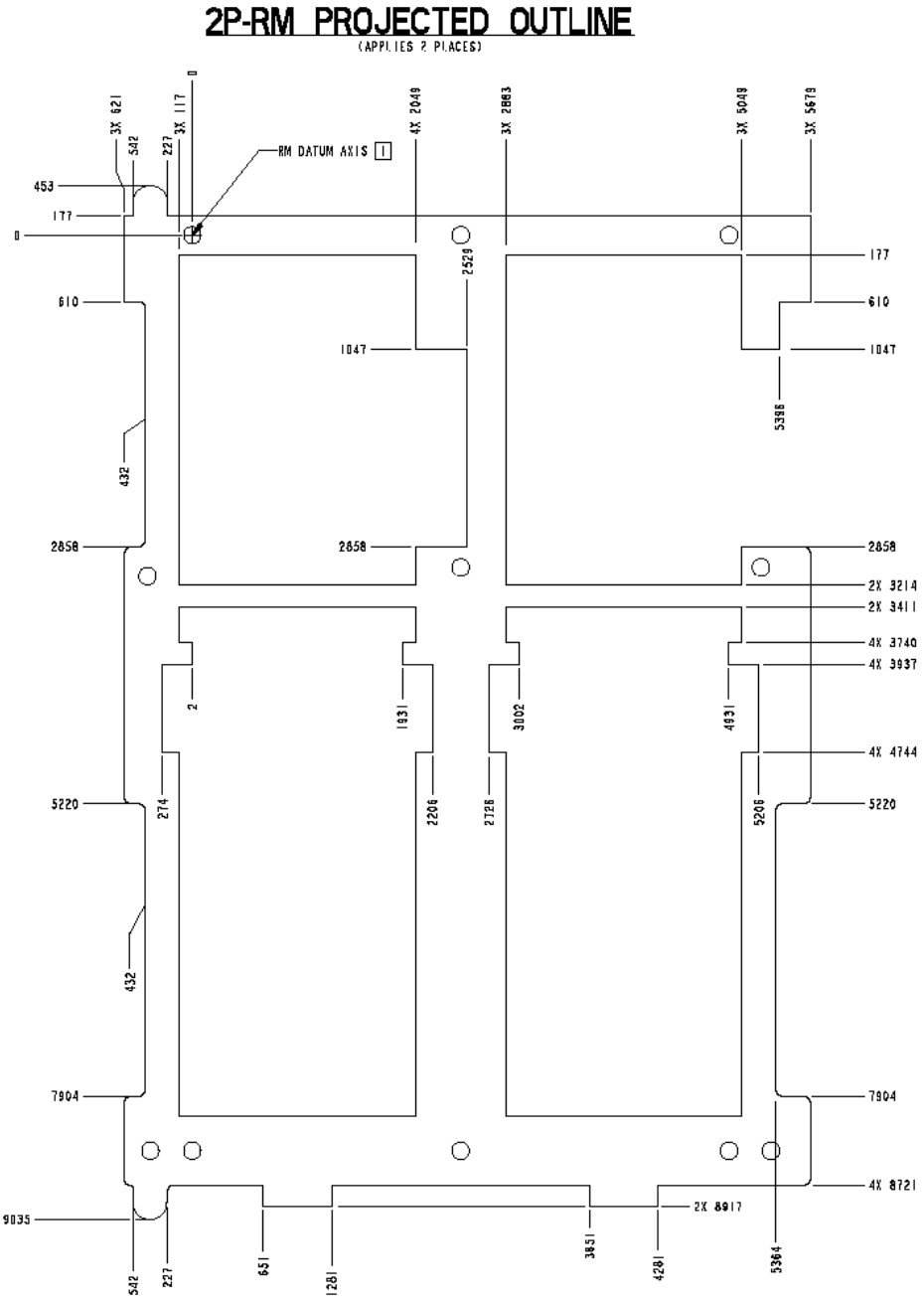


Figure 2-22. Processor Retention Mechanism

2.6.4 Thermal Requirements

Components requiring forced convection cooling are shown in the following table. Refer to the listed reference documents for specific temperature and airflow requirements. The processors' enabled heat sinks require tightly ducted, dedicated flow to meet thermal requirements. Careful attention to specifications and reference documents will ensure that cooling requirements for these components can be met. Maximum board operating temperatures are dependent on system layout and airflow. Board components not listed in the table will be adequately cooled if the cooling requirements for the listed components are met.

Table 2-29. Critical Processor Board Components

Component	Specifications[1]		Reference Document	Heat Sink
Processors	T_{IHS}	5°C -85 °C	Intel® Itanium® 2 EMTS	Intel Enabled
Chip set - SNCM	$T_{Junction}$	105 °C	Intel®E8870 EMTS	Intel Enabled
T-D2Ds	Free stream velocity and $T_{Ambient}$	spec has: 300LFM, temp is 0 to 55 °C	T-D2D specification	Integral

2.6.5 Quality and Reliability Target

The quality and reliability targets are outlined in the *25-GS3000 Specification* and *Environmental Standards Handbook (Intel document# 662394-05).*

Quality goals outlined for the processor baseboard are:

- Intel® Board Factory Line fall out 3000 DPM
- Board-level VCLF (Verified Customer Line Fallout) < 5000 DPM at FLQ (Full Qual Level)

Reliability goals outlined for the processor baseboard are:

- Board Mean Time Between Failure (MTBF) goal > 250,000 hours at 35°C operating temperature.

[1] Specifications listed here are subject to change. See the reference document for the latest thermal information.

3. Memory Module

This section provides a more detailed look at the architecture and functionality of the DDR - based memory portion of the processor building block. This board is designed to support DDR memory and has eight DIMM sites. It is designed to interface with the Intel® 870 chip set and uses Intel DMH devices to increase memory capacity and translate from Rambus signaling to DDR signaling. The S870BN4 processor board is designed to support two memory boards, and both memory boards must be present for the system to operate.

3.1 Overview

The memory module consists of a printed circuit board (a.k.a., memory board) and a set of DIMMs mounted to it. The memory board plugs into a connector on the processor board. The memory module's primary features include:

- Support for up to 16 GB of DDR memory using eight 2-GB DIMMs. Each processor module contains two memory boards for a total of 32 GB per system.
- Eight DDR DIMM sockets for accepting 184-pin DDR DIMM modules.
- Two DMH devices per board. This allows two Rambus channels from the 870-memory controller (SNC) to be extended to four DDR channels on the memory board.
- The Rambus channel supports 400-MHz operation and the DDR channels support 100-MHz operation.
- Onboard 2.5-V to 1.25-V converter to provide DDR signal termination.
- Mezzanine connector allows for 4-mm board-to-board spacing between memory board and processor board. The low profile allows for a 4U form factor.

Figure 3-1 depicts the general architecture of the memory module and shows the placement of components and connectors on the memory board.

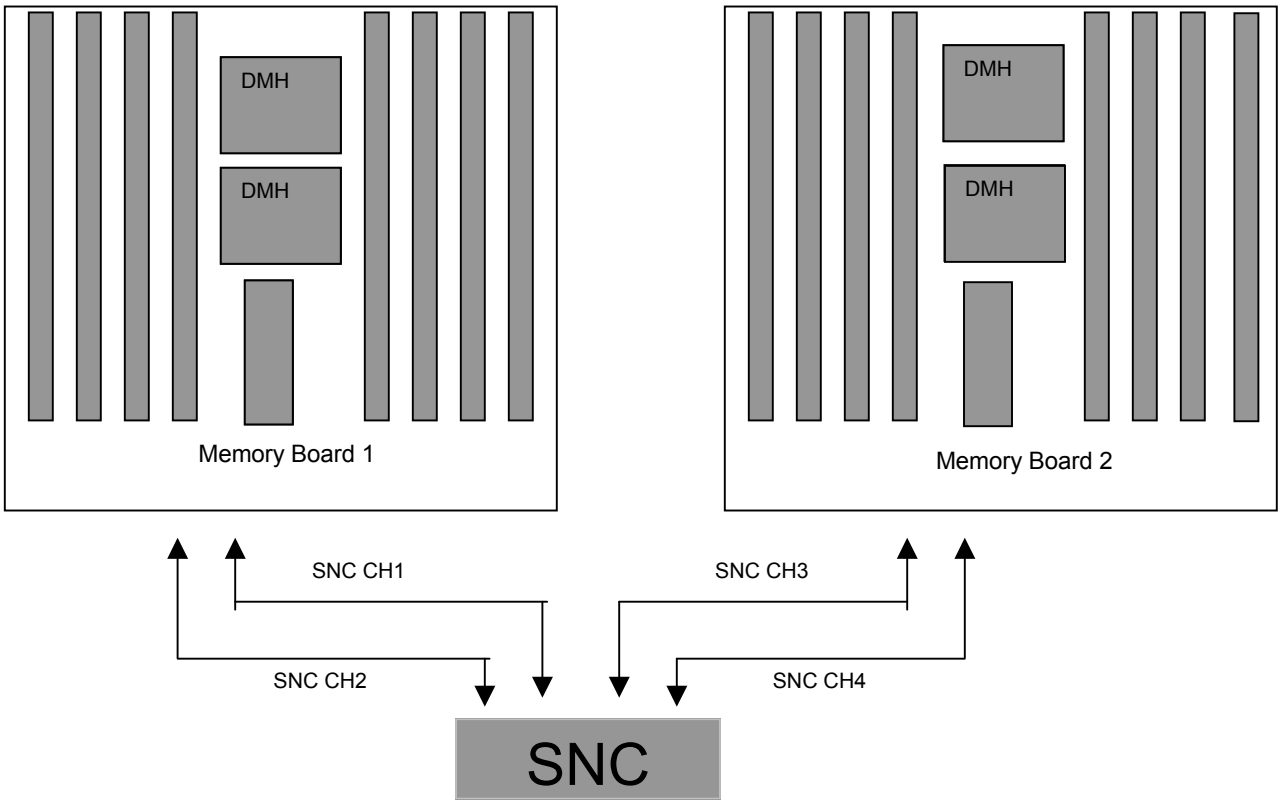


Figure 3-1. Top Level Intel® Server Board SR870BN4 Memory System Block Diagram

The following block diagram shows the flow of memory signals, excluding clocks, from the SNC to the DIMMs.

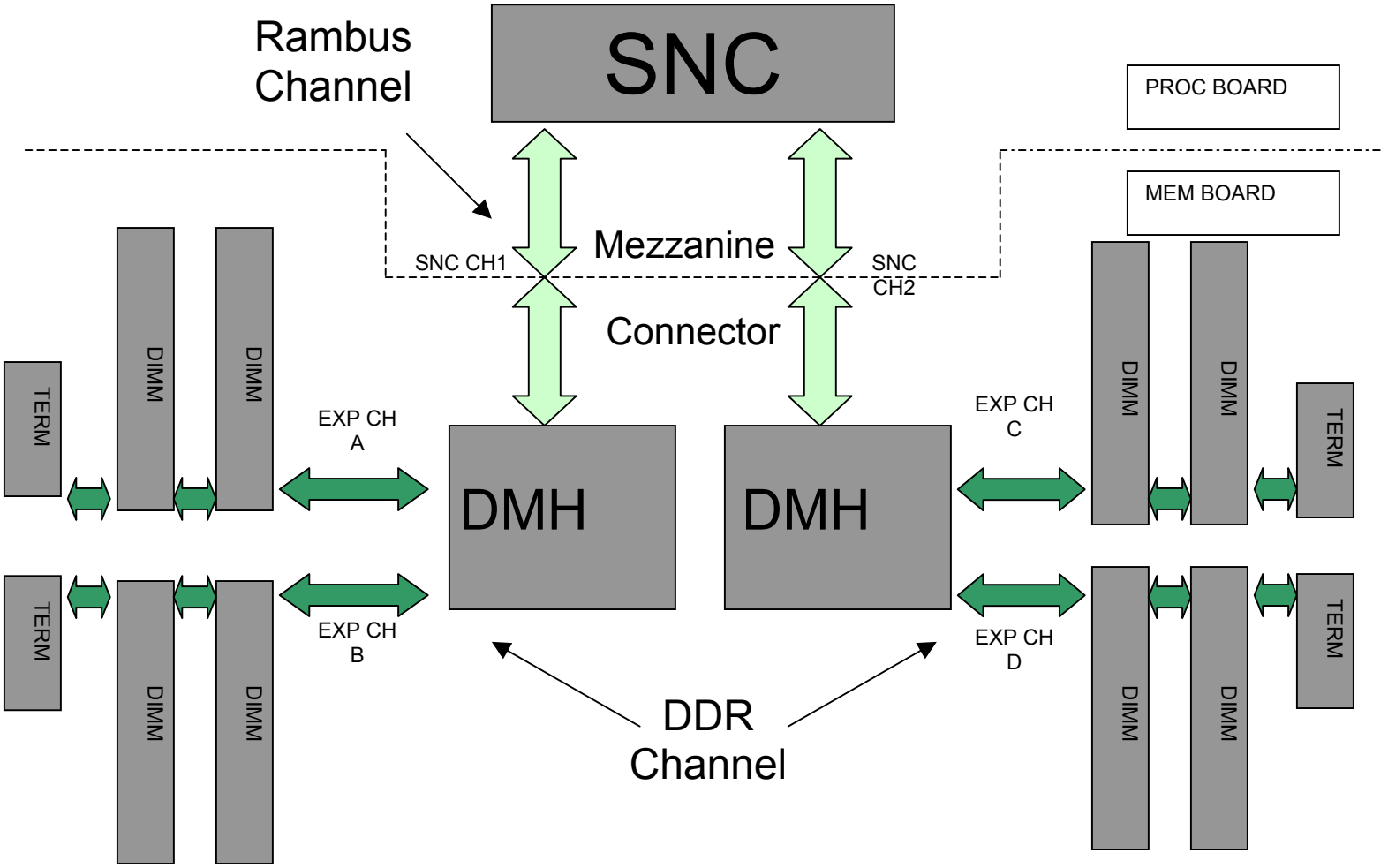


Figure 3-2. Memory Signals

The following diagram shows the flow of Rambus and DDR clocks. Each block arrow represents a differential pair of clocks.

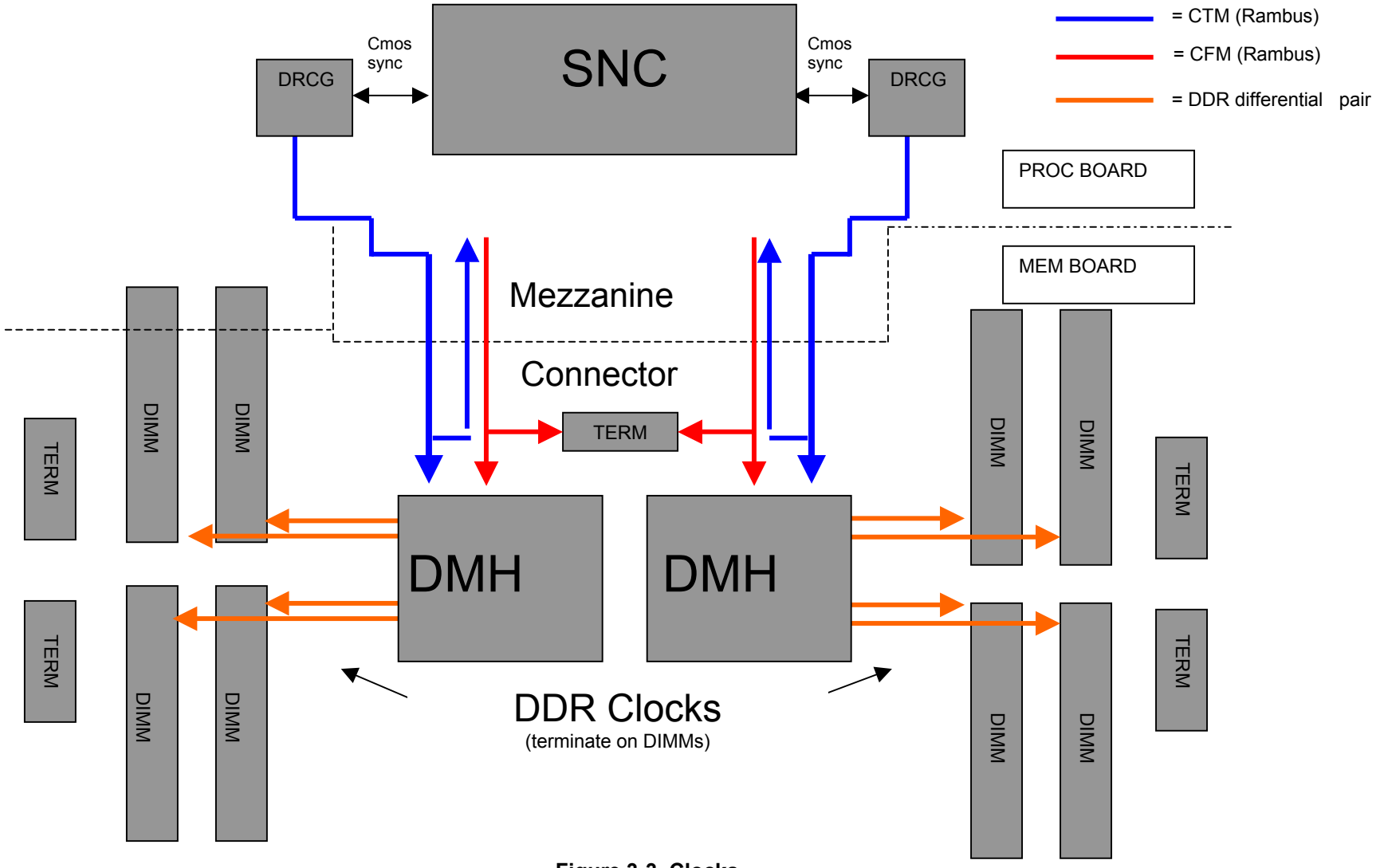


Figure 3-3. Clocks

The following block diagram illustrates the reset signals on the board.

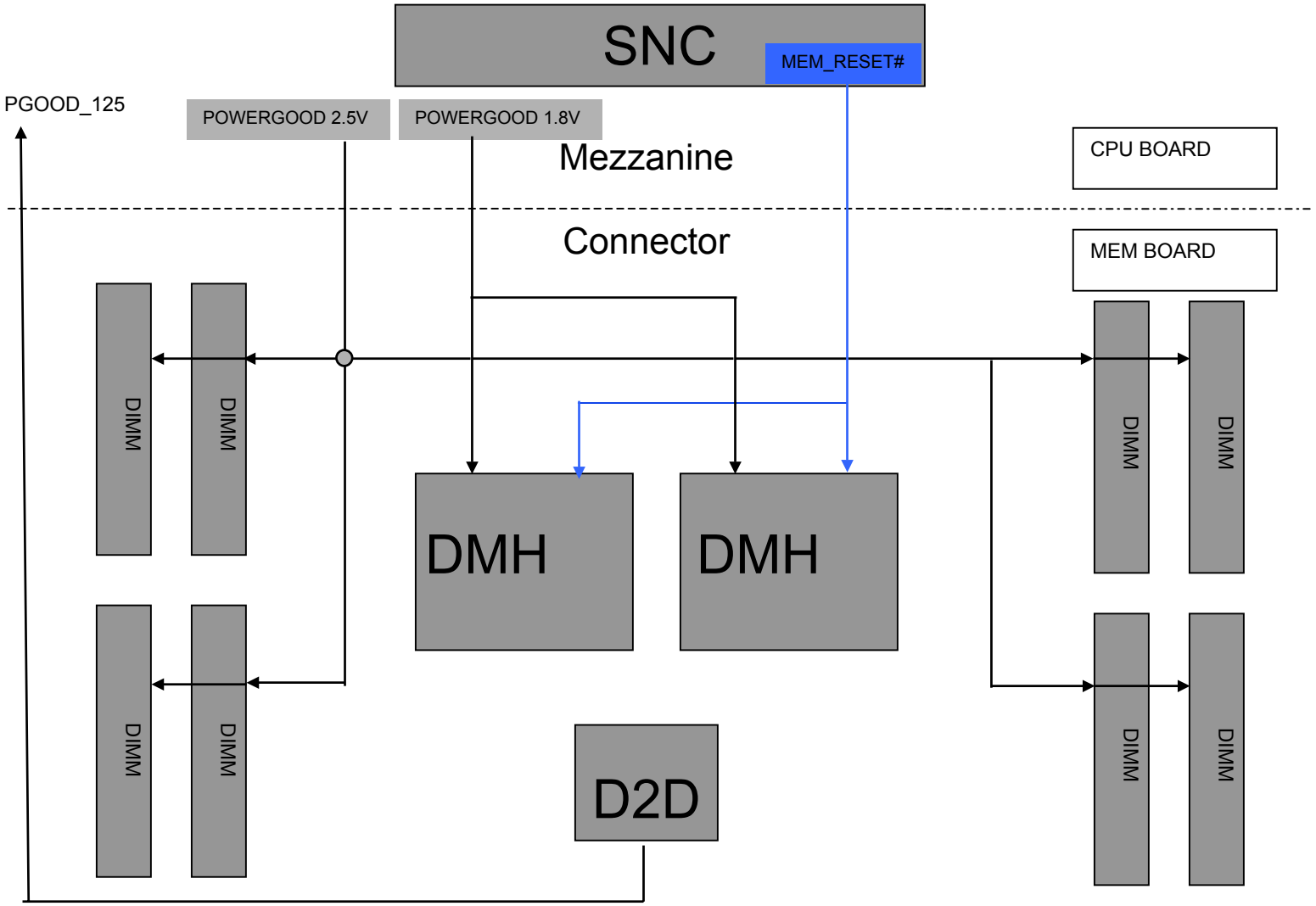


Figure 3-4. Reset Signals

This final block diagram illustrates some of the miscellaneous signals left on the memory board.

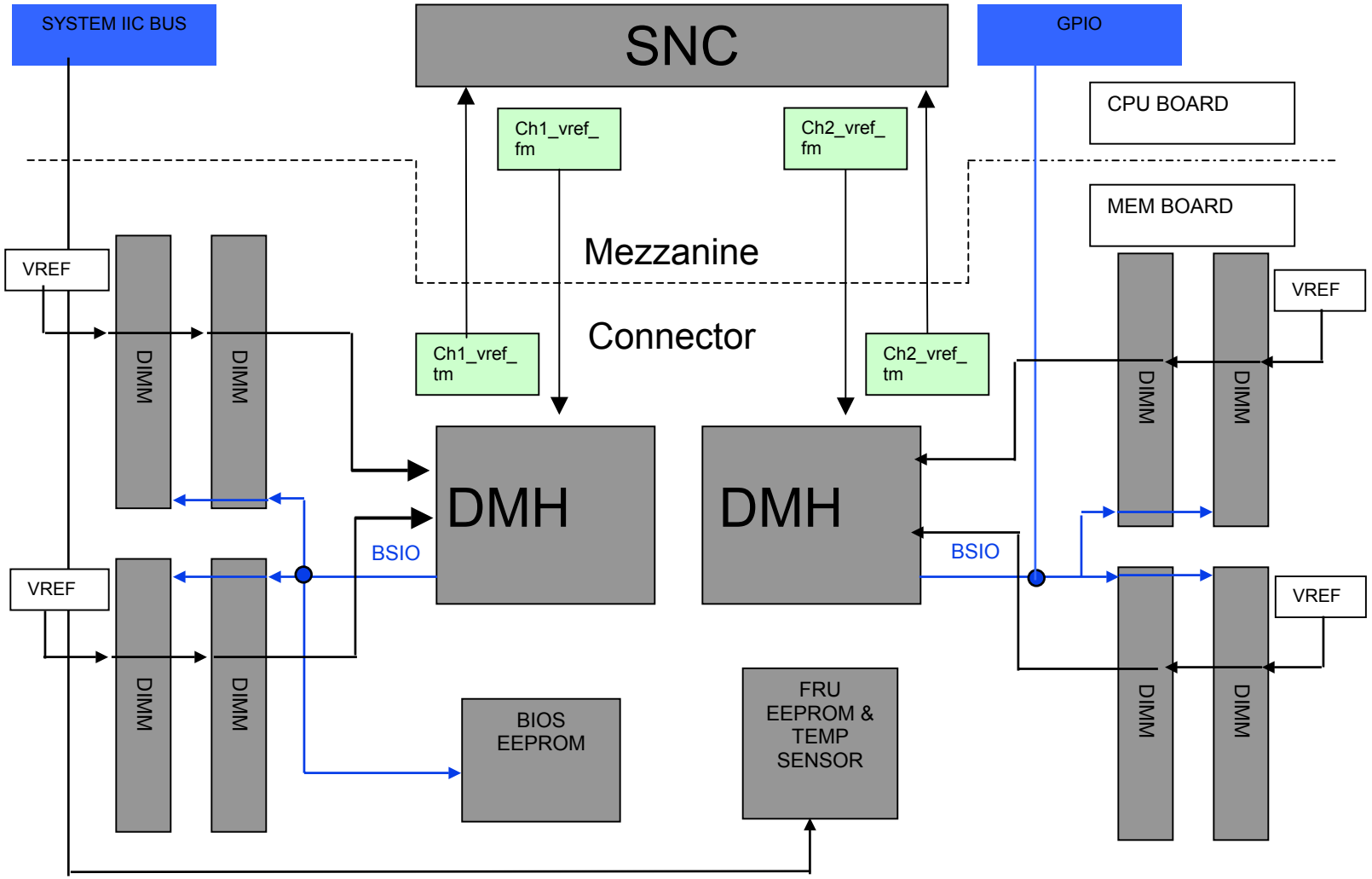


Figure 3-5. Miscellaneous Signals

3.2 Functional Architecture

This section describes how each functional block operates.

3.2.1 DDR Memory Array

The memory array on the Server Board S870BN4 DDR memory board consists of eight DIMM sockets. Two SNC Rambus memory channels are split into four DDR channels using the DMH devices. Each channel consists of two DIMM sockets. A Server System SR870BN4 requires two memory boards for a total of 16-DIMM sockets per system. This also makes a total of four SNC memory channels. Each SNC channel has a maximum bandwidth of 1.6 GB/s, for a total of 6.4 GB/s for the system.

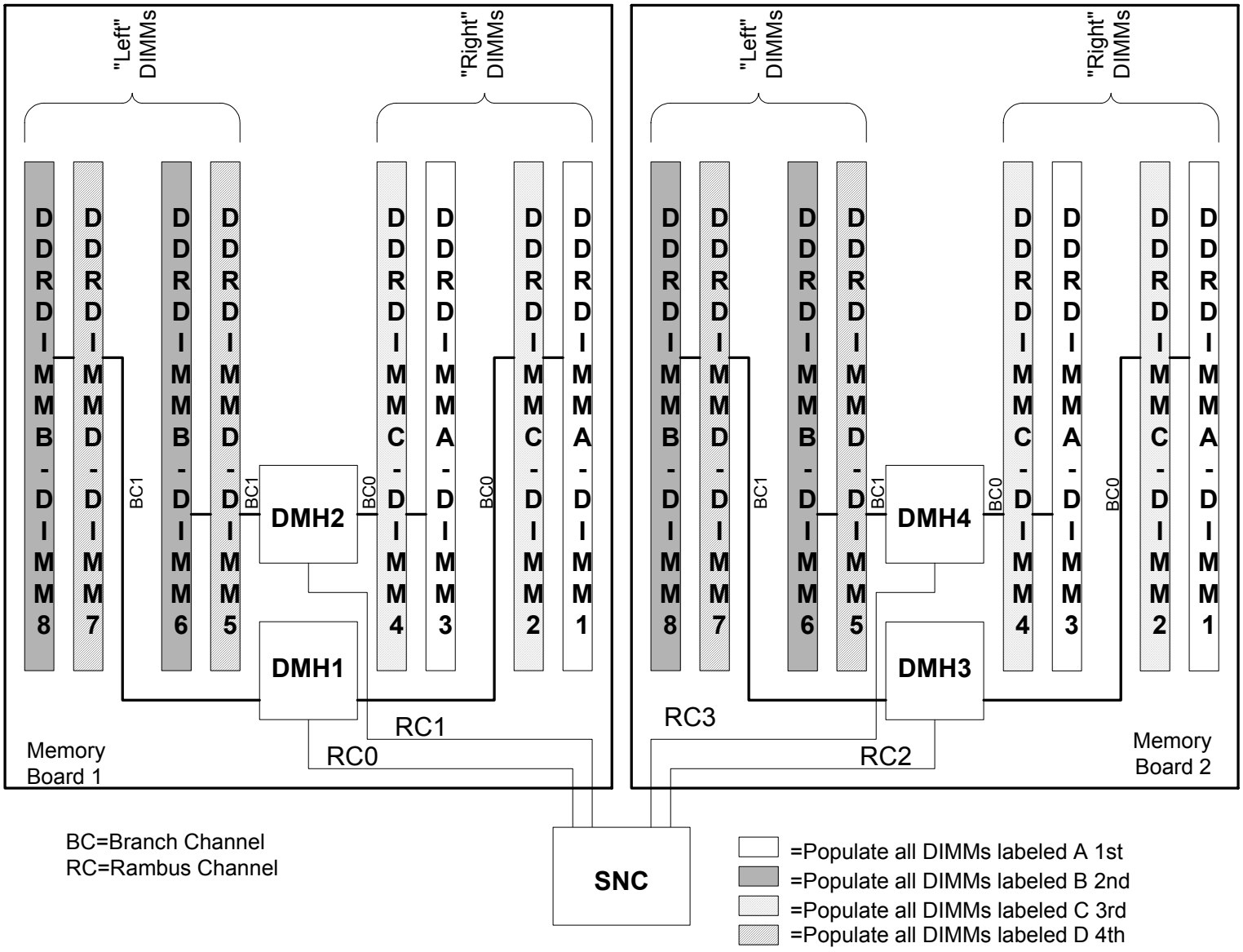
3.2.1.1 Memory Configurations

This memory board will support the following DDR DRAM technologies and DIMM sizes *(all combinations not yet known).* A subset of these will be validated. Pease refer to the *Intel® Server System SR870BN4 Memory Validation Test Plan* for details on supported and tested configurations.

Table 3-1. Available Memory Configurations

Device Technology	DIMMs				Node Cap (MB)	
					Min	Max
Mb	# devices	Org	MB x72	MB	4	16
64	9	2Mx8	8	64	256	1024
	18	2Mx8 stk 4Mx4	16	128	512	2048
	36	4Mx4stk	32	256	1024	4096
128	9	4Mx8	16	128	512	2048
	18	4Mx8stk 8Mx4	32	256	1024	4096
	36	8Mx4stk	64	512	2048	8192
256	9	8Mx8	32	256	1024	4096
	18	8Mx8 stk 16Mx4	64	512	2048	8192
	36	16Mx4stk	128	1024	4096	16384
512	9	16Mx8	64	512	2048	8192
	18	16Mx8 stk 32Mx4	128	1024	4096	16384
	36	32Mx4stk	256	2048	8192	32768
1024	9	32Mx8	128	1024	4096	16384
	18	32Mx8 stk 64Mx4	256	2048	8192	32768

3.2.1.2 DIMM Population Rules



The following rules apply to populating the array:

The DIMMs off each DMH must be symmetrical with the DIMMs off all the other DMHs. That is, commonly shaded/named DIMM slots in the preceeding diagram must hold the same type of DIMM on DMH 1, 2, 3, and 4. The memory upgrade granularity is the row of 4 DIMMs, one on each DMH, which collectively provides a cache line. Memory must be added to both mezzanine boards for a complete row. Follow the silkscreen numbering convention for adding DIMMs, populating all DIMMs labeled A, then B, and so on.

1. Within a single row, all DIMMs must be identical (i.e., the same size/technology DIMM with the same number of devices). Contents of all rows do not have to be identical.
2. The two DDR branch channels on an DMH do not need to have the same number or type of DIMMs.
3. DIMMs must be populated according to the silk-screen on the memory board, per the shading population instructions in the preceeding diagram.
4. For best performance,the amount of memory in the “left” DIMMs should equal the amount of memory in the “right” DIMMs.

Up to four different DIMM technologies (rows) are supported. Thus, each of the four possible DIMM rows can be different technologies. For best performance, the amount of memory on each DMH DDR branch channel should be the same.

3.2.2 DMH

The DMH component provides the ability to support two DDR “branch channels” on one SNC Rambus expansion channel. It acts as a translator for turning Rambus accesses into DDR accesses and vice versa. See the *DMH External Design Specification* or the *Component Specification* for more details.

3.2.3 System Management Interface

The memory board contains an integrated Field Replaceable Unit (FRU) EEPROM / temperature sensor which is connected to the system I^2C bus coming from the processor board. This I^2C bus is separate from the Serial Presence Detect (SPD) bus coming out of the DMH devices used for accessing DIMM SPD EEPROMs. The integrated EEPROM / temperature sensor is a Dallas* DS1624 part. Refer to the data sheet for this device for specific programming information.

The I^2C address for this device depends on which MegArray* connector the memory board connects to on the processor board. A bit, coming from the processor board, sets the Least Significant Bit (LSB) of the device address. The following table identifies the device address by processor MegArray* location.

Table 3-2. Device Address by Processor MegArray* Location

Processor MegArray Location	Memory Board FRU EEPROM / Temp Sensor Address
Topside MegArray	1001110b
Bottom side MegArray	1001111b

Read-only access to the EEPROM provides the current revision and serial number of the board. The device can hold 256 bytes of data. The temperature sensor can measure temperatures ranging from –55 °C to +125 °C in 0.03125 °C increments.

3.2.4 Embedded 2.5-V to 1.25-V D2D

The memory board contains one 2.5-V to 1.25-V D2D for providing the DDR termination voltage. Per Dynamic Data Read (DDR) specification, the converter output is required to track DC fluctuations in the 2.5-V input. In a worst-case loading condition, the converter will be required to source or sink 6 Amps of current. The converter provides Over Current Protection (OCP), Over Voltage Protection (OVP), and a power good signal that is routed down to the processor board for determining overall system power good status.

3.3 Signal Descriptions

3.3.1 Rambus Signals

These signals comprise the Rambus memory bus. Rambus Signal Level is used for most Rambus signals.

Table 3-3. Rambus Signals

Signal Name	Type	Description
CH(2:1)_DQA(8:0)	RSL	Data Bus A. A nine-bit bus carrying a byte of read or write data between SNC and DMH.
CH(2:1)_DQB(8:0)	RSL	Data Bus B. A nine-bit bus carrying a byte of read or write data between SNC and DMH.
CH(2:1)_RQ(7:0)	RSL	Row/Column Request. An eight-bit bus carrying control and address info for row and column accesses between SNC and DMH.
CH(2:1)_CTM, CH(2:1)_CTM#	RSL	Clock to Master. A differential clock pair originating at the SNC DRCG. It crosses the MegArray* connector, taps off of the DMH, and finishes back at the SNC. It is used for DMH to SNC transactions.
CH(2:1)_CFM, CH(2:1)_CFM#	RSL	Clock from Master. An unbuffered version of CH(2:1)_CTM. It originates at the SNC, enters the DMH, and is terminated on the memory board. It is used for SNC to DMH transactions.
CH(2:1)_EXCC, CH(2:1)_EXRC	RSL	Expander Column Control and Row Control. Sideband signals used when multiple MRH-R devices reside on one bus. Left in design for possible future MRH-R implementations.
CH(2:1)_SCK	CMOS	Serial Clock. Clock source for accessing DMH control registers.
CH(2:1)_CMD	CMOS	Serial Command. Used for reading and writing DMH control registers.
CH(2:1)_SIO	CMOS	Serial I/O. Used for reading and writing DMH control registers. This is a 1-MHz signal.

3.3.2 DDR Signals

These signals comprise the DDR stick channels from the DMH to the DDR DIMM sockets. SSTL is Stub Series Terminated Logic.

Table 3-4. DDR Signals

Signal Name	Type	Description
CH(A:D)_A(14:0)	SSTL	SDRAM Address. Used for providing multiplexed row and column address to SDRAM.
CH(A:D)_BA(1:0)	SSTL	SDRAM Bank Active. Used to select the bank within a device.
CH(A:D)_DQ(71:0)	SSTL	SDRAM Data. Independent data paths to allow simultaneous data movement on both DMH channels.
CH(A:D)_RAS#	SSTL	SDRAM Row Address Strobe. Used with CS#, CAS#, and WE# to specify the SDRAM command.
CH(A:D)_CAS#	SSTL	SDRAM Column Address Strobe. Used with CS#, RAS#, and WE# to specify SDRAM command.
CH(A:D)_WE#	SSTL	SDRAM Write Enable. Used with CS#, RAS#, and CAS# to specify SDRAM command.
CH(A:D)_CS(7:0)#	SSTL	SDRAM Chip Select. Used for selecting one of eight SDRAM rows.
CH(A:D)_CKE	SSTL	SDRAM Clock Enable. Used for signaling self refresh entry and self refresh exit commands to an SDRAM row.
CH(A:D)_CLK(3:0), CH(A:D)_CLK(3:0)#	SSTL	SDRAM Clocks. Each DIMM gets its own differential clock. Runs at 100 MHz.
CH(A:D)_DQS(17:0)#	SSTL	SDRAM Data Strobe. Used for determining when read and write data is valid.
BC(1:0) SRCAL	SSTL	Slew Rate Calibration. Used for slew rate calibration.
SREF(1:2)	SSTL	SDRAM Feedback Output. Used to calibrate SDRAM clock.
SREFFB(1:2)	SSTL	SDRAM Feedback Input. Used to calibrate SDRAM clock.

3.3.3 Miscellaneous Signals

Table 3-5. Miscellaneous Signals

Signal Name	Type	Description
MEM_RESET#	CMOS 1.8 V	**Memory Reset.** This signal is used for resetting the DMH internal logic during power up sequence.
PGOOD1_8V	CMOS 1.8 V	**DMH Powergood.** Provides asynchronous reset to entire DMH core.
PGOOD2_5V	CMOS 2.5 V	**DIMM Powergood.** All register outputs on each DIMM are asynchronously forced low when this signal is low.
I2C_CLK	CMOS OD 3.3 V	**I2C clock.** System I2C bus used for system management.
I2C_DATA	CMOS OD 3.3 V	**I2C data.** System IIC bus used for system management.
MRHD(1:0)_SCL	CMOS OD 2.5 V	**MRHD IIC CLOCK.** IIC bus driven by DMH devices. Used primarily for reading EEPROM devices on DIMMs.
MRHD(1:0)_SDA	CMOS OD 2.5 V	**MRHD IIC DATA**. IIC bus driven by DMH devices. Used primarily for reading EEPROM devices on DIMMs.

Signal Name	Type	Description
MEM_PRES(2:1)	CMOS	**Memory Present.** Signal used for processor board to determine if memory board is present and fully seated.
PGOOD_125	CMOS OD 3.3 V	**Powergood 1.25 V.** This is an output from the 1.25-V D2D. It is used by the processor board to determine system powergood status.
SENSE_25	Analog	**Sense 2.5 V.** Sense line for 2.5 V. Used by 2.5-V D2D on processor board.
SENSE_RTN	Analog	**Sense Return.** Sense return for 2.5 V. Used by 2.5-V D2D on CPUB board.
SENSE_125	Analog	**Sense 1.25 V.** Sense line for 1.25 V. Used by voltage monitor on processor board.

3.3.4 Voltage References

Table 3-6. Voltage Reference Signals

Signal Name	Type	Description
CH(2:1)_VREF_TM	Analog	**Rambus Voltage Reference to Master.** RSL voltage reference generated on memory board and used by SNC.
CH(2:1)_VREF_FM	Analog	**Rambus Voltage Reference from Master.** RSL voltage reference generated on processor board and used by DMH.
CH(A:D)_VREF	Analog	**DDR Voltage Reference.** Voltage references used by DDR channels.
12V	Analog	**12 Volts.** Used for control circuitry in 1.25-V converter.
3.3V STDBY	Analog	**3.3 Volts Standby.** Used to power FRU EEPROM / temperature sensor.
2.5V	Analog	**2.5 Volts.** Used to power DMH, DIMMs, and 1.25-V converter.
1.8V	Analog	**1.8 Volts.** Used by DMH RACs and RSL termination.
1.25V	Analog	**1.25 Volts.** Used for DDR termination.

3.4 Electrical, Mechanical, and Environmental Specifications

This section specifies the operational parameters and physical characteristics of the Server Board S870BN4 DDR-based memory module board. This is a board-level specification only.

3.4.1 Absolute Maximum Ratings

Operation of the memory module, at conditions beyond those shown in Table 3-7, may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 3-7. Absolute Maximum Ratings

Feature	Absolute Maximum Rating
Operating Temperature	10 °C to 35 °C
Storage Temperature	-55 °C to +150 °C

Note: Chassis design must provide proper airflow.

The rest of this section specifies normal operating conditions for the memory board, as well as mechanical specifications for the module and connector interface to the processor board.

3.4.2 Thermal

The memory module is susceptible to failure if the proper temperature and airflow are not maintained.

Memory power dissipation can vary widely between devices from different vendors. Depending on the memory vendors supported, required airflow also would vary. DDR thermal specifications have not been finalized and exact flow requirements are to be determined.

3.4.3 Memory Board Thermal Requirements

Components requiring forced convection cooling are shown in the following table. Refer to the reference documents for specific temperature and airflow requirements. Memory power dissipation can vary widely between devices from different vendors. Depending on the memory vendors supported, required airflow may vary. As a guideline, the DIMM power shown in this table can be supported if the ambient temperature delivered to the DIMMs is $\leq$ 40°C and air velocity is > 170 lfm. 95°C DRAM junction temperature was assumed to be the specification limit. Maximum board operating temperatures are dependent on system layout and airflow. Board components not listed in the table will be adequately cooled if the cooling requirements for the listed components are met.

Table 3-8. Critical Memory Board Components

Component	Specifications		Reference Document	Heat Sink
Memory	$P_{Dissipation}$	11 W per DIMM in maximum configuration, 14 W per DIMM in minimum configuration	Memory data sheet	None
Chipset – MRHD	$T_{Junction}$	105 °C	Intel® 870 EMTS	Intel Enabled

3.4.4 Electrical

This section describes the memory module's electrical and power consumption requirements.

3.4.5 Voltage Tolerances

The processor baseboard must provide 12 V, 3.3 V, 2.5 V, 1.8 V, and RDRAM Vref (1.4 V) to this memory board. An onboard 2.5-V to 1.25-V converter generates DDR Vterm (1.25 V), and DDR Vref is generated by a resistor divider from 2.5 V. Table 3-9 specifies acceptable tolerance ranges.

Table 3-9. Acceptable Tolerance Ranges

DC Voltage	Tolerance

DC Voltage	Tolerance
12 V	12 V +/- 5 %
3.3 V	3.3 V +/- 5 %
2.5 V (Vdd)	2.5 V +/- 0.2 V
1.8 V	1.8 V +/- 0.1 V
1.4 V (RDRAM Vref)	1.4 V +/- 0.2 V
1.25 V (DDR Vref)	Minimum = (Vdd/2) – 0.05 V Maximum = (Vdd/2) + 0.05 V
1.25 V (DDR Vterm)	DDR Vref +/- 0.04 V

3.4.5.1 Power Consumption

The amount of power consumed by the memory module is highly dependent on the amount and type of memory installed.

Table 3-10 specifies power consumption for each supplied voltage. The assumption is that there are eight DIMMS with 36, 512-Mb DRAM devices each.

Table 3-10. Voltage Power Consumption

DC Voltage	Power
2.5 V	74.6 W
1.8 V	4.40 W
1.4 V	(Negligible)
1.25 V	7.78 W

The calculations for obtaining these numbers are shown in the following tables.

Table 3-11. Calculations for Voltage Power Requirements – 2.5 V

	# Devices	Watt/Dev	Total
Active DDR Devices	36	0.90	32.40 W
Standby DDR Devices	252	0.09	22.68 W
1.25 V Conversion (85% efficient)	1	9.15	9.15 W
DMH	2	5.20	10.40 W
Total 2.5-V Power			74.63 W
Total 2.5-V Current			29.85 A

Table 3-12. Calculations for Voltage Power Requirements – 1.8 V

	# Devices	Watt/Dev	Total
DMH Core	2	1.00	2.00 W

	# Devices	Watt/Dev	Total
RSL Channel Termination	2 channels	1.20 / channel	2.40 W
Total 1.8-V Power			4.40 W
Total 1.8-V current			2.44 A

Table 3-13. Calculations for Voltage Power Requirements – 1.25 V

	# Devices	Watt/Dev	Total
DDR Channel Termination	2 channels	3.89/channel	7.78 W
Total 1.25-V Power			7.78 W
Total 1.25-V Current			**6.22 A**

3.4.6 Mechanical

Figure 3-6 presents a placement diagram of the memory module, showing its mechanical specifications and connectors.

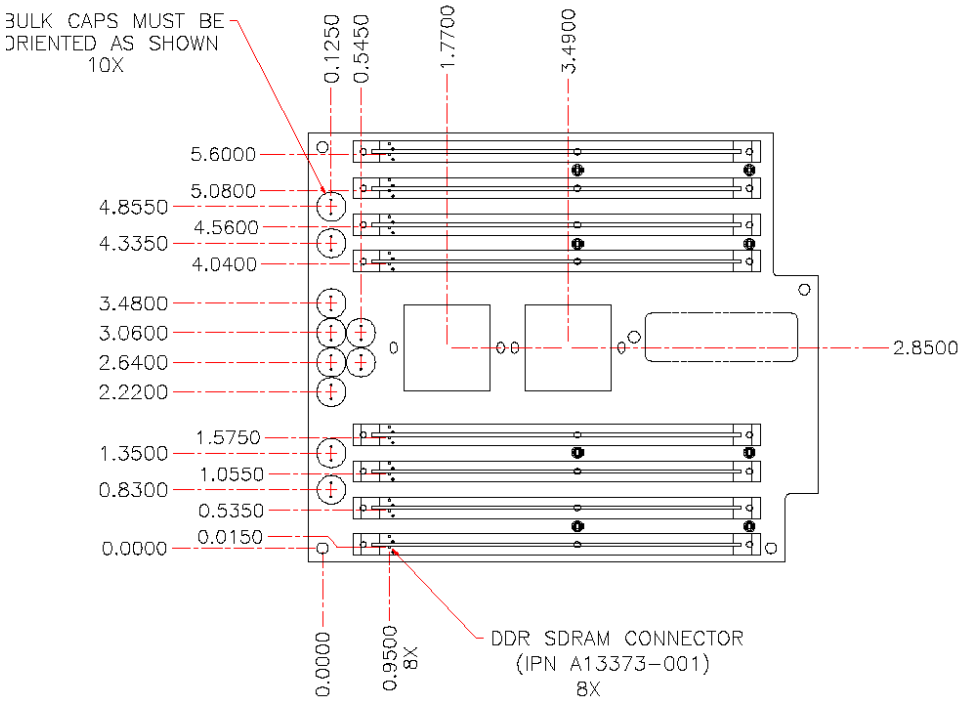


Figure 3-6. Memory Board Mechanical Diagram

3.4.7 Connectors

The following table lists the specifications for the memory module connectors. Refer to the manufacturer's documentation for more information.

Table 3-14. Memory Module Connector Specifications

Item	Quantity	Manufacturer and Part Number	Description
1	1	FCI-Berg* 84739-001 Rev 6	Memory to processor board connector
3	8	Foxconn* AT09217-P1 Molex* 87657-0012 FCI-Berg* 100008315-20302 Tyco* 390432-1	DIMM sockets

4. 4-Way I/O Board

This chapter describes the architecture and design of the Server Board S870BN4 I/O board used in the 4-way Server System SR870BN4. The I/O board mates with the S870BN4 processor board and other boards of the S870BN4 board set through the S870BN4 midplane board. The Server System SR870BN4 I/O riser mates directly onto the I/O board and together they contain all of the I/O interfaces for the S870BN4 board set.

4.1 Features

The I/O board has the following features:

- Intel® E8870 chip set based on Scalability Port system interface
- Six functionally independent Peripheral Component Interconnect (PCI) bus segments
  - Three hot-plug 133-MHz, 64-bit PCI-x slots
  - Five hot-plug 100-MHz, 64-bit PCI-x slots
- Integrated dual channel LSI* 53C1030 Ultra-320 Low Voltage Differential SCSI (LVDS) controller
- I/O riser support connector for I/O interface
- On-board power conversion from 48-V bulk power
- System reset and clock generation circuits
- I^2C server management interface
- Redundant hot-plug system fan interface

4.2 Architectural Overview

This section provides an overview of the I/O board, showing functional blocks and the component placement diagrams of the I/O board.

The Server Board S870BN4 4-way I/O board provides the basis for a scaleable, high-performance I/O subsystem. Six 64-bit PCI-x bus segments are supported (all are peer busses) via three P64H2 PCI-x expander bridge components. The P64H2 expander bridge components provide up to 133-MHz PCI-x and PCI 2.2 support. There are a total of eight PCI-x, 3.3-V, 64-bit hot-plug capable slots. Three slots are full length, 133 MHz, each on an independent segment. Four slots are 100 MHz on two independent segments, of which three are PCI short form factor (174,63mm) and one is PCI long form factor (312mm). One slot is short form factor, 100 MHz, and contains an on-board SCSI controller on an independent segment.

BIOS flash storage, server management, video and system I/O are contained on a separate I/O riser board that plugs into the I/O board. The I/O riser card interfaces to the Server I/O Hub (SIOH) component using a Hublink 1.5 bus. An Integrated Drive Electronics (IDE) bus controlled from the I/O riser is routed through the I/O riser connector and to the midplane disk bay connector located on the edge of the I/O board. System devices, such as CD-ROM/DVD and LS240 floppy, use the IDE bus. In addition, the I/O riser provides 5-V STDBY and 3.3-V STDBY voltages to the I/O board.

The I/O board contains both plug-in D2D modules and embedded D2D converters necessary to provide power to the on-board circuits, PCI adapters, and to provide required voltages to other

system components. The I/O board receives other voltages from the I/O riser, SCSI backplane and the system power supplies. The bulk supply for the D2D modules comes from a system-wide 48-V bulk power distribution.

The I/O board interfaces to the system management controller located on the I/O riser. System management features include voltage sensing, temperature sensing, board identification, error logging, fan status, fan speed control, and SCSI bus mode status.

The I/O board provides the main system clock generation. 200-MHz differential clocks are provided for I/O board components and for the processor board components. Additional clocks are provided for the I/O board's circuitry and to the I/O riser's circuitry.

The I/O board contains the system reset and power sequence control.

The following figure illustrates the general architecture of the I/O board.

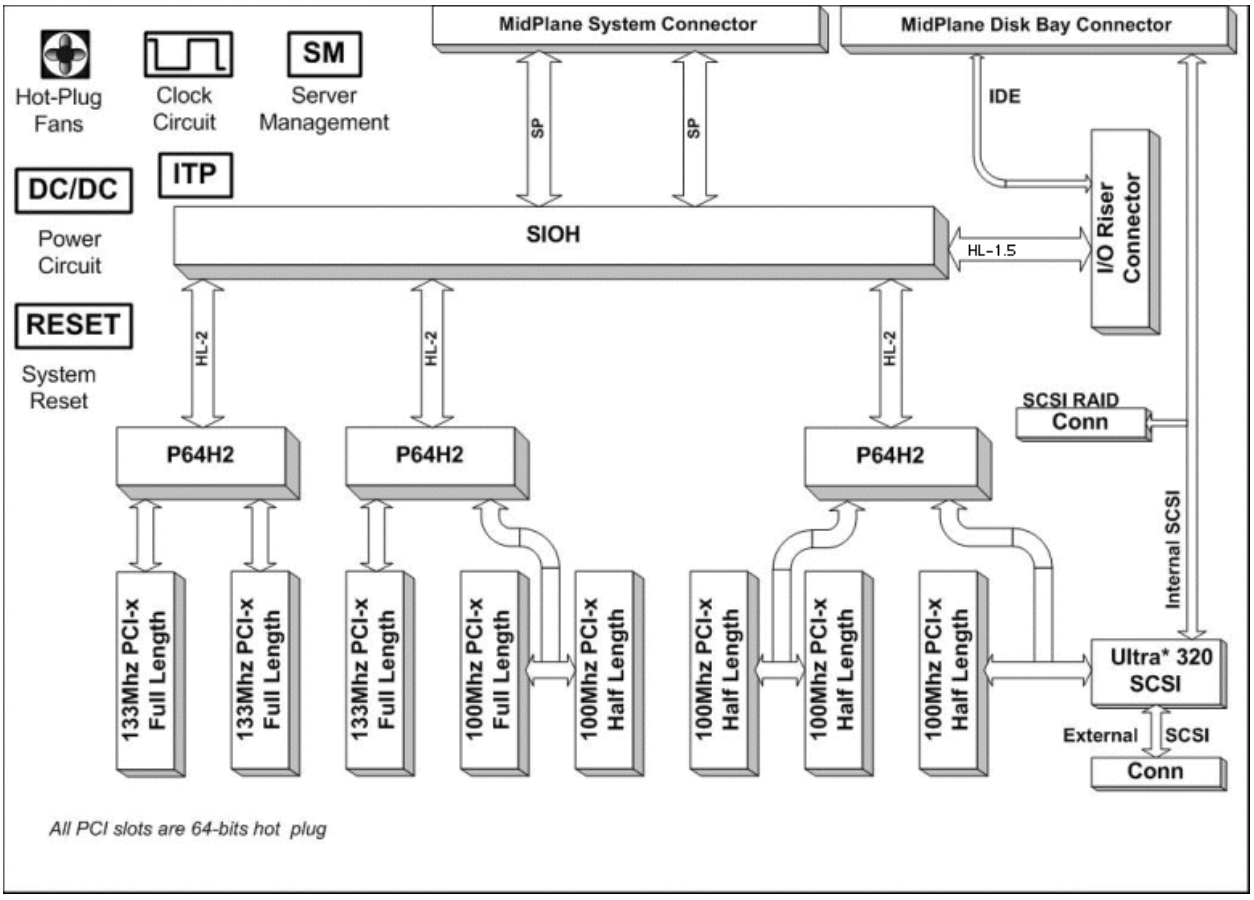


Figure 4-1. I/O Board Block Diagram

4.3 Buses and Interfaces

4.3.1 Midplane System Interface

The I/O interface from the processor board is provided by the Intel® 870 chip set Scalability Port (SP) bus. The bus routes from the midplane connector to the SIOH component. The SIOH then produces four independent HL2 busses, three of which interface to the three PCI bridge components (P64H2) and 1 HL1.5 bus to the ICH4 on the IO Riser. Each P64H2 component then produces two independent 133-MHz, 64-bit PCI-x capable bus segments. Actual bus speed and protocol are determined by adapter type and number of busloads.

The SP bus is a simultaneous, bi-directional bus that provides a peak bandwidth of 3.2 GB/s. Each HL2 bus is a source-synchronous bus capable of providing a peak bandwidth of 1 GB/s. Details of the various busses are contained in their respective specifications.

In addition, the midplane interface contains other signals that connect to the processor/memory module, front panel, and power supply backplane boards. These signals include clocks, reset, server management, power control, front panel, and debug.

The midplane system interface also provides the main power for the I/O board and I/O riser, as well as the connection for power to other system components.

4.3.2 Midplane Disk Bay Interface

The I/O board contains a midplane connector that connects to a disk bay interface backplane (SCSI backplane). This interface includes an Ultra-320 SCSI bus and a UDMA 33 IDE bus. Certain miscellaneous control signals are provided as well.

4.3.2.1 SCSI

The I/O board contains two Ultra 320-compliant SCSI channels. One channel is used internally while the other is targeted for external system use. The internal channel supports LVD signaling only, while the external channel supports both LVD and single-ended (SE) signaling. With LVD signaling, the channels can each support a maximum data rate of 320 MB/sec.

The internal channel routes to the midplane's disk bay connector where it can be connected to internal SCSI devices. There is an optional connector on the bus that allows an external controller to drive the internal bus.

The external connector cables route from the I/O board to the bulkhead mounted connector.

4.3.2.2 Integrated Device Electronics Interface

The I/O board passes the IDE bus, generated on the I/O riser, to the midplane's disk bay connector for use by internal devices. It performs no logic or buffering for this bus.

4.3.3 Peripheral Component Interconnect (PCI) Busses

The I/O board contains six separate peer PCI bus segments from three P64H2 PCI bridge controllers. Bus speeds and types can be a maximum of 100-MHz PCI-x or 133-MHz PCI-x, depending on number of slots and devices per segment.

All buses adhere to the following specifications as applicable:

- *PCI Specification*, *Revision 2.2*
- *PCI-PCI Bridge Specification*, *Revision 1.1*
- *PCI Hot-Plug Specification*, *Revision 1.0*
- *PCI-X Specification*, *Revision 1.0*

4.3.4 I/O Riser Board Interface

To conserve space on the I/O board, most system I/O functions, as well as server management functions, have been placed on a riser card attached to the I/O board. These functions include video controller, serial port, Local Area Network (LAN) port, Universal Serial Bus (USB) ports, BIOS flash hubs, and other legacy interfaces as necessary.

The server management controller and related functions are present on the I/O riser card. Both Intelligent Chassis Management Bus (ICMB) and Intelligent Platform Management Bus (IPMB) functions are supported, as well as private server management buses.

The I/O riser contains an IDE bus controller. The IDE bus is routed to the I/O board where it is further routed to the midplane's disk bay connector.

The I/O riser also contains an In-System Programming (ISP) bus that can be used to update certain Programmable Logic Devices (PLD) in the system, including those on the I/O board.

The I/O riser contains the system's JTAG controller. This controller is connected to the midplane system interface and typically interfaces to devices on the processor board. It does not connect to devices on the I/O board. The I/O riser contains IOXAPIC and 8259-compatible interrupt circuits. Certain interrupt signals from the I/O board are sent to these circuits.

The I/O riser card converts 12V STDBY to +5V STDBY (standby) and +3.3V STDBY, and supplies this to the I/O board.

4.3.5 Hot-Plug Fan Interface

The main system fan power and control is provided on the I/O board. Hot-pluggable fan modules interconnect to the I/O board through individual blind-mate connectors. Server management-controlled hardware monitors fan status and system temperatures and can detect and report a fan failure or system over-temperature. The interface can then adjust fan speed, if necessary, to improve the cooling capabilities of the system. The interface contains LED signals that can provide an intuitive user indicator of a failed fan. The LEDs are located in a suitable viewing location on the fan Customer Replaceable Unit (CRU).

4.3.6 PCI Power Management Interface

The PCI Power Management Interface structure provides a standard interface to control power management features, and is compliant with *PCI Bus Power Management Interface Specification, Revision 1.1*. This interface allows PCI adapters to initiate specific power management events such as system wake-up.

4.3.7 PCI Hot-Plug Control Interface

All of the I/O board's PCI slots are hot pluggable (please note that the IO Riser is not hot pluggable). The hot-plug controllers for the slots are contained in the P64H2 components. External logic controlled by the P64H2's hot-plug circuitry switch power, clocks, and bus signals to each slot. A Hot Plug Indicator Board (HPIB) control panel connector is provided to the switch and LED signals for the HPIB, which is mounted on the rear of the system. This board contains the user switches and LED indicators used during a hot-plug event.

The P64H2's hot-plug controller can operate in serial or parallel mode. Since no PCI bus contains more than two slots, all the hot-plug controllers on the I/O board operate in parallel mode. Individual power enable, bus enable, clock enable and reset signals from the P64H2 control each slot.

All 100-MHz slots have two slots/devices per bus. Switch-able Field Effect Transistors (FETs) are used between the PCI bus and the slot to disconnect the PCI bus signals during a hot-plug event.

The 133-MHz slots all have only one slot per bus. The P64H2 is capable of putting the PCI bus in a quiescent state during a hot-plug event so that FET switches are not required. The PCI clock for this segment is also controlled by the P64H2 and does not require an external FET.

Both 100 and 133mhz slots require external power circuitry.

4.3.8 D2D Power Interface

The I/O board contains T-D2D/A-D2D SSI-compliant power converter connectors to generate 5 V and 3.3 V power. The plug-in converters operate from 48-V input power.

4.3.9 Hardware Status Interface

The I/O board contains six LEDs that indicate basic hardware status. Light pipes will allow these LEDs to be viewed from outside the top cover of the unit. LEDs will report the status of board interlock signals, main power supply POWER_OK, and system reset.

In addition, there are four LEDs that indicate a failed D2D converter.

4.3.10 In-Target Probe (ITP) Interface

The I/O board contains an In-Target Probe (ITP) connector that allows an ITP analyzer to monitor and control certain devices on the board. The SIOH can be monitored and controlled by the ITP.

4.4 Placement Diagrams

Figure 4-2 shows the position of the primary components of the I/O board.

Table 4-1 identifies the major components and their respective reference designators.

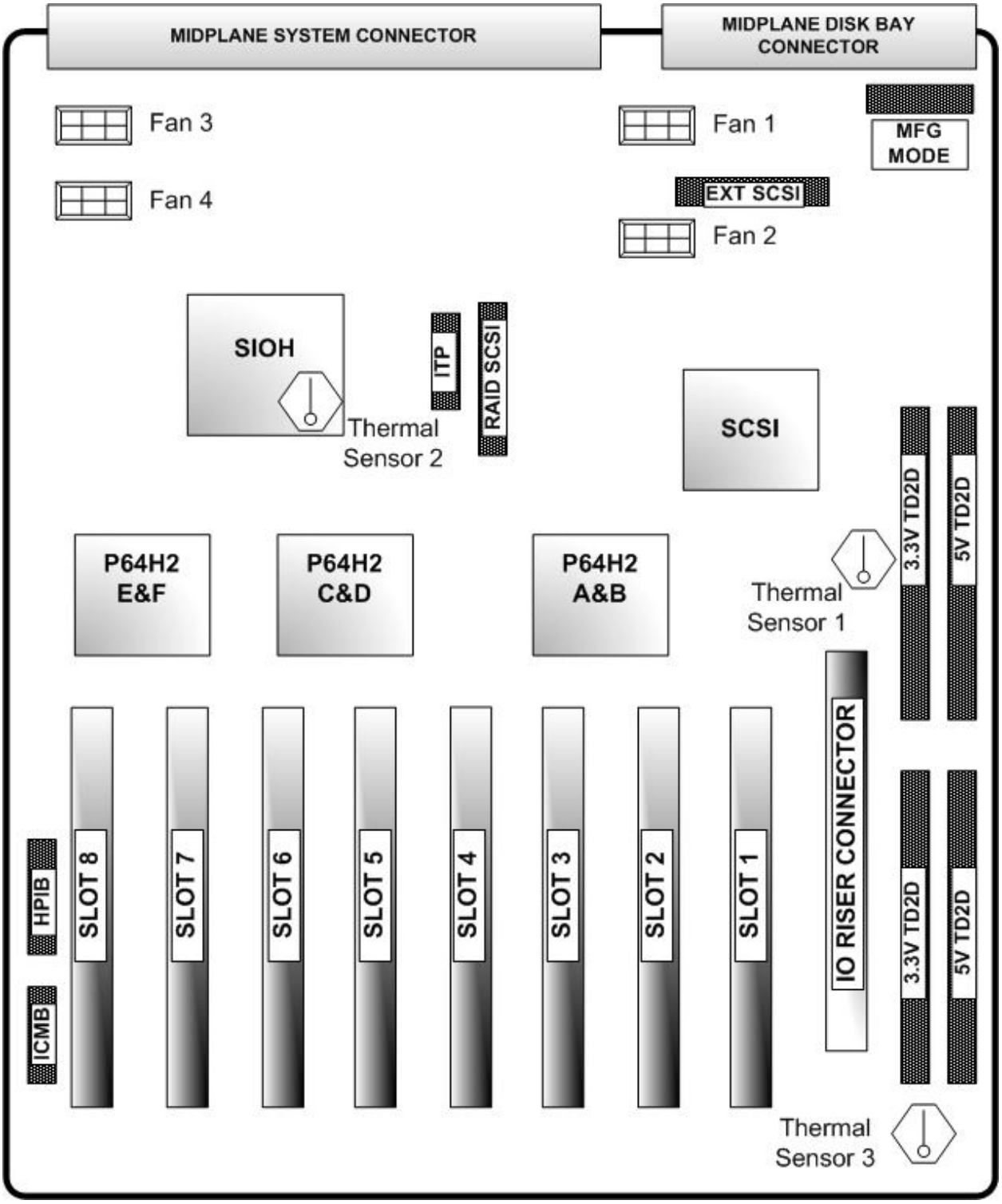


Figure 4-2. I/O Board Placement Plot

Table 4-1. I/O Board Component Reference

Reference Designator	Name and Description	Reference Designator	Name and Description
J5J1	Midplane interface connector	J1J2	Midplane disk bay connector
J4J1	Fan 1 connector	J4G1	Fan 2 Connector
J8J1	Fan 3 connector	J8H1	Fan 4 Connector
J6G1	ITP connector	J4H1	External SCSI connector
J2C1	3.3V_A D2D connector	J2F3	3.3V_B D2D connector
J1C1	5V_A D2D connector	J1F1	5V_B D2D connector
J3A1	PCI Slot 1 connector	J4A1	PCI Slot 2 connector
J5A1	PCI Slot 3 connector	J5A2	PCI Slot 4 connector
J6A1	PCI Slot 5 connector	J7A1	PCI Slot 6 connector
J8A1	PCI Slot 7 connector	J9A1	PCI Slot 8 connector
J2B1	I/O riser connector	J9D1	HPIB connector
J9C1	ICMB connector	J1J1	Manufacturing Mode site
U8F1	SIOH	U5E3	P64H2 AB
U7E1	P64H2 CD	U9E1	P64H2 EF
U3F1	SCSI Controller		

4.5 Functional and Logical Blocks

This section includes a detailed description of the functional and logical blocks on the I/O board. Included are the connector pinouts and signal descriptions on all user-accessible I/O board connector interfaces. The signal mnemonics defined here may appear in descriptive text throughout this document. An "_L" following a signal name indicates that the signal is active-low (note that this is the same convention used on schematics for active-low signals). One colon, between numbers in square brackets or parentheses, indicates a range of signals (e.g., the notation [13:0] is a range of 14 unique signals).

4.5.1 Midplane Interface

The principal interface to the I/O board is the midplane interface. This interface contains two separate connectors: the system connector and the disk bay connector. The I/O board connects to the system midplane board through these connectors. This interface provides connectivity to the processor/memory module, front panel, SCSI backplane, and system power.

The system connector contains two SP buses, which connects the Scalable Node Controller (SNC) component on the processor/memory module to the SIOH component on the I/O board. In addition, this interface contains processor sideband signals including clocks, error, interrupt, processor power sequence control, server management, JTAG, and ISP. Also, front panel and system power supply control signals are included. The interface also contains the main I/O board 48-V, 12 V, and 12VSTDBY power rails and power returns.

The disk bay connector contains a SCSI bus and IDE bus. There are also LCD display signals that can be used to interface with a front panel LCD display module mounted on the SCSI backplane. Some miscellaneous signals are present to interface to the SCSI backplane as well. The LCD portion of the system is an un-validated feature.

4.5.1.1 Midplane Connectors

The I/O board connects to the system midplane through both the system connector and the disk bay connector.

The IO Board midplane connector uses a 6-row Molex*/Teradyne* VHDM connector. This provides the necessary signal density and high-speed signal integrity requirements for the interface signals. In addition, the IO Board midplane connector provides the power interface for the I/O board. Table 4-2 lists the IO board's midplane connector signals. Table 4-3 lists the power pinouts.

Table 4-2. Midplane System Connector Signal List

	F	E	D	C	B	A
1	CPU_INTERLOCK_L	rsvd	rsvd	+3.3V_STDBY	+3.3V_STDBY	IO_INTERLOCK_L
2	GROUND	rsvd	GROUND	RSVD	GROUND	RSVD
3	rsvd	GROUND	rsvd	GROUND	RSVD	GROUND
4	rsvd	rsvd	EVBPIN_L	EVBPOUT_L	SERIAL_LOAD	SERIAL_CLK
5	BD_ID1	BD_ID0	P64H2_ERR_L2	P64H2_ERR_L1	P64H2_ERR_L0	SERIAL_DATA
6	BD_ID4	BD_ID3	BD_ID2	BD_TYPE2	BD_TYPE1	BD_TYPE0
7	IVXB_ERR_L	rsvd	BD_ID6	BD_ID5	ISP_SDO_LCD7	LCD_RW
8	rsvd	CHASS_ID_L	LCD6	ISP_EN_L	ISP_SDI_CPU	LCD_RS
9	I2C_IO_SDA	I2C_IO_SCL	LCD4	ISP_SCLK_CPU	ISP_MODE_LCD5	LCD_E
10	I2C_CPU_SCL	I2C_CPU_SDA	MIDP_ID2	ON_LED_L	RSVD	RSVD
11	PPODOE	SP1GPIO0	GEN_FLT_LED_L	COOL_FLT_LED_L	PROCHOT_L	PLD_STPCLK_L
12	SP0GPIO0	EV_L0	EV_L1	POWER_FLT_LED_L	EV_L2	EV_L3
13	THERMALERT_L	HP_INT_L	rsvd	SPEAKER	FP_ID_LED_L	RSVD
14	ERR_L0	ERR_L1	ERR_L2	POWER_SW_L	BERROUT_L	INT_OUT_L
15	rsvd	rsvd	BINITIN_L	RESET_SW_L	RSVD	BERRIN_L
16	AIPPODPG	CD2D33EN	BINITOUT_L	SDINT_SW_L	IS_TRST_L	IS_TMS
17	PMI_L	FERR_L	rsvd	IS_TCK	IS_TDI	IS_TDO
18	A20M_L	IGNNE_L	INIT_L	RSVD	INTR	NMI
19	PWRGOOD	NODE_PG	rsvd	SNC_RESETI_L	RSVD	RESETO_L
20	GROUND	GROUND	MIDP_ID0	MIDP_ID1	GROUND	GROUND
21	rsvd	rsvd	GROUND	GROUND	CLK200_BCLK	CLK200_BCLK_L
22	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
23	GROUND	SP0AD6	SP0AD5	GROUND	SP0AD13	SP0AD14
24	SP0AD4	GROUND	SP0AD7	SP0AD12	GROUND	SP0AD15
25	SP0AVREFH1	SP0AVREFL1	GROUND	SP0AVREFH3	SP0AVREFL3	GROUND

	F	E	D	C	B	A
26	GROUND	SP0AD3	SP0AEP0	GROUND	SP0AD11	SP0ASSO
27	SP0ASTBN0	GROUND	SP0AD2	SP0ARSVD	GROUND	SP0AD10
28	SP0AEP1	SP0ASTBP0	GROUND	SP0ASTBP1	SP0ASTBN1	GROUND
29	GROUND	SP0AEP2	SP0AD1	GROUND	SP0ALLC	SP0AD9
30	SP0AVREFL0	SP0AVREFH0	GROUND	SP0AVREFL2	SP0AVREFH2	GROUND
31	SP0AD0	GROUND	CPU_3.3VSTDBY_GD	SP0AD8	GROUND	V48EN
32	GROUND	SP0BD0	GROUND	STDBYEN	SP0BD8	GROUND
33	SP0BD1	SP0BVREFH0	SP0BVREFL0	GROUND	SP0BVREFH2	SP0BVREFL2
34	SP0BSTBN0	GROUND	SP0BEP2	SP0BD9	GROUND	SP0BLLC
35	GROUND	SP0BSTBP0	GROUND	SP0BSTBN1	SP0BSTBP1	GROUND
36	SP0BEP0	SP0BD2	SP0BEP1	GROUND	SP0BD10	SP0BRSVD
37	SP0BVREFL1	GROUND	SP0BD3	SP0BSSO	GROUND	SP0BD11
38	GROUND	SP0BVREFH1	GROUND	SP0BVREFL3	SP0BVREFH3	GROUND
39	SP0BD5	SP0BD7	SP0BD4	GROUND	SP0BD15	SP0BD12
40	GROUND	GROUND	SP0BD6	SP0BD14	GROUND	SP0BD13
41	SP1AD4	SP1AD6	SP1AD5	GROUND	SP1AD13	SP1AD14
42	SP1AVREFH1	GROUND	SP1AD7	SP1AD12	GROUND	SP1AD15
43	GROUND	SP1AVREFL1	GROUND	SP1AVREFH3	SP1AVREFL3	GROUND
44	SP1AEP1	SP1AD3	SP1AEP0	GROUND	SP1AD11	SP1ASSO
45	SP1ASTBP0	GROUND	SP1AD2	SP1ARSVD	GROUND	SP1AD10
46	GROUND	SP1ASTBN0	GROUND	SP1ASTBP1	SP1ASTBN1	GROUND
47	SP1AVREFL0	SP1AEP2	SP1AD1	GROUND	SP1ALLC	SP1AD9
48	SP1AD0	SP1AVREFH0	GROUND	SP1AVREFL2	SP1AVREFH2	GROUND
49	SNCFWHWP_L	GROUND	SNCFWHDIS_L	SP1AD8	GROUND	IA64_IA32
50	GROUND	SP1BD0	GROUND	IS0_JTAGEN_L	SP1BD8	GROUND
51	SP1BD1	SP1BVREFH0	SP1BVREFL0	GROUND	SP1BVREFH2	SP1BVREFL2
52	SP1BSTBP0	GROUND	SP1BEP1	SP1BD9	GROUND	SP1BLLC
53	GROUND	SP1BEP2	GROUND	SP1BSTBN1	SP1BSTBP1	GROUND
54	SP1BEP0	SP1BD2	SP1BSTBN0	GROUND	SP1BD10	SP1BRSVD
55	SP1BVREFL1	GROUND	SP1BD3	SP1BSSO	GROUND	SP1BD11
56	GROUND	SP1BVREFH1	GROUND	SP1BVREFL3	SP1BVREFH3	GROUND
57	SP1BD5	SP1BD7	SP1BD4	GROUND	SP1BD15	SP1BD12
58	SP0SYNC	GROUND	SP1BD6	SP1BD14	GROUND	SP1BD13
59	GROUND	GROUND	SP1SYNC	GROUND	SP0PRES	SP1PRES
60	CPU_INTERLOCK_L	INTRUDER_L	GROUND	PS_ON_L	PS_OK_ORED	GROUND

Table 4-3. Midplane VHDM Power Connector Pinout

	PW11	48V	48V RTN	PW15	
	PW12	48V	48V RTN	PW16	

	PW13	48V	48V RTN	PW17	
	PW14	48V	48V RTN	PW18	
	PW21	48V	48V RTN	PW25	
	PW22	48V	48V RTN	PW26	
	PW23	48V	48V RTN	PW27	
	PW24	48V	48V RTN	PW28	
	PW31	12V	12VSTBY	PW35	
	PW32	12V	12VSTBY	PW36	
	PW33	12V	12VSTBY	PW37	
	PW34	12V	12VSTBY	PW38	

The IO Board's disk bay connector uses a 6-row Molex/Teradyne High-Density Metric (HDM) connector. This provides the necessary signal density and high-speed signal integrity requirements for the IDE and SCSI signals. This connector system allows for the midplane to incorporate a true dual-sided midplane connector so that the disk bay tray can dock into the opposite side of the connector from the I/O. This arrangement allows for direct connection of the signals from the I/O to the disk bay without any routing required on the midplane.

Table 4-4 lists the disk bay connector signals and pinout. Only one SCSI channel goes to the disk bay.

Table 4-4. Midplane Disk Bay Connector Signal List and Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	B_DB_8P	B_DB_11P	B_DB_10P	B_DB_9P	ISP_MODE_LCD5	SCSI_INTERLOCK_L
2	B_DB_8N	B_DB_11N	B_DB_10N	B_DB_9N	PWRGOOD	ISP_SDI_SCSI
3	B_CD_P	B_REQ_P	B_IO_P	SCSI_B_DIFFSENSE	+5V_STDBY	SCSI_PWRGD
4	B_CD_N	B_REQ_N	B_IO_N	GROUND	I2C_IPMB_SDA	SENSE_12VP
5	B_MSG_P	B_SEL_P	GROUND	GROUND	I2C_IPMB_SCL	SCSI_5V_SAMPLE
6	B_MSG_N	B_SEL_N	ISP_SDI_CPU	PCI_IDE_RST_PLD_L	GROUND	GROUND
7	B_ACK_P	B_RST_P	GROUND	PDD7	GROUND	GROUND
8	B_ACK_N	B_RST_N	PDD8	PDD6	GROUND	GROUND
9	B_ATN_P	B_BSY_P	PDD9	PDD5	GROUND	GROUND
10	B_ATN_N	B_BSY_N	PDD10	PDD4	GROUND	GROUND
11	B_DB_7P	B_DB_P0P	PDD11	PDD3	GROUND	GROUND
12	B_DB_7N	B_DB_P0N	PDD12	PDD2	GROUND	GROUND
13	B_DB_5P	B_DB_6P	PDD13	PDD1	GROUND	GROUND
14	B_DB_5N	B_DB_6N	PDD14	PDD0	GROUND	GROUND

Pin	Row A	Row B	Row C	Row D	Row E	Row F
15	B_DB_3P	B_DB_4P	PDD15	GROUND	GROUND	GROUND
16	B_DB_3N	B_DB_4N	GROUND	PDDREQ	GROUND	GROUND
17	B_DB_1P	B_DB_2P	GROUND	PDIOW_L	GROUND	LCD_E
18	B_DB_1N	B_DB_2N	GROUND	PDIOR_L	GROUND	LCD_RS
19	ABDB_P1P	B_DB_0P	ISP_SDO_LCD7	PIORDY	GROUND	+3.3V_B
20	B_DB_P1N	B_DB_0N	GROUND	PDDACK_L	GROUND	+3.3V_B
21	B_DB_14P	B_DB_15P	IRQ14	PDA1	+3.3V_B	+3.3V_B
22	B_DB_14N	B_DB_15N	PDA2	PDA0	+3.3V_STDBY	+3.3V_STDBY
23	B_DB_12P	B_DB_13P	PDCS3_L	PDCS1_L	3.3V_D2D4_PWRGD	LCD_RW
24	B_DB_12N	B_DB_13N	GROUND	LCD6	ISP_EN_L	ISP_SCLK_SCSI

Table 4-5. Midplane Connector Current Rating

Voltage	Source/Load	# Pins	Current Carrying Capability*
+48V	Power Supply	2 **	20A
+12VSTDBY	Power Supply	1 **	10A
+12V	SCSI Backplane	1 **	10A
+5VSTDBY	SCSI Backplane	1	.5A
+3.3VSTDBY	CPU/Front Panel	2	1A

Note: *Represents the current rating of the connector at 1 amp per pin, derated 50%. The actual amount of power available from the sources will be different.
** These are power blades rated at 10A each, including derating factors.

4.5.2 Server I/O Hub (SIOH)

The SIOH component is a member of the 870 chip set and provides the electrical and logical interface between the two SP buses from the midplane (processor/memory module) and four HL2 buses. The SIOH also provides an 8-bit Hublink 1 (HL1) bus to interface to the I/O riser card. This interface supports Hublink 1.5.

Three of the HL2 buses interface the SIOH to three P64H2 PCI bridge components. The fourth HL2 bus is unused.

In addition to the HL2 busses, an 8-bit HL1.5 bus is provided by the SIOH to interface to the ICH4 I/O component contained on the I/O riser card. It is through this interface that the system communicates to the video, serial, LAN, and USB ports.

The SIOH BUSID is set for hx7 and the NODEID is set for hx1C.

See the 870 chip set specifications for more information on specific SIOH operation and chip pinout and for details on the SP, HL1 and HL2 buses.

4.5.2.1 SIOH Power and Thermal Requirements

The SIOH requires 3.3 V, 1.8 V, 1.5 V and 1.3 V for its operation. 3.3 V is used to terminate certain 3.3 V-level signals. 1.8 V is used by the HL1.5 port termination. 1.5 V is used by the component's core and the HL2 port termination. 1.3 V is used by the SP port termination. The SIOH requires a heatsink for proper thermal operation. See Section 4.5.22 for details on the thermal requirements.

4.5.3 P64H2

The P64H2 component is the PCI bridge controller component. It connects to the system through the HL2 buses coming from the SIOH component. There are three P64H2 components in the system. Each component has two independent PCI bus interfaces capable of supporting up to 133-MHz PCI-x bus operation.

See the P64H2 specifications for more details on the chip's functionality and pinout.

4.5.3.1 Power and Thermal Requirements

The P64H2 requires 1.8 V and 3.3 V for its operation. 1.8 V is used by the component's core and HL2 port termination. 3.3 V is used by the PCI ports termination. The P64H2 does not require a heatsink for proper thermal operation. See Sections 4.5.22 for details on the thermal requirements.

4.5.4 PCI Buses

There are six independent PCI buses, two each from the three P64H2 PCI bridge chips. The type and number of slots and the location in the system chassis determine the speed, type, voltage and card length. Table 4-6 summarizes the characteristics for the eight slots.

Table 4-6. Summary of PCI Slot Characteristics

Slot	Connector	PCI Bus	Key	Speed/Type	Form Factor
SLOT 1[1]	J3A1	Bus A	3.3 V	100 MHz PCI-x	Short
SLOT 2	J4A1	Bus B	3.3 V	100 MHz PCI-x	Short
SLOT 3	J5A1	Bus B	3.3 V	100 MHz PCI-x	Short
SLOT 4	J5A2	Bus C	3.3 V	100 MHz PCI-x	Short
SLOT 5	J6A1	Bus C	3.3 V	100 MHz PCI-x	Long
SLOT 6	J7A1	Bus D	3.3 V	133 MHz PCI-x	Long
SLOT 7	J8A1	Bus E	3.3 V	133 MHz PCI-x	Long
SLOT 8	J9A1	Bus F	3.3 V	133 MHz PCI-x	Long

Notes: [1] Bus A contains the embedded SCSI controller

4.5.4.1 PCI Bus Segment A

PCI Bus Segment A contains one 100-MHz, 64-bit PCI-x slot and an on-board Ultra-320 SCSI interface component. The slot number is SLOT 1 and is keyed for 3.3 V operation. The slot can accept short form factor PCI adapters only (chassis limitation).

The bus is routed from the P64H2 controller to the SCSI component, to the FET switches, and finally to SLOT 1. These FET switches are required to isolate the slot from the SCSI component during a hot-plug event. Pull-up resistors are provided on the PCI signals in accordance with the PCI specification, and series resistors are provided in the PCI bus to improve signal integrity.

See Section 4.5.7 for details on the on-board SCSI interface.

See Table 4-15 for 3.3-V PCI slot pinout.

See Table 4-38 for interrupt mapping.

The IDSEL# routing for PCI Bus Segment A is identified in Table 4-7.

Table 4-7. IDSEL# Mapping for PCI Bus Segment A

AD Signal	Component/ PCI Slot Number
AD17	SLOT 1
AD18	SCSI component

4.5.4.2 PCI Bus Segment B

PCI Bus Segment B contains two 100-MHz, 64 bit PCI-x slots. The slots are numbered SLOT 2 and SLOT 3 and are keyed for 3.3 V operation. Both slots can accept short form factor PCI adapters only (chassis limitation). The bus is routed from the P64H2 controller to two sets of FET switches. Each set of FET switches connects to a slot. These FET switches are required to isolate the slots from each other during a hot-plug event. Pull-up resistors are provided on the PCI signals in accordance with the PCI specification.

See Table 4-15 for 3.3-V PCI slot pinout.

See Table 4-38 for interrupt mapping.

The IDSEL# routing for PCI Bus Segment B is identified in Table 4-8.

Table 4-8. IDSEL# Mapping for PCI Bus Segment B

AD Signal	Component/ PCI Slot Number
AD17	SLOT 2
AD18	SLOT 3

4.5.4.3 PCI Bus Segment C

PCI Bus Segment C contains two 100-MHz, 64 bit PCI-x slots. The slots are numbered SLOT4 and SLOT 5 and are keyed for 3.3 V operation. SLOT 4 can accept short form factor PCI adapters only (chassis limitation). SLOT 5 can accept short or long form factor PCI adapters.

The bus is routed from the P64H2 controller to two sets of FET switches. Each set of FET switches connects to a slot. These FET switches are required to isolate the slots from each other during a hot-plug event. Pull-up resistors are provided on the PCI signals in accordance with the PCI specification.

See Table 4-15 for 3.3-V PCI slot pinout.

See Table 4-38 for interrupt mapping.

The IDSEL# routing for PCI Bus Segment C is identified in Table 4-9.

Table 4-9. IDSEL# Mapping for PCI Bus Segment C

AD Signal	Component/ PCI Slot Number
AD17	SLOT 4
AD18	SLOT 5

4.5.4.4 PCI Bus Segment D

PCI Bus Segment D contains one 133-MHz, 64-bit PCI-x slot. This slot is numbered SLOT 6 and is keyed for 3.3 V operation. SLOT 6 can accept short or long form factor PCI adapters.

The bus is routed from the P64H2 controller to the slot. The P64H2 provides the necessary isolation during a hot-plug event. Pull-up resistors are provided on the PCI signals in accordance with the PCI specification.

See Table 4-15 for 3.3-V PCI slot pinout.

See Table 4-38 for interrupt mapping.

The IDSEL# routing for PCI Bus Segment D is identified in Table 4-10.

Table 4-10. IDSEL# Mapping for PCI Bus Segment D

AD Signal	Component/ PCI Slot Number
AD17	SLOT 6

4.5.4.5 PCI Bus Segment E

PCI Bus Segment E contains one 133-MHz, 64-bit PCI-x slot. This slot is numbered SLOT 7 and is keyed for 3.3 V operation. SLOT 7 can accept short or long form factor PCI adapters.

The bus is routed from the P64H2 controller to the slot. The P64H2 provides the necessary isolation during a hot-plug event. Pull-up resistors are provided on the PCI signals in accordance with the PCI specification.

See Table 4-15 for 3.3-V PCI slot pinout.

See Table 4-38 for interrupt mapping.

The IDSEL# routing for PCI Bus Segment E is identified in Table 4-11.

Table 4-11. IDSEL# Mapping for PCI Bus Segment E

AD Signal	Component/ PCI Slot Number
AD17	SLOT 7

4.5.4.6 PCI Bus Segment F

PCI Bus Segment F contains one 133-MHz, 64-bit PCI-x slot. This slot is numbered SLOT 8 and is keyed for 3.3 V operation. SLOT 8 can accept short or long form factor PCI adapters.

The bus is routed from the P64H2 controller to the slot. The P64H2 provides the necessary isolation during a hot-plug event. Pull-up resistors are provided on the PCI signals in accordance with the PCI specification.

See Table 4-15 for 3.3-V PCI slot pinout.

See Table 4-38 for interrupt mapping.

The IDSEL# routing for PCI Bus Segment F is identified in Table 4-12.

Table 4-12. IDSEL# Mapping for PCI Bus Segment F

AD Signal	Component/ PCI Slot Number
AD17	SLOT 8

4.5.4.7 PCI Signal Descriptions

The following tables are a summary of PCI signal pins, including the signal mnemonic, electrical type, full name, and brief description. The PCI implementation on the I/O board supports 33 MHz pci, and 66 MHz, 100 MHz, 133 MHz, 64-bit PCI-x bus operation. The electrical types are shown in *Table 4-13*. The signals supported are listed in *Table 4-14*.

Table 4-13. PCI Electrical Levels

Type	Description
In	Input is a standard input-only signal.
o/d	Open Drain allows multiple devices to share signals as a wired-OR.
Out	Totem Pole Output is a standard active driver.
s/t/s	Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time, subject to specific timing restrictions.
t/s	Tri-State is a bi-directional, tri-state input/output pin.

Table 4-14. PCI Signal Descriptions

Signal(s)	Type	Name and Description
ACK64_L	s/t/s	**Acknowledge 64-bit Transfer** indicates that the PCI target is willing to transfer data using 64 bits.
AD[63:00]	t/s	**Address and Data** are multiplexed; during the first clock of a transaction (address phase), they contain a 32-bit physical address, during subsequent clocks, data. As address bits, AD0 and AD1 have no significance; instead, they are encoded to indicate the burst type.
C/BE[7:0]_L	t/s	**Bus Command and Byte Enable** are multiplexed; during the address phase of a transaction, C/BE[3:0]_L defines the bus command; during the data phase C/BE[3:0]_L determines which byte lanes carry valid data.
DEVSEL_L	s/t/s	**Device Select**, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates whether any device on the bus has been selected.
FRAME_L	s/t/s	**Cycle Frame** is driven by the current master to indicate the beginning and duration of an access.
GNT_L	In	**Grant** indicates to the agent that the arbiter has granted access to the bus. This is a point-to-point signal. Every master has its own GNT_L.
IDSEL	In	**Initialization Device Select** is used as a chip select, instead of the upper 20 address lines, during configuration read and write transactions.
INT[A:D]_L	In	**PCI interrupt** signals from add-in card. Onboard devices may also generate these signals, which are managed by the PID.
IRDY_L	s/t/s	**Initiator Ready** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. During a write, IRDY_L indicates that valid data is present. During a read, it indicates the master is prepared to accept data.
LOCK_L	s/t/s	**Lock** indicates an atomic operation that may require multiple transactions to complete.

Signal(s)	Type	Name and Description
PCIXCAP	In	**PCIXCAP** indicates to a device if the bus segment supports PCI-X.
M66EN	In	**66MHZ_Enable** indicates to a device if the bus segment is operating at 66 or 33 MHz.
PAR	t/s	**Parity** indicates even parity across AD[31:00] and C/BE[3:0]_L. Parity generation is required by all PCI agents.
PAR64	t/s	**Parity64** indicates even parity for the upper 32 bits of data on AD[63:32].
PCICLK		**Bus Clock** for this PCI segment, synchronous with processor local bus. May be either 33 MHz or 30 MHz, depending on processor frequency. Default is 33 MHz.
PERR_L	s/t/s	**Parity Error** reports a data parity error on all commands except Special Cycle.
REQ_L	Out	**Request** indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own REQ_L.
REQ64_L	s/t/s	**Request 64-bit Transfer**, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits.
PCIRST_L	In	**Reset** forces the PCI sequencer of each device to a known state.
SERR_L	o/d	**System Error** reports address parity errors, data parity errors on Special Cycle commands, or any other system error where the result will be catastrophic.
STOP_L	s/t/s	**Stop** indicates the current target is requesting the master to stop the current transaction.
TRDY_L	s/t/s	**Target Ready** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. During a read, TRDY_L indicates that valid data is present. During a write, it indicates the target is prepared to accept data.
3.3Vaux	In	**3.3Vaux** 3.3-volt auxiliary power source delivers power to the PCI add-in card for generation of power management events when the main power to the card has been turned off by software.

4.5.4.8 PCI Slot Pinouts

The following table lists the pinouts for the 3.3-V keyed slot.

Table 4-15. 3.3-V PCI Slot Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST_L	A48	GND	B1	-12V	B48	AD10
A2	+12V	A49	AD9	B2	TCK	B49	M66EN
A3	TMS	A50	GND	B3	GND	B50	GND
A4	TDI	A51	GND	B4	TDO	B51	GND
A5	+5V	A52	C/BEO_L	B5	+5V	B52	AD8
A6	INTA_L	A53	+3.3V	B6	+5V	B53	AD7
A7	INTC_L	A54	AD6	B7	INTB_L	B54	+3.3V
A8	+5V	A55	AD4	B8	INTD_L	B55	AD5
A9	RESERVED	A56	GND	B9	PRSNT1_L	B56	AD3
A10	+3.3V	A57	AD2	B10	RESERVED	B57	GND
A11	RESERVED	A58	AD0	B11	PRSNT2_L	B58	AD1
A12	3.3V KEYWAY	A59	+3.3V	B12	3.3V KEYWAY	B59	+3.3V
A13		A60	REQ64_L	B13		B60	ACK64_L
A14	3.3Vaux	A61	+5V	B14	RESERVED	B61	+5V
A15	RESET_L	A62	+5V	B15	GND	B62	+5V
A16	+3.3V	A63	GND	B16	CLK	B63	RESERVED
A17	GRANT_L	A64	C/BE7_L	B17	GND	B64	GND

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A18	GND	A65	C/BE5_L	B18	REQ_L	B65	C/BE6_L
A19	RESERVED	A66	+3.3V	B19	+3.3V	B66	C/BE4_L
A20	AD30	A67	PAR64	B20	AD31	B67	GND
A21	+3.3V	A68	AD62	B21	AD29	B68	AD63
A22	AD28	A69	GND	B22	GND	B69	AD61
A23	AD26	A70	AD60	B23	AD27	B70	+3.3V
A24	GND	A71	AD58	B24	AD25	B71	AD59
A25	AD24	A72	GND	B25	+3.3V	B72	AD57
A26	IDSEL	A73	AD56	B26	C/BE3_L	B73	GND
A27	+3.3V	A74	AD54	B27	AD23	B74	AD55
A28	AD22	A75	+3.3V	B28	GND	B75	AD53
A29	AD20	A76	AD52	B29	AD21	B76	GND
A30	GND	A77	AD50	B30	AD19	B77	AD51
A31	AD18	A78	GND	B31	+3.3V	B78	AD49
A32	AD16	A79	AD48	B32	AD17	B79	+3.3V
A33	+3.3V	A80	AD46	B33	C/BE2_L	B80	AD47
A34	FRAME_L	A81	GND	B34	GND	B81	AD45
A35	GND	A82	AD44	B35	IRDY_L	B82	GND
A36	TRDY_L	A83	AD42	B36	+3.3V	B83	AD43
A37	GND	A84	+3.3V	B37	DEVSEL_L	B84	AD41
A38	STOP_L	A85	AD40	B38	PCIX_CAP	B85	+5V
A39	+3.3V	A86	AD38	B39	LOCK_L	B86	AD39
A40	SDONE	A87	GND	B40	PERR_L	B87	AD37
A41	SB0_L	A88	AD36	B41	+3.3V	B88	+3.3V
A42	GND	A89	AD34	B42	SERR_L	B89	AD35
A43	PAR	A90	GND	B43	+3.3V	B90	AD33
A44	AD15	A91	AD32	B44	C/BE1_L	B91	GND
A45	+3.3V	A92	RESERVED	B45	AD14	B92	RESERVED
A46	AD13	A93	GND	B46	GND	B93	RESERVED
A47	AD11	A94	RESERVED	B47	AD12	B94	GND

4.5.5 PCI Hot-Plug Interface

All eight slots adhere to the *PCI Hot-Plug Specification, Revision 1.0.* The respective P64H2 components contain the hot-plug controller for each of the particular bus segments. External devices such as FET switches, power controllers, and the hot-plug LED board connector are used to complete the hot-plug interface.

The I/O board operates in Connect Bus First (CBF) mode. In this mode, the bus signals to the adapter being added to the system that it will be connected to the bus prior to reset being released.

The P64H2's hot-plug controller can operate in three modes depending on the number of slots/devices attached. The modes are single slot, dual slot, and multi-slot (more than two). Only single-slot and dual-slot modes are used on the I/O board.

4.5.5.1 Single Slot Mode

The PCI bus segments containing only a single slot and no embedded devices have their PCI hot-plug controllers operate in single-slot mode. In this mode, the P64H2 will put the PCI bus in a quiescent state during the hot-plug event (all PCI bus signals are driven LOW). In addition, the PCI clock for this slot is also driven LOW. In this manner, it is not necessary to provide the traditional FET switches for the PCI bus and clock signals. Only the power control devices are required, in addition to the P64H2, to complete the hot-plug control circuit.

The PCI clocks are sourced from the P64H2. No FET is required, as the P64H2 will drive the clock to the slot LOW during a hot plug event.

Two clock outputs from the P64H2 each drive a series terminator resistor. One driver connects to the PCI slot and the other to the feedback pin on the P64H2. The clock traces are matched length (minus a 3-inch offset on the slot clock to account for the clock routing on the adapter) to allow the Phase Locked Loop (PLL) to align the clock to the internal circuits of the P64H2 with the circuits on the adapter. Unlike the two-slot configuration, the clocks cannot be 'ganged' since the P64H2 will drive its slot clock LOW during a hot-swap procedure, but expects its feedback clock to remain operational.

4.5.5.2 Dual Slot Mode

The PCI bus segments that contain two slots or one slot and one onboard device have their PCI hot-plug controllers operate in dual-slot mode. In this mode, the P64H2 has individual control signals for each of the two slots to control bus FET switches, clock FET switches, reset, power control, MRL and attention switches, and attention LEDs. No serial de-multiplexing logic is required to decode the hot-plug controller's individual slot control, as is the case when the controller is in multi-slot mode.

The PCI clocks are sourced from the P64H2 and driven through a FET device. This allows the hot-plug controller to quiesce the clock to the slot.

The clocks are isolated to each slot using a CBT3125 FET switch. All PCI clocks are routed through FET switches, including the feedback clock and SCSI chip clock, in order to have identical topologies on the clocks. The clock driver pins from the P64H2 are 'ganged' together (all connected) to form a 'star' route to separate series terminator resistors. This arrangement reduces the pin-to-pin skew of the clock driver to virtually zero. The clock traces are matched length (minus an approximate 3-inch offset on the slot clocks to account for the clock routing on the adapter) to allow the PLL to align the clock to the internal circuits of the P64H2 with the circuits on the adapter.

4.5.5.3 PCI Field Effect Transistor (FET) Switches

For those segments that operate in dual-slot mode, the PCI bus signals are isolated from the slot by using FET switches. In particular, CBT6820 and CBT6810 (or equivalent) bus isolation switches are used. The CBT6820/10 components have a pre-charge feature (VBIAS) that minimizes signal distortions on the PCI bus by pulling the signals to a high state on the adapter prior to closing the FET switches. Since the CBT6820 has only a single VBIAS pin, the I/O board uses individual parts per slot (instead of using each part to drive both slots). This allows the VBIAS to be powered only when the adapter is powered.

4.5.5.4 PCI Reset

The PCI Reset_L signal is driven from the hot-plug controller individually to each slot or device on the bus segment. In this manner, the hot-plug controller is able to cycle reset appropriately during a hot-plug event.

4.5.5.5 PCI Power Control

Each PCI slot, regardless of operational mode, has external power control circuitry. This circuitry controls the application of power to each slot and monitors for power abnormalities such as over-current or under-voltage.

An MIC2590 (or equivalent) device is used to provide power control and monitoring for the 5-V, 3.3-V, 12-V, N12-V and 3.3VAUX power rails. The MIC2590 is a dual device that can independently control power for two slots. The device controls external power FETs to switch the 5-V and 3.3-V rails (due to relatively large current requirements), but contains internal FETs to control the relatively low current of the +12-V, –12-V and 3.3VAUX rails. The MIC2590 interfaces directly to the hot-plug controller for power-on control and fault reporting for 5-V, 3.3-V, 12-V, and N12-V rails.

The 3.3VAUX power rail is controlled indirectly from the HPIB LED board's MRL switch. The signal from the HPIB LED board is routed through a PLD to allow gating of the 3.3VAUX power enable, should that be necessary.

The MIC2590 monitors the individual power rails for over-current and under-voltage conditions. If a fault occurs, the MIC2590 will latch off the power rails and activate the FAULTx output. The P64H2's hot-plug controller monitors this fault signal. In addition, the fault status, as well as other functions, can be read from the MIC2590 over the I^2C port by server management. See the component specification for the MIC2590 on details concerning its operation.

4.5.5.6 HPIB PCI Hot-Plug LED/Switch Connector

The PCI Hot-Plug LED/Switch connector provides the interface from the hot-plug controller to the LEDs and switches contained on the HPIB board. Each slot has two switches and two LEDs associated with it.

The switches are the Module Retention Latch (MRL) and User Attention Switch. The MRL is associated with a mechanical interlock device and is OPEN if the interlock is positioned to allow a board to be added or removed. The User Attention Switch can be accessed by pressing the switch and thus alerting the system that a hot-plug event is requested.

The LEDs consist of one GREEN and one AMBER in color. These are sequenced as outlined in the hot-plug specification.

A chassis identification LED is also located on the HPIB. This signal is driven from the I/O board in response to a server management command. The function of the signal is to help identify the chassis by flashing the LED in response to a user request. Note that the front panel interface also contains a similar signal.

Both 3.3 V main and 3.3VSTDBY power are supplied to the HPIB board. These rails are protected by fuses on the I/O board. Fuse F9C1 protects 3.3 V main and fuse F9C2 protects the 3.3VSTDBY rail. *Table 4-16* lists the connector pinout.

Table 4-16. PCIHP LED/Switch Connector

Pin #	I/O	Description
1	I	Slot 1 Amber LED Cathode
2	I	Slot 1 Green LED Cathode
3	O	Slot 1 MRL Switch
4	O	Slot 2 MRL Switch
5	I	Slot 2 Amber LED Cathode
6	I	Slot 2 Green LED Cathode
7	I	Slot 3 Amber LED Cathode
8	I	Slot 3 Green LED Cathode
9	O	Slot 3 MRL Switch
10	O	Slot 4 MRL Switch
11	I	Slot 4 Amber LED Cathode
12	I	Slot 4 Green LED Cathode
13	I	Slot 5 Amber LED Cathode
14	I	Slot 5 Green LED Cathode
15	O	Slot 5 MRL Switch
16	O	Slot 6 MRL Switch
17	I	Slot 6 Amber LED Cathode
18	I	Slot 6 Green LED Cathode
19	I	Slot 7 Amber LED Cathode
20	I	Slot 7 Green LED Cathode
21	O	Slot 7 MRL Switch
22	O	Slot 8 MRL Switch
23	I	Slot 8 Amber LED Cathode
24	I	Slot 8 Green LED Cathode
25	O	Slot 1 Attention Switch
26	O	Slot 2 Attention Switch
27	O	Slot 3 Attention Switch
28	O	Slot 4 Attention Switch
29	O	Slot 5 Attention Switch
30	O	Slot 6 Attention Switch
31	O	Slot 7 Attention Switch
32	O	Slot 8 Attention Switch
33	PWR	+3.3V_aux
34	I	Chassis ID LED
35	PWR	+3.3V_aux
36	PWR	GND
37	PWR	+3.3V
38	PWR	GND
39	PWR	+3.3V
40	PWR	GND

4.5.6 PCI Power Management Interface

The PCI Power Management Interface structure provides a standard interface to control power management features, and is compliant with the *PCI Bus Power Management Interface Specification, Revision 1.1*. Each PCI slot has 3.3VAUX power, which is used to power logic on the adapter that needs to remain active when the rest of the system is powered down. The adapter is able to 'wake up' the system by issuing a Power Management Event (PME), initiated by asserting the PME_L signal. The PME_L signal is routed to the server management controller on the I/O riser, which can issue a system power-on sequence if desired. The power management policies of the system ultimately dictate what action is taken as a result of a PME.

Only slots 1-5 support the PME function. This limitation is due to only having three PME_L signals available to the I/O riser and the requirement to have only a single PCI bus drive one PME_L signal (for deadlock prevention). The individual slot PME_L signals route to a PLD and are then gated to the respective I/O riser PME_L signals. See Section 4.5.5.5 and *Figure 4-3* for information regarding hot-plug control of the 3.3VAUX power. See *Figure 4-3* for a diagram of the PCI AUX control and PME generation.

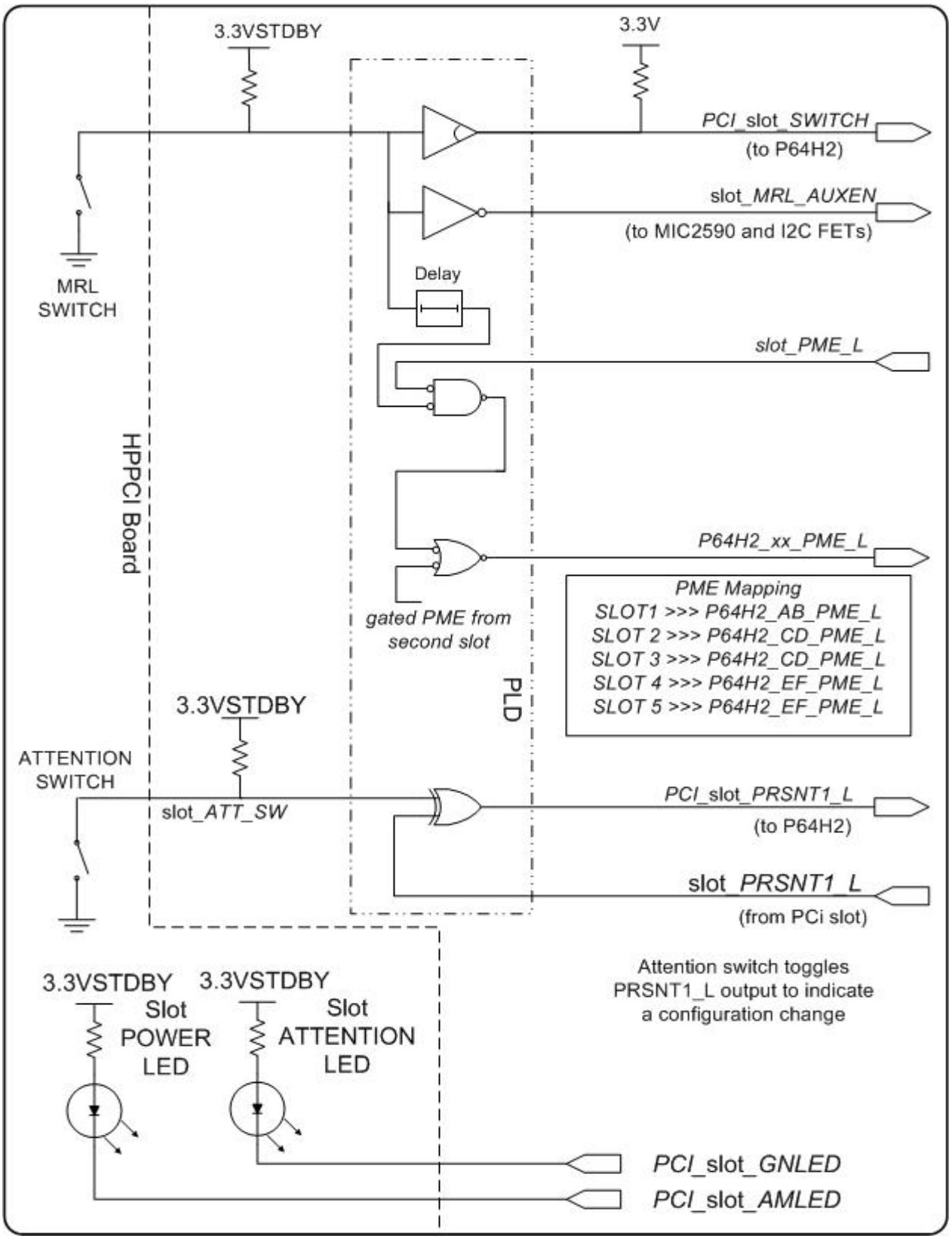


Figure 4-3. PCI AUX Control and PME Control

4.5.7 SCSI Interface

A single LSI* 53C1030 Ultra 320 LVDS controller provides the integrated SCSI interfaces. The controller resides on PCI Bus Segment A. The controller communicates as a 64-bit PCI-x device for optimum performance. The controller's PCI-x interface can operate at a bus speed of up to 100 MHz depending on the capabilities of any adapter installed into SLOT 1. The configuration registers define PCI-related parameters for the ISP12320 device. The ISP12320 supports all mandatory registers in the PCI configuration space header including the Vendor ID, Device ID, Class Code, Revision ID, Header Type, and Command and Status fields.

The ISP12320 supports two Ultra 320 LVDS channels. One is intended for control of internal drives, and the other is intended for high-speed connection to an external SCSI device. SCSI port 'A' of the ISP12320 controls the internal SCSI channel. The internal channel is routed to the midplane disk bay connector to permit interfacing to internal disk devices. The internal channel has been validated only for LVDS operation. SCSI port 'B', of the ISP12320, controls the external SCSI channel. The external channel connector is located near the ISP12320 chip where it can be cabled to the system chassis bulkhead connector. The external channel can be operated with LVDS or SE signaling, provided the external cabling supports the required signaling.

The internal channel also has a standard SCSI connector that allows an external controller (typically RAID) to interface with the SCSI backplane. Attaching a cable to the 'RAID' connector will disable the on-board SCSI controller and the on-board SCSI terminators.

The ISP12320 operates on 1.8 V and 3.3 V. 1.8 V powers the ISP12320's core and 3.3 V powers the PCI and SCSI interfaces.

The ISP12320 uses an 80-MHz crystal to clock the SCSI interface.

Refer to the LSI 53C1030 data sheets at http://www.lsilogic.com for more details on the SCSI controller operation.

4.5.7.1 SCSI Signal Description

Table 4-17 provides a summary of the SCSI connector signal pins, including the signal mnemonic, name, and brief description.

Table 4-17. SCSI Signal Descriptions

Signal Name	Type	Description
-ACK[P,M]	LVDS	Transfer Acknowledge.
-ATN[P,M]	LVDS	Attention.
-BSY[P,M]	LVDS	Bus Busy.
-C/D[P,M]	LVDS	Control/Data. If true (logic 0) = Control Phase. If false (logic 1) = Data Phase.
-DB(0:15) [P,M]	LVDS	Data Bus.
-DBP(0:1) [P,M]	LVDS	Parity. DBP0: DB(15:8). DBP1: DB(7:0).

Signal Name	Type	Description
-I/O[P,M]	LVDS	Direction. If true (logic 0) I = Input to initiator. If false (logic 1) O = Output from initiator.
-MSG[P,M]	LVDS	Message Phase.
-REQ[P,M]	LVDS	Transfer Request.
-RST[P,M]	LVDS	Bus Reset. All devices on bus will reset.
-SEL[P,M]	LVDS	Arbitration.
DIFFSENSE	Analog	SCSI Mode Sense.
GROUND	Power	Electrical Ground.
TERMPWR	Power	Terminator Power. Static 5 volts.

4.5.7.2 SCSI Connector Pinout

See *Table 4-2* for the pinout of the midplane disk bay connector containing the internal SCSI bus.

See *Table 4-18* for the internal and external SCSI connector pinout.

Table 4-18. SCSI Connector Pinout – LVDS Mode

Signal Name	Conn. Pin	Cable Pin	Cable Pin	Conn. Pin	Signal Name
+DB(12)	1	1	2	35	-DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
+DB(0)	6	11	12	40	-DB(0)
+DB(1)	7	13	14	41	-DB(1)
+DB(2)	8	15	16	42	-DB(2)
+DB(3)	9	17	18	43	-DB(3)
+DB(4)	10	19	20	44	-DB(4)
+DB(5)	11	21	22	45	-DB(5)
+DB(6)	12	23	24	46	-DB(6)
+DB(7)	13	25	26	47	-DB(7)
+DB(P0)	14	27	28	48	-DB(P0)
GROUND	15	29	30	49	GROUND
DIFSENSE	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED (NC)	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
+ATN	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND*
+BSY	23	45	46	57	-BSY
+ACK	24	47	48	58	-ACK
+RST	25	49	50	59	-RST
+MSG	26	51	52	60	-MSG
+SEL	27	53	54	61	-SEL
+C/D	28	55	56	62	-C/D
+REQ	29	57	58	63	-REQ
+I/O	30	59	60	64	-I/O
+DB(8)	31	61	62	65	-DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

*Note: on the ‘RAID” connector, this pin is defined as RAID_PRES_L which is pulled to ground when a cable is attached, thus indicating the need to disable the on-board SCSI controller and on-board terminators.

4.5.8 IDE Interface

The IDE bus is controlled from the I/O riser board and passes through the I/O board to the midplane disk bay connector. This permits interfacing to internal devices in the disk bay such as CDROM, DVDROM, DVDRAM, or LS240 floppy devices. The I/O board does not provide any logic or buffering for this bus.

4.5.8.1 IDE Signal Descriptions

Refer to *Table 4-19* for a summary of the IDE interface connector signal pins that pass through the midplane disk bay connector, including the signal mnemonic, name, and brief description.

Table 4-19. IDE Signal Descriptions

Signal	Name and Description
CS1P_L	Select Command Register Block.
CS3P_L	Select Control Register Block.
DA[2:0]	Register Select Address (from ISA address bus).
DACK_L	Direct Memory Access (DMA) Acknowledge.
DD[15:0]	ISA Data.
DIOR_L	Read Request. Handshake request for read operations.
DIOW_L	Write Request. Handshake request for write operations.
DRQ	Direct Memory Access (DMA) request.
IORDY	Ready. Optional. Device ready for operation (high).
IRQ14	Interrupt Request.
RSTDRV_L	Reset. Forces drivers on the ISA bus to initialize.

4.5.8.2 IDE Connector Pinout

See *Table 4-2* for the pinout of the midplane disk bay connector.

4.5.9 I/O Riser Interface

The I/O riser connector provides system I/O, IDE, server management, ISP, JTAG, interrupt, and power interfaces.

4.5.9.1 System I/O Interface

The I/O riser communicates to the system principally over the 8-bit HL1.5 bus that connects the SIOH component on the I/O board to the ICH4 component on the I/O riser. This bus provides adequate bandwidth for system I/O functions while using only 16 signals.

This bus meets specific routing and electrical reference parameters in order to comply with strict signal integrity requirements. The signal-to-ground ratio in the connector has been chosen to meet the impedance and cross-talk parameters of this bus.

4.5.9.2 IDE Bus

A single IDE bus is generated from the I/O riser ICH4 controller. This bus is passed to the I/O board through the I/O riser interface connector. See Section 4.5.8 for a description of this interface.

4.5.9.3 Server Management

The I/O riser contains the server management controller. The signals necessary to interface to the system's server management functions pass through the I/O riser interface connector. See Section 4.5.10 for details on the server management functions on the I/O board.

4.5.9.4 In-System Programming (ISP) Interface

The I/O riser provides the capability to update certain PLDs contained within the system. The ISP interface passes through the I/O riser Interface. See Section 4.5.11 for more information on the ISP capabilities of the I/O board. See also the I/O riser chapter for additional information on the ISP controller.

4.5.9.5 Joint Test Action Group (JTAG)

The I/O board passes a standard JTAG interface between the I/O riser and the midplane. This allows the I/O riser to communicate with the JTAG circuit on the processor board. This interface is not used on the I/O board.

The I/O board uses an ITP connector to communicate with the SIOH. See Section 4.5.27 for information on the ITP interface.

4.5.9.6 I/O Riser Power

Table 4-20 lists the current rating of the I/O riser connector. Note that this does not define the actual power available from the I/O board or the I/O riser.

Table 4-20. I/O Riser Connector Current Rating

Voltage	Source	# Pins	Current Carrying Capability*
3.3 V	I/O board	13	6.5 A
5 V	I/O board	8	4 A
12-V STDBY	Power supply (through I/O board)	7	3.5 A
5-V STDBY	I/O riser	2	1 A
3.3-V STDBY	I/O riser	12	6 A

Note: *Represents the current rating of the connector at 1 amp per pin, derated 50%. The actual amount of power available from the sources will be different.

4.5.9.7 I/O Riser Pinout

Table 4-21 lists the pinout for the I/O riser interface connector.

Table 4-21. I/O Riser Connector Pinout

Signal Name			Signal Name	Signal Name			Signal Name
RISER_INTERLOCK0_L	B121	A121	CLK33_FWH4	GND	B61	A61	CLK66_ICH2
3.3V	B120	A120	GND	CLK33_PLD2	B60	A60	GND
GND	B119	A119	CLK33_FWH8	GND	B59	A59	INTRUDER_L
HL0	B118	A118	GND	P5V_STDBY	B58	A58	MMGPI_L
GND	B117	A117	CLK33_FWH5	PROCHOT_L	B57	A57	HPC_INTR_L
HL1	B116	A116	GND	STPCLK_L	B56	A56	RSVD
GND	B115	A115	HUBLINK_CONFIG	V_BAT	B55	A55	RSVD
HL2	B114	A114	GND	GND	B54	A54	POWER_SW_L
GND	B113	A113	HL_PAR	I2C_IPMB_SCL	B53	A53	RESET_SW_L
HL3	B112	A112	GND	I2C_IPMB_SDA	B52	A52	SDINT_SW_L
GND	B111	A111	HL_REQM	I2C_PCI_SCL	B51	A51	INIT_L
HL_STB	B110	A110	HL_REQI	I2C_PCI_SDA	B50	A50	SNCFWHWP_L
GND	B109	A109	IA64_IA32	RSVD	B49	A49	CHASS_ID_L
HL_STB_L	B108	A108	SNC_BERRIN_L	RSVD	B48	A48	GND
GND	B107	A107	CORR_ERR_L	GND	B47	A47	CLK14_ICH2
HL4	B106	A106	3.3V	I2C_SYS_SCL	B46	A46	GND
GND	B105	A105	5VSTDBY	I2C_SYS_SDA	B45	A45	RSVD
HL5	B104	A104	GND	I2C_SMB_SCL	B44	A44	SPEAKER
GND	B103	A103	CLK33_FWH6	I2C_SMB_SDA	B43	A43	ON_LED_L
HL6	B102	A102	GND	I2C_IO_SCL	B42	A42	PWR_FLT_LED_L
GND	B101	A101	CLK33_FWH9	I2C_IO_SDA	B41	A41	COOL_FLT_LED_L
HL7	B100	A100	GND	3.3V	B40	A40	GEN_FLT_LED_L
GND	B99	A99	CLK33_FWH7	IS_TCK	B39	A39	GND
5V	B98	A98	GND	IS_TDI	B38	A38	LCD_RS
3.3V	B97	A97	3.3VSTDBY	IS_TDO	B37	A37	LCD_E
GND	B96	A96	HL_STOP	IS_TMS	B36	A36	LCD_RW
PCI_IDE_RST_L	B95	A95	BUF_32KHz	IS_TRST_L	B35	A35	ISP_SCLK_LCD4
PDCS1_L	B94	A94	PDCS3_L	5V	B34	A34	ISP_MODE_LCD5
PDA2	B93	A93	PDA1	GND	B33	A33	LCD6
IRQ14	B92	A92	PDA0	RSVD	B32	A32	ISP_SDO_LCD7
PDDACK_L	B91	A91	PDIOR_L	NODE0_HP_INT_L	B31	A31	ISP_SDI
PDIOW_L	B90	A90	PIORDY	P3.3V_STDBY_GD	B30	A30	ISP_EN_L
PDDREQ	B89	A89	PDD0	GND	B29	A29	IO_REV_ID0
PDD14	B88	A88	PDD15	IO_REV_ID1	B28	A28	SERR_L
PDD1	B87	A87	PDD2	PWRGOOD	B27	A27	PS_ON_L
GND	B86	A86	3.3V	P12V_STDBY	B26	A26	SM_PWROK
PDD12	B85	A85	3.3V	P12V_STDBY	B25	A25	PLD_RST_L
PDD3	B84	A84	GND	P12V_STDBY	B24	A24	EX_RESET_L
PDD4	B83	A83	PDD13	P12V_STDBY	B23	A23	IO_REV_ID2
PDD10	B82	A82	PDD11	P12V_STDBY	B22	A22	SYS_D2D_EN
PDD9	B81	A81	PDD5	P12V_STDBY	B21	A21	ICMB_ID1_RX
PDD8	B80	A80	A20M_L	P12V_STDBY	B20	A20	ICMB_ID2_RX

Signal Name			Signal Name	Signal Name			Signal Name
PDD6	B79	A79	FERR_L	GND	B19	A19	ICMB_ID_TXEN
PDD7	B78	A78	IGNNE_L	3.3VSTDBY	B18	A18	ICMB_TX
INTOUT_L	B77	A77	ERR1_CORR	3.3VSTDBY	B17	A17	ICMB_RX
BOOT_INT1_L	B76	A76	INTR	3.3VSTDBY	B16	A16	ICMB_TXEN
BOOT_INT0_L	B75	A75	NMI	3.3VSTDBY	B15	A15	RSVD
P64H2_AB_PME_L	B74	A74	PMI_L	3.3VSTDBY	B14	A14	IS0_JTAGEN_L
P64H2_CD_PME_L	B73	A73	3.3V	GND	B13	A13	GND
P64H2_EF_PME_L	B72	A72	3.3V	3.3VSTDBY	B12	A12	5V
3.3VSTDBY	B71	A71	GND	3.3VSTDBY	B11	A11	GND
3.3VSTDBY	B70	A70	GND	3.3VSTDBY	B10	A10	CLK33_NIC
RSVD	B69	A69	3.3V	3.3VSTDBY	B9	A9	GND
GND	B68	A68	GND	GND	B8	A8	CLK33_VID
PHP_DIS_IO_L	B67	A67	3.3V	3.3V	B7	A7	GND
ICH2_PWROK	B66	A66	GND	3.3V	B6	A6	CLK33_SIO
GND	B65	A65	CLK33_ICH2	GND	B5	A5	GND
3.3V	B64	A64	GND	5V	B4	A4	CLK14_SIO
GND	B63	A63	CLK48 _ICH2	5V	B3	A3	GND
CLK33_BMC	B62	A62	GND	5V	B2	A2	5V
				RISER_INTERLOCK1_L	B1	A1	5V

4.5.10 Server Management Functions

The I/O board contains the following server management functions:

- Fan control
- Temperature sensing
- Voltage sensing
- Reset control
- System Event Log (SEL)
- FRU Information

The server management controller, contained on the I/O riser, controls the functions listed above.

4.5.10.1 Block Diagram

Figure 4-4 presents a block diagram of the server management sub-system.

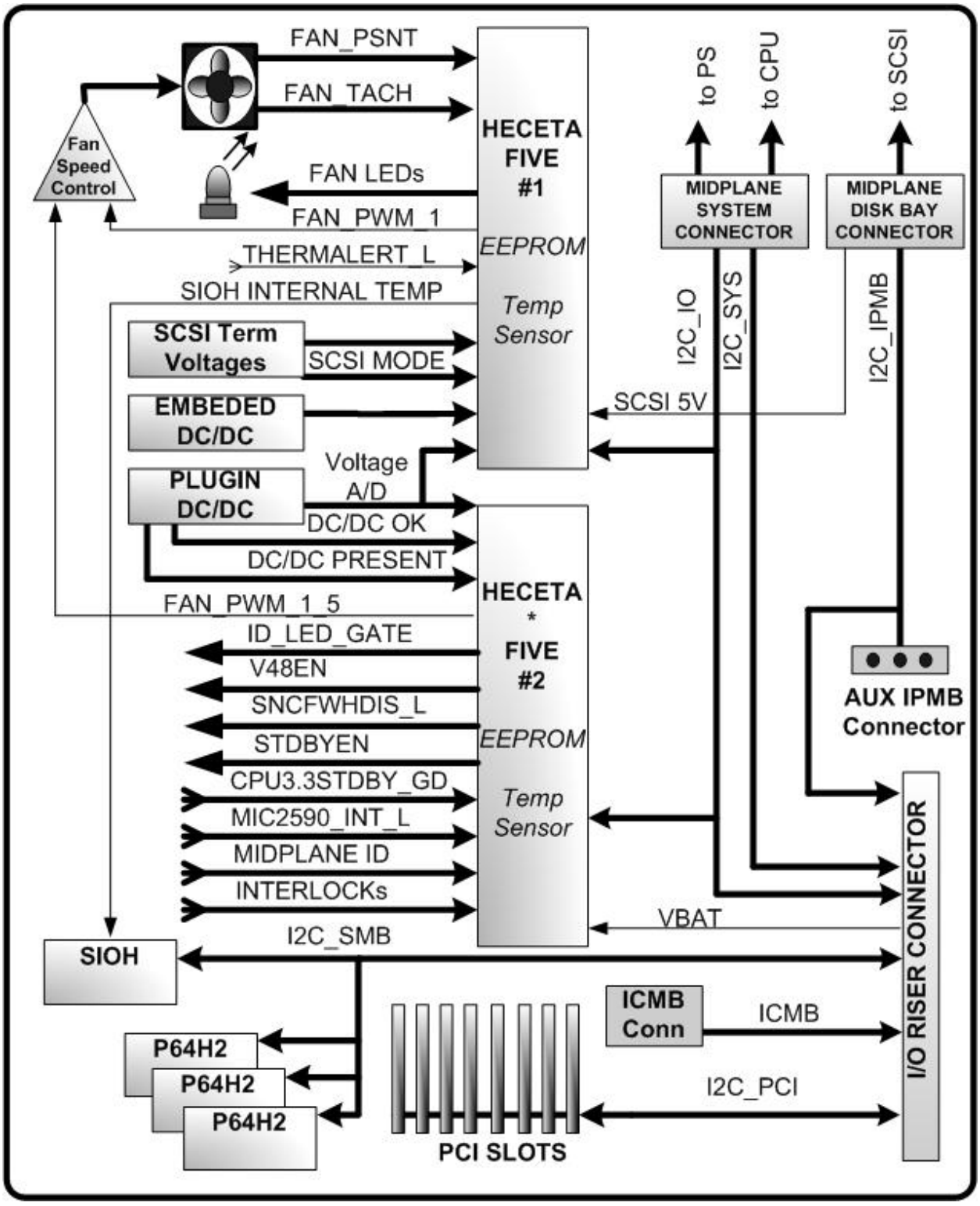


Figure 4-4. Server Management Block Diagram

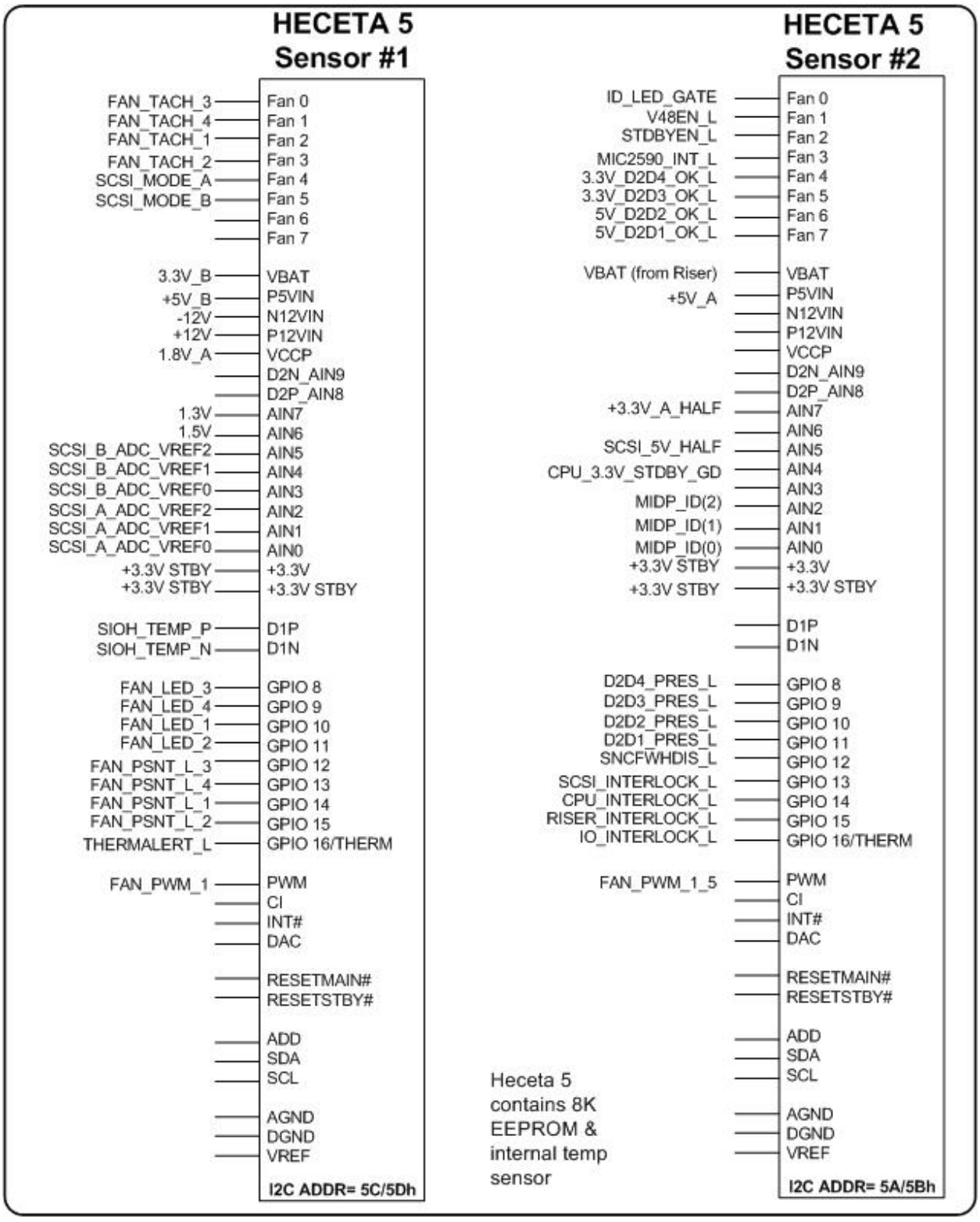


Figure 4-5. Server Management Sensor Assignment

Table 4-22. Server Management Address Map

Device	Reference	I^2C Bus	Address Range
Heceta5 #1	U2E1	I2C_IO	5C/5D
Heceta5 #2	U1A1	I2C_IO	5A/5B
MIC2590 (1,2)	U3B1	I2C_IO	80/81
MIC2590 (3,4)	U5B1	I2C_IO	82/83
MIC2590 (5,6)	U6B1	I2C_IO	84/85
MIC2590 (7,8)	U8B1	I2C_IO	86/87
SIOH	U8F1	I2C_SMB	EC/ED
P64H2 AB	U5E3	I2C_SMB	CA/CB
P64H2 CD	U7E1	I2C_SMB	C8/C9
P64H2 EF	U9E1	I2C_SMB	C4/C5

4.5.10.2 Fan Control

The I/O board contains the fan control and power circuits for the main system fans. There are four fans in the system (excluding those inside the power supply) and they operate in a 3 + 1 redundant system. There are two sets of fan controls and interfaces. One controls a pair of 1.5-inch fans that serve as the cooling mechanism for the system's processors; the other controls a pair of 1-inch fans that serve as the cooling mechanism for the system's memory and other logic. Both sets of fans serve as the cooling mechanism for the I/O sub-system. The cooling system is redundant in that a single fan failure can occur and the system will continue to operate, although possibly with reduced performance.

The fans are powered directly from the 48-V power distribution rail. Normally, the fans run at a reduced speed in order to lower the overall noise generated by the system. However, the fans can operate at full speed in order to improve the cooling capacity of the system. This is done in response to the failure of a fan or to the detection of unusually high temperatures within the system. The server management sub-system monitors individual fan speeds in order to detect fan failures and also monitors various system temperature sensors to detect abnormal system and component temperatures. The server management sub-system can then increase the speed of the fans to improve airflow and reduce system temperatures.

The fan speed is controlled by the HECETA5's Pulse-Width Modulation (PWM) circuits. The normal fan speed is typically lower than full speed in order to reduce the noise level of the system. This level is set by server management software by writing to the HECETA5's PWM speed registers. There are separate PWM controls for the 1-inch and 1.5-inch fan sets. This allows server management to control the speed of the two sets independently.

Fan speed defaults to high speed at power on.

The HECETA5 server management controller also provides the fan speed detection. Each fan contains a tachometer (FAN_TACH_x) signal, whose pulse rate is proportional to the actual fan speed. Server management software can poll the HECETA5 device and determine if fans are operating within specified speed ranges. The software can then initiate a specified action in response to a slow or stalled fan such as increasing the speed of the remaining fans and/or alerting the user of a fan failure. In addition to reporting the failure to a system console, the server management controller is also able to illuminate an LED contained on the fan assembly

to indicate which fan failed. There is a present indication (FAN_PSNT_L_x) for each fan that can be read from the server management interface. This allows the server management software to differentiate between reading a fan failure indication with a failed fan, or with a fan that has been removed.

The fans physically and electrically interface to the I/O board through individual six-pin blind mate connectors. This arrangement allows a fan CRU to be designed such that it can easily be removed or installed while the system continues to operate (hot-plug fan CRUs).

Table 4-25 lists the tachometer and LED control bit assignments. *Table 4-23* lists the signal descriptions for the fan interface. *Table 4-24* lists the connector pinout.

Table 4-23. Fan Connector Signal Description

Signal	Signal Description
48V	48-volt fan power supply
48V RTN	Return for 48-volt power
SPEED	PWM control for fan speed setting
TACH	Tachometer output from fan that indicates actual fan speed
PRESENCE_L/LED	Indicates physical fan presence and controls the LED
GND	Return for control signals – connected to logic GND

Table 4-24. Fan Connector Pinout

Signal	Pin	Pin	Signal
48V	1	4	48V RTN
SPEED (PWM)	2	5	GND
TACH	3	6	PRESENCE/LED

Table 4-25. Server Management Fan Control Assignment

Signal	Function	I^2C Port	Pin Name
FAN_TACH_1	Fan 1 (1") tachometer input	5C/5D	FAN 2
FAN_TACH_2	Fan 2 (1") tachometer input	5C/5D	FAN 3
FAN_TACH_3	Fan 3 (1.5") tachometer input	5C/5D	FAN 0
FAN_TACH_4	Fan 4 (1.5") tachometer input	5C/5D	FAN 1
FAN_PSNT_L_1	Fan 1 (1") present input-0 (low) is present	5C/5D	GPIO 14
FAN_PSNT_L_2	Fan 2 (1") present input-0 (low) is present	5C/5D	GPIO 15
FAN_PSNT_L_3	Fan 3 (1.5") present input-0 (low) is present	5C/5D	GPIO 12
FAN_PSNT_L_4	Fan 4 (1.5") present input-0 (low) is present	5C/5D	GPIO 13
FAN_LED_1	Fan 1 (1") failed LED output-1 is failure (LED on)	5C/5D	GPIO 10
FAN_LED_2	Fan 2 (1") failed LED output-1 is failure (LED on)	5C/5D	GPIO 11
FAN_LED_3	Fan 3 (1.5") failed LED output-1 is failure (LED on)	5C/5D	GPIO 8
FAN_LED_4	Fan 4 (1.5") failed LED output-1 is failure (LED on)	5C/5D	GPIO 9
FAN_PWM_1	1" fans normal (low) speed setting- 0=full speed	5C/5D	PWM
FAN_PWM_1_5	1.5" fans normal (low) speed setting- 0=full speed	5A/5B	PWM

4.5.10.3 Temperature Sensing

The I/O board contains three temperature sensors located at strategic points on the board to allow the server management controller to monitor internal temperatures. The sensors are connected to the server management controller over the I^2C bus. Specific temperature thresholds are set in the server management software; they are not hardwired on the board. Server management can use the temperature readings to report internal system conditions to a user interface and/or use it to adjust fan speed should the internal temperature warrant a change in cooling requirements.

Figure 4-2 shows the approximate location of the thermal sensors. Thermal Sensor 1 is located in the HECETA5 server management device itself and measures ambient temperature in that location of the board. Thermal Sensor 2 is a diode located in the SIOH device and is monitored by the HECETA5 #1 D1P and D1N- pins. Thermal Sensor 3 is located in the HECETA5 #2 server management device and measures ambient temperature in that location of the board.

4.5.10.4 Voltage Sensing

The server management controller can monitor critical system voltages on the I/O board. Analog to Digital converters (A/D) inside the HECETA5's server management controllers convert the voltage signals into a digital format that is readable on the I^2C bus. This includes all the voltages used on the I/O board except 5VSTDBY, which is monitored on the I/O riser. It also includes the 5-V voltage rail used on the SCSI backplane since it cannot be monitored on that board. Due to lack of 5-V scaled A/D inputs, this voltage is scaled externally by half using a voltage divider. Thus the actual voltage read will be half the actual SCSI 5-V rail. Also the 3.3V_A voltage is scaled externally by half using a voltage divider. *Table 4-26* lists the voltages that can be monitored by the server management system on the I/O board.

Table 4-26. Voltage Sense List

Voltage	Principal Use	I²C Port	Pin Name
1.3V	SIOH SP Termination	5C/5D	AIN7
1.5V	SIOH Core	5C/5D	AIN6
1.8V_A	P64H2 Core	5C/5D	VCCP
3.3V_A	PCI 3.3-V supply and other 3.3-V devices. Note that the A/D reading will be ½ the actual voltage.	5A/5B	AIN7
3.3V_B	PCI 3.3-V supply and other 3.3-V devices	5C/5D	VBAT
3.3V STDBY	PCI AUX and other standby devices	5C/5D	3.3V STDBY
“	“	5C/5D	3.3V MAIN
“	“	5A/5B	3.3V STDBY
“	“	5A/5B	3.3V MAIN
5V_A	PCI 5-V supply and other 5-V devices	5A/5B	P5VIN
5V_B	PCI 5-V supply and other 5-V devices	5C/5D	P5VIN
SCSI_5V_HALF	SCSI backplane’s 5-V power rail. Note that the A/D reading will be ½ the actual voltage.	5A/5B	AIN5
12V	PCI 12-V supply	5C/5D	P12VIN
N12V	PCI negative 12-V supply	5C/5D	N12VIN
VBAT	I/O Riser’s battery voltage	5A/5B	VBAT
SCSI_A_ADC_VREF0	SCSI A termination voltage 0	5C/5D	AIN0
SCSI_A_ADC_VREF1	SCSI A termination voltage 1	5C/5D	AIN1
SCSI_A_ADC_VREF2	SCSI A termination voltage 2	5C/5D	AIN2
SCSI_B_ADC_VREF0	SCSI B termination voltage 0	5C/5D	AIN3
SCSI_B_ADC_VREF1	SCSI B termination voltage 1	5C/5D	AIN4
SCSI_B_ADC_VREF2	SCSI B termination voltage 2	5C/5D	AIN5

4.5.10.5 Plug-in D2D Control

In addition to being able to read the output voltage of the plug-in D2Ds, server management can also determine if all the D2Ds are installed and if their Power_OK signals are asserted. *Table 4-27* lists the server management port assignments.

Table 4-27. Server Management D2D Control Assignment

Signal	Function	I²C Port	Pin Name
D2D1_PRES_L	5V D2D1 present- 0=present	5A/5B	GPIO11
D2D2_PRES_L	5V D2D2 present- 0=present	5A/5B	GPIO10
D2D3_PRES_L	3.3V D2D3 present- 0=present	5A/5B	GPIO9
D2D4_PRES_L	3.3V D2D4 present- 0=present	5A/5B	GPIO8
5V_D2D1_OK_L	5V D2D1 power is OK- 0=OK	5A/5B	GPIO 7
5V_D2D2_OK_L	5V D2D2 power is OK- 0=OK	5A/5B	GPIO 6
3.3V_D2D3_OK_L	3.3V D2D3 power is OK- 0=OK	5A/5B	GPIO 5
3.3V_D2D4_OK_L	3.3V D2D4 power is OK- 0=OK	5A/5B	GPIO 4

4.5.10.6 Reset Control

The server management controller can initiate certain reset sequences by driving signals from the I/O riser to the I/O board. See Section 4.5.14 for details of the reset circuit.

4.5.10.7 Field Replaceable Unit (FRU) Information

The I/O board contains two EEPROMs, which store the Field Replaceable Unit (FRU) information. Board assembly number, serial number, and other board-specific information are stored here.

4.5.10.8 Miscellaneous Server Management Functions

Table 4-28 lists other miscellaneous functions controlled by server management.

Table 4-28. Server Management Miscellaneous Control Assignment

Signal	Function	I^2C Port	Pin Name
THERMALERT_L	Thermalert signal from the processor board.	5C/5D	GPIO16
SCSIMODE_A	Indicates SCSI bus A is operating in single-ended mode (Signal = LOW) or LVD mode (signal = HIGH).	5C/5D	GPIO4
SCSIMODE_B	Indicates SCSI bus B is operating in single-ended mode (Signal = LOW) or LVD mode (signal = HIGH).	5C/5D	GPIO5
IO_INTERLOCK_L	If signal = LOW, indicates that I/O board is fully seated in the midplane.	5A/5B	GPIO16
RISER_INTERLOCK_L	If signal = LOW, indicates that riser board is fully seated in the I/O board.	5A/5B	GPIO15
CPU_INTERLOCK_L	If signal = LOW, indicates that CPU board is fully seated in the midplane.	5A/5B	GPIO14
SCSI_INTERLOCK_L	If signal = LOW, indicates that SCSI backplane board is fully seated in the midplane.	5A/5B	GPIO13
SNCFWDIS_L	Output to set the state of the SNC firmware hub disable signal to processor.	5A/5B	GPIO12
MIC2590_INT_L	Indicates the state of the combined interrupt from the four hot plug PCI power controllers (MIC2590's).	5A/5B	GPIO3
STDBYEN	Output to set the state of the standby enable signal to the processor hot-plug circuit.	5A/5B	GPIO2
48VEN	Output to set the state of the 48 volt enable signal to the processor hot-plug circuit.	5A/5B	GPIO1
ID_LED_GATE	Drives the chassis ID LED circuit (signal HIGH = LED ON).	5A/5B	GPIO0
CPU_3.3VSTDBY_GD	Indicates the state of the processor 3.3VSTDBY power good signal.	5A/5B	AIN4
MIDP_ID(2)*	Midplane ID bit 2.	5A/5B	AIN2

Signal	Function	I²C Port	Pin Name
MIDP_ID(1)*	Midplane ID bit 1.	5A/5B	AIN1
MIDP_ID(0)*	Midplane ID bit 0.	5A/5B	AIN0

* Midplane ID signals are used to indicate the revision of the midplane board.

4.5.11 In-System Programming Bus

The I/O board contains four PLDs. These devices are Lattice* 2064VE or 2128VE PLDs. These devices can be programmed through the server management controller on the I/O riser using the ISP bus. The ISP_ENABLE_L selects when the bus is being driven with ISP data. *Figure 4-6* shows the ISP diagram for the I/O board. *Table 4-29* lists the bypass resistors for the processor and SCSI backplane. Note that the ISP logic must also be disabled on the processor or SCSI backplane in order to bypass those boards properly. Zero ohm resistors are used to bypass.

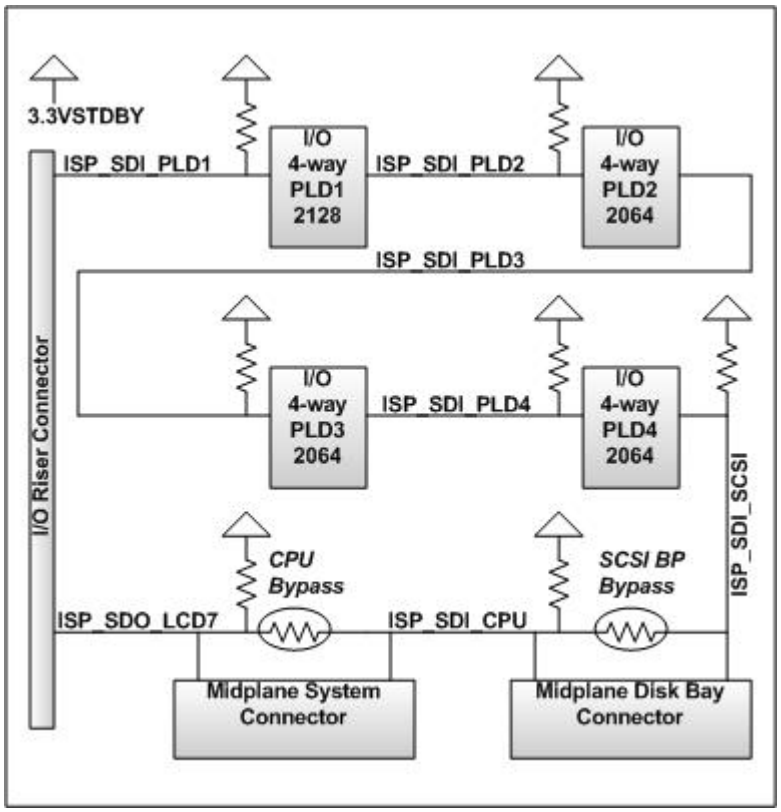


Figure 4-6. In-System Programmable Diagram

Table 4-29. ISP Bypass Resistors

Component/Board Bypassed	Resistor (populate to bypass)
Processor Board	R6J12
SCSI Backplane	R2J22

4.5.12 Power System

The I/O board is designed to operate in Server Systems Infrastructure (SSI) -distributed power architecture. In this type of system, main power is distributed over a 48-V rail. This allows for greater power to be delivered using less current and, thus, smaller power connectors into the board. The 48-V rail is converted locally to provide point-of-load power converters for 3.3 V and 5 V. This results in tighter voltage regulation and better control of power under local conditions.

In addition to the main 48-V rail, the I/O board receives additional voltages from the midplane system connector. 12VSTDBY (Standby) is provided from the system power supplies. This voltage is present at any time AC is available to the main power converters. This voltage is used to control the D2D converters and is passed to the I/O riser to generate 3.3VSTDBY and 5VSTDBY.

The I/O board also receives 12 V from the midplane system connector. This 12-V power rail is derived from the system 48-V rail on the SCSI backplane and, thus, is present only when main power is on. 12 V is used to power the PCI slots and to control some of the embedded converter circuits.

The I/O board also receives two voltages that are generated from the I/O riser. These are 5VSTDBY and 3.3VSTDBY. These voltages are used by the I/O board and are also furnished to the midplane system connector to be used by other system components.

Embedded converter circuits on the I/O board generate other required voltages locally.

Figure 4-7 shows the power distribution on the I/O board.

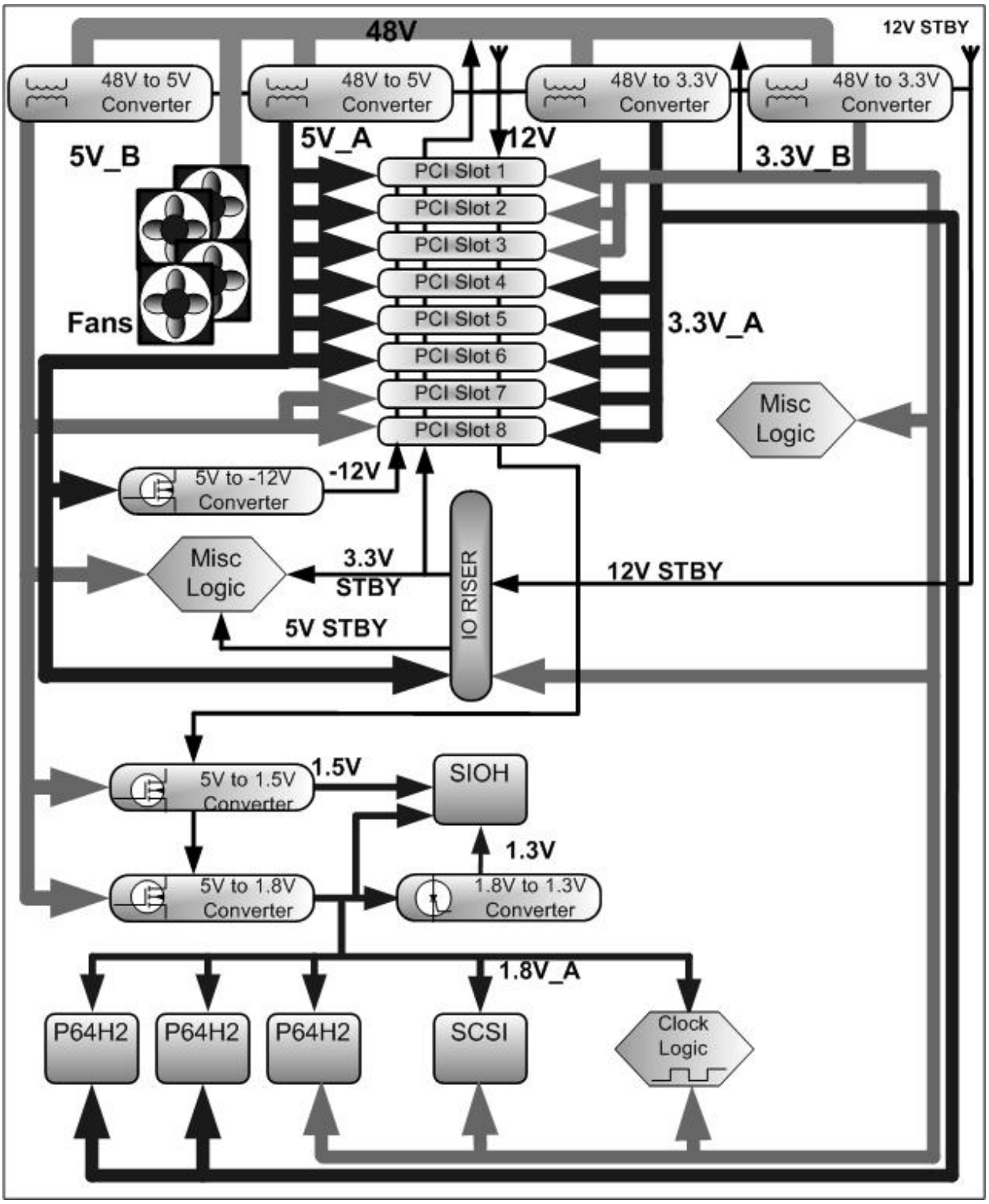


Figure 4-7. Power Distribution

4.5.12.1 3.3-V and 5-V Power

The I/O board generates 3.3 V and 5 V from the system-supplied 48-V rail. It uses two 100-W T-DC-to-DC (D2D) plug-in converters to provide the necessary power for each voltage. These converters support a current share mode such that a pair of converters can supply a common rail. However, the I/O board has separate output rails labeled 3.3V_A, 3.3V_B, 5V_A, and 5V_B. The T-D2D converters come in two variations. A 5 V-only version is used to provide the 5-V power. A Voltage Identification (VID) version is used to provide the 3.3 V. VID signals on the interface are set to a binary value that corresponds to a 3.3-V output. Note that the T-D2D version only supports two output levels: 3.3 V and 2.5 V. The AD2D version supports a full range of output levels. The value is fixed by resistor populations, tied to GND, or left open and pulled up on the converter. The 5-V and 3.3-V connectors are uniquely keyed to prevent inserting the incorrect D2D version.

The converter interface provides the control and monitoring of the converters themselves. The Enable signal allows the system to control the converters output. The Power Good signal indicates that the converters are operating under proper conditions. This signal is monitored by the reset circuitry to indicate when the board has proper power to its circuits.

Table 4-30 lists the pinout for the 5-V D2D converter.

Table 4-31 lists the pinout for the VID D2D converter.

Table 4-30. 5-V T-D2D Connector Pinout

Signal	Pin	Pin	Signal
48V	1	70	48V_RTN
48V	2	69	48V_RTN
48V	3	68	48V_RTN
NC	4	67	NC
(KEY PIN)	5	66	12V
NC	6	65	NC
OK	7	64	PRESENT_L
NC	8	63	NC
NC	9	62	NC
NC	10	61	NC
NC	11	60	SHARE
PWRGD	12	59	OUTEN
NC	13	58	NC
NC	14	57	NC
SENSE_N	15	56	SENSE_P
GND	16	55	GND
GND	17	54	GND
+5V	18	53	+5V
+5V	19	52	+5V
GND	20	51	GND
GND	21	50	GND
+5V	22	49	+5V

Signal	Pin	Pin	Signal
+5V	23	48	+5V
GND	24	47	GND
GND	25	46	GND
+5V	26	45	+5V
+5V	27	44	+5V
GND	28	43	GND
GND	29	42	GND
+5V	30	41	+5V
+5V	31	40	+5V
GND	32	39	GND
GND	33	38	GND
+5V	34	37	+5V
+5V	35	36	+5V

Table 4-31. VID T-D2D Connector Pinout

Signal	Pin	Pin	Signal
48V	1	70	48V_RTN
48V	2	69	48V_RTN
48V	3	68	48V_RTN
(KEY PIN)	4	67	NC
NC	5	66	12V
NC	6	65	NC
OK	7	64	PRESENT_L
NC	8	63	VID4
VID3	9	62	VID2
VID1	10	61	VID0
NC	11	60	SHARE
PWRGD	12	59	OUTEN
NC	13	58	NC
NC	14	57	NC
SENSE_N	15	56	SENSE_P
GND	16	55	GND
GND	17	54	GND
+3.3V	18	53	+3.3V
+3.3V	19	52	+3.3V
GND	20	51	GND
GND	21	50	GND
+3.3V	22	49	+3.3V
+3.3V	23	48	+3.3V
GND	24	47	GND
GND	25	46	GND
+3.3V	26	45	+3.3V
+3.3V	27	44	+3.3V
GND	28	43	GND
GND	29	42	GND
+3.3V	30	41	+3.3V
+3.3V	31	40	+3.3V
GND	32	39	GND
GND	33	38	GND
+3.3V	34	37	+3.3V
+3.3V	35	36	+3.3V

The I/O board contains individual fault identification LEDs for each of the D2Ds. These are controlled by the error PLD. The PLDs will latch the LED if the D2D is present and enabled but does not return its PWRGD signal. The LEDs will stay ON even when main power is removed. It is reset if standby power is removed or if main power is re-applied and the fault has been removed. *Table 4-32* lists the D2D locations and their associated fault LEDs.

Table 4-32. D2D Fault LEDs

D2D	Voltage Rail	LED
D2D1-J1C1	5V_A	DS1D2
D2D2-J1F1	5V_B	DS1D3
D2D3-J2C1	3.3V_A	DS1D1
D2D4-J2F3	3.3V_B	DS1D4

4.5.12.2 1.3 V, 1.5 V, and 1.8 V Power

1.3 V, 1.5 V, and 1.8 V power is generated locally on the I/O board for use by internal circuits. Both buck switching and linear power circuits are used. The following table lists the power circuits and loads.

Table 4-33. 1.3 V, 1.5 V, 1.8 V, -12 V Converter Specifications

Converter	E in	E out	I out*	Maximum I out	Margin Range	di/dt	DC Tol.	Maximum Deviation (DC + AC)	Type
1.3 V SP	1.8 V	1.3 V	2 A	2 A	±5 % to 10 %	20 A/uS	± 1.5 %	± 5 %	Linear
1.5 V SIOH Core	5 V	1.5 V	11.6 A	12.5 A	±5 % to 10 %	20 A/uS	± 1.5 %	± 5 %	Buck
1.8 V P64H2 Core	5 V	1.8 V	7 A	8.5 A	±5 % to 10 %	20 A/uS	± 1.5 %	± 5 %	Buck
-12 V	5 V	-12 V	2.6 A	3 A	±5 % to 10 %	2 A/uS	± 3 %	± 5 %	Maxim

Note: *Indicates converter circuit source capability (not load).

The buck circuits are based on a TPS5211 (Happy Valley*) controller. The linear circuit is based on an EZ1581* linear regulator.

4.5.12.3 Input Power Requirements

Table 4-34 lists the power requirements for voltage rails sourced by the I/O board. Note that the I/O board sources and supplies power on some voltage rails (e.g., +12VSTDBY is sourced by the I/O board from the midplane and then supplied to the I/O riser). Power requirements for these boards are shown here for reference only and are subject to change without notice in this specification. Please refer to the latest specification for these boards for their power

requirements. Also see *Table 4-5* and *Table 4-20* for current ratings on the midplane and I/O riser connectors.

Table 4-34. Input Power Requirements

Voltage Rail	Source	I/O Power Only	External Power Supplied from I/O		Total Power
			Board	Power	
+48V	Midplane (Power Supply)	320 Watts	None	none	320 Watts
+12VSTDBY	Midplane (Power Supply)	5 Watts	I/O riser	23 Watts	28 Watts
+12V	Midplane (SCSI Backplane)	26 Watts	None	none	26 Watts
+3.3VSTDBY	I/O riser	7.5 Watts	CPU and Front Panel	2.5 Watts	10 Watts
+5VSTDBY	I/O riser	.5 Watt	SCSI Backplane	.75 Watt	1.25 Watt

4.5.12.4 PCI 3.3 V and 5 V Power Restrictions

The PCI slots are powered from both the 5 V and 3.3 V rails. Each slot can support the PCI maximum power allotment of 25 watts. However, there are limits to the overall power that all PCI slots can draw, due to the maximum power available from the D2D converters (i.e., every slot cannot draw the maximum power). Also, since the PCI slots receive their power from different converters, there are limits within the group of slots belonging to a particular converter rail. *Table 4-35* lists the PCI slot groupings, the total power per group and the average power per slot.

Table 4-35. PCI 3.3 V and 5 V Power Restrictions

Group	Slots in Group	Total Power for Group	Average Power per Slot
5V_A	SLOT 1-6	75 Watts	15 Watts
5V_B	SLOT 7-8	60 Watts	20 Watts
3.3V_A	SLOT 4-8	90 Watts	18 Watts
3.3V_B	SLOT 1-3	54 Watts	18 Watts

4.5.12.5 Power Sequence

The T-D2D's and the Happy Valley converters each contain enable and power good signals that allow for precise control of power sequencing. The Reset PLD, in addition to the sequencing clock enables and reset signals, controls this sequence. The linear converters power up upon receiving the proper input voltage.

The power-up sequence is shown in *Figure 4-8* and *Figure 4-9*. This sequence shows the activity that starts with system power-on as initiated by the server management controller or the front panel power switch. This sequence concludes with power rail up, clocks running, and power-on reset still active. Refer to *Figure 4-12* for information on release of power-on reset.

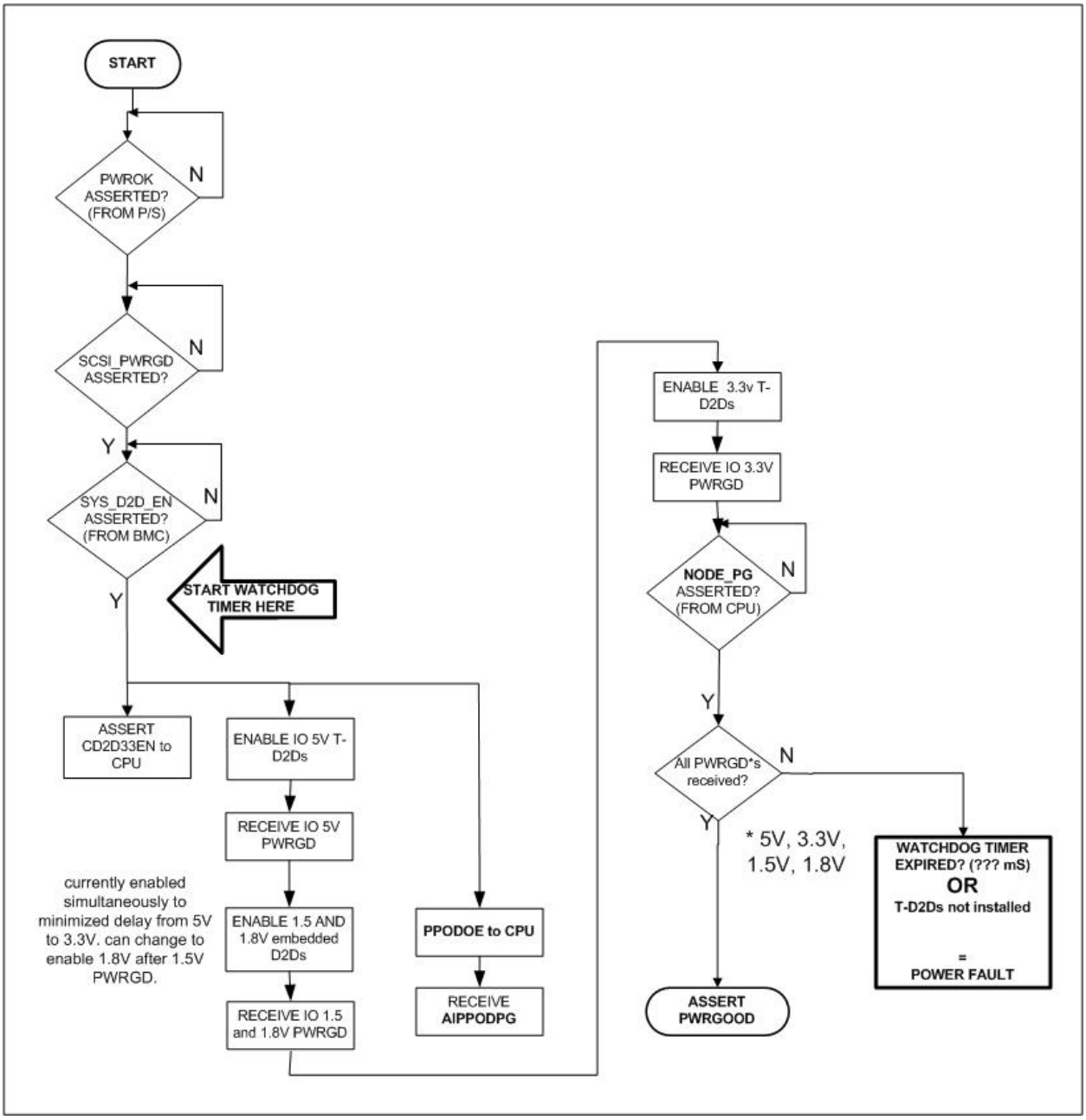


Figure 4-8. Power Sequence Flow

Power sequence timing is shown in *Figure 4-9*.

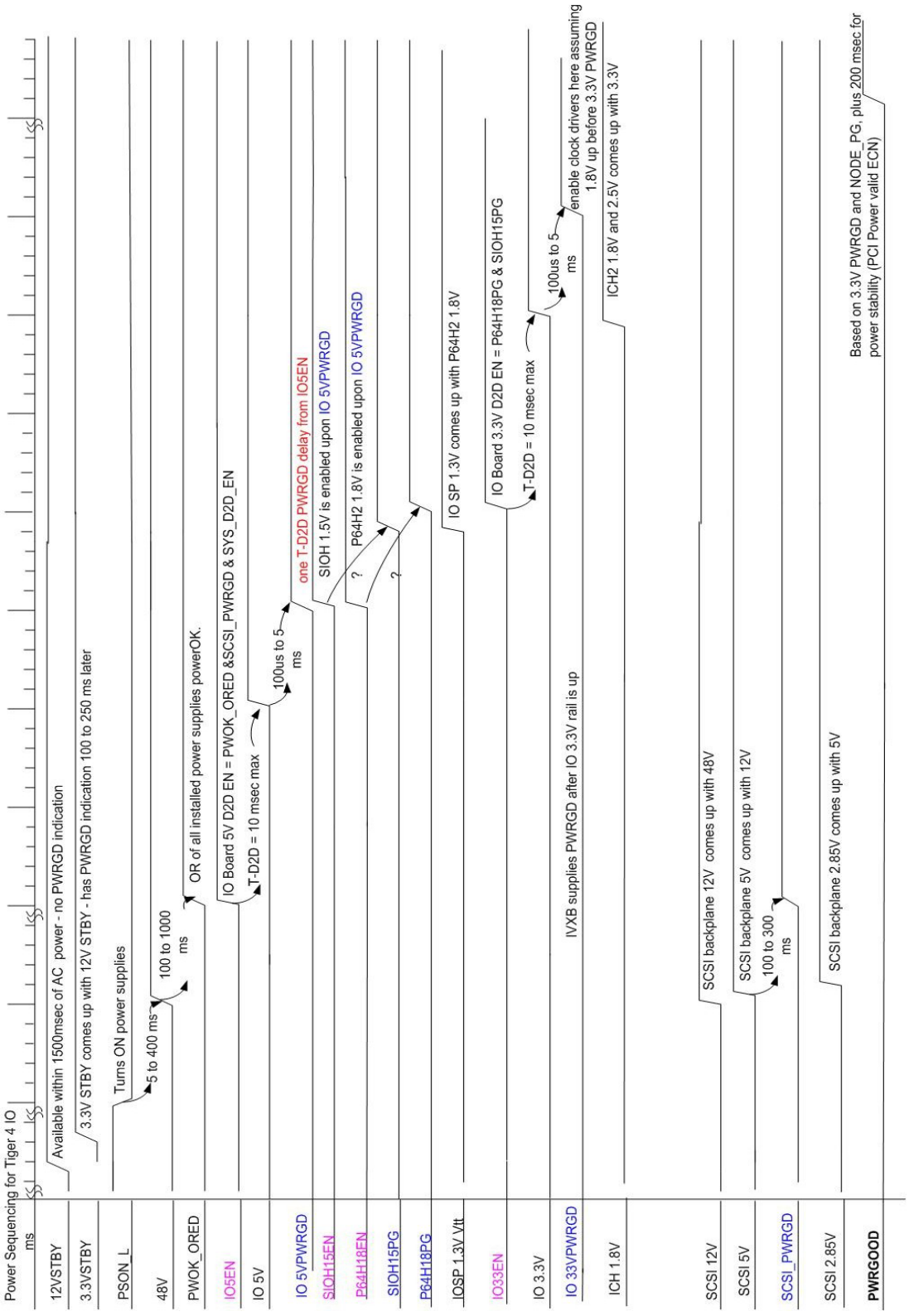


Figure 4-9. Power Sequence Timing

4.5.13 Clock Generation Logic

The I/O board contains the main clock generation circuits used by major system components. See *Figure 4-10* for a diagram of the clock generation logic.

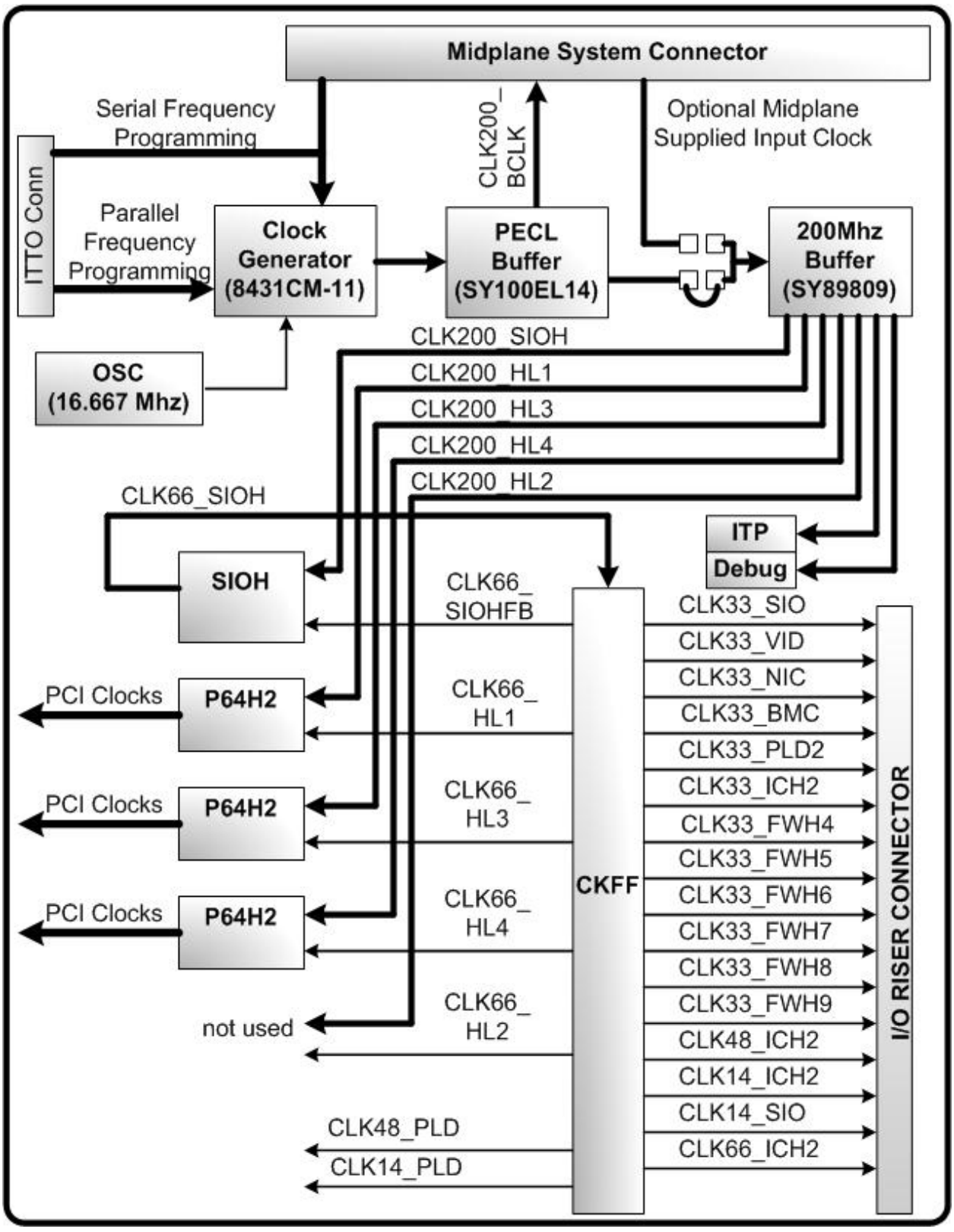


Figure 4-10. Clock Block Diagram

4.5.13.1 200-MHz Clock Generation and Distribution

The main system clocks operate at 200 MHz. These are generated from a CK429S frequency synthesizer, and buffered through a 100EL14 clock distribution chip. The 100EL14 provides two copies of LVPECL level clocks. One is used on the I/O board to drive a SY89809 HSTL clock buffer. The other is sent to the midplane system connector for use by other system components.

The CK429S synthesizer uses a 16.667-MHz crystal to provide a reference frequency.

Two pins command the CK429S to enter one of four operational modes: spread spectrum, non-spread, and two test modes. This control interface is through a Power Up Latch (PUL) register feature. The register may be written by the Spread Spectrum Clocking (SSC) CTL [1:0] pins when power is applied to the part. The register becomes disabled sometime after power is applied. Only by removing all power can initial programmed values be overwritten.

SSC is a feature of this component. In SSC mode, the main output is modulated at 30 kHz to reduce Electro-Magnetic Interference (EMI) noise. In Diagnostic mode, the Voltage-Controlled Oscillator (VCO) is disabled and a signal from an external source may be connected to the TEST_IO pin on the part. This is useful for manufacturing in-circuit testing and allows a way to toggle outputs at a lower frequency throughout the system clock tree.

Table 4-36. CK429S Operational Mode

COMMANDS					OPERATIONAL MODES
SSC_CTL [1:0] [1]	VCO	SSC	FOUT, /FOUT	TEST_IO	
0 0	—	—	—	OUTPUT	Reserved
0 1	Run	Run	200 MHz	HI-Z	Default SSC; Modulation Factor = ½ Percent
1 0	Stop	Stop	TEST_IO	INPUT	Diagnostic Mode, (1 MHz ≤ TEST_IO ≤ 200 MHz)
1 1	Run	Stop	200 MHz	HI-Z	No SSC Modulation

4.5.13.2 200-MHz Positive Emitter Coupled Logic (PECL) Clocks

A SY100EL14V Positive Emitter Coupled Logic (PECL) driver provides the clock source to the processor/memory module through the midplane system connector and to the I/O board's Low Voltage High Speed Transceiver Logic (LVHSTL) buffer. No timing skew is guaranteed between the two outputs.

4.5.13.3 200-MHz LVHSTL Clocks

A SY89809L clock buffer is used to convert the 200-MHz LVPECL distribution clock into six copies of LVHSTL differential clocks that are used by the I/O board's 870 chip set components. Specifically, one copy is used by the SIOH, and three copies are used by the three P64H2's. One copy is used for the ITP interface. See the *SY89809 Specification* for more details of this buffer.

4.5.13.4 CKFF

An ICS* 9250BG-24 (CKFF) or equivalent clock generation chip is used to provide various additional clocks. A 14.31818 MHz oscillator is used to provide the 14.318 MHz outputs and the 48 MHz outputs. The 66-MHz clock output from the SIOH is used to create the 66 MHz and the 33 MHz outputs. The 66 MHz outputs are buffered only, and the 33 MHz outputs are divided by two and lag the 66-MHz clocks by typically 2.5ns, as required by the ICH2. *Table 4-37* shows the clocks and target devices driven from the CKFF.

Table 4-37. CKFF Clocks and Target Devices

Frequency	Board	Signal Name	Target Devices
66 MHz	I/O board	CLK66_SIOHFB	SIOH (feedback clock)
66 MHz	I/O board	CLK66_HL1	P64H2 AB
66 MHz	I/O board	CLK66_HL2	not used
66 MHz	I/O board	CLK66_HL3	P64H2 CD
66 MHz	I/O board	CLK66_HL4	P64H2 EF
66 MHz	I/O riser	CLK66_ICH2	I/O riser's ICH4
33 MHz	I/O riser	CLK33_SIO	I/O riser's super I/O chip
33 MHz	I/O riser	CLK33_VID	I/O riser's video chip
33 MHz	I/O riser	CLK33_NIC	I/O riser's network interface controller
33 MHz	I/O riser	CLK33_BMC	I/O riser's server management controller
33 MHz	I/O riser	CLK33_PLD2	I/O riser's PLD2
33 MHz	I/O riser	CLK33_ICH2	I/O riser's ICH4
33 MHz	I/O riser	CLK33_FWH4	I/O riser's firmware hubs 4
33 MHz	I/O riser	CLK33_FWH5	I/O riser's firmware hubs 5
33 MHz	I/O riser	CLK33_FWH6	I/O riser's firmware hubs 6
33 MHz	I/O riser	CLK33_FWH7	I/O riser's firmware hubs 7
33 MHz	I/O riser	CLK33_FWH8	I/O riser's firmware hubs 7 and 8
33 MHz	I/O riser	CLK33_FWH9	I/O riser's firmware hubs 7 and 8
48 MHz	I/O board	CLK48_PLD	I/O board's PLD2
48 MHz	I/O riser	CLK48_ICH2	I/O riser's ICH4
14.318 MHz	I/O board	CLK14_PLD	I/O board's PLD1
14.318 MHz	I/O riser	CLK14_ICH2	I/O riser's ICH4
14.318 MHz	I/O riser	CLK14_SIO	I/O riser's super I/O chip

4.5.13.5 PCI Clocks

The P64H2 provides the clocks that drive the PCI slots and the embedded SCSI device's PCI interface. The P64H2 can provide clock speeds of 33 MHz, 66 MHz, 100 MHz, or 133 MHz based upon the particular PCI bus segment requirements. The P64H2 provides a separate clock driver per slot or device. However, the 100-MHz buses 'gang' the outputs (electrically connected together) in order to reduce the pin-to-pin skew to virtually zero. Separate termination resistors are used per clock load. Also, separate hot-plug FETs are used to control the clocks during hot-plug operation. These are included on all clocks, even if hot-plug switching is not required, in order to equally balance the clock topology. The 133 MHz use separate clock outputs and series termination resistors since the P64H2 controls the clock during hot-plug operation. See the *P64H2 Specification* for more details on the PCI clock generation circuits.

4.5.14 Reset Generation Logic

The I/O board provides the central reset control for the system. Most of the reset control is provided through a Lattice* 2128VE PLD.

Figure 4-11 depicts the reset circuitry for the Server System SR870BN4.

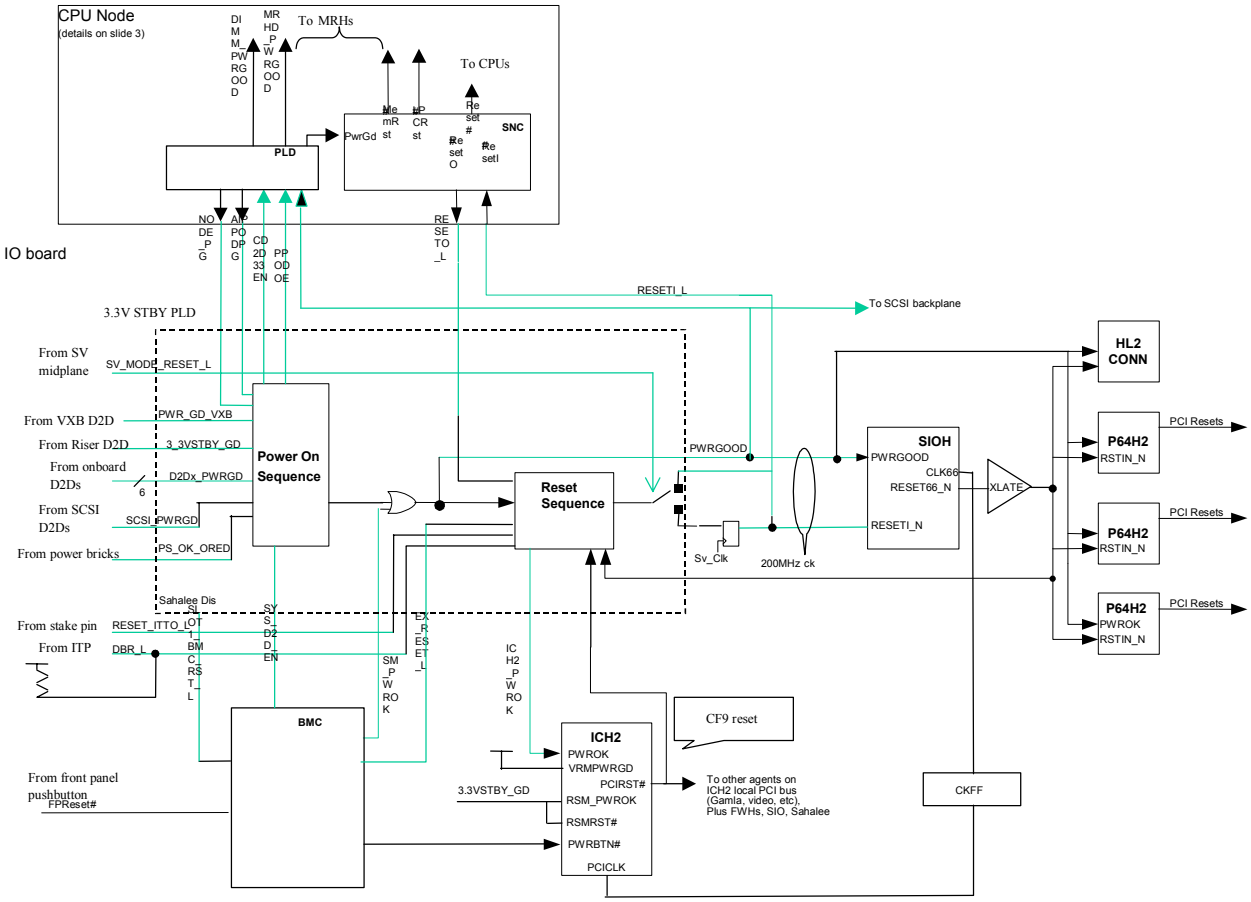


Figure 4-11. System Reset Block Diagram

Figure 4-12 shows the sequence of events that occurs during reset.

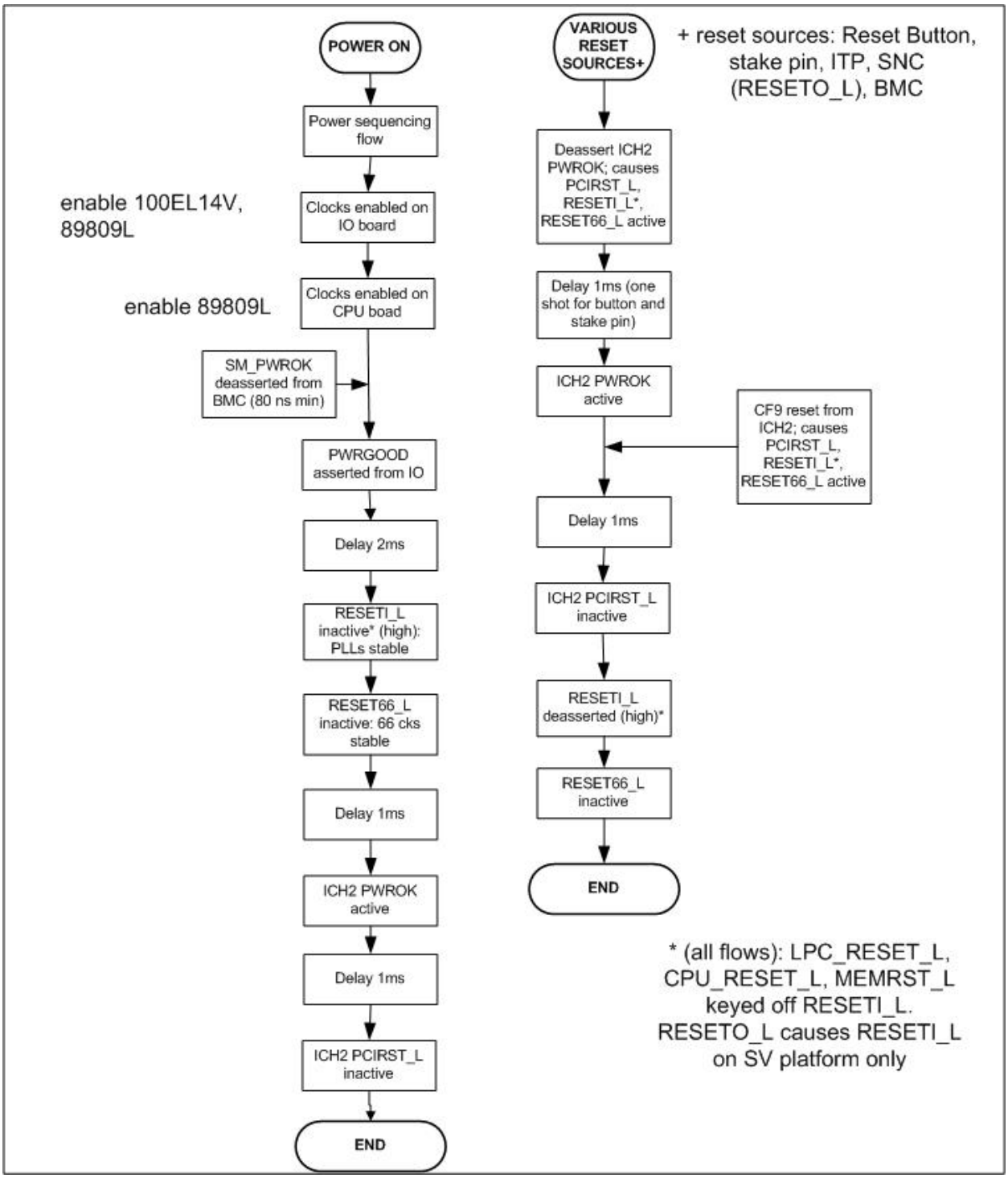


Figure 4-12. Reset Flow

Figure 4-13 shows the approximate timing of the events, which occur during a reset.

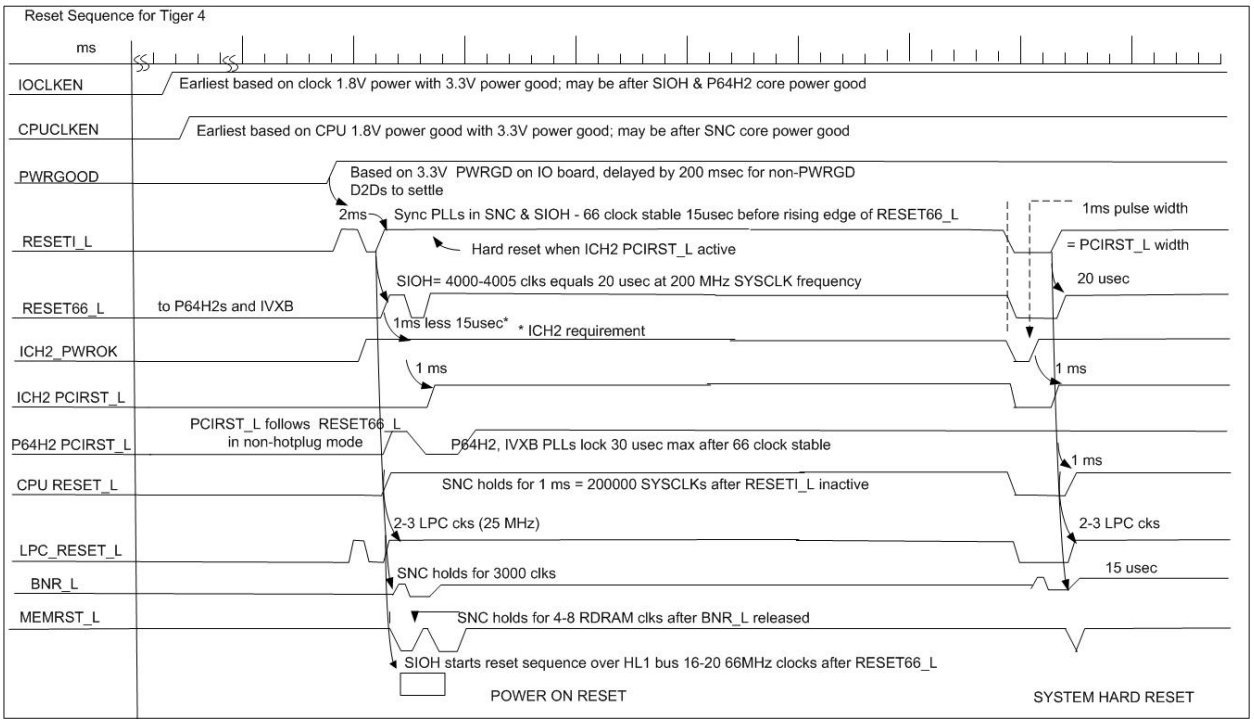


Figure 4-13. Reset Timing

4.5.15 Interrupts and Errors

The I/O board contains routing and logic that is part of the overall interrupt and error structure of the Server Board SR870BN4 board set. Interrupts and errors from the processor/memory module, PCI subsystem, and I/O board chip set are routed through logic on the I/O board and connected to the interrupt logic on the I/O riser.

The I/O board supports both message-based interrupts as well as 8259-based interrupts. Message-based interrupts can be routed directly through the PCI controller as well as through the I/O APIC logic on the I/O riser.

See the *Intel® Server System SR870BN4 External Architecture Specification* for more information on the system-wide interrupt and error logic.

4.5.15.1 PCI Interrupts

The I/O board contains the interrupt interface for the PCI subsystem. Two types of interrupt delivery are supported. The standard PCI interrupt signals (INTA-INTD) or Message Signaled Interrupts (MSI). In either case, the P64H2's route the interrupts to the processors via interrupt messages through the HL2, or optionally through the boot interrupt signals to the I/O riser during boot. *Table 4-38* lists the PCI IRQ mapping.

Table 4-38. IRQ Mapping

Slot/IRQ	P64H2-AB		Slot/IRQ	P64H2-CD		Slot/IRQ	P64H2-EF
Slot 1-IRQ A	PAIRQ0		Slot 4-IRQ A	PAIRQ0		Slot 7-IRQ A	PAIRQ0
Slot 1-IRQ B	PAIRQ1		Slot 4-IRQ B	PAIRQ1		Slot 7-IRQ B	PAIRQ1
Slot 1-IRQ C	PAIRQ2		Slot 4-IRQ C	PAIRQ2		Slot 7-IRQ C	PAIRQ2
Slot 1-IRQ D	PAIRQ3		Slot 4-IRQ D	PAIRQ3		Slot 7-IRQ D	PAIRQ3
SCSI A	PAIRQ4		Slot 5-IRQ A	PAIRQ4		Slot 8-IRQ A	PBIRQ0
SCSI B	PAIRQ5		Slot 5-IRQ B	PAIRQ5		Slot 8-IRQ B	PBIRQ1
Slot 2-IRQ A	PBIRQ0		Slot 5-IRQ C	PAIRQ6		Slot 8-IRQ C	PBIRQ2
Slot 2-IRQ B	PBIRQ1		Slot 5-IRQ D	PAIRQ2		Slot 8-IRQ D	PBIRQ3
Slot 2-IRQ C	PBIRQ2		Slot 6-IRQ A	PBIRQ0			
Slot 2-IRQ D	PBIRQ3		Slot 6-IRQ B	PBIRQ1			
Slot 3-IRQ A	PBIRQ4		Slot 6-IRQ C	PBIRQ2			
Slot 3-IRQ B	PBIRQ5		Slot 6-IRQ D	PBIRQ3			
Slot 3-IRQ C	PBIRQ6						
Slot 3-IRQ D	PBIRQ7						

Note: PAIRQ7 for each P64H2 is used for the HPC_INTR_L (hot-plug interrupt) signal.

4.5.15.2 System Interrupts

In addition to the PCI interrupts, the I/O board also generates and routes several other interrupts. They include the following:

Hot-Plug Interrupt: The signal *HP_INT_L* is generated from the processor/memory module when the hot-plug switch is pressed. This is to indicate a request to hot plug the processor/memory module. The signal is debounced and sent to the server management sub system and the interrupt logic. Note that since the four-way I/O board only supports a single processor/memory module, hot plugging the module is not part of the normal system operation.

Int_Out: The SIOH and SNC INT_OUT_L signals are asserted for scalability port hot plug and performance events. The *INT_OUT_L* signal from the SNC is translated to 3.3 V level before crossing the midplane. It is gated with the *INT_OUT_SIOH_L* signal from the SIOH before being sent to the I/O riser.

BINITIN_L: The *BINITIN_L* signal is sent to the SNC to generate the BINIT_L signal to the processor.

BERRIN_L: The *BERRIN_L* signal is sent to the SNC to indicate a non-correctable error to the SNC. Also, a copy of the signal, *SNC_BERRIN_L*, is sent to the I/O riser interrupt logic.

Figure 4-14 shows the connectivity of the interrupts from the midplane interfaces, PCI sub-system, and I/O board chip set.

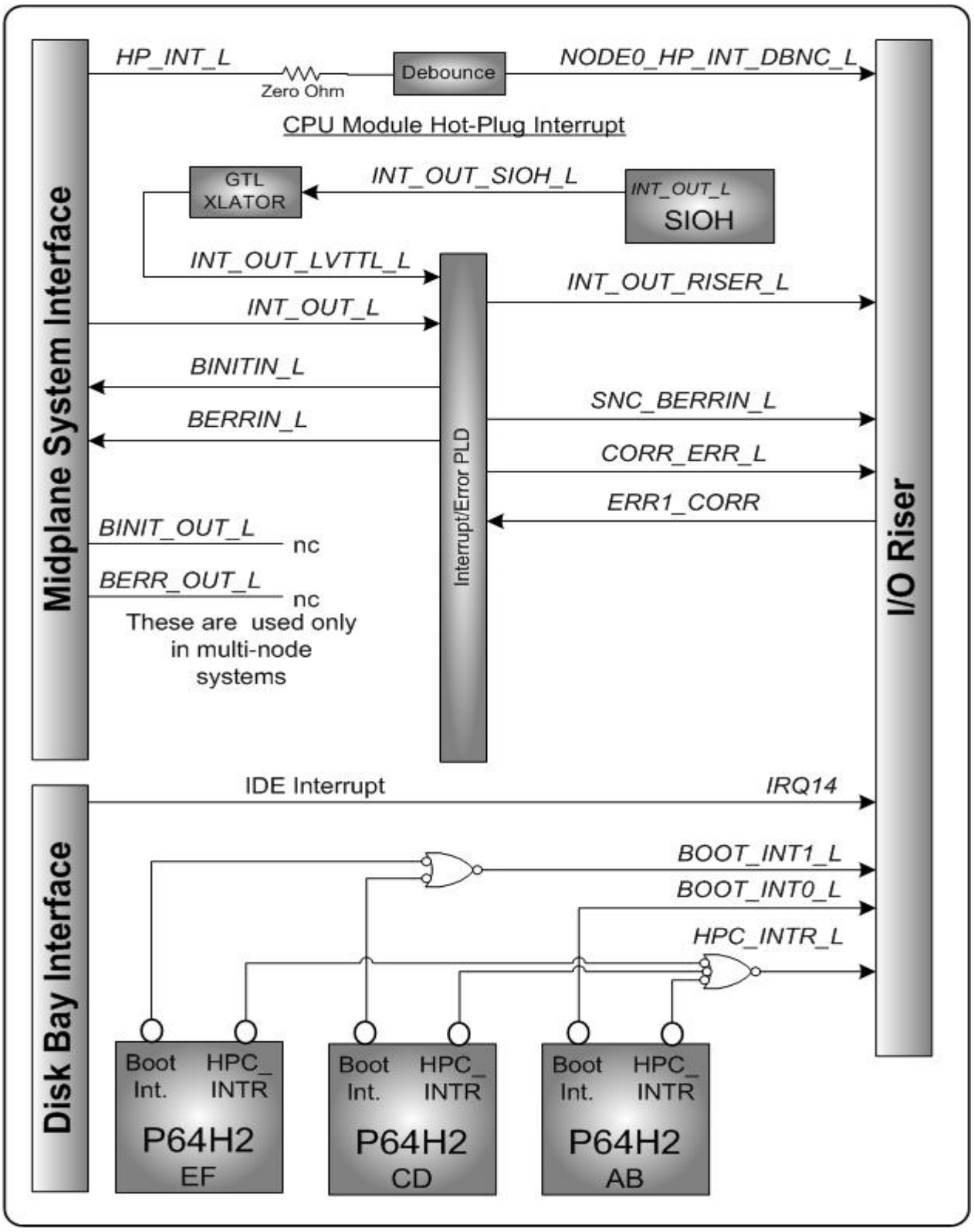


Figure 4-14. Interrupt Block Diagram

4.5.16 Error Handling Logic

The I/O board contains error-handling logic that controls both correctable and non-correctable errors from the 870 chip set. The signal ERR_L(0) (wire-or'ed from the SNC and SIOH) represents correctable errors from the chip set. It generates the CORR_ERR_L signal, which is driven to the I/O riser IOAPIC logic. The signal ERR_L(2) (wire-or'ed from the SNC and SIOH) represents non-correctable errors from the chip set. It is gated with the ICH SERR signal to generate the SNC_BERRIN_L, which is driven to the I/O riser IOAPIC logic. The SIOH/SNC ERR1 signal can be routed to either the CORR_ERR_L or to the SNC_BERRIN_L signal, as determined by the setting of the I/O signal ERR1_CORR from the I/O riser.

The gating logic is contained in the interrupt/error PLD. *Figure 4-15* shows the error diagram for the I/O board.

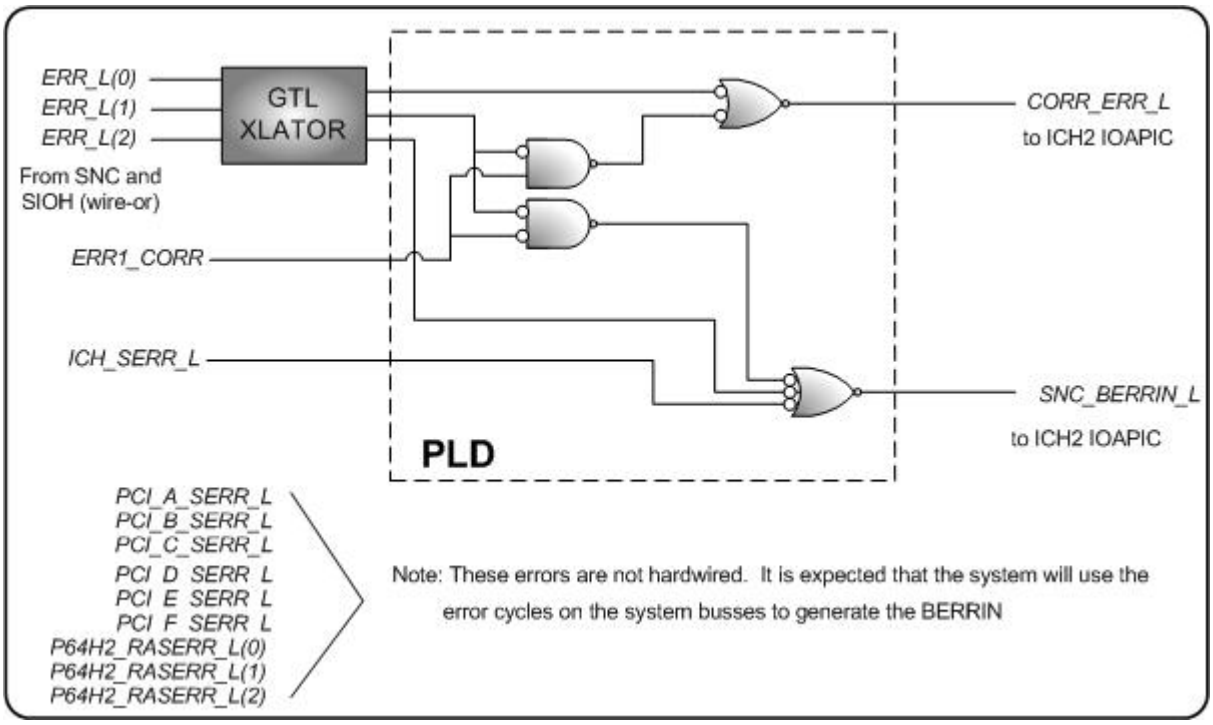


Figure 4-15. Error Handling Logic Diagram

4.5.17 Front Panel Interface

The I/O board interfaces to the system front panel board through signals that pass through the midplane system connector. *Table 4-39* lists the signals and functions associated with the front panel.

Table 4-39. Front Panel Interface

Signal Name	Function
ON_LED_L	Main power indication
COOL_FLT_LED_L	Cooling system failure indication
POWER_FLT_LED_L	Power system fault indication
GEN_FLT_LED_L	General system fault indication
FP_LED_L	Chassis identification indication
SPEAKER	Speaker control signal
CHASS_ID_L	Chassis identification switch from front panel
POWER_SW_L	Main system power switch
RESET_SW_L	Main system rest switch
SDINT_SW_L	Main system interrupt switch

4.5.18 Internal Power-On Connector

The I/O board has a connector that allows the POWER_SW_L signal to be driven active by an internal adapter board (typically a server management board). Activating this signal will cause the system to execute a power cycle, the same as if the front panel power switch is activated. The signal must be driven to ground only when a power cycle is needed. It should be left open at all other times.

Table 4-40. Internal Power-On Connector Pinout (J9E1)

SIGNAL	PIN#
GND	1
POWER_SW_L	2
GND	3
nc	4

4.5.19 Manufacturing Mode

The I/O board contains a manufacturing mode connector site that manufacturing can use to select special BIOS routines that improve manufacturing test time. The connector site is located at J1J1. Installing the special manufacturing mode connector will signal the I/O riser to go into manufacturing mode. The connector can be installed from the top or bottom.

4.5.20 ICMB/IPMB Connectors

The I/O board supports both an external ICMB and an internal IPMB connector. Both are used for server management functions in the system. There are three ICMB channels. The ICMB channel is the principal ICMB communication port. The ICMB ID1 and ICMB_ID2 channels provide the chassis identification functions. The ICMB connector cables to a chassis bulkhead connector board that supports the standard ICMB connector receptacles. *Table 4-41* and *Table 4-42* show the pinouts of the two connectors.

Table 4-41. ICMB Connector Pinout (J9C1)

SIGNAL	PIN#	PIN#	SIGNAL
GND	1	2	(key)
ICMB_A	3	4	ICMB_B
GND	5	6	ICMB_ID1_A
ICMB_ID1_B	7	8	GND
ICMB_ID2_B	9	10	ICMB_ID2_A

Table 4-42. IPMB Connector Pinout (J9D1)

SIGNAL	PIN#
I2C_IPMB_SDA	1
GND	2
I2C_IPMB_SCL	3

4.5.21 Board Revision ID

The I/O board can set a revision ID that is readable by BIOS to indicate significant changes in the hardware design that BIOS may need to account for in its routines. The ID is set by resistor populations and is read from the I/O riser. See the I/O Riser chapter for details on reading the bit settings. *Table 4-43* lists the resistor populations to set the board revision ID. Zero ohm resistors are used when populating.

Table 4-43. Board Revision ID

Revision	R2B10	R2B9	R2B11
0	Populate	Populate	Populate
1	Populate	Populate	De-Populate
2	Populate	De-Populate	Populate
3	Populate	De-Populate	De-Populate
4	De-Populate	Populate	Populate
5	De-Populate	Populate	De-Populate
6	De-Populate	De-Populate	Populate
7	De-Populate	De-Populate	De-Populate

4.5.22 General Board Thermal Specifications

The general temperature limits for the board are shown in the following table. Refer to the following section for specific cooling requirements for the components on the board. Individual component specifications may be more stringent than the general board thermal specifications.

Table 4-44. General Board Thermal Specifications

Parameter	Condition	Minimum	Maximum
Temperature	Operating	0 °C	55 °C
	Non-operating	-40 °C	70 °C
Air Velocity	Operating	0.75 m/s (150 lfm)	NA

4.5.23 I/O Board Thermal Requirements

Components requiring forced convection cooling are shown in the following table. Refer to the reference documents for specific temperature and airflow requirements. Careful attention to specifications and reference documents will ensure that cooling requirements for these components can be met. Maximum board operating temperatures are dependent on system layout and airflow. Board components not listed in the table will be adequately cooled if the cooling requirements for the listed components are met.

Table 4-45. Critical I/O Board Components

Component		Specifications[1]		Reference Document	Heat Sink
Chip set	SIOH	$T_{Junction}$	105 °C	Intel® 870 EMTS	Intel Enabled
	P64H2	$T_{Junction}$	105 °C	P64H2 TAN	None
	SCSI	$T_{Junction}$	115 °C	53C1030 Specification	None (assume airflow >>100LFM)
T-D2Ds		Free stream velocity and $T_{Ambient}$	150 lfm @ 45 °C, 300 lfm @ 55 °C	T-D2D Specification	Integral
PCI Adaptors		Various		PCI Adaptor Specification	NA

4.5.24 EMI Reduction Features

The I/O board contains several features to reduce the electromagnetic radiation. Most high-speed signals, including the primary buses and clocks, are contained on internal layers surrounded by ground planes. The I/O board does not contain any connectors that directly extend outside of the chassis enclosure.

The main clock circuit supports a spread spectrum feature that minimizes EMI by varying the clock frequency over a small range.

The I/O board's digital ground is connected to the chassis via ground pads located on the backside of the Printed Circuit Board (PCB), around four mounting holes. Zero ohm resistors exist to select whether the mounting hole ground ring connects to the board's ground planes. *Table 4-46* shows the resistors associated with the mounting holes. Removal of the resistor disconnects the mounting hole ring from the board ground.

Table 4-46. Mounting Hole EMI Resistors

Mounting Hole	Resistor
Zone 8A	R2L1
Zone 4A	R6L1
Zone 5D	R5R1
Zone 5H	R5V1

4.5.25 Mechanical Features

The I/O board uses a combination 'hook and slot' and mounting hole method for its primary mechanical attachment to the chassis. Eight slots in the PCB accept a metal hook in the chassis tray to locate and secure the board in the chassis. Three of these can also accept a standard mounting screw. There is also a single mounting hole, only (no slot), that accepts the standard mounting screw. This allows the attachment of the board with a minimum of screws, thus improving assembly time by reducing the chance for damage from screw insertion. The board is placed on the tray, guided by plastic blocks, over the metal slots. The board is slid into the final position on the tray, thus locking the board under the metal hook.

One or more mounting screws are attached to fully secure the board in the chassis. The reason for the combination mounting holes/slots is to allow for additional ground connections to the chassis to improve EMI. The system engineer can trade off for EMI or a reduction in the number of screws required, by selecting 'hook and slot' or mounting screws for these attach points.

The midplane system (VHDM) connector is equipped with guide blocks that accept guide pins located on the midplane system connector assembly. This provides the final locating feature before the midplane connectors are mated.

4.5.25.1 Board Outline and Key Dimensions

Figure 4-16 shows the overall board dimensions and the PCI slot spacing. Refer to the mechanical board outline drawing for the complete mechanical specifications.

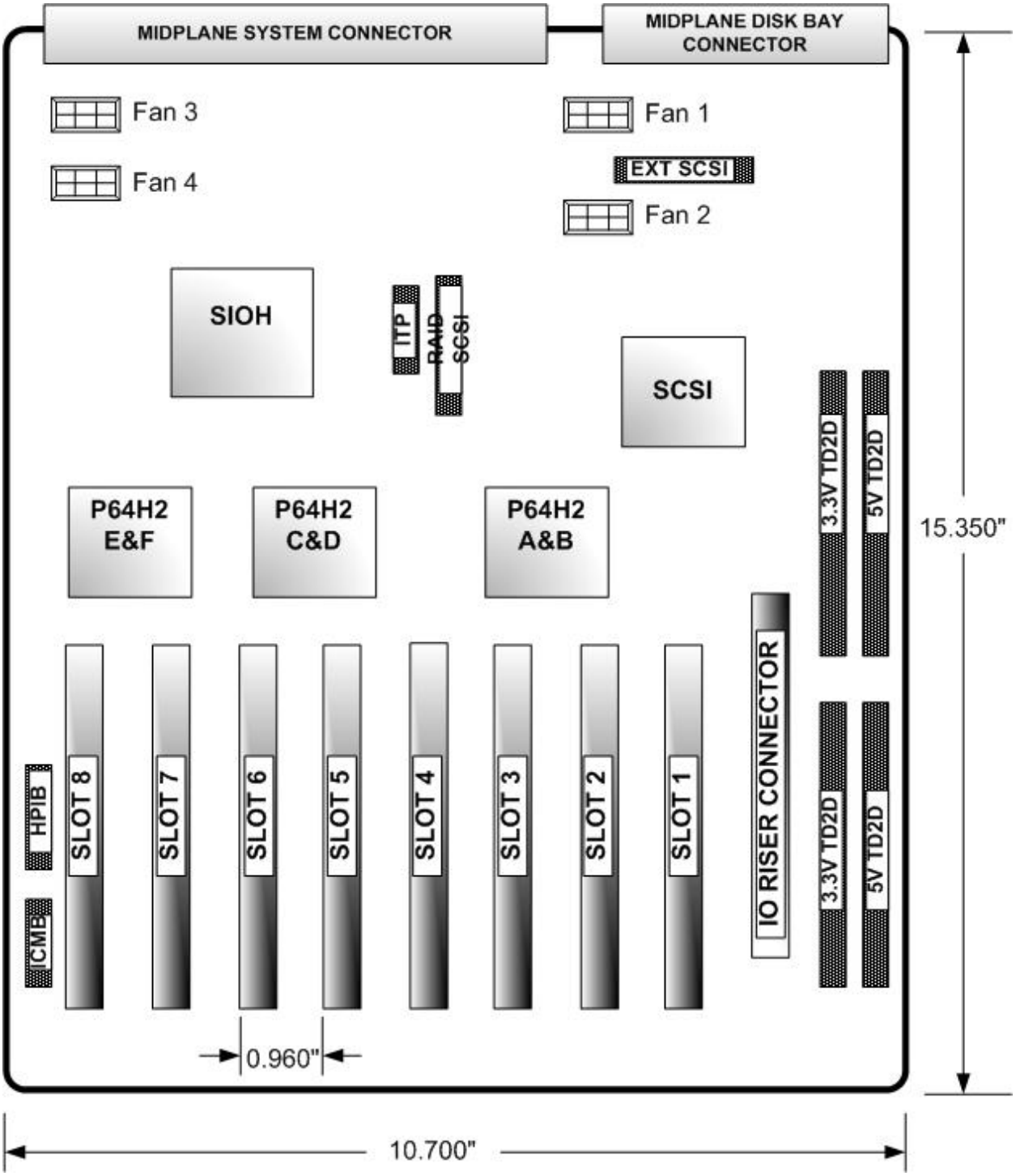


Figure 4-16. Board Outline Drawing and Key Dimensions

4.5.25.2 Weight

The I/O board weighs approximately 3 lbs, not including the PCI adapters, I/O riser, or D2D's.

4.5.26 240 VA Safety

The I/O board contains 240VA safety hazard potentials that must be shielded from user-accessible areas. These hazards exist due to the presence of the 48-V bulk supply on components, connectors, or plug-in D2D converters.

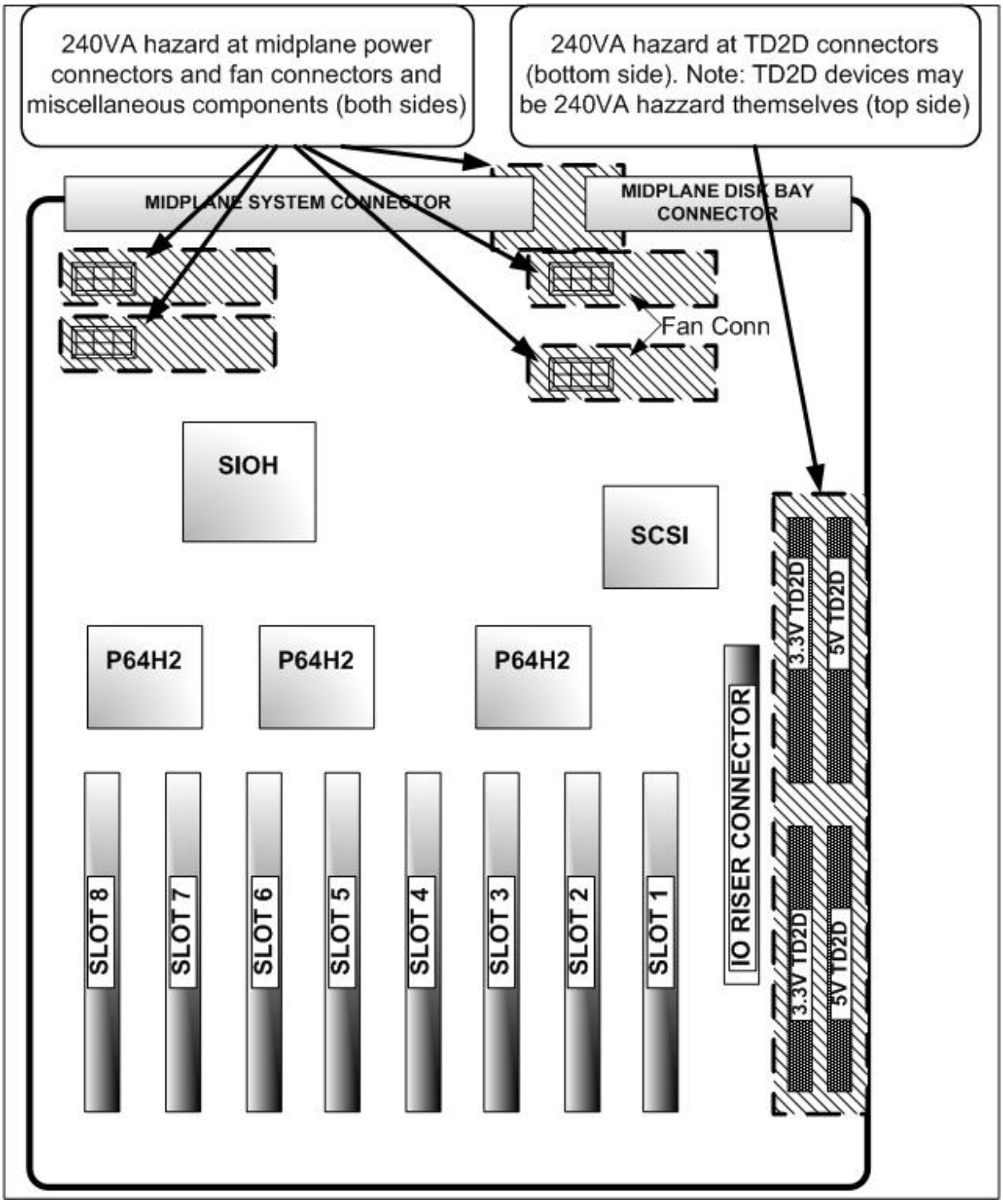


Figure 4-17. 240VA Hazard Diagram

4.5.26.1 48-V Power

The 48-V power rail exceeds the 240VA specification and must be shielded from user access. This rail is present on the midplane system connector (power blocks) and the T-D2D converters and connectors along with various miscellaneous components.

4.5.26.2 3.3-V and 5-V Power

The 3.3-V and 5-V power rails are each split into two separate regions and thus, do not exceed the 240VA hazard specification.

4.5.27 In-Target Probe (ITP)

An ITP connector is available to enable access to certain chips on the I/O board. The ITP interface is compatible with the ITP specification for the 870 chip set. *Figure 4-18* shows the diagram of the ITP connections. *Table 4-47* shows the specific connections to the ITP connector.

Table 4-47. ITP Connector Pinout

Signal Name			Signal Name
GND	1	2	GND
BMP_L(0)	3	4	DBA_L
EV_L(1)	5	6	DBR_L
EV_L(2)	7	8	GND
EV_L(3)	9	10	TDI
BMP_L(4)	11	12	TMS
EV_L(0)	13	14	TRST_L
ITP_RESETI_L	15	16	TCK
FBO	17	18	FBI
CLK200_ITP	19	20	GND
CLK200_ITP_L	21	22	PWR
EV_L(0)	23	24	TDO
GND	25	26	(KEY)

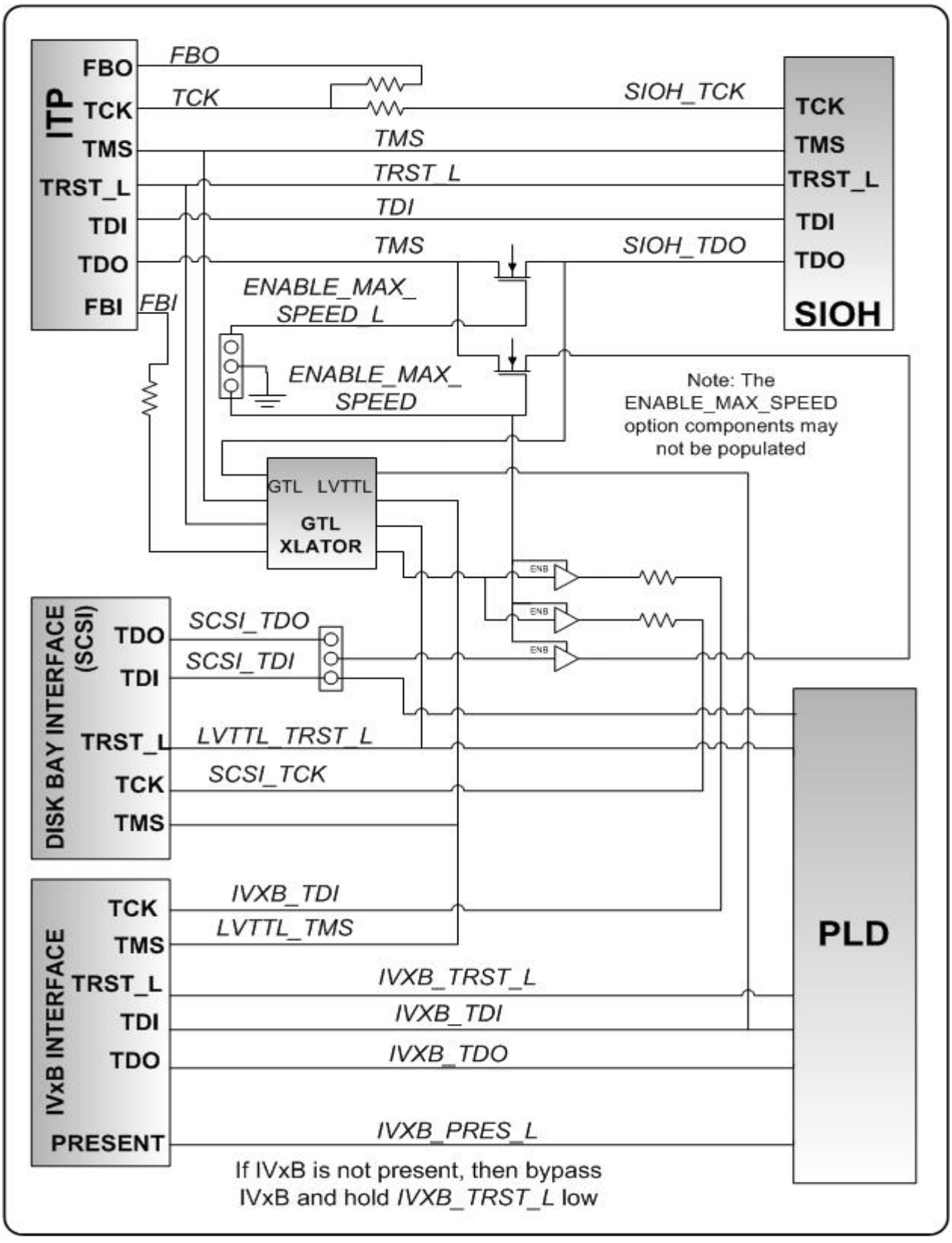


Figure 4-18. ITP Diagram

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5. I/O Riser Card

This chapter describes the architecture and specification of the Server Board S870BN4 I/O riser card which mates with the Server Board S870BN4 I/O board through a 242-pin slot one connector. The following is the function and features of the I/O riser card.

5.1 Features

The I/O riser card has the following features:

- ICH4 base controller support
  - Hublink 1.5 Interface
  - One Integrated Device Electronics (IDE) interface supporting two ATA33 devices
  - Four USB Ports
  - PCI Bus
  - LPC Bus

- Baseboard Management Controller (BMC) Server Management Chip (LPC interface)
  - Six Server Management I^2C buses including the Intelligent Platform Management Bus (IPMB)
  - Intelligent Chassis Management Bus (ICMB) access via ICMB adapter
  - Emergeny Management Port (EMP) access via shared serial port
  - Front panel switches and LED support
  - Voltage monitors

- SMC* Super I/O (LPC interface)
  - One serial port

- ATI* Rage XL video chip (PCI interface)
- Four firmware hubs (LPC interface)
- Intel® 82540EM 10/100/1000 Ethernet controller (PCI interface)

5.2 Architectural Overview

The I/O riser is a functional extension of the I/O board. The I/O riser plugs into the I/O board using a 242-pin edge finger interface into a slot-one type connector. The I/O riser card provides the Server System SR870BN4 with three main functionalities: (1) I/O interface, (2) server management, and (3) a portion of the system standby power.

The on-board ICH4 is the central Application Specific Integrated Circuit (ASIC) of the I/O riser card. The chip supports:

- Hublink 1.5 interface
- 32-bit, 33-MHz PCI Bus
- 4-bit Low Pin Count (LPC) bus

- One IDE bus[2]
- Four USB ports

An ATI video controller and Gigabit Ethernet controller are on the PCI bus behind the ICH4. They provide video and Local Area Network (LAN) for the system. A Super I/O controller resides on the LPC bus and provides the system RS232 serial port.

The BMC component connects to the ICH4 via LPC bus and is the main engine of the systems server management. The BMC supports ICMB, IPMB, and EMP ports. It also has six general I^2C buses and eight A2D pins for power monitoring. General Purpose I/Os (GPIOs) are used to support system functionality such as power up and reset sequence, front panel access, and in-system programming (ISP)/JTAG programming.

The I/O riser has two on-board standby power converters. One is the HIP6004* D2D converter, which delivers up to 6.9 Amps, 3.3-V standby power. As the system requires less than 300 mA of 5-V standby power, a TL780 regulator is used. Please refer to Section 5.11: Power/Standby Power for detailed information on the power-up sequencing required for these power converters.

[2] The ICH4 IDE bus supports up to ATA100. However, the I/O riser is only designed to support ATA33 due to the length of the cable.

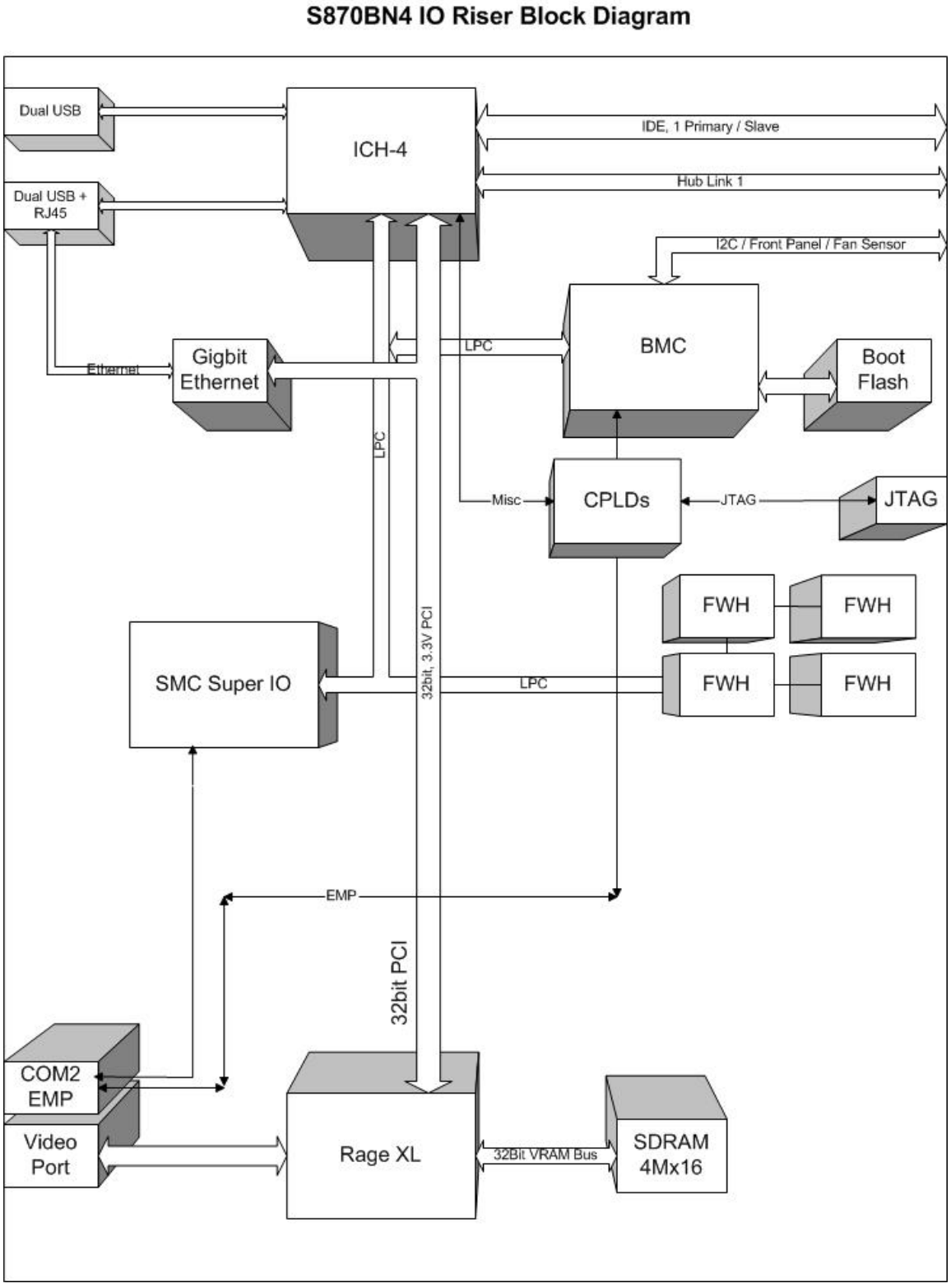


Figure 5-1. Block Diagram of the Intel® Server Board S870BN4 I/O Riser Card

5.3 Major Components

5.3.1 ICH4

The ICH4 is a 421-pin Enhanced Ball Grid Array (EBGA), Intel® 82801DA chip. It is the main I/O interface ASIC that the I/O riser uses. It is placed directly above the slot one-edge finger connector to provide the shortest trace length of its Hublink 1.5 interface. The I/O riser provides the following features:

- PCI Bus Interface
  - Supports PCI at 33 MHz, 32 bit
  - Supports PCI Specification, Revision 2.2
- Integrated IDE Controller
  - Independent timing of up to two drives
  - Ultra* ATA 33
  - Implements Write Ping-Pong Buffer for fast write performance
- USB
  - Two USB host controller with total four ports
  - USB 2.0 compliant
  - Supports wake-up from sleeping state
- Interrupt Controller
  - Supports up to eight PCI interrupt pins
  - Two cascade 82C59
  - Integrated I/O APIC capability
  - 15 interrupts supported in 8259 mode; 24 supported in I/O APIC mode
  - Support serial interrupt protocol
  - Support Front-Side bus (FSB) interrupt delivery
- 1.0-V core with 3.3-V I/O
  - 5-V tolerant buffers on IDE, PCI, USB Over Current (OC) and legacy signals
- Hublink 1.5 Interface
  - Use enhanced mode in I/O riser design
- Firmware HUB interface (mux with LPC bus pins)
  - Supports BIOS memory size up to 8 MBs
- LPC Bus
  - Allows connect of legacy chip such as Super I/O
  - Supports two master/Direct Memory Access (DMA) devices
- SM Bus
  - Supports host interface; allow delivery POST80 code
  - Supports slave interface (not used in I/O riser design)
- Real-Time Clock (RTC)
  - 256-byte battery-backed CMOS RAM
  - Hardware implementation to indicate century rollover

The following table gives a short description and design notes on each of the ICH4 signals. For detailed pin descriptions, please see the *ICH4 External Design Specification*.

Table 5-1. ICH4 Signals

Signal Group / Name	Description	Signal Routing
Hublink Interface	Hublink 1.5 Interface	Routed to I/O board with top and bottom ground reference
Integrated LAN	LAN Interface (IF) signals	No connection, not supported by I/O riser.
EEPROM IF	EEPROM for Internal LAN	EE_DOUT PD, others floating.
FWH Interface	Firmware Hub (FWH) Interface, Mux-ed with LPC Bus.	Connects to all FWH devices. Also connects to BMC and Super I/O devices.
PCI Interface	32-bit, 33-MHz PCI Bus	Video controller and 82540EM Ethernet Controller.
IDE Interface	I/O riser only supports ATA33	Primary IDE signals are routed to Slot 1 interface. The secondary IDE has no connection
LPC IF	LPC interface, mux-ed with Firmware Hub (FWH) IF. Support two Master/DMA devices	Signals are routed to FWH, Super I/O and BMC. There are total 6 devices on this bus. ICH4 has internal pull up resistor for those pins
AC 97 Link	AC 97 Link, five signals	Unused, floating, internal pull down. BIOS set AC97 Shutoff bit = 1 in AC97 Global Control Register (I/O Addr: NABMBAR + 2 Ch).
Interrupt Interface		
SERIRQ	Serial Interrupt Request	Routed to Super I/O serial IRQ.
PIRQ[H:A]	PCI Interrupt, eight lines,	Pull up via 10 K Res, for detail Peripheral Interrupt Request (PIRQ) mapping, see Section 5.9: IRQ and Bus Master.
IRQ[14]	Legacy IRQ, one line	IRQ14 connects to primary IDE.
APICCLK	APIC clock	Not used, pull down.
APICD[1:0]	APIC Data	Not used, pull down.
USB Interface	USB Interface, 12 pins	Routed to USB socket, Transient Voltage Suppression diode is installed for surge protect. Also, 1.1 A fused is used for over current protection.
Power Management		
THRM_L	Thermal Alarm / Input	Not used, pull up.
SLP_S3_L	S3 Sleep Control / Output	Not used, pull up.
SLP_S5_L	S5 Sleep Control / Output	Routed to PLD2, then routed to BMC's XINT1 (IRQ input).
PWROK	Power OK / Input	The I/O board sends ICH4_PWROK signal to PLD2. After validation, PLD2 will route this signal to PWROK pin of ICH4 chip. See Section 5.6.2: Power Up Sequence
PWRBTN_L	Power Button / Input	Routed from BMC to PLD2. PLD2 can route this out to ICH4 PWRBTN_L input. See Section 5.6.2: Power Up Sequence for details.
RI_L	Ring Indicate / Input	Used as a general-purpose input. BMC's Server Management Interrupt (SMI) output connects to this pin to generate Scalable Coherent Interconnect (SCI).

Signal Group / Name	Description	Signal Routing
RSMRST_L	Resume well reset / input	Connected to 3_3VSTDBY_GD. After the HIP6004 D2D deliveries stable (within 10%) 3.3-V standby power, the Dallas* DS1815 chip will delay 150 ms, then assert this standby good signal.
RSM_PWROK	Resume well power Ok / Input	Connected to 3_3VSTDBY_GD. Assert signal when standby power is stable for 150 ms. (ICH4 spec. only requires 10 ms.)
SUS_STAT_L	Suspend Status / Output	Routed to PLD2. Not used in PLD design.
SUSCLK	Suspend Clock / Output	32-kHz clock output, routed to BMC and Super I/O.
VRMPWRGD	Voltage Regulating Modules (VRM) Power Good / Input	Not used, pull up.
Processor Interface		
A20M_L	Mask A20 / Output	
CPUSLP_L	Processor Sleep / Output	
FERR_L	Numeric Coprocessor Error / Input	
IGNNE_L	Ignore Numeric Error / Output	
INIT_L	Initialization / Output	
INTR	Processor IRQ / Output	
NMI	Non-maskable IRQ / Output	
SMI_L	System Management IRQ / Output	
STPCLK_L	Stop Clock Request / Output	
RCIN_L	Keyboard Controller Reset Processor/Input	
A20GATE	A20 Gate / Input	
CPUPWRGD	Processor Power Good / Output, Open Drain	
SMBus Interface		
SMBDATA	SMBus Data / Output, OD	Route to J3A1 for POST 80 port
SMBCLK	SMBus Clock / Output, OD	Route to J3A1 for POST 80 Port
SMBALERT_L	SMB Alert / Input	Used as GP11, routed to PROCHOT_L, see Section 5.9: IRQ and Bus Master for detail.
System Management Interface		
INTRUDER_L	Intruder Detect / Input	Routed to Slot1 for intruder detection circuit.
SMLINK[1:0]	System Management Link / BI	Unused, pull up.
Real Time Clock	RTCX1, RTCX2 two pins	Connect to 32-kHz crystal.
Clocks		
CLK14	Clock input	14.31818 MHz from I/O Board, for 8254 timer.
CLK48	Clock Input	48-MHz clock from I/O Board, for USB controller.
CLK66	Clock Input	66-MHz clock from I/O Board, for ICH4 core.
Misc. signals		
SPKR	Speaker / Output	Speaker signal output routed to PLD2. Will be Or-ed with speaker output from BMC.
RTCRST_L	Real Time Clock (RTC) Reset / Input	Real-time circuit reset via Resistor/Capacitor (RC) array.
TP0	Test Point / Input	Pull up.
FS0	Function Strap / Input	Reserved, NC.

Signal Group / Name	Description	Signal Routing
Power and Ground		
Vcc3_3	3.3-V supply for I/O buffer	Connected to VCC, 3.3 V.
Vcc1_5	1.5-V supply for core	From 3.3 V->1.5 V regulator.
V5REF	5-V reference input	5-V reference from +5-V, Power up sequence required. See Section 5.6.2: Power Up Sequence for details.
VccSus3_3	3.3-V Standby	On board 12v Standby to 3.3v Standby D2D.
VccSus1_5	1.5-V Standby	From 3.3 V->1.5 V STDBY regulator / transistor.
V5REF_Sus	5-V Standby Reference	From 5V_stdby, Power up sequence required.
VccRTC	Real time clock power	From 3.3 V or battery.
VBIAS	RTC well bias voltage	From battery reference, see Section 5.6.2: Power Up Sequence for details.
V_CPU_I/O	Processor I/O voltage	From 1.5-V regulator.
Vss	Ground	Digital Ground.
GPIO (General Purpose Input/Output)		

Table 5-2. ICH4 Strap Option

Part	Default	Description
R7D4	Install	No boot option for ICH4.
R6C11	DNI	Test for ICH4's GPIO16 (Integrated PU resistor).

5.3.2 BMC

The BMC ASIC contains an ARM7TDMI core and associated peripherals. It is designed for use as the central server management controller in a server system. The BMC contains the logic needed for executing firmware, controlling the system, monitoring sensors, and communicating with other systems and devices via various interfaces.

In this implementation, the BMC is running at 40 MHz from an external oscillator. The server management circuitry is supplied with standby power. The BMC has a parallel bus that is used to connect SRAM and boot flash. Two Complex Programmable Logic Devices (CPLDs) are designed to route server management signals and expand the BMC's I/O ports.

Table 5-3 contains the BMC pinout. For detailed descriptions of BMC functionality, see Section 5.5.5, "Server Management". The BMC is used to support the following features on the I/O riser card:

- ARM7TDMI processor core with JTAG connection for In-Circuit Emulation (ICE). See JTAG Section 5.7.4 for details.
- 32 KB of internal program/data RAM.
- External parallel bus interfaces: Supports 4 MB SRAM and 4 MB bottom boot Flash. The parallel bus is also routed to PLD1 for BMC expansion port. See Section 5.4, "Buses and Interfaces".

- 32-input interrupt controller supporting internal peripherals and eight external interrupts.
- Two 16550-compatible serial Universal Asynchronous Receiver/Transmitters (UARTs) with integrated baud rate generators. One is used as the EMP port and another UART is used as the ICMB port.
- Real-Time Operating System (RTOS) timer
- Watchdog timer
- RTC synchronization clock divider. A 32-kHz clock is provided from ICH4.
- Eight 10-bit A/D converter channels. Five of those are used to monitor 12V_stdby, 2.5 V, 5V_stdby, 1.5V_stdby and 1.5 V. Other voltages are monitored on the I/O board.
- LPC interface supporting the following features:
  - Slave interfaces: three 8042 Keyboard Controller Style (KCS) interfaces
  - Snoop Interface: specific I/O write cycle data snooping
  - Master Interface
- Two master/slave, four master-only I^2C interfaces. This includes I^2C for IPMB, PCI, LAN, SYS, SMB and I/O. See Section 5.4, “Buses and Interfaces”.
- Many pins usable as general purpose I/O.
- Four LED drivers to support the Power On, General Fault, Fan Fault, and Power Fault LEDs.
- Parallel bus interface with CPLDs to delivery BMC expansion ports.
- Support ISP chain via BMC’s expansion port. See CPLD design for detail.
- 40-MHz clock from external oscillator.
- 156-pin Ball Grid Array (BGA) package.

Table 5-3. BMC Pins and Signals Group Description

Signal Group / Name	Description
SMM_A[22:0]	Output, BMC memory address. Routed to SRAM, BMC Flash and PLD1.
SMM_D[15:0]	Bi-direction, BMC data bus. Routed to SRAM, BMC Flash and PLD1.
BMC_RST_R_L	Input, BMC reset line. Generated from PLD2. BMC could be reset by 3.3 V Standby Power Good.
BMC_CLK	BMC clock input, 40-MHz from oscillator (45/55 Duty cycle required).
LPC_LDRQ1_L	LPC bus master channel one, routed to ICH4 LDRQ1.
BMC_SMI_L	BMC server management interrupt. Routed to ICH4’s RI_L pin, which is able to generate system configure interrupt (SCI).

Signal Group / Name	Description
BUF1_PCIRST_L	PCI Reset line. Resets BMC LPC bus.
BUS_ISOLATE_L	When Voltage Controlled Current (VCC) power is not present, this signal will isolate BMC from LPC bus.
LPC BUS	Five-wire LPC bus interface. Connects to ICH4, SIO, FWH.
XINT[0..7]	BMC IRQs. Connects to miscellaneous server management signals.
PMI_L	Platform Management Interrupt (PMI) IRQ line from CPLD.
BMC Serial Port 0	Used as EMP port.
BMC Serial Port 1	Used as Intelligent Chassis Management Bus (ICMB) port.
BMC I2C Buses	Six I^2C* buses, routed to I/O board, processor board, memory, etc.
FP_SYS_PWR_L	Output, System Power LED. Routed to front panel.
FP_PWR_FAIL_L	Output, Power Fail LED. Routed to front panel.
FP_COOL_FAIL_L	Output, Fan Fail LED. Routed to front panel.
FP_GEN_FAULT_L	Output, General Fault LED. Routed to front panel.
BMC_SPK_DATA	Output, speaker output signal. Routed to CPLD where AND-ed with ICH4 speaker out signal. The AND-ed output signal routed to front panel.
BOOT_OK_L	Output, BMC Boot Ok signal sends to I/O board.
PIRQE	Input to BMC, active high interrupt. Inverted from PIRQE_L of ICH4.
A2D[0..7]	BMC AD converter input pins. Monitor I/O riser power voltage.
BMC_VREF	Voltage reference for A2D converter. Need 2.5 V input.
BMC_PLD_RST_L	Output from BMC, reset the Programmable Logic Devices (PLDs).
BMC_D2D_EN	D2D enable, routed to PLD, which buffers this signal, and pass to I/O board.
PS_ON_L	Output from BMC, power switch on signal routed to I/O board.
SM_PWRBTN_L	Power button signal, routed to PLD. PLD sends this signal out to ICH4 and I/O board.
POWER_SW	Power on switch input to BMC. Signal comes from front panel.
RESET_SW	Reset switch input to BMC. Signal comes from front panel.
SDINT_SW	SDINT switch input to BMC. Signal comes from front panel.
XP0_EN_L	Extension port 0 enable. Routed to PLD. (Reserved)
XP1_EN_L	Extension port 1 enable. Routed to PLD. (Reserved)
XP2_EN_L	Extension port 2 enable. Routed to PLD. (Reserved)
BMC_WE_L	BMC write enable. Routed to SRAM, Flash, PLD.
BMC_OE_L	BMC output enable. Routed to SRAM, Flash, PLD.
BMC_CS0_L	BMC chip select output for PLD extension port.
BMC_CS1_L	BMC chip select output for Static Random Access Memory (SRAM).
BMC_UPDATE	BMC update request, connected to jumper.

5.3.3 Firmware Hub (FHW)

The I/O riser contains a total of four firmware hub flash parts (PLCC32 package). All FWHs are on the same LPC bus with quick switch isolation. This isolation is required for quick parallel programming on an In-Circuit Test (ICT) machine. Each FWH will have a dedicated 33 MHz clock. Those clocks are length matched to 4.5 inches with 50-Ohm impedance.

3.3 V is connected to VPP pins of the FWHs. Three Complementary Metal Oxide Silicon (CMOS) transistors (Q8B2, Q9B1, Q9B2) isolate this power. For normal FWH write access, the 3.3 V power is always on the VPP pin. For manufacture programming, an ICT machine call will

pull low the transistors' gate (pin 1), thus, isolating the 3.3 V from VPP. At the same time, ICT can inject 12 V power on VPP. This can dramatically speed up the programming process.

Each FWH has five general input pins, giving a total of 30 General Purpose Inputs (GPIs). FWHs with ID 4, 6, 8 have their GPIs connected to Printed Circuit Board (PCB) revision bits. FWHs with ID 3, 5, 7 have their GPIs connected to BIOS strap input. Unused GPIs are pulled up via 3.3-K resistors. The following table shows the GPI pins and their usage.

Table 5-4. Firmware Hub General Purpose Input

FWH GPI	Device / Pin	Functionality
GPI0	U8D3, U9D1, U8E2 / 6	PCB Revision ID, Bit 0
GPI1	U8D3, U9D1, U8E2 / 5	PCB Revision ID, Bit 1
GPI2	U8D3, U9D1, U8E2 / 4	PCB Revision ID, Bit 2
GPI3	U8D3, U9D1, U8E2 / 3	PCB Revision ID, Bit 3
GPI4	U8D3, U9D1, U8E2 / 30	Unused, pull up
GPI5	U8E1, U9C1, U9E1 / 6	PHP Disable Jumper
GPI6	U8E1, U9C1, U9E1 / 5	Clear CMOS input
GPI7	U8E1, U9C1, U9E1 / 4	Clear Password input
GPI8	U8E1, U9C1, U9E1 / 3	Recover Boot input
Others	U8E1, U9C1, U9E1 / 30	Unused, pull up

* Note: When north bridge FWH is disabled (on processor board), the FWH with ID 8 and 9 will set the ID at 0 and 1.

5.3.4 Super I/O

The SMC* Super I/O is used in the I/O riser to provide one serial port. The device is sitting on an LPC bus and has an AMI* BIOS inside. The serial port address setting is at 0x2E as the default. For details on these I/O ports, see Section 5.5, "I/O Ports and Interface".

5.3.5 Video

The I/O riser uses an ATI Rage XL video controller. Its core processors run at 2.5 V, while its I/O has a 3.3-V interface. The video circuit has 8-MB SDRAM support. The video controller is on the PCI bus with IDSEL = AD17. It does not use the PCI IRQ line. The following is the video circuit's resistor stuff option.

Table 5-5. Video Circuit Resistor Stuff Option

Resistor	Default	Description
R6N2	DNI	DNI = video enable, Install = video disable

5.3.6 82540EM* 10/100/1000 Ethernet

The I/O riser contains a 10/100/1000 Ethernet 82540EM controller. It is a fast Ethernet multifunction PCI/CardBus controller. The 82540EM is designed to improve system network throughput by offloading communication tasks to the 82540. It also integrates advanced manageability features into one component. The 82540EM chip includes a System

Management Bus (SMB) port and provides 168-bit security encryption functionality. The following list describes the features of the 82540EM controller:

- On-chip protocol handling
  - Ipv4 checksum assistance
  - Enhanced IP address filtering
  - 802.3ac Virtual Local Area Network (VLAN) tagging and stripping capability
- Security
  - Triple Data Encryption Standard capability (168 bit)
  - Hashed-based Message Authentication Code Message Digest 5 and HMAC – secure Hash Algorithm 1 transmit authentication and receive verification support
  - Flexible and simple interface for Internet Protocol (IP) security encryption mode
  - IP security encryption off-load engine
  - Loopback of encrypted data for secondary use
- Performance enhancements
  - Delayed receive interrupt ability
  - Faster processing and lower bus utilization
- Manageability
  - Universal Network Interface Card (NIC) Driver interface integration
  - Active system health monitoring (integrated Alert on LAN)

In this implementation, the 82540EM Network Interface Card (NIC) is powered by standby power. However, since the device also sits on a normally powered PCI bus, a BUS_ISOLATE_L signal is used to isolate the 82540EM device from the PCI bus while VCC is absent. The 82540EM's SMB bus connects to the BMC's I2C_LAN bus. This BMC I^2C bus is dedicated and used for 82540EM NIC only.

There is a 256-word EEPROM for this NIC. It is used to store MAC address and PCI configuration information.

The following is the 82540EM device's pin and signal description.

Table 5-6. 82540EM Signal Description

Signal Group / Name	Description
PCI Bus	Routed to ICH4 PCI BUS. IDSEL = 16. Interrupt = PIRQC_L.
NIC_SMBALRT_L	Output from 82540EM, routed to PLD and then to BMC XINT0.
I2C_LAN_SCL	SMB bus, routed to BMC.
I2C_LAN_SDA	SMB bus, routed to BMC.
3_3VSTDBY_GD	3.3-V Standby Power Good, used to reset 82540EM.
EEPROM Interface	4-wire EEPROM interface.
Flash / Modem Interface	Floating, feature not supported.
LILED	Active LED, solid Green means Link
ACTLED	Active LED, Blink means activity.
100_L	Speed LED, Green means 100 Mbit transfer (blank means 10Mbps speed).

1000_L	Speed LED, Yellow means 1 GB transfer.
TDP0, 1,2,3	Transmitter positive, (4 wires).
TDN0,1,2,3	Transmitter negative, (4 wires) differential with above signals.

5.4 Buses and Interfaces

5.4.1 Hublink 1.5 Interface

The I/O riser plugs into the I/O board via a 242-pin slot one connector. Its main interface, Hublink 1.5, links the ICH4 to the Server I/O Hub (SIOH) on the I/O board. The Hublink compensation (Romp) resistor value is 45.3 Ohm, 1 percent, and is pulled to 1.5V. As this bus requires minimum vias and shortest possible routing length, it is routed as a 5-millimeter trace in an internal layer, with GND planes above and below. The routed trace space is 20 millimeters, and target impedance is 50 Ohm.

Table 5-7. Hublink (HL) Interface Pinout

Signal Group / Name	Description	Signal Routing
HL[7:0]	Hub link (HL) data path	Routed to Slot one edge finger. Connect to I/O Board HL[7:0]
HL8	Hub link interface, also known as HL_REQM	Routed to Slot one edge finger. Connect to I/O Board HL_REQM
HL9	Hub link interface, also known as HL_REQI	Routed to Slot one edge finger. Connect to I/O Board HL_REQI
HL10	Hub link interface, also known as HL_STOP	Routed to Slot one edge finger. Connect to I/O Board HL_STOP
HL11	Hub link interface, also known as HL_PAR	Routed to Slot one edge finger. Connect to I/O Board HL_PAR
HL_STB	Hub link Strobe	Routed to Slot one edge finger. Connect to I/O Board HL_STB
HL_STB_L	Hub link Strobe Complement	Routed to Slot one edge finger. Connect to I/O Board HL_STB_L
HL_COMP	Hub Interface Compensation	Pulled to 1.5V via 45.3 Ohm Resistor

5.4.2 Integrated Drive Electronics (IDE) Interface

The ICH4 supports two IDE buses. The I/O riser will only route the primary IDE channel to the Slot One connector interface to the I/O board. The IDE bus on the I/O riser is designed for ATA33. The PCB trace impedance is targeted at 60 Ohms. Since the ICH4 incorporates the serial resistor termination on the IDE bus except IDE-RESET, no extra termination is required. However, a 22-Ohm resistor is used for the IDE RESET signal. This IDE RESET signal is a buffered reset from ICH4's PCI Reset.

5.4.3 LPC Bus

The ICH4 supports a 4-bit, 33-MHz LPC bus. The LPC bridge function of the ICH4 resides in PCI Device 31: Function 0. For details of the PCI configuration register for the LPC bridge, see the most current *ICH4 EPS.* The following devices sit on the LPC bus:

- Firmware Hub Flash – There are a total of four PLCC package firmware hub flashes that sit on the firmware hub bus. This firmware hub bus is also known as the LPC bus since they are muxed together. The firmware hub bus signal bits 3 ~ 0 are mapped to the LPC bus data address bits 3 ~ 0. The firmware hub signal bit 4 is mapped to the LPC bus' LFRAME#.
- Super I/O – The SMC 47B272 LPC super I/O part is used. It takes LPC DMA channel 0 of the ICH4.
- BMC – The BMC sits on the LPC bus to allow communication to the ICH4. The BMC takes LPC DMA channel 1 from the bus. When the main power is off, the BUS_ISOLATE_L will assert a low signal to the LPCPD_L pin. This will shut off the BMC's LPC bus. This is necessary, as the BMC is running on standby power, while the ICH4 LPC bus runs on main power.

Table 5-8. LPC Bus Pin List

Signal Group / Name	Description	Comments
LPC_LAD[3:0]_L	LPC Multiplexed Command, Address and Data, I/O	All have internal pull ups.
LPC_LFRAME_L	LPC Frame, Output	Indicates the start of cycle.
LPC_LDRQ[1:0]_L	LPC Serial DMA/Master Request Inputs	Channel 0 routed to Super I/O*. Channel 1 routed to BMC.

5.4.4 PCI Interface

The ICH4 PCI interface provides a 33 MHz, PCI Revision 2.2-compliant implementation. All PCI signals are 5 V tolerant. The ICH4 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH4 requests.

Note that most transactions targeted to the ICH4 will first appear on the external PCI bus before being claimed by the ICH4. The exceptions are I/O cycles involving USB, IDE, and AC'97. These transactions will complete over the hub interface without appearing on the external PCI bus.

In the I/O riser design, there are two devices that sit on this 32-bit PCI bus.

- ATI* Rage XL Video controller
- Intel® 82540 EM Ethernet controller

The video controller has 8 MB SDRAM support and does not use any PCI IRQ line. The Ethernet controller is the Intel® 82540EM. It has 168-bit encryption features with server management support. The following table lists the PCI IRQ, DMA, and IDSEL distribution.

Table 5-9. PCI IRQ, DMA, and IDSEL Distribution

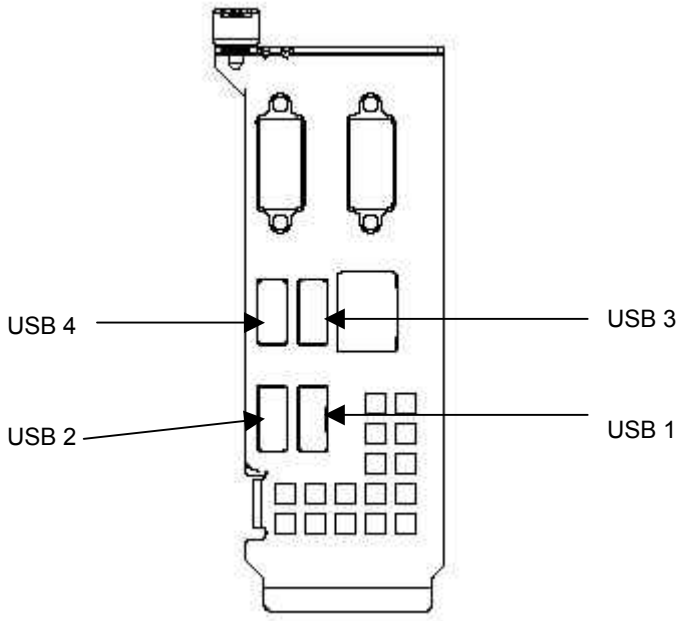
Video	IDSEL = AD17 Bus Master = REQ2 IRQ = None
Intel® 82540 EM LAN	IDSEL = AD16 Bus Master = REQ1 IRQ = PIRQC

5.5 I/O Ports and Interface

5.5.1 USB

There are two USB controllers inside the ICH4. Each controller supports two USB 1.1 compatible ports for a total of four USB ports. The following is the physical USB assignment to the external jacks.

- J1D1, top socket --- USB 1
- J1D1, bottom socket --- USB 2
- JA1D1, top socket --- USB 3
- JA1D1, bottom socket --- USB 4



Inside the ICH4, the USB PCI configuration registers sit on D31:F2/F4. See the following table for mapping information. For details of each register, see the *ICH4 EPS.*

Table 5-10. ICH4 Mapping Table

Offset	Mnemonic	Register Name/Function	Function 2 Default	Function 4 Default	Type
00–01h	VID	Vendor ID	8086h	8086h	RO
02–03h	DID	Device ID	2442h	2444h	RO
04–05h	CMD	Command Register	0000h	0000h	R/W
06–07h	STA	Device Status	0280h	0280h	R/W
08h	RID	Revision ID	See Note	See Note	RO
09h	PI	Programming Interface	00h	00h	RO
0Ah	SCC	Sub Class Code	03h	03h	RO
0Bh	BCC	Base Class Code	0Ch	0Ch	RO
0Eh	HTYPE	Header Type	00h	00h	RO
20–23h	Base	Base Address Register	00000001h	00000001h	R/W
2C–2Dh	SVID	Subsystem Vendor ID	00	00	RO
2E–2Fh	SID	Subsystem ID	00	00	RO
3Ch	INTR_LN	Interrupt Line	00h	00h	R/W
3Dh	INTR_PN	Interrupt Pin	03h	03h	RO
60h	SB_RELNUM	Serial Bus Release Number	10h	10h	RO
C0–C1h	USB_LEGKEY	USB Legacy Keyboard/ Mouse Control	2000h	2000h	R/W
C4h	USB_RES	USB Resume Enable	00h	00h	R/W

5.5.2 Ethernet Port

The external jack JA1D1 is a USB and RJ45 combination jack. The RJ45 Ethernet port sits on top of dual USB ports. It contains an Ethernet transformer with resistor network and two color LEDs. It has a 120-ohm termination resistor on its transformer. On the transformer, several external 49.9-ohm termination resistors are installed. Below are definitions of the speed/status LEDs.

- Speed LED: Yellow On, 1000-Mbps Ethernet
  Speed LED: Green On, 100-Mbps Ethernet
  Speed LED: Off, 10-Mbps Ethernet
- Status LED: Green On, Ethernet link detected
- Status LED: Off, Ethernet link not found
- Status LED: Green Flashing, Ethernet data activity

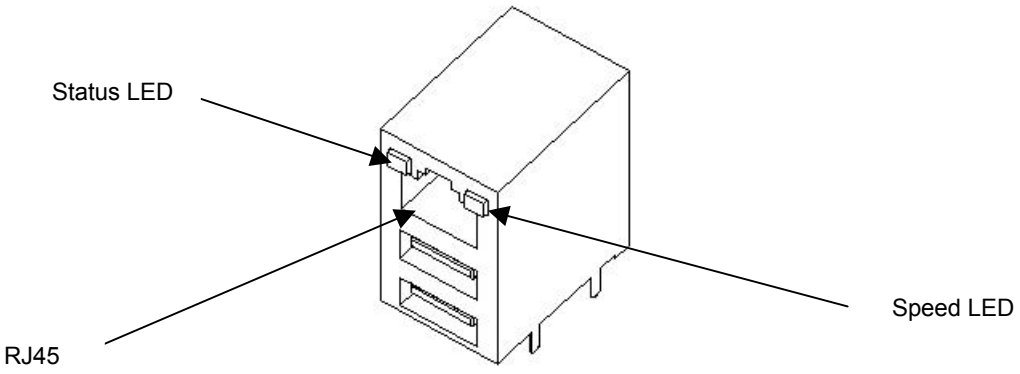


Figure 5-2. LED and RJ45 Locations

5.5.3 Serial Port

The SMC* Super I/O has two serial ports. However, the Server Board S870BN4 I/O riser only uses COM2. The COM2 connects to J1B1, which is a video and serial combination jack. The COM1 is connected to J1A1 for debug purposes only. The serial port supports base address 0 x 02E and 0 x 04E. The I/O riser default setting is 0 x 02E. This is done by pulling GPIO24 low during boot up. This GPIO24 is controlled by a CPLD.

5.5.4 Video Jack

The I/O riser uses a combination jack - J1B1 from video and serial port. The following is the pinout of J1B1's video port.

Table 5-11. Video Jack (J1B1) Pinout

Pin 1	Video Red Color Signal
Pin 2	Video Green Color Signal
Pin 3	Video Blue Color Signal
Pin 4	NC
Pin 5	GND
Pin 6	GND
Pin 7	GND
Pin 8	GND
Pin 9	NC
Pin 10	GND
Pin 11	NC
Pin 12	MONID1, I2C bus
Pin 13	VID_HSYNC
Pin 14	VID_VSYNC

Pin 15	MONID2, I2C bus

5.5.5 I²C* Post Code Header

The I/O riser has a 5-pin header (fourth pin removed) for the I²C post code adapter. The header is located at J3A1. The I²C signals are from the ICH4's SMB bus. The data and clock signals are pulled up to 3.3V standby. The following is the pin assignment.

Pin 1	12V Standby
Pin 2	SMBDATA
Pin 3	SMBCLK
Pin 4	NC – pin removed
Pin 5	Ground

5.5.6 ISP Headers

The I/O riser has two ISP headers. The header at location J8A1 is for PLD1 (U7B1), and the header at location J7A2 is for PLD2 (U5B2) and the system chain. Both headers are 8-pin headers with the fifth pin removed. The following is the pin assignment for the header. For details of the ISP function, see Section 5.7.5.

Pin 1	3.3V Standby
Pin 2	TDO
Pin 3	TDI
Pin 4	Enable
Pin 5	NC – removed pin
Pin 6	TMS
Pin 7	Ground
Pin 8	TCLK

5.5.7 Switch

The I/O riser has one 5-position switch at location S8A1. The default setting is at "OFF". When the user wants to perform a recovery boot or clear CMOS, the user needs to set the appropriate switch to the "ON" position. The following is a switch position assignment.

	Switch " OFF"	Switch " ON"
Pin 1	No Action	Recovery Boot
Pin 2	No Action	Clear Password
Pin 3	No Action	Clear CMOS
Pin 4	No Action	No Action – Pin removed
Pin 5	No Action	BMC update

Note: Manufacture default: all switch settings are at "OFF".

5.5.8 Jumper

The I/O riser has one 5-pin header (J7A3) used as a jumper. It serves two functionalities: hot-plug disable and Fault Resilient Boot (FRB) disable.

Below is the default setting of the jumper pin (no jumper required).

1	2	3	4	5

For PHP_DIS_JP function (hot plug disable), put jumper on pins 1 and 2.

For FRB_DIS_JP function (FRB disable), put jumper on pins 4 and 5.

The I/O riser also has a 3-pin header (J7A1) used for BMC boot block protection. The default is no connection, which means the BMC boot block is protected. When installing a jumper on J7A1, pins 2 and 3, the boot block protection is disabled, and thus, allows the updating of BMC code in the boot block .

5.6 Server Management

5.6.1 Server Management Block Diagram

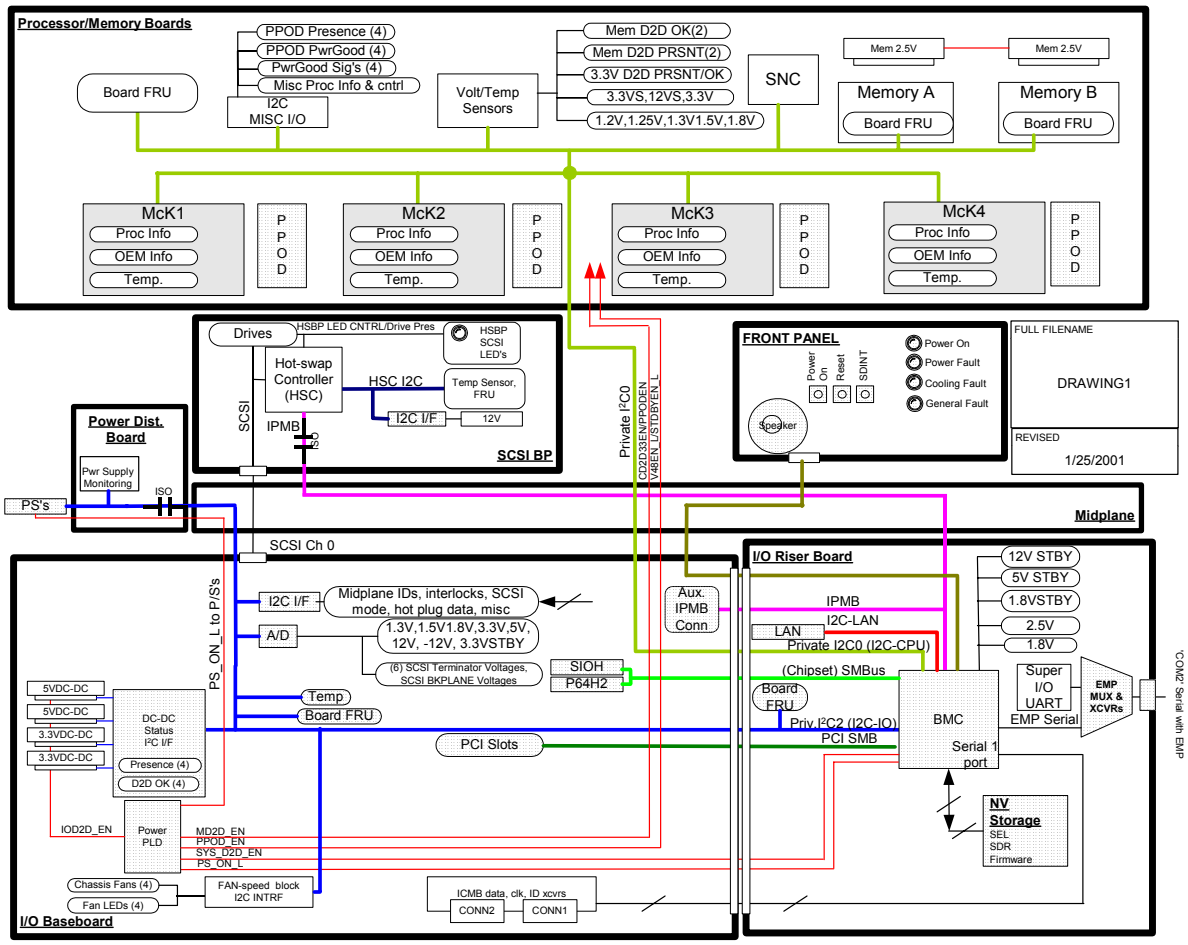


Figure 5-3. Server Management Block Diagram

5.6.2 Power Up Sequence

The BMC controls the system power-up sequence. It detects the front panel switch and generates corresponding power-up controls to the system.

For example, when the power button is pushed, the BMC will debounce this signal. It will make sure that the system is not in a critical state, such as PLD programming, and check if interlock is good. If certain interlock, standby voltages, etc., conditions are met, the BMC will generate BMC_D2D_EN, PS_ON, and SM_PWRBTN_L. These signals will inform the system that the power switch is on and the D2D power supplies need to be turned on.

When the BMC detects this power-on switch activity again, it will again debounce the signal. If the button is held for more than four seconds, the platform will turn off. For more detail, see the *SR870BN4 Server Management EPS*.

5.7 I/O Riser Reset

Most ASICs on the I/O riser are reset by either PCIRST_L (PCI Bus reset line) or by 3_3VSTBY_GD (3.3-V Standby Power Good).

The first time the I/O riser receives power from a 12-V standby, the on-board D2D, which converts 12-V standby to 3.3-V standby, delivers 3.3V_STDBY output immediately. The external reset generator, Dallas* 1815 (Ref Des. U5C2), will detect the voltage output of 3.3V_STDBY. When this device detects approximately 3 V, it will delay the circuit for 150 ms then send out an active low reset signal to the 3_3VSTBY_GD line. This is the indication that standby power is good and all circuits running on standby power should reset at this time.

When the main power in the system is turned on and the PCI clocks are stable for at least 1 ms, the I/O board's reset circuit will assert the PWROK signal to the I/O riser. This signal is received by CPLD (Ref U5B1) and the CPLD will respond by asserting the PWROK signal to the ICH4. After the ICH4 detects PWROK = 1, it will reset itself and assert PCIRST# signals to all PCI and LPC buses. The PCIRST_L is buffered through CPLD and distributed to the video, Super I/O, BMC, FWH, and 82540 Ethernet.

5.7.1.1 ICH4 Reset

The ICH4's resume power well is reset by 3_3VSTBY_GD. For its PCI and LPC bus, the ICH4 itself generates PCIRST_L when it receives PWROK =1. The ICH4 core can also reset by the Hublink interface if it receives a reset packet.

5.7.1.2 BMC Reset

The BMC is run on standby power only. Thus, the BMC core can be reset by 3_3VSTBY_GD signal.

For the BMC's LPC bus, the reset is from PCIRST_L. Again, the CPLD buffers PCIRST_L from the ICH4 and delivers an exact copy to the BMC's LPC reset pin. The PCIRST_L is buffered due to a fan-out situation. There are a total of 11 devices that need PCIRST_L.

5.7.1.3 Super I/O Reset

The Super I/O can be reset by PCIRST_L. Again, it is also buffered from CPLD U5B1. This reset not only resets the LPC interface of the Super I/O, but also resets its core.

5.7.1.4 Video Reset

Either PCIRST_L or the BMC can reset the video controller. This reset line is decoded by the CPLD. The CPLD will assert the reset line when it (1) receives PCIRST_L from ICH4, or (2), detects vid_reset bit=1 on BMC's extension port.

5.7.1.5 82540EM Ethernet Reset

The 82540EM Ethernet controller is on 3.3-V standby. It is reset by 3_3VSTBY_GD during initial standby power on. This device can also be reset by buffered PCIRST_L from CPLD and ICH4.

5.7.1.6 CPLD Reset

The CPLD is reset by the 3_3VSTDBY_GD and BMC_PLD_RST_L line. During initial power up (i.e., once AC is applied), the CPLD is reset while 3.3-V standby stabilizes. Also, after ISP programming of the PLD, the BMC sends out a BMC_PLD_RST_L to reset the PLD again.

5.7.2 I^2C, IPMB and FRU

There are a total of six I^2C buses that the BMC supports. The first I^2C bus is also known as IPMB. The IPMB bus is pulled to 5-V standby while the others are pulled to 3.3-V standby (the I/O riser is the only board that pulls the I^2C buses high). The following list describes the six I^2C buses:

1. I2C_IPMB: generated from the BMC I2C0. It connects to the I/O board and SCSI backplane. It is also internally routed to the ICMB port of the BMC.
2. I2C_SYS: generated from the BMC and goes to the SNC, memory boards, and processor boards.
3. I2C_LAN: generated from the BMC and goes to the 82540 Ethernet only.
4. I2C_PCI: goes to the PCI slots on the I/O board.
5. I2C_I/O: goes to the I/O board for D2D, A/D. The I/O riser also has a 24C32 Field Replaceable Unit (FRU) sitting on this bus (FRU Address Strap: A2,A1,A0 = 1,0,1).
6. I2C_SMB, goes to the I/O boards SIOH, and P64H2.

The following is a detailed I^2C connection diagram from the *SR870BN4 Server Management EAS*.

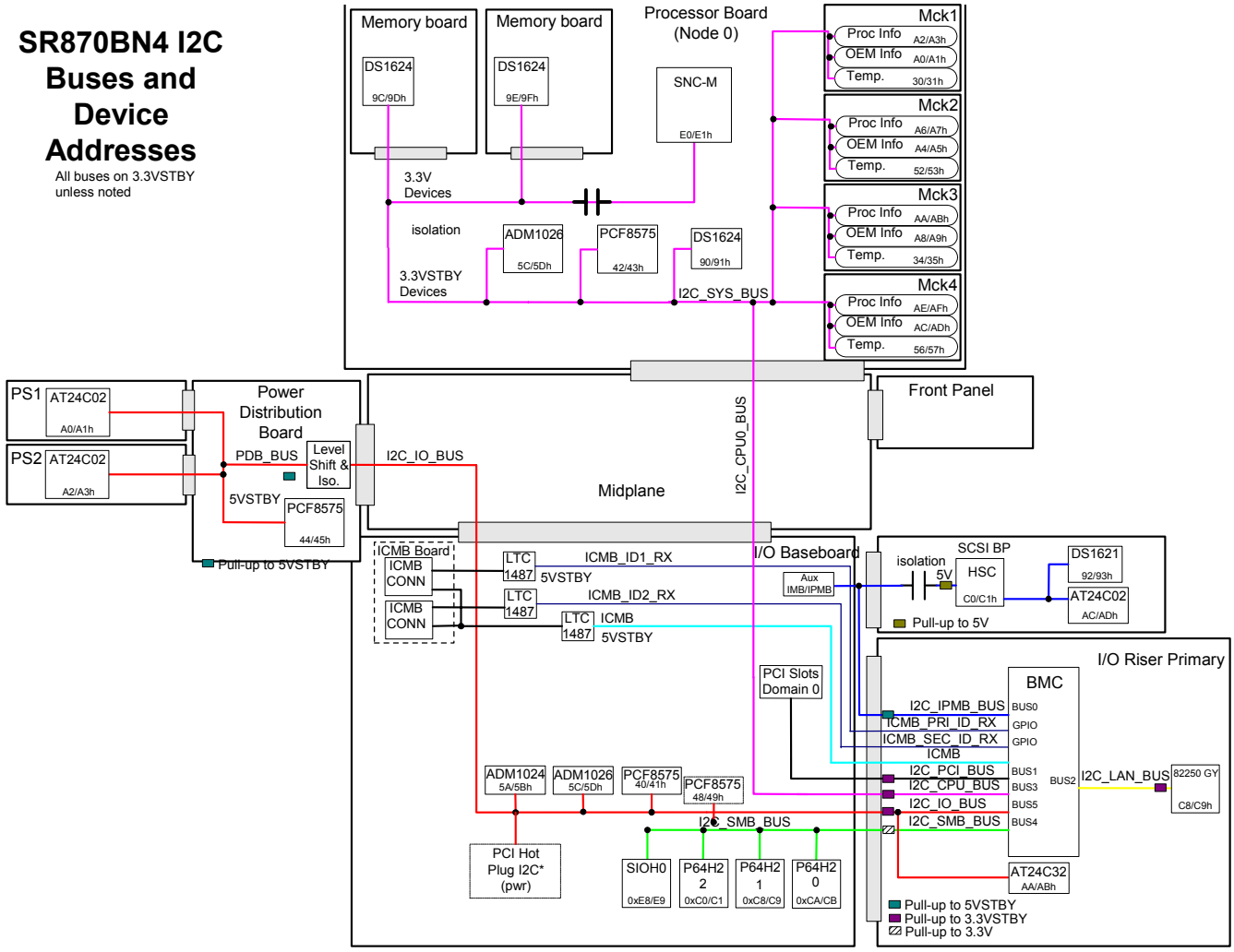


Figure 5-4. Intel® Server System SR870BN4 I²C Buses and Device Addresses

5.7.3 Inter-Chassis Management Bus (ICMB) and Emergency Management Port (EMP)

ICMB signals are routed from the BMC directly to the slot-one edge finger. There will be an ICMB dongle installed on the I/O board to carry the signals out to the back of the I/O tray. The following list describes the six ICMB signals with ICMB ID support.

Table 5-12. ICMB Signal List

Signal Group / Name	Description
ICMB_TX	Transmitter line, output
ICMB_RX	Receiver line, input
ICMB_TXEN	Transmitter enable, output, active high
ICMB_ID_TXEN	ID transmitter enable, output, active high
ICMB_ID1_RX	ID1 receiver line, input
ICMB_ID2_RX	ID2 receiver line, input

The EMP port is shared with the Super I/O's serial port (COM2). It is handled by three 74HC4066's that mux these two ports into one RS232 device. There are two mutually exclusive signals to select which bus to send out through the I/O riser's DB9 connector.

Table 5-13. EMP Signal List

Signal Group / Name	Description
EMP_MUX	Output from BMC. This signal is routed to PLD. Active high '1' means select EMP_EN = 1 and COM2_EN = 0. Power on default is EMP_MUX=1.
EMP_EN	Output from PLD. When EMP_EN = 1, select EMP port out to DB9 connector.
COM2_EN	Output from PLD. When COM2_EN = 1, select serial port (COM2) out to DB9 connector. There will never be any time that EMP_EN and COM2_EN go high at the same time.

5.7.4 JTAG

The BMC's JTAG port can be a master or slave. The signals are passed through resistors and routed directly to the edge finger. The I/O board takes those signals and connects them to the system JTAG chain. In master mode, the BMC is the master on the system JTAG chain. For details, see the *SR870BN4 External Architecture Specification.*

The BMC can also be a slave on the JTAG port. There is an ICE header installed on the JTAG chain, J6A1, and a 2 x 8 Dual In-Line Package (DIP) header. A firmware developer can plug in a JENNI ICE emulator in this header to debug code.

The default setting for the BMC is in the JTAG master mode.

Table 5-14. Intel® Server Board S870BN4 I/O Riser JTAG Stuff option

Resistor	Stuff Option
R6C1	Stuffed: for BMC JTAG Port Master mode (default). Per the schematic, this is the TDI (data input) signal.
R5C1	Empty: for BMC JTAG Slave mode. ICE enabled. Stuffed; TDO (data output)
R5C4	This is stuffed; Clock signal
R5C5	Stuffed; IO_TMS signal

R5C6	Stuffed; Reset signal.

5.7.5 ISP Chain

The BMC is the master of the ISP chain. Its memory space is decoded by the I/O riser's PLD1 to map a portion of that into the ISP chain. For example, when the BMC writes data to the memory address "2XXXX0" (HEX), the PLD1 will know this is for the ISP chain. It will convert the data into the ISP chain. Note that the PLD will only pass the lower five bits (bit 0,1,2,3,4) of data to the ISP chain.

The ISP chain is also shared with the LCD signal. Two signals, LCD_E_L and ISP_EN_L, give current data bus status. When LCD_E_L is low, the shared data bus is for the LCD interface. When ISP_EN_L is low, the bus is for the ISP chain. These two signals are decoded from the BMC's flash memory address and will never be low at the same time. The Lattice* CPLD handles all logic here. For example, when the BMC sends data to the address "2XXXXF" (HEX), the PLD will deliver the lower five bits of data to the shared LCD/ISP bus. The CPLD will also assert LCD_E_L = '0' and ISP_EN_L='1'. This indicates that the bus is used for the LCD interface at that time. Note that the LCD feature is neither validated nor tested.

There are two ISP headers installed on the I/O riser. The first header, J8A1, is used for programming the PLD1. Since PLD1 is used to decode the ISP chain signal, it cannot be programmed by the BMC and must be programmed from this header. The second header, J7A2, is sitting on the ISP chain. A user can scan and program the system ISP chain via this header. It is an alternative programming solution rather than using the BMC.

The following figure shows the basic block diagram of the ISP chain of the Server System SR870BN4.

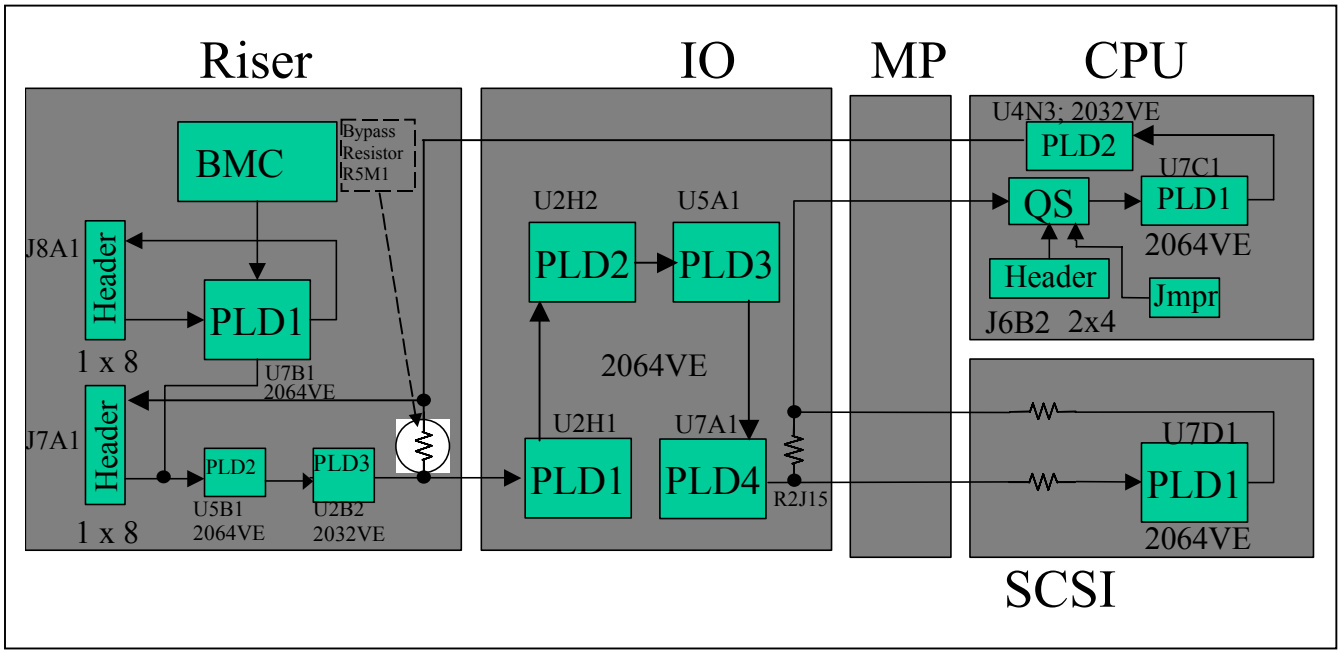


Figure 5-5. Intel® Server System SR870BN4 System ISP Chain Block Diagram

5.7.6 Front Panel Interface

All the front panel interfaces go to the BMC controller. There are a total of three switch inputs, four LED outputs, and one speaker output.

Table 5-15. Front Panel Interface

Signal Name	Description	Connection
POWER_SW	Power switch input, de-bounced on I/O board	BMC GPIO, PLD
RESET_SW	Reset switch input, de-bounced on I/O board	BMC GPIO, PLD
SDINT_SW	SDINT switch, de-bounced on I/O board	BMC GPIO, PLD
SPEAKER	Active driven by MMBT3904	CPLD, BMC, ICH4
ON_LED	Power On LED, OD, Active Low output, 20 mA maximum	BMC GPIO
PWR_FLT_LED	Power fail LED, OD, Active Low output, 20 mA maximum	BMC GPIO
COOL_FLT_LED	Fan fail LED, OD, Active Low output, 20 mA maximum	BMC GPIO
GEN_FLT_LED	Gen fail LED, OD, Active Low output, 20 mA maximum	BMC GPIO

Note: The LCD interface is provided on the I/O riser hardware. Check the *BMC Firmware EPS* to see if this option is supported or not.

5.7.7 CPLD Interface

There are three Lattice* 2064VE PLDs on the I/O riser. The first CPLD is used to handle address decoding for the ISP chain, LCD signals, and server management expansion port.

Since the first PLD decodes the ISP chain data, it is not in the ISP chain. This CPLD can only be programmed by an on-board ISP header.

The second CPLD is used mainly for server management signal routing and power on / reset sequence emulation. Most miscellaneous logic is also handled by this PLD.

The third PLD is the smaller version ISP2032. It handles Serial Over LAN, the Serial port, and an EMP port switching circuit.

5.7.7.1 PLD1

PLD1 is located at U7B1. It decodes the BMC memory address to form an ISP bus, an LCD bus, and three 8-bit registers. See the address mapping table below.

Server Board S870BN4 I/O Riser

A21	A20	A19	A3	A2	A1	Description
0	X	X	X	X	X	Flash Boot Block, Protected by SMM_BB_UNPROT_L
1	0	0	X	X	X	Flash address
1	0	1	X	X	X	BMC to BMC
1	1	0	X	X	X	Expansion Port - see next table for detail
1	1	1	X	X	X	Reserved

Server System SR870BN4 - Expansion Port Detail

A21	A20	A19	A3	A2	A1	Description
1	1	0	0	0	0	Expansion Port 0
1	1	0	0	0	1	Expansion Port 1
1	1	0	0	1	0	Expansion Port 2
1	1	0	0	1	1	Expansion Port 3, Reserved
1	1	0	1	0	0	Expansion Port 4, Reserved
1	1	0	1	0	1	Expansion Port 5, Reserved
1	1	0	1	1	0	Expansion Port 6, LCD Bus
1	1	0	1	1	1	Expansion Port 7, ISP BUS

PLD1 uses a 6-bit address. The address is mapped according to the above table, thus determining which port it is. For example, when A21=1, A20=1, A19=0, A3=1, A2=1, A1 =1, it is an ISP port.

The following table futher defines which databit handles which signal at a particular port.

Server Board S870BN4 I/O Riser Expansion Bus Mapping Table

ISP Mapping Table -- (Register)

Datapin	Default	Assigned to:	Schematic Netname	Reference
D7	0	*Reserved*		
D6	0	*Reserved*		
D5	0	*Reserved*		
D4	1	**Enable**	ISP_EN_L	
D3	1	**SDO**	ISP_SDO_LCD7	Read only for ISP
D2	1	**SDI**	LCD6_PLD2_SDI	
D1	1	**MODE**	ISP_MODE_LCD5	
D0	1	**SCLK**	ISP_SCLK_LCD4	

LCD Mapping Table (Register)

Datapin	Default	Assigned to:	Schematic Netname	Reference
D7		*Reserved*		
D6	1	**Read/Write_N**	LCD_RW	U7B1 pin 77
D5	0	**Reset (active high)**	LCD_RS	U7B1 pin 76
D4	0	**Enable (active high)**	LCD_E	U7B1 pin 78
D3	1	**LCD7**	ISP_SDO_LCD7	U7B1 pin 72
D2	1	**LCD6**	LCD6_PLD2_SDI	U7B1 pin 70
D1	1	**LCD5**	ISP_MODE_LCD5	U7B1 pin 69
D0	1	**LCD4**	ISP_SCLK_LCD4	U7B1 pin 68

Expansion Port 0 (Register)

Data Bus	Default	Assigned to:	Schematic Netname	Notes
D7	1	**CON_DIR_L**		Read / Write
D6	1	**CLR_CMOS**	Open Drain	Read / Write
D5	1	**VIDEO_BLANK_N**		Read / Write
D4	1	**EX_RESET_N**		Read / Write
D3	1	**IS1_JTAGEN_N**		Read / Write
D2	1	**IS0_JTAGEN_N**		Read / Write
D1	1	**BMC_SDINT_L**		Read / Write
D0	1	**SM_PWROK**		Read / Write

Expansion Port 1 / Read Only

Data Bus	Default	Read from:	Schematic Netname	Notes
D7	0	**Reserved**		
D6	0	**Reserved**		
D5	0	**Reserved**		
D4	0	**Reserved**		
D3	0	**Reserved**		
D2	NC	**CLR_CMOS**		READ ONLY
D1	NC	**SMM_BB_UNPROT_L**		READ ONLY
D0	0	**Reserved**		

Expansion Port 2 (Latch)

Data Bus	Default	Read from:	Schematic Netname	Notes
D7	0	**Reserved**		
D6	0	Reserved		
D5	0	**Latch Mask for D3**		1 = mask enable
D4	0	**Latch Mask for D2**		1 = mask enable
D3	0	**NODE1_HP_INT_L**		Write 0 to clear
D2	0	**NODE0_HP_INT_L**		Write 0 to clear
D1	0	**SDINT_SW_L**		Write 0 to clear
D0	0	**Reserved**		Write 0 to clear

The ISP chain and LCD chain use a flip-flop to hold data. In the board design, they share the data pins. Thus, the Server Board S870BN4 I/O riser only allows one activity at anytime. When the ISP chain on the Server System SR870BN4 is being utilized, the I/O riser cannot send out LCD signals at the same time.

Expansion port 0 has eight flip-flops. Thus, the BMC can read and write to those flip-flops. Each flip-flop connects to one external signal. Thus, the flip-flops work like extended GPIO for the BMC.

Expansion port 1 is a read-only port. This serves as a read-only GPI for the BMC.

Expansion port 2 has eight latches. The latch holds important signals and interrupts. The BMC can clear the latches by writing a zero to the port.

There is a special signal “CLR_CMOS” in this PLD design. This allows the BMC to clear the CMOS. Also, there is an external switch S8A1 that can also clear CMOS. The PLD implements this by using an open drain output. By writing zero to expansion port 0 data D6, the BMC is able to clear the CMOS activity. When expansion port 0, data bit D6 is at high, this means that BMC does not clear the CMOS line. The external switch can be low and high. The BMC is able to read the external switch setting by reading expansion port 1, data D2.

5.7.7.2 PLD2

PLD2 is located at U5B2. It is used to buffer the PCI reset and to route some server management signals. When the BMC is not ready, it is also used to power on the whole system. See the following diagram.

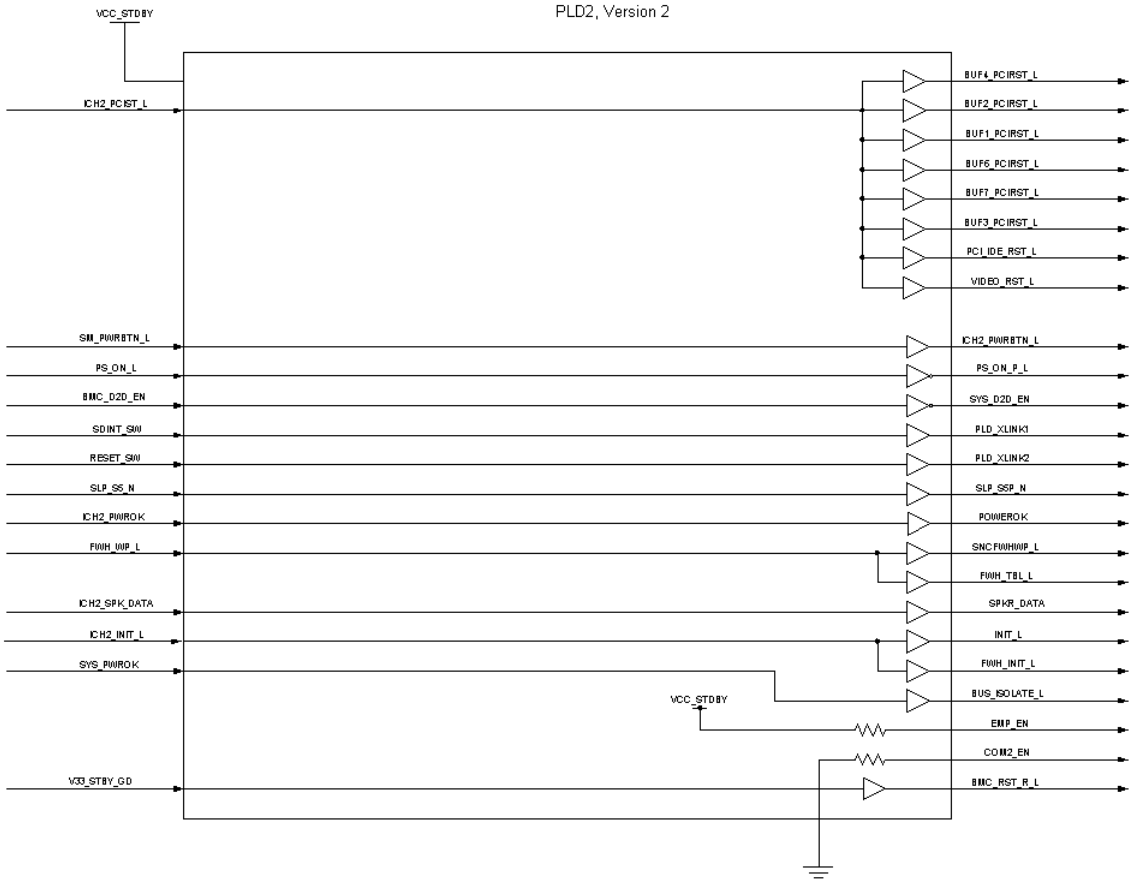


Figure 5-6. PLD2 - Miscellaneous Control PLD

5.8 Clock

There are seven frequency clocks on the I/O riser. Four are from the I/O board's CKFF; three are from crystals. The following table shows the chips and associated clocks.

Table 5-16. Intel® Server Board S870BN4 I/O Riser Clock Signals

SR870BN4 I/O riser CLOCK					
Net Name	**Frequency**	**Slot 1 Pin #**	**Destination**	**Impedance**	**Length**
CLK33_FWH4	33 MHz	A121	FWH ID = 4	50	4.5 inch
CLK33_FWH6	33 MHz	A103	FWH ID = 6	50	4.5 inch
CLK33_FWH5	33 MHz	A117	FWH ID = 5	50	4.5 inch
CLK33_FWH7	33 MHz	A99	FWH ID = 7	50	4.5 inch

CLK33_ICH2	33 MHz	A65	ICH4	50	4.5 inch
CLK33_NIC	33 MHz	A10	NIC	50	4.5 inch
CLK33_SIO	33 MHz	A6	SIO	50	4.5 inch
CLK33_VID	33 MHz	A8	Video	50	4.5 inch
CLK33_BMC	33 MHz	B62	BMC	50	4.5 inch
CLK66_ICH2	66 MHz	A61	ICH4	50	4.5 inch
CLK48_ICH2	48 MHz	A63	ICH4	50	4.5 inch
CLK14_SIO	14 MHz	A4	SIO	50	4.5 inch
CLK14_ICH2	14 MHz	A47	ICH4	50	4.5 inch

Chips	Clock 66 MHz	Clock 33 MHz	Clock 14 MHz	Clock 48 MHz	Other
ICH4	1	1	1	1	One 32-kHz crystal
BMC	1	1			One 40 MHz oscillicator
Super I/O		1	1		One 32 kHz from ICH4
Video		1			One 29.498928-MHz crystal
FWH (6 chips)		6			
82540 LAN		1			One 25-MHz crystal
Lattice PLD		1			

There are a total of nine 33-MHz clocks passing from the I/O board. These clocks are for two types of buses, the PCI and LPC. They sit next to the ground pin and are all routed at 4.50 inches in length. Most clocks are targeted at 50-Ohm impedance, except the firmware hubs. The Server Board S870BN4 I/O riser will not share the clocks; each firmware hub will have a dedicated 33-MHz clock from the I/O boards.

The 66-MHz clock is routed to the ICH4 only. It has a special one millisecond timing relationship between this clock and 33-MHz. This is handled in the I/O board's CKFF. The BMC cannot use this clock because the CKFF is powered by a regular VCC. In this case, a 40-MHz oscillator is installed for the BMC only. This oscillator is running from 3.3V_STDBY, thus, providing server management clock at sleep state (S3, S5).

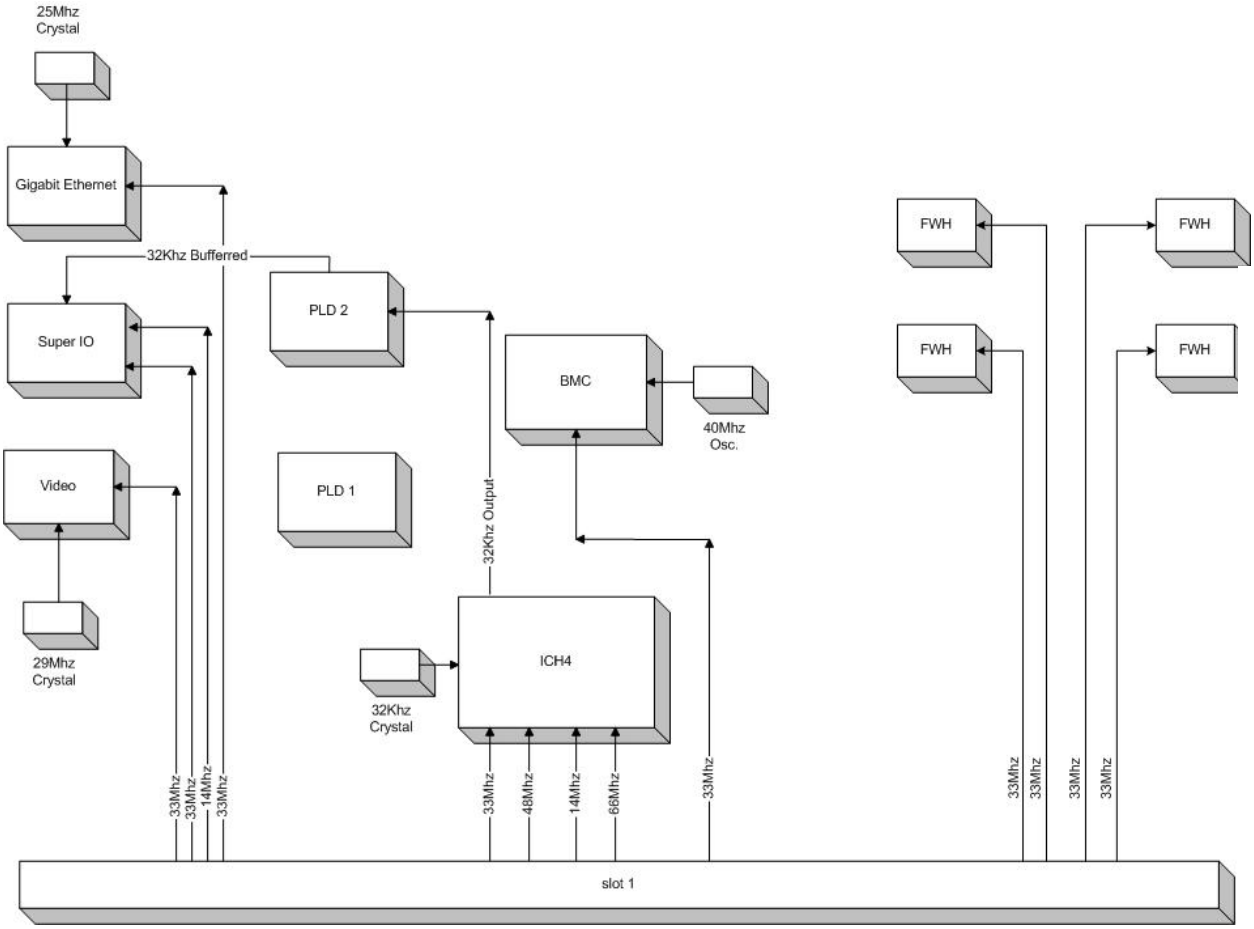


Figure 5-7. Intel® Server Board S870BN4 I/O Riser Clock Distribution

5.9 IRQ and Bus Master

The following table presents the IRQ and bus master/DMA map of the ICH4.

Note: The ATI* video controller will not have an interrupt since it is for special video command only.

For a description of compatibility interrupt and error interrupts, refer to the *Intel® Server System SR870BN4 External Architecture Specification.*

Table 5-17. IRQ and Bus Master / DMA Map

ICH4 IRQ	Device
IRQ14	IDE0
IRQ15	IDE1
PIRQA	BOOT_INT1_L
PIRQB	BOOT_INT0_L
PIRQC	82540 NIC
PIRQD	Reserved (USB1)
PIRQE	BMC (Inverted by CPLD)
PIRQF	SNC_BERRIN_L
PIRQG	CORR_ERR_L
PIRQH	Reserved (USB2)
SERIRQ	Super I/O
DMA0	Free
DMA1	82540 NIC
DMA2	Video

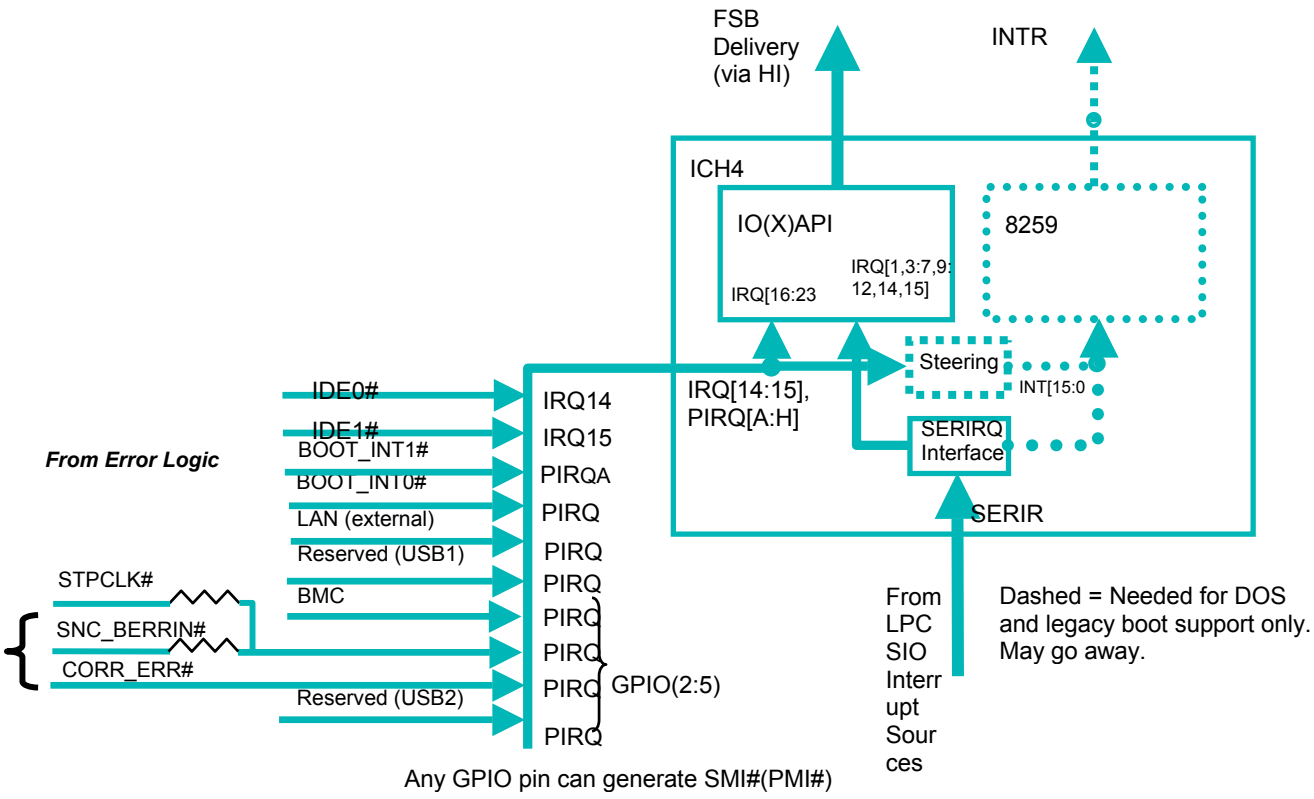


Figure 5-8. ICH4 IRQ Routing

The ICH4 provides the standard ACPI General Purpose Event (GPE) registers and controls the generation of the ACPI Scalable Coherent Interconnect (SCI) interrupt. Many sources of the SCI are internal to the ICH4, but the ICH4's GPIO 0 -15 can also generate SCI to the ICH4. The following figure shows the connectivity of those GPIOs.

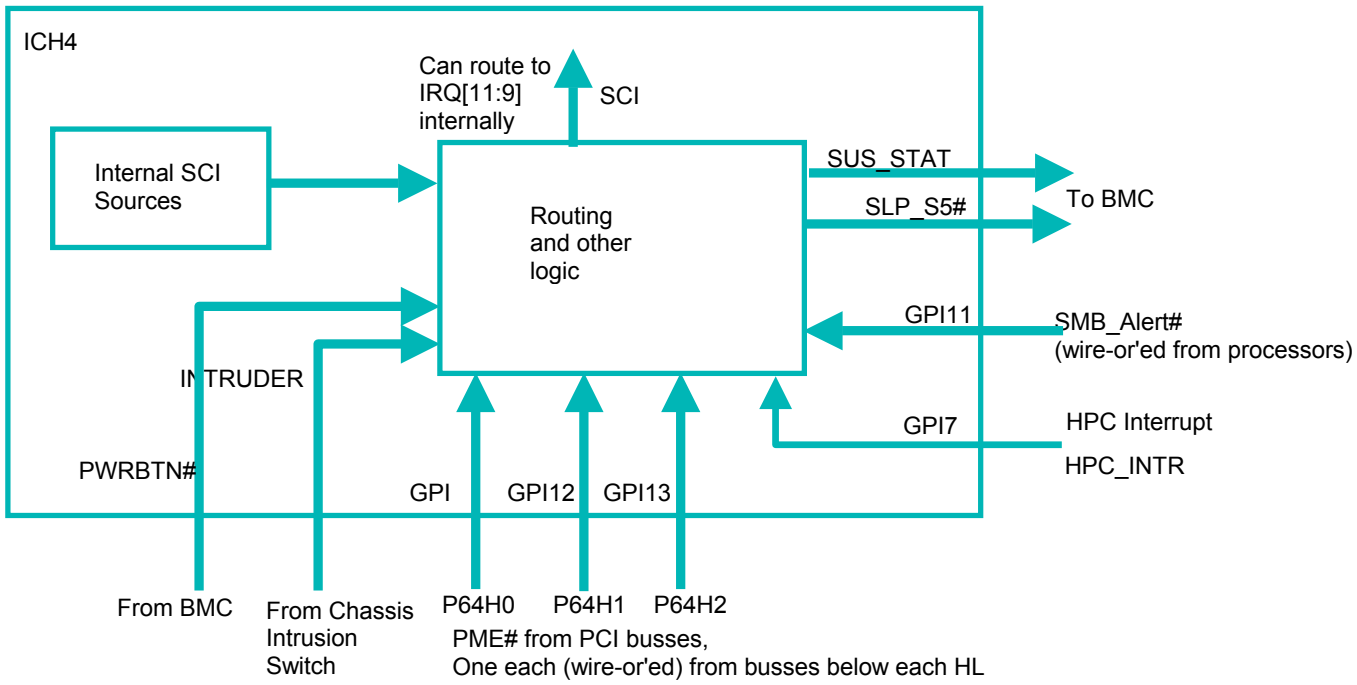


Figure 5-9. GPIO Connectivity

Note: This figure does not show the 870-INTOUT# signal for domain partitioning.

5.10 I/O Riser and I/O Board Interface

The following is the pinout list of the I/O riser's slot one edge finger.

Table 5-18. I/O Riser's Slot One Edge Finger Pinout

I/O Board	I/O Riser	Signal Name				Signal Name	I/O Riser	I/O Board
		Interlock01	B121		A121	CLK33_FWH4		
		VCC	B120		A120	GND		
		GND	B119		A119	CLK33_FWH8	FWH	CKFF
SIOH	ICH4	HL0	B118		A118	GND		
		GND	B117		A117	CLK33_FWH5	PCI2	CKFF
SIOH	ICH4	HL1	B116		A116	GND		
		GND	B115		A115	RESV1		
SIOH	ICH4	HL2	B114		A114	GND		
		GND	B113		A113	HL_PAR	ICH4	SIOH
SIOH	ICH4	HL3	B112		A112	GND		
		GND	B111		A111	HL_REQM	ICH4	SIOH

I/O Board	I/O Riser	Signal Name				Signal Name	I/O Riser	I/O Board
SIOH	ICH4	HL_STB	B110		A110	HL_REQI	ICH4	SIOH
		GND	B109		A109	IA64_IA32	FWH	CPU
SIOH	ICH4	HL_STB_L	B108		A108	SNC_BERRIN_L	ICH4-IRQF	I/O Board
		GND	B107		A107	CORR_ERR_L	ICH4-IRQG	I/O Board
SIOH	ICH4	HL4	B106		A106	VCC		
		GND	B105		A105	P5V_STDBY		
SIOH	ICH4	HL5	B104		A104	GND		
		GND	B103		A103	CLK33_FWH6	FWH	
SIOH	ICH4	HL6	B102		A102	GND		
		GND	B101		A101	CLK33_FWH9	FWH	CKFF
SIOH	ICH4	HL7	B100		A100	GND		
		GND	B99		A99	CLK33_FWH7	PLD1	CKFF
		P5V	B98		A98	GND		
		VCC	B97		A97	VCC_STDBY		
		GND	B96		A96	HL_STOP		
IDE CON	ICH4	PCI_IDE_RST_L	B95		A95	BUF_32KHZ		
IDE CON	ICH4	PDCS1_L	B94		A94	PDCS3_L	ICH4	IDE CON
IDE CON	ICH4	PDA2	B93		A93	PDA1	ICH4	IDE CON
IDE CON	ICH4	IRQ14	B92		A92	PDA0	ICH4	IDE CON
IDE CON	ICH4	PDDACK_L	B91		A91	PDIOR_L	ICH4	IDE CON
IDE CON	ICH4	PDIOW_L	B90		A90	PIORDY	ICH4	IDE CON
IDE CON	ICH4	PDDREQ	B89		A89	PDD0	ICH4	IDE CON
IDE CON	ICH4	PDD14	B88		A88	PDD15	ICH4	IDE CON
IDE CON	ICH4	PDD1	B87		A87	PDD2	ICH4	IDE CON
IDE CON		GND	B86		A86	VCC		
IDE CON	ICH4	PDD12	B85		A85	VCC		
IDE CON	ICH4	PDD3	B84		A84	GND		
IDE CON	ICH4	PDD4	B83		A83	PDD13	ICH4	IDE CON
IDE CON	ICH4	PDD10	B82		A82	PDD11	ICH4	IDE CON
IDE CON	ICH4	PDD9	B81		A81	PDD5	ICH4	IDE CON
IDE CON	ICH4	PDD8	B80		A80	A20M_L	ICH4	CPU?
IDE CON	ICH4	PDD6	B79		A79	FERR_L	ICH4	CPU?
IDE CON	ICH4	PDD7	B78		A78	IGNNE_L	ICH4	CPU?
870	ICH4	870_INTOUT_L	B77		A77	ERR1_CORR		
P64H2	ICH4-IRQA	BOOT_INT1_L	B76		A76	INTR	ICH4	CPU?
P64H2	ICH4_IRQB	BOOT_INT0_L	B75		A75	NMI	ICH4	CPU?
P64H2	ICH4	P64H0_PME_L	B74		A74	PMI_L	ICH4, BMC	CPU
P64H2	ICH4	P64H1_PME_L	B73		A73	VCC		
P64H2	ICH4	P64H2_PME_L	B72		A72	VCC		
		VCC_STDBY	B71		A71	GND		
		VCC_STDBY	B70		A70	GND		
		PLD2_SLOT1_IO2	B69		A69	VCC		
PULL HI	ICH4	SLAVE_BMC	B68		A68	GND		
		PLD2_SLOT1_IO3	B67		A67	VCC		

I/O Board	I/O Riser	Signal Name				Signal Name	I/O Riser	I/O Board
I/O	ICH4	ICH4_PWROK	B66		A66	GND		
		GND	B65		A65	CLK33_ICH4	ICH4	CKFF
		VCC	B64		A64	GND		
		GND	B63		A63	CLK48 _ICH4	ICH4	CKFF
CKFF	BMC	CLK33_BMC	B62		A62	GND		
		GND	B61		A61	CLK66_ICH4	ICH4	CKFF
CKFF	PLD2	CLK33_PLD2	B60		A60	GND		
		GND	B59		A59	INTRUDER_L		
		P5V_STDBY	B58		A58	MMGPI		
	ICH4	PROCHOT_L	B57		A57	HPC_INTR_L	ICH4, GPI7	
CPU	ICH4	STPCLK_L	B56		A56	SMBDATA		
		V_BAT	B55		A55	SMBCLK		
		GND	B54		A54	POWER_SW	BMC	Front Panel
Ser. Mag	BMC	I2C_IPMB_SCL	B53		A53	RESET_SW	BMC	Front Panel
Ser. Mag	BMC	I2C_IPMB_SDA	B52		A52	SDINT_SW	BMC	Front Panel
Ser. Mag	BMC	I2C_PCI_SCL	B51		A51	INIT_L		
Ser. Mag	BMC	I2C_PCI_SDA	B50		A50	SNCFWHWP_L		
8 way I/O	Only	BMC2BMC_SCL	B49		A49	FP_CHASIS_ID_SW_L		
		BMC2BMC_SDA	B48		A48	GND		
		GND	B47		A47	CLK14_ICH4	ICH4	CKFF
Ser. Mag	BMC	I2C_SYS_SCL	B46		A46	GND		
Ser. Mag	BMC	I2C_SYS_SDA	B45		A45	BMC_SLOT1_1		
Ser. Mag	BMC	I2C_SMB_SCL	B44		A44	Speaker	CPLD	Front Panel
Ser. Mag	BMC	I2C_SMB_SDA	B43		A43	ON_LED	BMC	Front Panel
Ser. Mag	BMC	I2C_IO_SCL	B42		A42	PWR_FLT_LED	BMC	Front Panel
Ser. Mag	BMC	I2C_IO_SDA	B41		A41	COOL_FLT_LED	BMC	Front Panel
		VCC	B40		A40	GEN_FLT_LED	BMC	Front Panel
I/O Board	BMC	IO_TCK	B39		A39	GND		
I/O Board	BMC	IO_TDI	B38		A38	LCD_RS	CPLD	Reserved
I/O Board	BMC	IO_TDO	B37		A37	LCD_E	CPLD	Reserved
I/O Board	BMC	IO_TMS	B36		A36	LCD_RW	CPLD	Reserved
I/O Board	BMC	IO_TRST_L	B35		A35	ISP_SCLK_LCD4	CPLD	Reserved
		P5V	B34		A34	ISP_MODE_LCD5	CPLD	
		GND	B33		A33	LCD6	CPLD	Reserved
		NODE1_HP_INT_L	B32		A32	ISP_SDO_LCD7	CPLD	Reserved
		NODE0_HP_INT_L	B31		A31	ISP_SDI	CPLD	Reserved
		P3.3V_STDBY_GD	B30		A30	ISP_EN_L	CPLD	ISP Chain
		GND	B29		A29	IO_ID0		
		IO_ID1	B28		A28	SERR_L		
		SYS_PWROK	B27		A27	PS_ON_L	PLD2	
		P12V_STDBY	B26		A26	SM_PWROK		
		P12V_STDBY	B25		A25	PLD_RST_L		
		P12V_STDBY	B24		A24	EX_RESET_L		

I/O Board	I/O Riser	Signal Name				Signal Name	I/O Riser	I/O Board
		P12V_STDBY	B23		A23	IO_ID2		
		P12V_STDBY	B22		A22	SYS_D2D_EN	PLD2	
		P12V_STDBY	B21		A21	ICMB_ID1_RX		
		P12V_STDBY	B20		A20	ICMB_ID2_RX		
		GND	B19		A19	ICMB_ID_TXEN		
		VCC_STDBY	B18		A18	ICMB_TX		
		VCC_STDBY	B17		A17	ICMB_RX		
		VCC_STDBY	B16		A16	ICMB_TXEN		
		VCC_STDBY	B15		A15	IS1_JTAGEN_L		
		VCC_STDBY	B14		A14	IS0_JTAGEN_L		
		GND	B13		A13	GND		
		VCC_STDBY	B12		A12	P5V		
		VCC_STDBY	B11		A11	GND		
		VCC_STDBY	B10		A10	CLK33_NIC	NIC	CKFF
		VCC_STDBY	B9		A9	GND		
		GND	B8		A8	CLK33_VID	Video	CKFF
		VCC	B7		A7	GND		
		VCC	B6		A6	CLK33_SIO	SIO	CKFF
		GND	B5		A5	GND		
		P5V	B4		A4	CLK14_SIO	PCI1	CKFF
		P5V	B3		A3	GND		
		P5V	B2		A2	P5V		
		Interlock1	B1		A1	P5V		

5.11 Power/Standby Power

The I/O riser has a total of seven different power rails. It receives 3.3 V main and 5 V main directly from the I/O board. The I/O riser receives 12-V Standby from the I/O board, which the I/O riser uses to convert into 3.3-V Standby and 5-V Standby. A portion of standby power is consumed on the I/O riser, but the majority is delivered back to the whole system. For ICH4 and video power, the I/O riser also needs to generate 1.5 V and 2.5 V power. The following list shows one Happy Valley* D2D circuit and four regulator circuits.

- HIP6004 D2D 12-V Standby → 3.3-V Standby, I Maximum = 6.9 A
- Regulator 12-V Standby → 5-V Standby, I Maximum = 300 mA
- Regulator 3.3 V → 1.5 V, I Maximum = 1 A for ICH4 core
- Zener* / FET 3.3-V Standby → 1.5-V Standby, I Maximum = 200 mA for ICH4 Power down
- Regulator 3.3 V → 2.5 V, I Maximum = 900 mA for Video chip

1.5-V/1.5-V Standby power is required by the ICH4 processor core while 2.5 V is required by the ATI video controller. 3.3-V Standby and 5-V Standby are generated from the I/O riser and delivered back to the system. Although the design of the 3.3-V Standby and 5-V Standby is 6.9-A and 300 mA, the I/O riser only uses a maximum of 1.4 A for 3.3-V Standby and 100 mA for 5-V Standby. Because of the height limitation on the lower portion of the I/O riser, a large capacitor cannot be placed on those standby power outputs near the Slot-1 edge. It is required that the I/O board has sufficient power when decoupling.

Both the BMC and ICH4 require power-up sequencing. The BMC requires that the 3.3-V Standby always powers up after the 5-V Standby, and powers down before 5-V Standby. In order to protect the BMC's 5 V tolerant I/O, several CMOS transistors are used to gate the 5-V Standby output from the regulator. The ICH4 requires that the 5-V input pins be powered first before the 3.3-V power is supplied to the I/O core. A simple diode (CR7D1) is used to solve this problem.

The following is the power distribution table for the I/O riser.

Table 5-19. Power Requirements for Intel® Server System SR870BN4 I/O Riser

3.3 V - Primary Supply (From I/O Board)			
Device	**Qty**	**Total Current (A)**	**Comment**
Video	1	0.90	Based on ATI* Rage 2C
SIO	1	0.02	SMC* LPC47S42x
FWH	6	0.53	Estimate based on RS-82802 FWH
ICH4 Core	1	1.67	Supply 1.8 V for ICH4 by regulator
Total 3.3 V		3.12	
5 V - Primary Supply (From I/O Board)		**2.26**	
Device	**Qty**	**Current (A)**	**Comment**
Miscellaneous 5 V components	1	0.1	RS232, miscellaneous,
PCI	1	3.00	PCI Maximum loading 3 Amp.
Total 5.0 V		3.1	
2.5 V - Power for Video device, Regulator from 3.3 Primary		**0.90**	
Device	**Qty**	**Current (A)**	**Comment**
ATI Rage* XL	1	0.90	0.9 A maximum.
Total 2.5 V		0.90	
2.5-V Regulator			
Efficiency (%)			Regulator from 3.3 V Primary --> 2.5 V, for video core
Thermal power (W)			

3.3 V - Primary Supply (From I/O Board)			
Device	Qty	Total Current (A)	Comment
Total Load on 3.3 V Primary		0.9	
1.5 V - Secondary Supply (Regulator from 3.3 V Primary)		**0.30**	
Device	**Qty**	**Current (A)**	**Comment**
ICH4	1	0.30	0.3 A Maximum
Total 1.5 V		0.30	
1.5-V Regulator			Regulator from 3.3 V Primary --> 1.8 V, for ICH4 core supply
Efficiency (%)			
Thermal power (W)			
Total Load on 3.3 V Primary		0.3	
1.5V_STDBY - Secondary Supply (Regulator from 3.3V_STDBY)		**0.12**	
Device	**Qty**	**Current (A)**	**Comment**
ICH4	1	0.12	120 mA maximum sleep power
Total 1.5V_STDBY		0.12	
1.5-V Regulator			1.5 V STDBY from Zener* and transistor regulation
Efficiency (%)			This is for ICH4 standby power. 120 mA maximum needed
Thermal power (W)			
Total Load on 3.3V_STDBY		0.120	
3.3-V Standby Supply		**4.43**	
Device	**Qty**	**Current (A)**	**Comment**
BMC (SM)	1	0.15	
Super I/O	1	0.001	SMC LPC47S42x
Server Management Devices	1	0.50	
ICH4	1	0.03	
I^2C bus level shifting	1	0.20	
82540 LAN device	1	0.20	82540 uses 200 mA at worst case
Lattice CPLD	2	0.24	
SPS I/O Board	1	3.11	Using SPS I/O for value
Non SPS I/O Board	1	2.88	Using SPS I/O for value
T4 Total 3.3 V STBY		4.43	

3.3 V - Primary Supply (From I/O Board)			
Device	Qty	Total Current (A)	Comment
3.3-V Standby Regulator			Embedded D2D regulated from 12V STBY --> 3.3V STBY
Efficiency (%)			Embedded D2D designed to handle maximum 6.9 A current
Thermal Power (W)			
T4 Total load on 12-V Standby		1.36	
5-V Standby Supply		0.20	
Device	**Qty**	**Current (A)**	**Comment**
ICMB Circuitry	**1**	**0.10**	
I/O Board	1	0.10	Using SPS I/O for value
Total 5 V STBY		0.20	
5 V Standby Regulator			12->5 Stdby Regulator designed for 250 mA maximum
Efficiency (%)			Put regulator near FAN
Thermal Power (W)			
Total load on 12-V Standby		0.20	
12 V Standby Supply (From I/O Board)		**1.99**	
Device	**Qty**	**Current (A)**	**Comment**
-12-V converter FET	1	0.14	
5-V Standby Converter	1	0.20	
5-V Standby Converter FET	1	0.14	
3.3V Standby Converter FET	1	0.14	
T4 3.3-V Standby Converter	1	1.36	
T4 Total 12-V STBY		1.99	

5.12 Strap Option Summary

Part	Default	Description
R6C11	DNI	Test for ICH4's GPIO16. (Integrated PU resistor)
R7D8	Install	45.3 Ohm pull 1.5V resistor to Hublink HL_COMP. Select Hublink-enhanced mode
R6M2	Install	PCI 33-MHz selection for video chip
R6N2	DNI	DNI = video enable, Install = video disable
R6M1	Install	Disable Video IRQ
R6C1	Install	Install = BMC is JTAG Master, ICE port disabled
R5C1	Install	Install = BMC is JTAG Master, ICE port disabled
R5C4	Install	Install = BMC is JTAG Master, ICE port disabled
R5C5	Install	Install = BMC is JTAG Master, ICE port disabled
R5C6	Install	Install = BMC is JTAG Master, ICE port disabled
C2D1	DNI	For Ethernet Electromagnetic Interference (EMI) Testing only
R5M1	DNI	DNI = ISP in normal status Install = ISP bypass resistor installed. OK to program I/O riser PLD standalone.

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6. Midplane Board

6.1 Introduction

The Server Board S870BN4 midplane section describes the basic functions and interface requirements of the midplane board. This board is designed to operate with the Server System SR870BN4 chassis.

6.2 Hardware Overview

The Server Board S870BN4 midplane board is a 10-layer printed circuit board, which interconnects the processor module, 4 Way I/O board, front panel, power distribution board, and SCSI backplane within the Server System SR870BN4.

6.2.1 S870BN4 Midplane

There are a total of six connectors located on the midplane board. Two VHDM connectors carry the scalability port bus between the processor module and I/O board. These VHDM connectors also carry miscellaneous signals that include clocks, reset, server management, and front panel. Each VHDM connector has three power modules used for power. In addition, the midplane contains two HDM connectors. These connectors provide direct blind mating from the I/O board and SCSI backplane to the midplane.

The midplane contains a connector interface to the power distribution board, which provides power to the processor/memory module, SCSI backplane and I/O Board. This connector contains two power blades that will be used for 48-volt power and 48-volt ground processor. The other pins on this connector are for power control signals, as well as delivering 12-volt standby to the processor module and I/O board. Additional pins are used for 12-volts coming from the SCSI backplane.

The midplane contains an edge card connector for the Server System SR870BN4 front panel that routes signals to the I/O board. Table 6-1 lists a summary of the connectors located on the midplane board.

Table 6-1. S870BN4 Midplane Features

Feature	Pins	Function
Connectors:		
VHDM	360 + 3P	Connects to PROCESSOR module
VHDM	360 + 3P	Connects to I/O Board
HDM	144	Connects to SCSI Backplane
HDM	144	Connects to the I/O board
Molex* Power	24 + 2P	Connects to the Power Distribution Board
AMP* Edge Card	14	Connects to the Front Panel

6.2.2 Block Diagram

Figure 6-1 illustrates the general overall architecture of the midplane board.

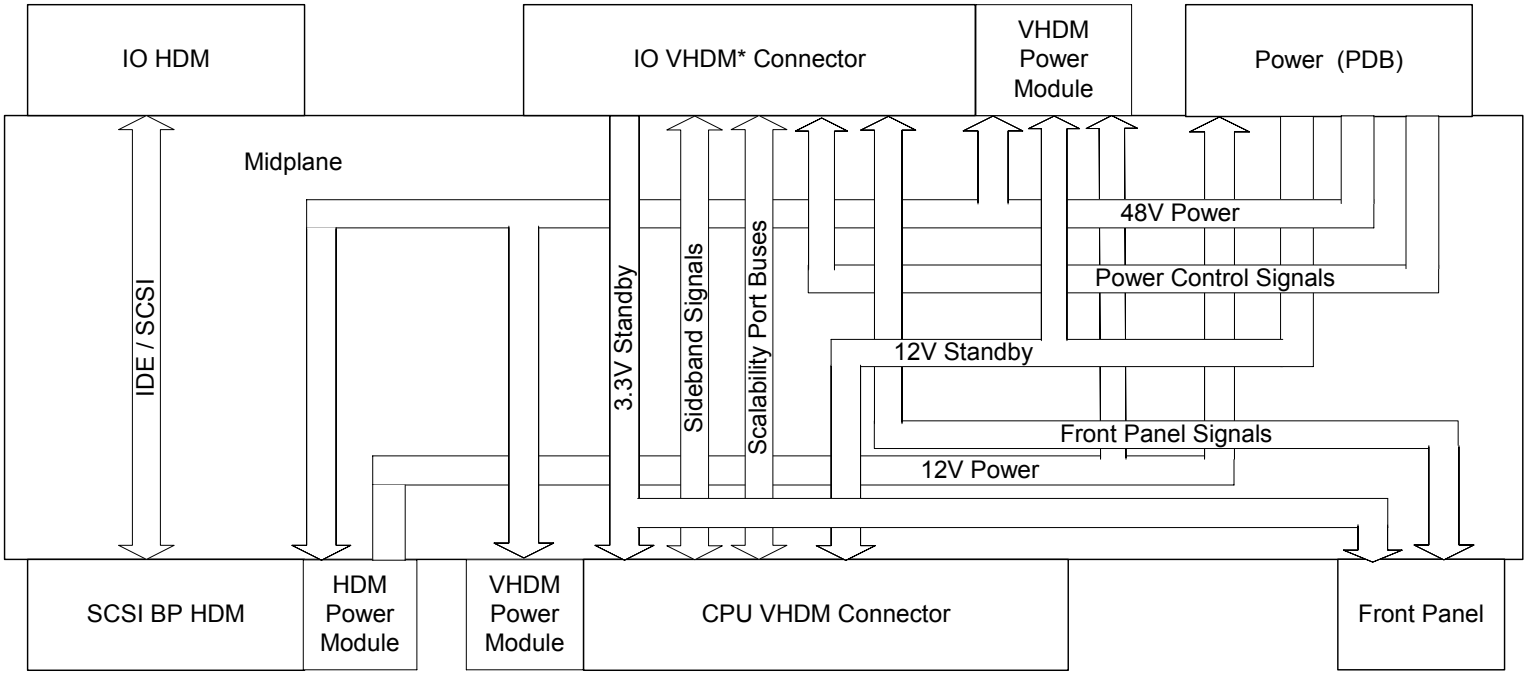

Figure 6-1. Midplane Block Diagram

6.2.3 Component Placement

Figure 6-2 illustrates the connector placement on the front side of the midplane board (primary side). Also illustrated is the placement of the ventilation holes. This side of the midplane board has three connectors: a VHDM header, an HDM header, and a 2x7 edge card connector. The VHDM header contains three power modules. This connector mates directly to the processor board. The HDM header, on this side of the board, also contains a power module. This connector mates directly to the SCSI backplane. The 2x7 edge card connector mates directly to the front panel.

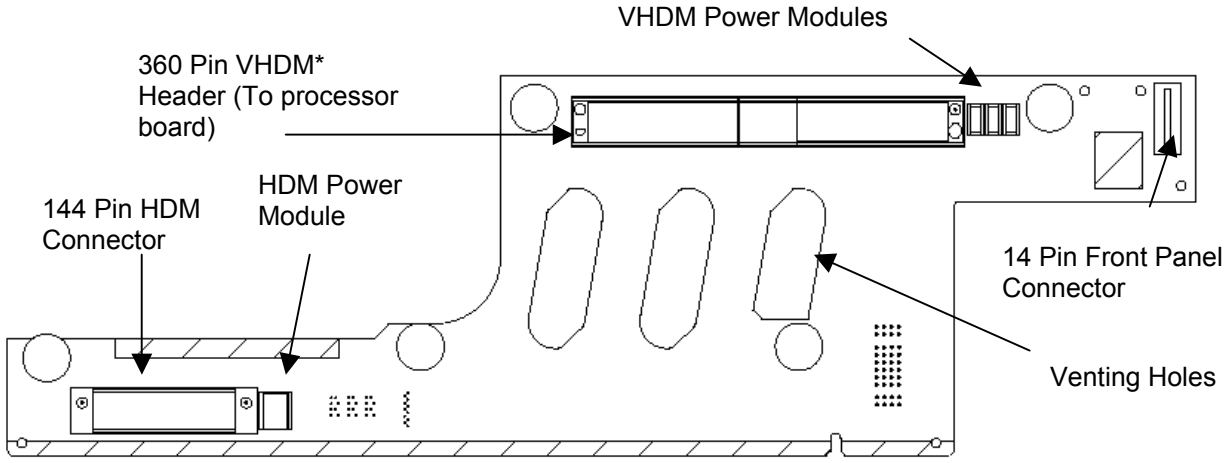

Figure 6-2. Intel® Server Board S870BN4 Midplane Primary Side (looking from processor side)

Figure 6-3 illustrates the connector placement on the backside of the midplane board (secondary side). This side of the board consists of three connectors. The connectors are a 4x6 + 2P, VHDM and HDM. The VHDM header contains three power modules and mates directly to the I/O board. The HDM connector on this side does not contain a power module. This HDM connector is basically a shroud that covers the pins that come through the midplane board from the primary side. The 24-pin with two power blades connector mates directly to the power distribution board.

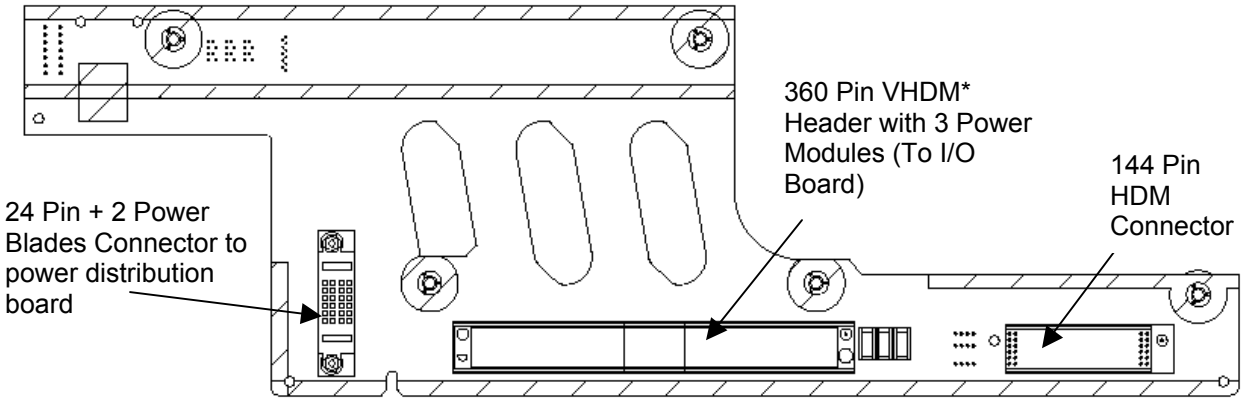

Figure 6-3. Intel® Server Board S870BN4 Midplane Secondary Side (looking from I/O side)

6.2.4 Component Part Numbers

Table 6-2 illustrates the connectors on the midplane and the corresponding manufacturer and Intel® part numbers.

Table 6-2. Connector Part Numbers

Connector	Manufacturer P/N Teradyne	Manufacturer P/N Molex	Intel P/N
6Row x 60Col VHDM with Power Module (PROCESSOR)	498-5125-002 496-5010-002 437-5050-000 498-5025-02	0740582502 070471002 0740296000 0740592502	728571-002 (6Row x 25Col) 728571-004 (6Row x 10Col) 728573-001 (Power Mod. Qty = 3) 728571-003 (6Row x 25Col)
6Row x 60Col VHDM with Power Module (IO)	Teradyne 498-5125-002 496-5010-002 437-5050-000 498-5025-02	0740582502 070471002 0740296000 0740592502	728571-002 (6Row x 25Col) 728571-004 (6Row x 10Col) 728573-001 (6Row x 25Col) 728571-003 (Power Mod. Qty = 3)
144 Pin HDM shroud with 1 guide (IO)	487-6124-090	738105000	710755-003
144 Pin HDM header with 1 guide and Power Module (SCSI BP)	437-5121-000	738022016 738022017 736560001	710754-011 (72 pin) 710754-012 (72 pin) 710591-002 (Power Mod.)

24 Pin Molex* with2 Power Blades	FCI-Berg 51666-001		A43180-001
14 Pin AMP* Edge Card connector	AMP 145269-4		A46681-001

6.2.5 Scalability Port

Scalability Port (SP) is a bus that allows simultaneous and bi-directional transmission of data on the same wire with a peak bandwidth of 3.2 GB/s in each direction. Details of the SP bus may be found in its respective specification. The SP bus will be routed on the midplane from the processor VHDM to the I/O VHDM. Currently, SP buses are routed at 45ohms. Sideband (SB) and Power (P) signals will also be located on these connectors. Figure 6-4 presents a block diagram displaying the two VHDM connectors on the midplane and where their respective SP signals are located. The figure is as seen from the primary side of the midplane.

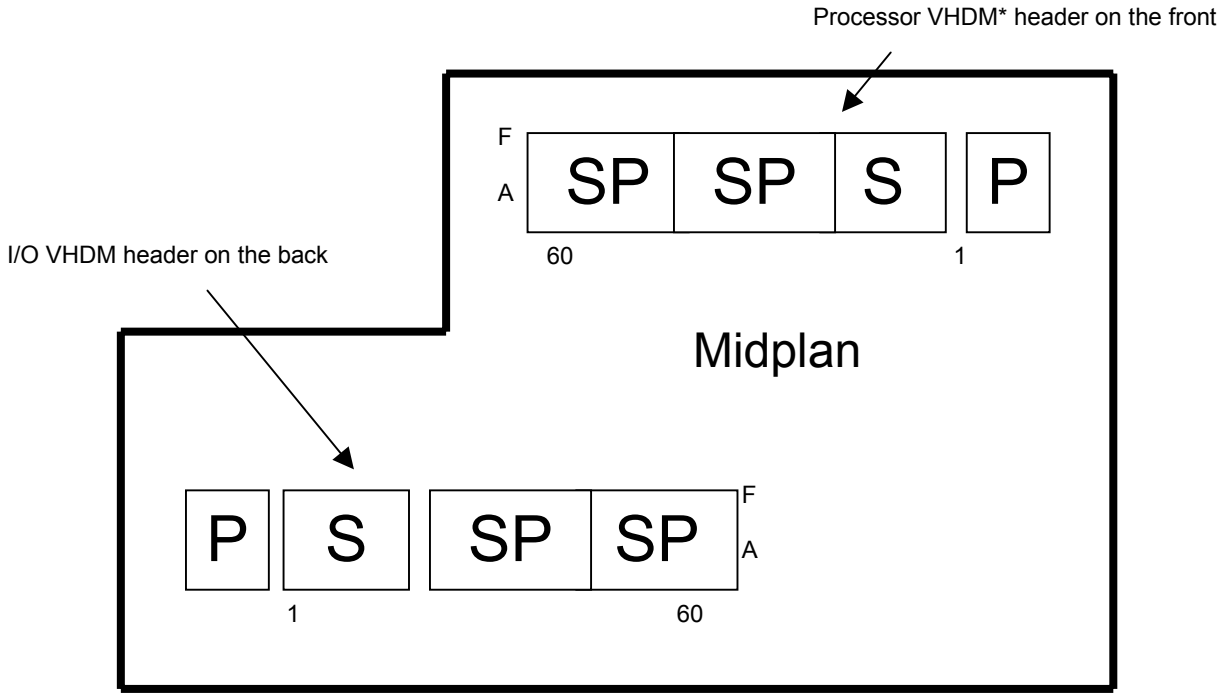

Figure 6-4. Signal Location on VHDM Connectors

6.3 Connector Pinouts

This section describes and tabulates the signals on the connectors.

6.3.1 Midplane/Power Distribution Board Interface

The interface between the midplane and power distribution board consist of one connector. This connector will deliver 48-volts to the I/O board, the processor board, and the SCSI backplane, and also deliver 12-volt standby to the I/O board and processor board. 12 volts will also come to this connector from the SCSI backplane. This will be used as a backup in case the fans on the power supply fail. The rest of the pins on this connector are used for power control signals.

Table 6-3. Midplane/Power Distribution Board Interface

Pin #	Signal	Description
P1	48V_GND	48-volt Return
P2	48V	48-volt Power
1A	12V_STDBY	12-volt Standby
2A	GND	Ground
3A	PS_OK_ORED	Power OK
4A	GND	Ground
5A	GND	Ground
6A	+12V	12-volts from SCSI BP (1A)
1B	12V_STDBY	12-volt Standby
2B	GND	Ground
3B	PS_ON_L	Power Supply On
4B	GND	Ground
5B	GND	Ground
6B	+12V	12-volts from SCSI BP (1A)
1C	12V_STDBY	12-volt Standby
2C	12V_STDBY	12-volt Standby
3C	GND	Ground
4C	I2C_IO_SDA	I2C Signals
5C	GND	Ground
6C	+12V	12-volts from SCSI BP (1A)
1D	12V_STDBY	12-volt Standby
2D	12V_STDBY	12-volt Standby
3D	GND	Ground
4D	I2C_IO_SCL	I2C Signals
5D	GND	Ground
6D	+12V	12-volts from SCSI BP (1A)

6.3.2 Midplane/Front Panel Interface

The interface between the midplane and front panel consists of one 14-pin edge card connector.

Table 6-4. Midplane/Front Panel Interface

Pin #	Signal	Description
1	COOL_FLT_LED	Fan/Temperature Fault
2	GEN_FLT_LED	HDD/Other Fault LED
3	PWR_FLT_LED	AC Power Fail LED
4	ON_LED	DC Power On LED
5	ID_LED	Chassis ID LED
6	SPEAKER	Speaker Drive Signal

7	CHASS_ID	Chassis ID
8	GND	Ground
9	GND	Ground
10	3.3V_STBY	Power Rail
11	3.3V_STBY	Power Rail
12	SDINT_SW	Non Maskable Interrupt
13	RESET_SW	Resets Server. POST Run
14	POWER_SW	Server DC Power On/Off Switch

6.3.3 Midplane / Processor Board Interface

The interface between the midplane and processor module consists of a 6 Row x 60 Column Teradyne*/Molex* VHDM connector with power module. The processor module will carry the right angle receptacle while the midplane carries the header. The VHDM connector has a high usable signal pin density as well as high-speed signal integrity, which is necessary for this application. Power is routed to the power module of this VHDM on the midplane from the power distribution board. Table 6-5 illustrates the VHDM connector pinout and signal description for the processor side.

Table 6-5. Midplane / Processor Interface (VHDM)

Pin #	Signal	Description
1A	RSVD	Reserved
2A	GND	Ground
3A	RSVD	Reserved
4A	RSVD	Reserved
5A	RSVD	Reserved
6A	GND	Ground
7A	RSVD	Reserved
8A	RSVD	Reserved
9A	RSVD	Reserved
10A	RSVD	Reserved
11A	CPU_INTERLOCK0_L	VHDM Connector interlocking detection
12A	I2C_CPU_SCL	I2C bus clock
13A	PPODOE	Enable processor
14A	SP0GPIO	Scalability Port General Purpose I/O
15A	THERMALERT_L	Indicates processor temperature out of range
16A	ERR0_L	Error Code Signal
17A	RSVD	Reserved
18A	AIPPODPG	All Installed PPOD Powergood
19A	PMI_L	Processor Management Interrupt
20A	A20M_L	A20 Mask
21A	PWRGOOD	Global Power Good from I/O Board
22A	SP0SYNC	Reset Synchronization
23A	SP1BD5	Scalability Port 1 Bus Signal

Pin #	Signal	Description
24A	GND	Ground
25A	SP1BVREFL1	Scalability Port 1 Bus Signal
26A	SP1BEP0	Scalability Port 1 Bus Signal
27A	GND	Ground
28A	SP1BSTBP0	Scalability Port 1 Bus Signal
29A	SP1BD1	Scalability Port 1 Bus Signal
30A	GND	Ground
31A	SNCFWHWP_L	
32A	SP1AD0	Scalability Port 1 Bus Signal
33A	SP1AVREFL0	Scalability Port 1 Bus Signal
34A	GND	Ground
35A	SP1ASTBP0	Scalability Port 1 Bus Signal
36A	SP1AEP1	Scalability Port 1 Bus Signal
37A	GND	Ground
38A	SP1AVREFH1	Scalability Port 1 Bus Signal
39A	SP1AD4	Scalability Port 1 Bus Signal
40A	GND	Ground
41A	SP0BD5	Scalability Port 0 Bus Signal
42A	GND	Ground
43A	SP0BVREFL1	Scalability Port 0 Bus Signal
44A	SP0BEP0	Scalability Port 0 Bus Signal
45A	GND	Ground
46A	SP0BSTBN0	Scalability Port 0 Bus Signal
47A	SP0BD1	Scalability Port 0 Bus Signal
48A	GND	Ground
49A	RSVD	Reserved
50A	SP0AD0	Scalability Port 0 Bus Signal
51A	SP0AVREFL0	Scalability Port 0 Bus Signal
52A	GND	Ground
53A	SP0AEP1	Scalability Port 0 Bus Signal
54A	SP0ASTBN0	Scalability Port 0 Bus Signal
55A	GND	Ground
56A	SP0AVREFH1	Scalability Port 0 Bus Signal
57A	SP0AD4	Scalability Port 0 Bus Signal
58A	GND	Ground
59A	BCLK	200 MHz System Clock
60A	GND	Ground
1B	GND	Ground
2B	RSVD	Reserved
3B	GND	Ground
4B	RSVD	Reserved
5B	GND	Ground

Pin #	Signal	Description
6B	RSVD	Reserved
7B	RSVD	Reserved
8B	RSVD	Reserved
9B	RSVD	Reserved
10B	RSVD	Reserved
11B	3.3V_STDBY	3.3-volt standby
12B	I2C_CPU_SDA	Connects to the processors, SNC, and misc. Server management functions on the processor and memory boards
13B	SP1GPIO	Scalability Port General Purpose I/O
14B	EV0_L	Event logic interconnect
15B	HP_INT_L	Node hot-plug interrupt
16B	ERR1_L	Error Code Signal
17B	RSVD	Reserved
18B	CD2D33EN	Enables 3.3V D2D on Processor Board
19B	FERR_L	Floating point error
20B	IGNNE_L	Ignore Numerical Error
21B	NODE_PG	Powergood from Processor Board D2Ds
22B	GND	Ground
23B	GND	Ground
24B	SP1BD7	Scalability Port 1 Bus Signal
25B	SP1BVREFH1	Scalability Port 1 Bus Signal
26B	GND	Ground
27B	SP1BD2	Scalability Port 1 Bus Signal
28B	SP1BEP2	Scalability Port 1 Bus Signal
29B	GND	Ground
30B	SP1BVREFH0	Scalability Port 1 Bus Signal
31B	SP1BD0	Scalability Port 1 Bus Signal
32B	GND	Ground
33B	SP1AVREFH0	Scalability Port 1 Bus Signal
34B	SP1AEP2	Scalability Port 1 Bus Signal
35B	SP1ASTBN0	Scalability Port 1 Bus Signal
36B	GND	Ground
37B	SP1AD3	Scalability Port 1 Bus Signal
38B	SP1AVREFL1	Scalability Port 1 Bus Signal
39B	GND	Ground
40B	SP1AD6	Scalability Port 1 Bus Signal
41B	GND	Ground
42B	SP0BD7	Scalability Port 0 Bus Signal
43B	SP0BVREFH1	Scalability Port 0 Bus Signal
44B	GND	Ground
45B	SP0BD2	Scalability Port 0 Bus Signal
46B	SP0BSTBP0	Scalability Port 0 Bus Signal

Pin #	Signal	Description
47B	GND	Ground
48B	SP0BVREFH0	Scalability Port 0 Bus Signal
49B	SP0BD0	Scalability Port 0 Bus Signal
50B	GND	Ground
51B	SP0AVREFH0	Scalability Port 0 Bus Signal
52B	SP0AEP2	Scalability Port 0 Bus Signal
53B	SP0ASTBP0	Scalability Port 0 Bus Signal
54B	GND	Ground
55B	SP0AD3	Scalability Port 0 Bus Signal
56B	SP0AVREFL1	Scalability Port 0 Bus Signal
57B	GND	Ground
58B	SP0AD6	Scalability Port 0 Bus Signal
59B	BCLK_L	200 MHz System Clock#
60B	GND	Ground
1C	RSVD	Reserved
2C	GND	Ground
3C	RSVD	Reserved
4C	GND	Ground
5C	RSVD	Reserved
6C	RSVD	Reserved
7C	RSVD	Reserved
8C	RSVD	Reserved
9C	RSVD	
10C	RSVD	
11C	3.3V_STDBY	3.3-volt standby
12C	BUSID1	Strap Bits that indicate the config. Bus # of SNC
13C	NODEID4	Strap Bits that indicate node ID to SNC
14C	EV1_L	Event logic interconnect
15C	RSVD	Reserved Pin
16C	ERR2_L	Error Code Signal
17C	BINITIN_L	
18C	BINITOUT_L	Indicates FSB BINIT# Pulled up to 3.3V on the processor board. SNC is 3.3V tolerant
19C	RSVD	Reserved Pin
20C	INIT_L	Processor Init
21C	RSVD	Reserved Pin
22C	SP1SYNC	Reset synchronization
23C	SP1BD6	Scalability Port 1 Bus Signal
24C	SP1BD4	Scalability Port 1 Bus Signal
25C	GND	Ground
26C	SP1BD3	Scalability Port 1 Bus Signal
27C	SP1BSTBN0	Scalability Port 1 Bus Signal
28C	GND	Ground

Pin #	Signal	Description
29C	SP1BEP1	Scalability Port 1 Bus Signal
30C	SP1BVREFL0	Scalability Port 1 Bus Signal
31C	GND	Ground
32C	SNCFWHDIS_L	
33C	GND	Ground
34C	SP1AD1	Scalability Port 1 Bus Signal
35C	GND	Ground
36C	SP1AD2	Scalability Port 1 Bus Signal
37C	SP1AEP0	Scalability Port 1 Bus Signal
38C	GND	Ground
39C	SP1AD7	Scalability Port 1 Bus Signal
40C	SP1AD5	Scalability Port 1 Bus Signal
41C	SP0BD6	Scalability Port 0 Bus Signal
42C	SP0BD4	Scalability Port 0 Bus Signal
43C	GND	Ground
44C	SP0BD3	Scalability Port 0 Bus Signal
45C	SP0BEP1	Scalability Port 0 Bus Signal
46C	GND	Ground
47C	SP0BEP2	Scalability Port 0 Bus Signal
48C	SP0BVREFL0	Scalability Port 0 Bus Signal
49C	GND	Ground
50C	3.3VSTDBY_FLT_L	3.3V Standby Fault
51C	GND	Ground
52C	SP0AD1	Scalability Port 0 Bus Signal
53C	GND	Ground
54C	SP0AD2	Scalability Port 0 Bus Signal
55C	SP0AEP0	Scalability Port 0 Bus Signal
56C	GND	Ground
57C	SP0AD7	Scalability Port 0 Bus Signal
58C	SP0AD5	Scalability Port 0 Bus Signal
59C	GND	Ground
60C	ISP_SDI	In-System Programming Data In
1D	GND	Ground
2D	GND	Ground
3D	RSVD	Reserved
4D	RSVD	Reserved
5D	RSVD	Reserved
6D	RSVD	Reserved
7D	RSVD	Reserved
8D	RSVD	Reserved
9D	RSVD	Reserved
10D	RSVD	Reserved

Pin #	Signal	Description
11D	NC	NO CONNECT
12D	BUSID2	Strap Bits that indicate the config. Bus # of SNC
13D	BUSID0	Strap Bits that indicate the config. Bus # of SNC
14D	NODEID3	Strap Bits that indicate node ID to SNC.
15D	NODEID2	Strap Bits that indicate node ID to SNC.
16D	NODEID1	Strap Bits that indicate node ID to SNC.
17D	RSVD	Reserved Pin
18D	NODEID0	Strap Bits that indicate node ID to SNC.
19D	IS_TCK	Test Clock to I/O board
20D	SYNC_CLK	Sync Clock
21D	RESETI_L	Resets SNC. SNC resets the FSB
22D	GND	Ground
23D	SP1BD14	Scalability Port 1 Bus Signal
24D	GND	Ground
25D	SP1BVREFL3	Scalability Port 1 Bus Signal
26D	SP1BSSO	Scalability Port 1 Bus Signal
27D	GND	Ground
28D	SP1BSTBN1	Scalability Port 1 Bus Signal
29D	SP1BD9	Scalability Port 1 Bus Signal
30D	GND	Ground
31D	IS_JTAGEN_L	
32D	SP1AD8	Scalability Port 1 Bus Signal
33D	SP1AVREFL2	Scalability Port 1 Bus Signal
34D	GND	Ground
35D	SP1ASTBP1	Scalability Port 1 Bus Signal
36D	SP1ARSVD	Scalability Port 1 Bus Signal
37D	GND	Ground
38D	SP1AVREFH3	Scalability Port 1 Bus Signal
39D	SP1AD12	Scalability Port 1 Bus Signal
40D	GND	Ground
41D	SP0BD14	Scalability Port 0 Bus Signal
42D	GND	Ground
43D	SP0BVREFL3	Scalability Port 0 Bus Signal
44D	SP0BSSO	Scalability Port 0 Bus Signal
45D	GND	Ground
46D	SP0BSTBN1	Scalability Port 0 Bus Signal
47D	SP0BD9	Scalability Port 0 Bus Signal
48D	GND	Ground
49D	STDBYEN	Standby Enable
50D	SP0AD8	Scalability Port 0 Bus Signal
51D	SP0AVREFL2	Scalability Port 0 Bus Signal
52D	GND	Ground

Pin #	Signal	Description
53D	SP0ASTBP1	Scalability Port 0 Bus Signal
54D	SP0ARSVD	Scalability Port 0 Bus Signal
55D	GND	Ground
56D	SP0AVREFH3	Scalability Port 0 Bus Signal
57D	SP0AD12	Scalability Port 0 Bus Signal
58D	GND	Ground
59D	GND	Ground
60D	ISP_SDO	In-System Programming Data Out
1E	GND	Ground
2E	RSVD	Reserved
3E	GND	Ground
4E	RSVD	Reserved
5E	RSVD	Reserved
6E	RSVD	Reserved
7E	RSVD	Reserved
8E	RSVD	Reserved
9E	RSVD	Reserved
10E	RSVD	Reserved
11E	12V_STDBY	12-volt standby
12E	RSVD	Reserved
13E	PROCHOT_L	Indicates the thermal throttled state
14E	EV2_L	Event logic interconnect
15E	RSVD	Reserved
16E	BERROUT_L	From SNC (M/F)
17E	RSVD	Reserved
18E	IS_TRST_L	Test Reset to I/O board
19E	IS_TDI	Test Data In from I/O board
20E	INTR	Interrupt Request
21E	SYNCEN_L	Sync Enable
22E	SP0PRES	Scalability port present
23E	GND	Ground
24E	SP1BD15	Scalability Port 1 Bus Signal
25E	SP1BVREFH3	Scalability Port 1 Bus Signal
26E	GND	Ground
27E	SP1BD10	Scalability Port 1 Bus Signal
28E	SP1BSTBP1	Scalability Port 1 Bus Signal
29E	GND	Ground
30E	SP1BVREFH2	Scalability Port 1 Bus Signal
31E	SP1BD8	Scalability Port 1 Bus Signal
32E	GND	Ground
33E	SP1AVREFH2	Scalability Port 1 Bus Signal
34E	SP1ALLC	Scalability Port 1 Bus Signal

Pin #	Signal	Description
35E	SP1ASTBN1	Scalability Port 1 Bus Signal
36E	GND	Ground
37E	SP1AD11	Scalability Port 1 Bus Signal
38E	SP1AVREFL3	Scalability Port 1 Bus Signal
39E	GND	Ground
40E	SP1AD13	Scalability Port 1 Bus Signal
41E	GND	Ground
42E	SP0BD15	Scalability Port 0 Bus Signal
43E	SP0BVREFH3	Scalability Port 0 Bus Signal
44E	GND	Ground
45E	SP0BD10	Scalability Port 0 Bus Signal
46E	SP0BSTBP1	Scalability Port 0 Bus Signal
47E	GND	Ground
48E	SP0BVREFH2	Scalability Port 0 Bus Signal
49E	SP0BD8	Scalability Port 0 Bus Signal
50E	GND	Ground
51E	SP0AVREFH2	Scalability Port 0 Bus Signal
52E	SP0ALLC	Scalability Port 0 Bus Signal
53E	SP0ASTBN1	Scalability Port 0 Bus Signal
54E	GND	Ground
55E	SP0AD11	Scalability Port 0 Bus Signal
56E	SP0AVREFL3	Scalability Port 0 Bus Signal
57E	GND	Ground
58E	SP0AD13	Scalability Port 0 Bus Signal
59E	ISP_MODE	In-System Programming Mode
60E	ISP_EN_L	In-System Programming Enable
1F	RSVD	Reserved
2F	GND	Ground
3F	RSVD	Reserved
4F	RSVD	Reserved
5F	RSVD	Reserved
6F	RSVD	Reserved
7F	RSVD	Reserved
8F	RSVD	Reserved
9F	RSVD	Reserved
10F	RSVD	Reserved
11F	12V_STDBY	12-volt standby
12F	RSVD	Reserved
13F	STPCLK_L	Stop clock for IA-32 support
14F	EV3_L	Event logic interconnect
15F	RSVD	Reserved
16F	INT_OUT_L	Used for Hot Plug module. Translated on processor board

Pin #	Signal	Description
17F	BERRIN_L	To SNC to generate machine check on FSB
18F	IS_TMS	Test Mode Select to I/O board
19F	IS_TDO	Test Data Out to I/O board
20F	NMI	Nonmaskable interrupt
21F	RESETO_L	From the SNC to reset the I/O subsystem
22F	SP1PRES	Scalability port present
23F	SP1BD13	Scalability Port 1 Bus Signal
24F	SP1BD12	Scalability Port 1 Bus Signal
25F	GND	Ground
26F	SP1BD11	Scalability Port 1 Bus Signal
27F	SP1BRSVD	Scalability Port 1 Bus Signal
28F	GND	Ground
29F	SP1BLLC	Scalability Port 1 Bus Signal
30F	SP1BVREFL2	Scalability Port 1 Bus Signal
31F	GND	Ground
32F	IA64_IA32	
33F	GND	Ground
34F	SP1AD9	Scalability Port 1 Bus Signal
35F	GND	Ground
36F	SP1AD10	Scalability Port 1 Bus Signal
37F	SP1ASSO	Scalability Port 1 Bus Signal
38F	GND	Ground
39F	SP1AD15	Scalability Port 1 Bus Signal
40F	SP1AD14	Scalability Port 1 Bus Signal
41F	SP0BD13	Scalability Port 0 Bus Signal
42F	SP0BD12	Scalability Port 0 Bus Signal
43F	GND	Ground
44F	SP0BD11	Scalability Port 0 Bus Signal
45F	SP0BDBG	Scalability Port 0 Bus Signal
46F	GND	Ground
47F	SP0BLLC	Scalability Port 0 Bus Signal
48F	SP0BVREFL2	Scalability Port 0 Bus Signal
49F	GND	Ground
50F	V48EN	48 V Enable
51F	GND	Ground
52F	SP0AD9	Scalability Port 0 Bus Signal
53F	GND	Ground
54F	SP0AD10	Scalability Port 0 Bus Signal
55F	SP0ASSO	Scalability Port 0 Bus Signal
56F	GND	Ground
57F	SP0AD15	Scalability Port 0 Bus Signal
58F	SP0AD14	Scalability Port 0 Bus Signal

Pin #	Signal	Description
59F	ISP_SCLK	In-System Programming Clock
60F	CPU_INTERLOCK1_L	VHDM Connector interlocking detection
PW11	48V	48V Power from PDB
PW12	48V	48V Power from PDB
PW13	48V	48V Power from PDB
PW14	48V	48V Power from PDB
PW15	48VGND	48V Ground to PDB
PW16	48VGND	48V Ground to PDB
PW17	48VGND	48V Ground to PDB
PW18	48VGND	48V Ground to PDB
PW21	48V	48V Power from PDB
PW22	48V	48V Power from PDB
PW23	48V	48V Power from PDB
PW24	48V	48V Power from PDB
PW25	48VGND	48V Ground to PDB
PW26	48VGND	48V Ground to PDB
PW27	48VGND	48V Ground to PDB
PW28	48VGND	48V Ground to PDB
PW31	48V	48V Power from PDB
PW32	48V	48V Power from PDB
PW33	48V	48V Power from PDB
PW34	48V	48V Power from PDB
PW35	48VGND	48V Ground to PDB
PW36	48VGND	48V Ground to PDB
PW37	48VGND	48V Ground to PDB
PW38	48VGND	48V Ground to PDB

6.3.3.1 NODEID and BUSID Assignments

NODEID signals are strap bits used to indicate the node ID to the Scalable Node Controller (SNC). BUSID signals are strap bits that indicate the configuration bus number of the SNC. These signals are pulled up on the processor board. The midplane will ground them or leave them as a no-connect depending on what the ID should be. For the four-way system, there is one SNC located on the processor board. Table 6-6 summarizes the NODEID and BUSID assignments.

Table 6-6. NODEID and BUSID Assignments

Signal	Value (1.5V CMOS)	Connection on Midplane
BUSID0	1	No Connect
BUSID1	1	No Connect
BUSID2	1	No Connect
NODEID0	0	Grounded

NODEID1	0	Grounded
NODEID2	0	Grounded
NODEID3	1	No Connect
NODEID4	1	No Connect

6.3.4 Midplane / I/O Board Interface

The interface between the I/O board and midplane consists of two separate connectors. The connectors are a VHDM connector and an HDM connector.

6.3.4.1 Midplane VHDM Connector

The interface between the midplane and I/O board consists of a 6 row x 60 column Teradyne*/Molex* VHDM connector with a power module. The I/O board will carry the right angle receptacle while the midplane carries the header. Power is routed to the power module of this VHDM on the midplane from the power distribution board. Table 6-7 illustrates the VHDM connector pinout as well as signal descriptions for the I/O side.

Table 6-7. Midplane / I/O Board Interface (VHDM)

Pin #	Signal	Description
1A	IO_INTERLOCK1_L	VHDM Connector interlocking detection
2A	RSVD	Reserved
3A	GND	Ground
4A	RSVD	Reserved
5A	RSVD	Reserved
6A	RSVD	Reserved
7A	LCD_RW	LCD Read Write
8A	LCD_RS	LCD Reset
9A	LCD_E	LCD Enable
10A	RSVD	Reserved
11A	STPCLK_L	Stop clock for IA-32 support
12A	EV3_L	Event logic interconnect
13A	RSVD	Reserved
14A	INT_OUT_L	Used for hot-plug module. Translated on processor board
15A	BERRIN_L	To SNC to generate machine check on FSB
16A	IS_TMS	Test Mode Select to I/O board
17A	IS_TDO	Test Data Out to I/O board
18A	NMI	Nonmaskable interrupt
19A	RESETO_L	From the SNC to reset the I/O subsystem
20A	GND	Ground
21A	BCLK_L	200 MHz System Clock
22A	GND	Ground
23A	SP0AD14	Scalability Port 0 Bus Signal
24A	SP0AD15	Scalability Port 0 Bus Signal
25A	GND	Ground

Pin #	Signal	Description
26A	SP0ASSO	Scalability Port 0 Bus Signal
27A	SP0AD10	Scalability Port 0 Bus Signal
28A	GND	Ground
29A	SP0AD9	Scalability Port 0 Bus Signal
30A	GND	Ground
31A	V48EN	48V Enable
32A	GND	Ground
33A	SP0BVREFL2	Scalability Port 0 Bus Signal
34A	SP0BLLC	Scalability Port 0 Bus Signal
35A	GND	Ground
36A	SP0BRSVD	Scalability Port 0 Bus Signal
37A	SP0BD11	Scalability Port 0 Bus Signal
38A	GND	Ground
39A	SP0BD12	Scalability Port 0 Bus Signal
40A	SP0BD13	Scalability Port 0 Bus Signal
41A	SP1AD14	Scalability Port 1 Bus Signal
42A	SP1AD15	Scalability Port 1 Bus Signal
43A	GND	Ground
44A	SP1ASSO	Scalability Port 1 Bus Signal
45A	SP1AD10	Scalability Port 1 Bus Signal
46A	GND	Ground
47A	SP1AD9	Scalability Port 1 Bus Signal
48A	GND	Ground
49A	IA64_IA32	
50A	GND	Ground
51A	SP1BVREFL2	Scalability Port 1 Bus Signal
52A	SP1BLLC	Scalability Port 1 Bus Signal
53A	GND	Ground
54A	SP1BRSVD	Scalability Port 1 Bus Signal
55A	SP1BD11	Scalability Port 1 Bus Signal
56A	GND	Ground
57A	SP1BD12	Scalability Port 1 Bus Signal
58A	SP1BD13	Scalability Port 1 Bus Signal
59A	SP1PRES	Scalability port present
60A	GND	Ground
1B	3.3V_STDBY	3.3-volt standby
2B	GND	Ground
3B	RSVD	Reserved
4B	RSVD	Reserved
5B	RSVD	Reserved
6B	RSVD	Reserved
7B	ISP_SDO_LCD7	In-System Programming Data Out

Pin #	Signal	Description
8B	ISP_SDI	In-System Programming Data In
9B	ISP_MODE_LCD5	In-System Programming Mode
10B	RSVD	Reserved
11B	PROCHOT_L	Indicates the thermal throttled state
12B	EV2_L	Event logic interconnect
13B	ID_LED	Chassis ID LED
14B	BERROUT_L	From SNC (M/F) only used in 8way
15B	RSVD	Reserved
16B	IS_TRST_L	Test Reset to I/O board
17B	IS_TDI	Test Data In from I/O board
18B	INTR	Interrupt Request
19B	RSVD	Reserved Pin
20B	GND	Ground
21B	BCLK	200 MHz System Clock
22B	GND	Ground
23B	SP0AD13	Scalability Port 0 Bus Signal
24B	GND	Ground
25B	SP0AVREFL3	Scalability Port 0 Bus Signal
26B	SP0AD11	Scalability Port 0 Bus Signal
27B	GND	Ground
28B	SP0ASTBN1	Scalability Port 0 Bus Signal
29B	SP0ALLC	Scalability Port 0 Bus Signal
30B	SP0AVREFH2	Scalability Port 0 Bus Signal
31B	GND	Ground
32B	SP0BD8	Scalability Port 0 Bus Signal
33B	SP0BVREFH2	Scalability Port 0 Bus Signal
34B	GND	Ground
35B	SP0BSTBP1	Scalability Port 0 Bus Signal
36B	SP0BD10	Scalability Port 0 Bus Signal
37B	GND	Ground
38B	SP0BVREFH3	Scalability Port 0 Bus Signal
39B	SP0BD15	Scalability Port 0 Bus Signal
40B	GND	Ground
41B	SP1AD13	Scalability Port 1 Bus Signal
42B	GND	Ground
43B	SP1AVREFL3	Scalability Port 1 Bus Signal
44B	SP1AD11	Scalability Port 1 Bus Signal
45B	GND	Ground
46B	SP1ASTBN1	Scalability Port 1 Bus Signal
47B	SP1ALLC	Scalability Port 1 Bus Signal
48B	SP1AVREFH2	Scalability Port 1 Bus Signal
49B	GND	Ground

Pin #	Signal	Description
50B	SP1BD8	Scalability Port 1 Bus Signal
51B	SP1BVREFH2	Scalability Port 1 Bus Signal
52B	GND	Ground
53B	SP1BSTBP1	Scalability Port 1 Bus Signal
54B	SP1BD10	Scalability Port 1 Bus Signal
55B	GND	Ground
56B	SP1BVREFH3	Scalability Port 1 Bus Signal
57B	SP1BD15	Scalability Port 1 Bus Signal
58B	GND	Ground
59B	SP0PRES	Scalability port present
60B	PS_OK_ORED	Power OK (to power distribution board)
1C	3.3V_STDBY	3.3-volt standby
2C	RSVD	Reserved
3C	GND	Ground
4C	RSVD	Reserved
5C	RSVD	Reserved
6C	RSVD	Reserved
7C	RSVD	Reserved
8C	ISP_EN_L	In-System Programming Enable
9C	ISP_SCLK	In-System Programming Clock
10C	ON_LED	Indicates when power is on (to FP)
11C	COOL_FLT_LED	Indicates cooling failure due to fan fail (to FP)
12C	PWR_FLT_LED	Indicates Power supply or D2D failure (to FP)
13C	SPEAKER	Speaker (to FP)
14C	POWER_SW	Power ON/OFF switch (to FP)
15C	RESET_SW	System reset switch (to FP)
16C	SDINT_SW	Used for OS debug
17C	IS_TCK	Test Clock to I/O Board
18C	RSVD	Reserved Pin
19C	RESETI_L	Resets SNC; the SNC resets the FSB
20C	MIDP_ID(1)	Midplane ID
21C	GND	Ground
22C	GND	Ground
23C	GND	Ground
24C	SP0AD12	Scalability Port 0 Bus Signal
25C	SP0AVREFH3	Scalability Port 0 Bus Signal
26C	GND	Ground
27C	SP0ARSVD	Scalability Port 0 Bus Signal
28C	SP0ASTBP1	Scalability Port 0 Bus Signal
29C	GND	Ground
30C	SP0AVREFL2	Scalability Port 0 Bus Signal
31C	SP0AD8	Scalability Port 0 Bus Signal

Pin #	Signal	Description
32C	STDBYEN	Standby Enable
33C	GND	Ground
34C	SP0BD9	Scalability Port 0 Bus Signal
35C	SP0BSTBN1	Scalability Port 0 Bus Signal
36C	GND	Ground
37C	SP0BSSO	Scalability Port 0 Bus Signal
38C	SP0BVREFL3	Scalability Port 0 Bus Signal
39C	GND	Ground
40C	SP0BD14	Scalability Port 0 Bus Signal
41C	GND	Ground
42C	SP1AD12	Scalability Port 1 Bus Signal
43C	SP1AVREFH3	Scalability Port 1 Bus Signal
44C	GND	Ground
45C	SP1ARSVD	Scalability Port 1 Bus Signal
46C	SP1ASTBP1	Scalability Port 1 Bus Signal
47C	GND	Ground
48C	SP1AVREFL2	Scalability Port 1 Bus Signal
49C	SP1AD8	Scalability Port 1 Bus Signal
50C	IS_JTAGEN_L	
51C	GND	Ground
52C	SP1BD9	Scalability Port 1 Bus Signal
53C	SP1BSTBN1	Scalability Port 1 Bus Signal
54C	GND	Ground
55C	SP1BSSO	Scalability Port 1 Bus Signal
56C	SP1BVREFL3	Scalability Port 1 Bus Signal
57C	GND	Ground
58C	SP1BD14	Scalability Port 1 Bus Signal
59C	GND	Ground
60C	PS_ON_L	Power Supply ON signal (to power distribution board)
1D	RSVD	Reserved
2D	GND	Ground
3D	RSVD	Reserved
4D	RSVD	Reserved
5D	RSVD	Reserved
6D	RSVD	Reserved
7D	RSVD	Reserved
8D	LCD6	
9D	LCD4	
10D	MIDP_ID(2)	Midplane ID
11D	GEN_FLT_LED	Indicates Board connectivity problems (to FP)
12D	EV1_L	Event logic interconnect
13D	RSVD	Reserved Pin

Pin #	Signal	Description
14D	ERR2_L	Error Code Signals
15D	BINITIN_L	
16D	BINITOUT_L	From SNC (M/F)
17D	RSVD	Reserved Pin
18D	INIT_L	Processor Init
19D	RSVD	Reserved Pin
20D	MIDP_ID(0)	Midplane ID
21D	GND	Ground
22D	GND	Ground
23D	SP0AD5	Scalability Port 0 Bus Signal
24D	SP0AD7	Scalability Port 0 Bus Signal
25D	GND	Ground
26D	SP0AEP0	Scalability Port 0 Bus Signal
27D	SP0AD2	Scalability Port 0 Bus Signal
28D	GND	Ground
29D	SP0AD1	Scalability Port 0 Bus Signal
30D	GND	Ground
31D	3.3VSTDBY_FLT_L	3.3V Standby Fault
32D	GND	Ground
33D	SP0BVREFL0	Scalability Port 0 Bus Signal
34D	SP0BEP2	Scalability Port 0 Bus Signal
35D	GND	Ground
36D	SP0BEP1	Scalability Port 0 Bus Signal
37D	SP0BD3	Scalability Port 0 Bus Signal
38D	GND	Ground
39D	SP0BD4	Scalability Port 0 Bus Signal
40D	SP0BD6	Scalability Port 0 Bus Signal
41D	SP1AD5	Scalability Port 1 Bus Signal
42D	SP1AD7	Scalability Port 1 Bus Signal
43D	GND	Ground
44D	SP1AEP0	Scalability Port 1 Bus Signal
45D	SP1AD2	Scalability Port 1 Bus Signal
46D	GND	Ground
47D	SP1AD1	Scalability Port 1 Bus Signal
48D	GND	Ground
49D	SNCFWHDIS_L	
50D	GND	Ground
51D	SP1BVREFL0	Scalability Port 1 Bus Signal
52D	SP1BEP1	Scalability Port 1 Bus Signal
53D	GND	Ground
54D	SP1BSTBN0	Scalability Port 1 Bus Signal
55D	SP1BD3	Scalability Port 1 Bus Signal

Pin #	Signal	Description
56D	GND	Ground
57D	SP1BD4	Scalability Port 1 Bus Signal
58D	SP1BD6	Scalability Port 1 Bus Signal
59D	SP1SYNC	Reset synchronization
60D	GND	Ground
1E	BYPEN66	
2E	RSVD	Reserved
3E	GND	Ground
4E	RSVD	Reserved
5E	RSVD	Reserved
6E	RSVD	Reserved
7E	RSVD	Reserved
8E	CHASS_ID	Chassis ID Switch Signal
9E	I2C_IO_SCL	I2C Clock connected to chipset (to power distribution board)
10E	I2C_CPU_SDA	I2C Clock connected to chipset
11E	SP1GPIO	Scalability Port General Purpose I/O
12E	EV0_L	Event logic interconnect
13E	HP_INT_L	Node hot-plug interrupt
14E	ERR1_L	Error Code Signals
15E	RSVD	TLB purge not done
16E	CD2D33EN	Enables 3.3V D2D on processor board
17E	FERR_L	Floating point error
18E	IGNNE_L	Ignore Numerical Error
19E	NODE_PG	Power good from processor board D2Ds
20E	GND	Ground
21E	SV_PECL_IN_L	200 MHz System Clock
22E	GND	Ground
23E	SP0AD6	Scalability Port 0 Bus Signal
24E	GND	Ground
25E	SP0AVREFL1	Scalability Port 0 Bus Signal
26E	SP0AD3	Scalability Port 0 Bus Signal
27E	GND	Ground
28E	SP0ASTBP0	Scalability Port 0 Bus Signal
29E	SP0AEP2	Scalability Port 0 Bus Signal
30E	SP0AVREFH0	Scalability Port 0 Bus Signal
31E	GND	Ground
32E	SP0BD0	Scalability Port 0 Bus Signal
33E	SP0BVREFH0	Scalability Port 0 Bus Signal
34E	GND	Ground
35E	SP0BSTBP0	Scalability Port 0 Bus Signal
36E	SP0BD2	Scalability Port 0 Bus Signal
37E	GND	Ground

Pin #	Signal	Description
38E	SP0BVREFH1	Scalability Port 0 Bus Signal
39E	SP0BD7	Scalability Port 0 Bus Signal
40E	GND	Ground
41E	SP1AD6	Scalability Port 1 Bus Signal
42E	GND	Ground
43E	SP1AVREFL1	Scalability Port 1 Bus Signal
44E	SP1AD3	Scalability Port 1 Bus Signal
45E	GND	Ground
46E	SP1ASTBN0	Scalability Port 1 Bus Signal
47E	SP1AEP2	Scalability Port 1 Bus Signal
48E	SP1AVREFH0	Scalability Port 1 Bus Signal
49E	GND	Ground
50E	SP1BD0	Scalability Port 1 Bus Signal
51E	SP1BVREFH0	Scalability Port 1 Bus Signal
52E	GND	Ground
53E	SP1BEP2	Scalability Port 1 Bus Signal
54E	SP1BD2	Scalability Port 1 Bus Signal
55E	GND	Ground
56E	SP1BVREFH1	Scalability Port 1 Bus Signal
57E	SP1BD7	Scalability Port 1 Bus Signal
58E	GND	Ground
59E	GND	Ground
60E	INTRUSION	Chassis Intrusion
1F	CPU_INTERLOCK_L	
2F	GND	Ground
3F	RSVD	Reserved
4F	RSVD	Reserved
5F	RSVD	Reserved
6F	RSVD	Reserved
7F	RSVD	Reserved
8F	RSVD	Reserved
9F	I2C_IO_SDA	I2C* Clock connected to chipset (to power distribution board)
10F	I2C_CPU_SCL	I2C Clock connected to chipset
11F	PPODOE	Enable processor
12F	SP0GPIO	Scalability Port General Purpose I/O
13F	THERMALERT_L	Indicates processor temp out of range
14F	ERR0_L	Error Code Signal
15F	RSVD	Reserved
16F	AIPPODPG	All installed PPOD powergood
17F	PMI_L	Processor Management Interrupt (SMI_L)
18F	A20M_L	A20 Mask
19F	PWRGOOD	Global Power good from I/O Board

Pin #	Signal	Description
20F	GND	Ground
21F	SV_PECL_IN	200 MHz System Clock
22F	GND	Ground
23F	GND	Ground
24F	SP0AD4	Scalability Port 0 Bus Signal
25F	SP0AVREFH1	Scalability Port 0 Bus Signal
26F	GND	Ground
27F	SP0ASTBN0	Scalability Port 0 Bus Signal
28F	SP0AEP1	Scalability Port 0 Bus Signal
29F	GND	Ground
30F	SP0AVREFL0	Scalability Port 0 Bus Signal
31F	SP0AD0	Scalability Port 0 Bus Signal
32F	RSVD	
33F	GND	Ground
34F	SP0BD1	Scalability Port 0 Bus Signal
35F	SP0BSTBN0	Scalability Port 0 Bus Signal
36F	GND	Ground
37F	SP0BEP0	Scalability Port 0 Bus Signal
38F	SP0BVREFL1	Scalability Port 0 Bus Signal
39F	GND	Ground
40F	SP0BD5	Scalability Port 0 Bus Signal
41F	GND	Ground
42F	SP1AD4	Scalability Port 1 Bus Signal
43F	SP1AVREFH1	Scalability Port 1 Bus Signal
44F	GND	Ground
45F	SP1AEP1	Scalability Port 1 Bus Signal
46F	SP1ASTBP0	Scalability Port 1 Bus Signal
47F	GND	Ground
48F	SP1AVREFL0	Scalability Port 1 Bus Signal
49F	SP1AD0	Scalability Port 1 Bus Signal
50F	SNCFWHWP_L	
51F	GND	Ground
52F	SP1BD1	Scalability Port 1 Bus Signal
53F	SP1BSTBP0	Scalability Port 1 Bus Signal
54F	GND	Ground
55F	SP1BEP0	Scalability Port 1 Bus Signal
56F	SP1BVREFL1	Scalability Port 1 Bus Signal
57F	GND	Ground
58F	SP1BD5	Scalability Port 1 Bus Signal
59F	SP0SYNC	Reset Synchronization
60F	IO_INTERLOCK0_L	VHDM* Connector interlocking detection
PW11	48V	48V Power from power distribution board

Pin #	Signal	Description
PW12	48V	48V Power from power distribution board
PW13	48V	48V Power from power distribution board
PW14	48V	48V Power from power distribution board
PW15	48VGND	48V Ground to power distribution board
PW16	48VGND	48V Ground to power distribution board
PW17	48VGND	48V Ground to power distribution board
PW18	48VGND	48V Ground to power distribution board
PW21	48V	48V Power from power distribution board
PW22	48V	48V Power from power distribution board
PW23	48V	48V Power from power distribution board
PW24	48V	48V Power from power distribution board
PW25	48VGND	48V Ground to power distribution board
PW26	48VGND	48V Ground to power distribution board
PW27	48VGND	48V Ground to power distribution board
PW28	48VGND	48V Ground to power distribution board
PW31	12V	12 V from SCSI BP
PW32	12V	12 V from SCSI BP
PW33	12V	12 V from SCSI BP
PW34	12V	12 V from SCSI BP
PW35	12V_STDBY	12 V standby from power distribution board
PW36	12V_STDBY	12 V standby from power distribution board
PW37	12V_STDBY	12 V standby from power distribution board
PW38	12V_STDBY	12 V standby from power distribution board

6.3.4.2 Midplane ID

There are three signals on the I/O VHDM that are reserved for the Server Board S870BN4 midplane ID. The signals are MIDP_(0), MIDP_(1), and MIDP_(2). These signals can be read from the I/O board. Grounding the net on the midplane results in a low ID (0); leaving the net unconnected results in a high ID (1). Table 6-8 summarizes this feature.

Table 6-8. Midplane ID

Board FAB	MIDP_(2)	MIDP_(1)	MIDP_(0)
Beta Board ID (Fab3)	0	1	0

6.3.4.3 Midplane HDM Connector (I/O Side)

The HDM connector on the I/O side is a 144-pin shroud with one guide. HDM has high signal-pin density along with high-speed signal integrity, which reduces cross talk. These features are required for SCSI and Integrated Drive Electronics (IDE) signals. This connector will not require any routing on the midplane board. The pins on the HDM will go directly through the midplane from the SCSI backplane side to the I/O board side. Figure 6-5 illustrates the HDM connector concept. Note that on the actual board, the 3x4 power module is located on the other side (left side) of the 144-pin header with two guide pins.

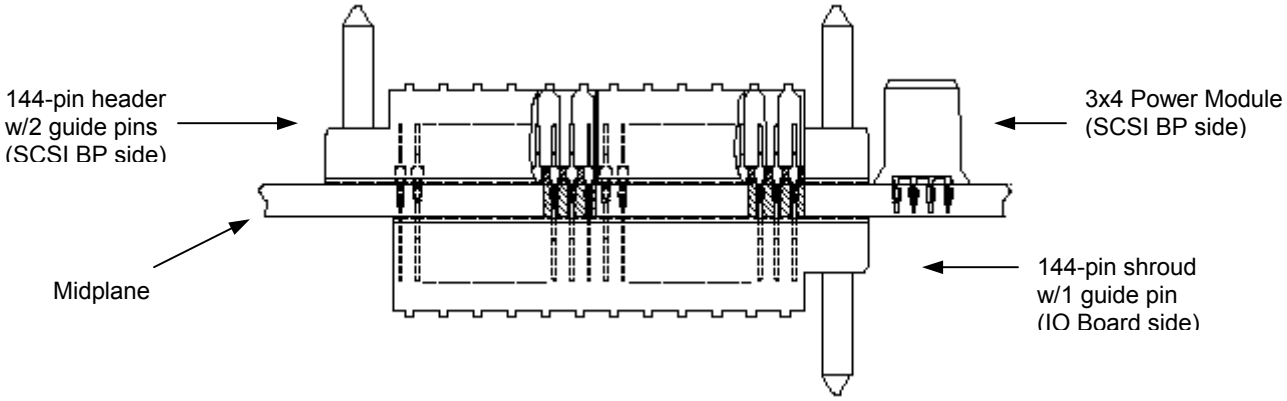

Figure 6-5. HDM Connector Concept

The signals go directly from the I/O HDM shroud, on the midplane, to the SCSI backplane HDM header, also on the midplane.

6.3.5 Midplane / SCSI Backplane Interface

The disk bay connector on the SCSI backplane side of the midplane is a 144-pin HDM header with two guides. This HDM connector also contains a power module. Power is routed on the midplane from the power distribution board to this HDM header. Table 6-9 shows the HDM power module pinout.

Table 6-9. HDM Power Module Pinout (SCSI Backplane Side)

Pin	Signal	Description
A (1)	12V	+12V Supply
D (2)	48V	+48V Supply
F (3)	48V GND	Isolated +48V Return

The following table shows the HDM connector pinout.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	SCSI_A:DB_12N	B1	SCSI_A:DB_13N	C1	HDM_MATED_0	D1	P_GND	E1	ISP_EN_L	F1	ISP_TCK
A2	SCSI_A: DB_12P	B2	SCSI_A: DB_13P	C2	P_CS3	D2	P_CS1	E2	S_CS3	F2	S_CS1
A3	SCSI_A: DB_14N	B3	SCSI_A: DB_15N	C3	P_DA2	D3	P_DA0	E3	S_DA2	F3	S_DA0
A4	SCSI_A: DB_14P	B4	SCSI_A: DB_15P	C4	P_IRQR	D4	P_DA1	E4	S_IRQR	F4	S_DA1
A5	SCSI_A: DB_P1N	B5	SCSI_A: DB_0N	C5	P_GND	D5	P_DMACK_L	E5	S_GND	F5	S_DMACK_L
A6	SCSI_A: DB_P1P	B6	SCSI_A: DB_0P	C6	SCSI_A:GND	D6	P_IORDY	E6	GND(12V RTN)	F6	S_IORDY
A7	SCSI_A: DB_1N	B7	SCSI_A: DB_2N	C7	P_GND	D7	P_DIOR_L	E7	S_GND	F7	S_DIOR_L
A8	SCSI_A: DB_1P	B8	SSI_A: DB_2P	C8	P_GND	D8	P_DIOW_L	E8	S_GND	F8	S_DIOW_L
A9	SCSI_A: DB_3N	B9	SCSI_A: DB_4N	C9	P_GND	D9	P_DMARQ	E9	S_GND	F9	S_DMARQ
A10	SCSI_A: DB_3P	B10	SCSI_A: DB_4P	C10	P_DD15	D10	P_GND	E10	S_DD15	F10	S_GND
A11	SCSI_A: DB_5N	B11	SCSI_A: DB_6N	C11	P_DD14	D11	P_DD0	E11	S_DD14	F11	S_DD0
A12	SCSI_A: DB_5P	B12	SCSI_A: DB_6P	C12	P_DD13	D12	P_DD1	E12	S_DD13	F12	S_DD1
A13	SCSI_A: DB_7N	B13	SCSI_A: DB_P0N	C13	P_DD12	D13	P_DD2	E13	S_DD12	F13	S_DD2
A14	SCSI_A: DB_7P	B14	SCSI_A: DB_P0P	C14	P_DD11	D14	P_DD3	E14	S_DD11	F14	S_DD3
A15	SCSI_A:ATN_N	B15	SCSI_A:BSY_N	C15	P_DD10	D15	P_DD4	E15	S_DD10	F15	S_DD4
A16	SCSI_A:ATN_P	B16	SCSI_A:BSY_P	C16	P_DD9	D16	P_DD5	E16	S_DD9	F16	S_DD5
A17	SCSI_A:ACK_N	B17	SCSI_A:RST_N	C17	P_DD8	D17	P_DD6	E17	S_DD8	F17	S_DD6
A18	SCSI_A:ACK_P	B18	SCSI_A:RST_P	C18	SCSI_A:GND	D18	P_DD7	E18	GND(12V RTN)	F18	S_DD7
A19	SCSI_A:MSG_N	B19	SCSI_A:SEL_N	C19	ISP_TDO	D19	P_RESET_L	E19	GND(12V RTN)	F19	S_RESET_L
A20	SCSI_A:MSG_P	B20	SCSI_A:SEL_P	C20	SCSI_A :GND	D20	SCSI_A:GND	E20	IPMCLK	F20	SCSI_5V_SAMPL
A21	SCSI_A:CD_N	B21	SCSI_A:REQ_N	C21	SCSI_A:IO_N	D21	SCSI_A:GND	E21	IPMBD	F21	12V_SENSE
A22	SCSI_A:CD_P	B22	SCSI_A:REQ_P	C22	SCSI_A:IO_P	D22	SCSI_A:DIFFSEN	E22	5V_Standby	F22	SCSI_PWRGD
A23	SCSI_A:8_N	B23	SCSI_A:DB_11N	C23	SCSI_A:DB_10N	D23	SCSI_A:DB_9N	E23	PWRGD	F23	ISP_TDI
A24	SCSI_A:8_P	B24	SCSI_A:DB_11P	C24	SCSI_A:DB_10P	D24	SCSI_A:DB_9P	E24	ISP_TMS	F24	HDM_MATED_1

6.4 Electrical and Mechanical Specifications

This section defines the electrical and mechanical outline of the Server Board S870BN4 midplane.

6.4.1 Midplane Board Thermal Requirements

The midplane board has no active components. There are no unique board thermal requirements other than those stated in the *SR870BN4 System EPS*.

6.4.2 Power Requirements

Table 6-10 shows the expected power draw seen by the midplane board. Note that the midplane does not have any active components. Also, the values may change depending on configuration.

Table 6-10. Power Requirements for the Intel® Server Board S870BN4 Midplane

12V Standby		
Device	**Power (W)**	**Current (A)**
Processor Board	12.77	1.05
IO Board	32.35	2.65
3.3V Standby		
Device	**Power (W)**	**Current (A)**
Processor Board	2.97	0.90
Front Panel	0.36	0.11
48V Power		
Device	**Power (W)**	**Current (A)**
Processor Board	748.41	15.59
IO Board	503.49	10.49
SCSI Backplane	127.56	2.66
12V Power		
Device	**Power (W)**	**Current (A)**
IO Board	25.60	2.17
Power Distribution Board	12.00	1.04

6.4.3 Mechanical Outline

Figure 6-6 illustrates the mechanical specification for the midplane board. Dimensions are in inches.

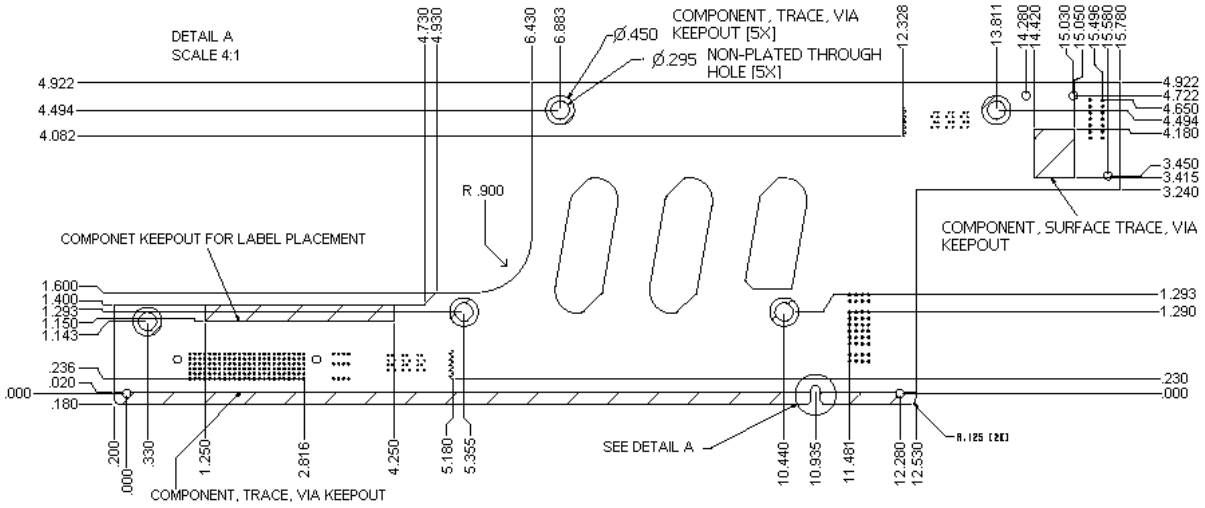

Figure 6-6. Intel® Server Board S870BN4 Midplane Mechanical Specification (Processor Side)

6.4.4 Venting Holes

The midplane contains three venting holes that are used for thermal purposes. They provide a way for the fans located on the I/O board to cool the processors located on the bottom side of the processor board. Figure 6-7 and Figure 6-8 illustrate the mechanical specifications for the two different types of ventilation holes. Dimensions are in inches.

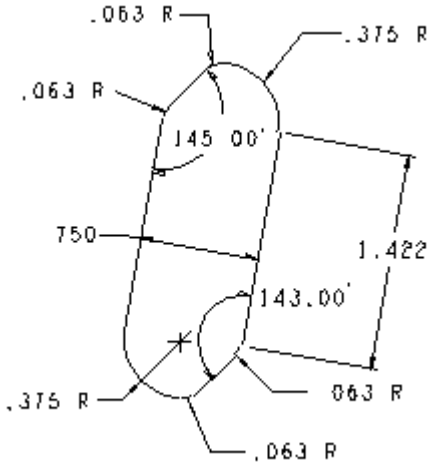

Figure 6-7. Intel® Server Board S870BN4 Midplane Ventilation Hole Specification (Type 1)

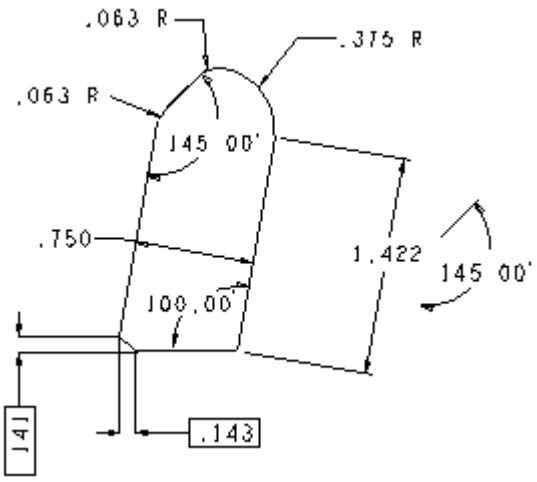

Figure 6-8. Intel® Server Board S870BN4 Midplane Ventilation Hole Specification (Type 2)

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Appendix A: Glossary

This appendix contains important acronyms and terms used in the preceding chapters.

Term	Description
A, Amp	ampere
AGTL+	assisted gunning transceiver logic+
BMC	baseboard management controller
C	centigrade
CMOS	complementary metal-oxide semiconductor
PROCESSOR	central processing unit
D2D	DC-to-DC
DDR	double data rate
DIMM	dual inline memory module
DMA	direct memory access
DMH	DDR memory hub
DRAM	dynamic random access memory
ECC	error correcting code
EDS	external design specification
EMTS	electrical, mechanical, and thermal specification
EPS	external product specification
FET	field effect transistor
FRB	fault resilient boot
FRU	field replaceable unit
FSB	front-side bus
FWH	firmware hub
GB	gigabyte – 1024 MB
GB/s	gigabytes per second
Gbit	gigabit
Hz	hertz (frequency of measurement = 1 cycle/second)
I/O	input/output
I^2C*	inter-integrated circuit
ID	identification
ISP	in-system programming
ITP	in-target probe
JTAG	Joint Test Action Group
LPC	low pin count
M	mega or million
m	milli
mA	milliamps
MB	megabyte – 1,024KB
MB/s	megabytes per second
Mbit	megabit
Mbit/s	megabits per second
MHz	megahertz

Term	Description
MP	multiprocessor
MRH-S	memory repeater hub (for SDRAM)
MT/s	megatransfer per second
PCB	printed circuit board
PCI	peripheral component interconnect
PID	programmable interrupt device
PLD	programmable logic device
PPOD	power pod
PROC	processor/memory complex
RAC	Rambus ASIC Cell
RAM	random access memory
RDRAM	RAMbus DRAM
RSL	Rambus signal level
SAPIC	streamlined APIC
SCSI	small computer systems interface
SCU	System Configuration Utility
SDRAM	synchronous dynamic RAM (DRAM type)
SM	server management
SMBus	I^2C server management bus
SMI	server management interrupt
SNC	scalable node controller
SNC-M	E8870 scalable node controller-Itanium 2
SP	scalability port
SRAM	static random access memory
SSTL	stub series terminated logic
STBY	standby
U	rack unit (1.75”)
USB	Universal Serial Bus
V	volt
VA	voltage ampere
Vac	alternating current (AC) voltage
Vdc	volts of direct current
VHDM	very high density module
VID	voltage identifier (ID)
VRM	voltage regulator module
Vstby	volts standby
Vtt	termination voltage
W	watt

Appendix B: Reference Documents

- *RS - Itanium 2 Processor Electrical, Mechanical and Thermal Specification*
- *RS - Itanium 2 Processor External Design Specification*
- *Itanium 2 Processor Power Pod Design Specification*
- *VHDM Connector Component Specification*
- *Meg-Array Memory Interface Connector Component Specification*
- *RS - Intel E8870 SNC-M (Scalable Node Controller-Itanium 2) External Design Specification (EDS)*
- *RS - Intel DMH (Memory Repeater Hub-DDR SRAM) External Design Specification (EDS)*
- *RS - Intel FWH (Firmware Hub) 82802AC External Design Specification (EDS.*
- *RS – Intel® E8870 Electrical, Mechanical and Thermal Specification*