Intel® Server System SSH4 Board Set

Technical Product Specification

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Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
10/2002	1.0	Initial release of this document.
12/18/02	1.1	Revised to include Intel® Xeon MP® processors (Gallatin) stepping, Adaptec 7902 U320 support, 100MHz PCI Unified in this document
07/21/03	1.3	Added Support for Intel® Xeon™ MP processor 2.8 GHz stepping, miscellaneous clarifying edits.
10/15/03	1.4	Revised to include PCI-X in Drawings and descriptions Added a section for Advanced Memory Configurations (memory mirroring/sparing)

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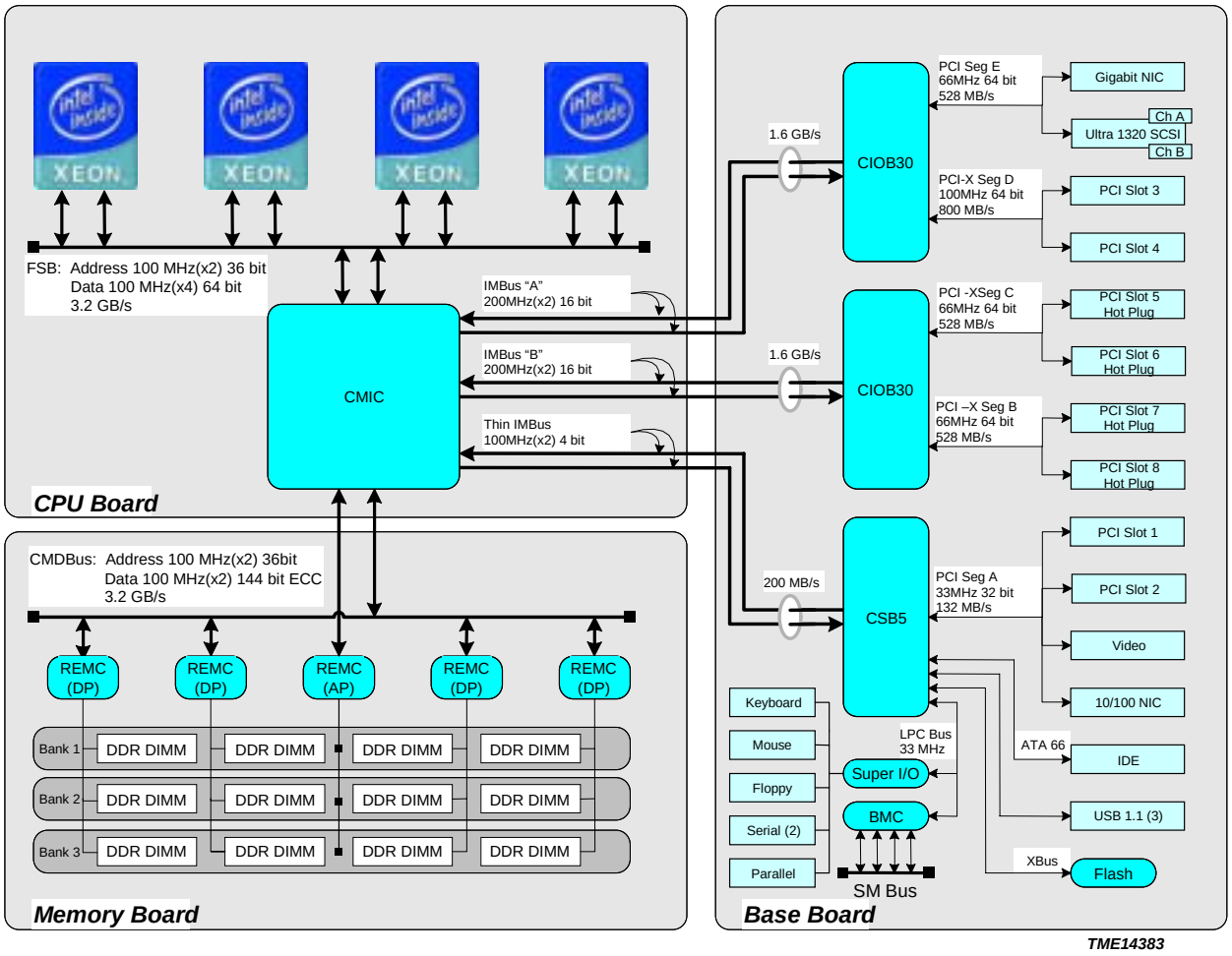
1. Introduction

This chapter provides an architectural overview of the Intel® Server System SSH4 board set, including functional blocks and their electrical relationships. The following figure shows the functional blocks of the SSH4 baseboard, Processor Board, and Memory Board.



1.1 Server System SSH4 Architecture

The server system SSH4 board set is designed around the Intel® Xeon™ processor and the ServerWorks* Grand Champion* HE chipset. This combination provides the basis for a high performance system with leading edge processor, memory, and I/O performance.

The SSH4 baseboard architecture provides for four 603-pin surface mount technology (SMT) zero insertion force (ZIF) lever-actuated processor sockets. It supports quad processing operation using the Intel® Xeon™ processor. It also contains eight industry standard PCI expansion slots supporting a mixture of 32-bit/33-MHz slots and 64-bit/100-MHz slots.

The baseboard provides an array of embedded I/O devices including a SCSI controller (with two external connection points), one embedded 10/100 Network Interface Controller, one embedded gigabit Network Interface Controller, and an ATI* Rage XL 2D/3D graphics accelerator with 4 MB graphics memory. Server management and monitoring hardware are also included.

The SSH4 memory subsystem consists of a single memory expansion board in the form of a memory riser board. This board supports up to 12 DDR registered SDRAM memory modules (DIMMs). Each DIMM may provide up to 2 GB of memory capacity, providing up to 24 GB of system memory.

The boardset provides the following features:

Table 1. Hardware Overview

Processor Board	**Processor**	Up to four Intel® Xeon™ processor MP (2.8GHz)
	Slot Type	PGA 603 Socket
	VRM	Four
	Termination	Automatic
Memory Board	**Memory Type**	2.5v buffered, ECC DDR SDRAM PC3200/PC2100-compliant DIMM (DDR200/DDR266)
	Slots	12
	Supported sizes	128 MB, 256 MB, 512 MB, 1 GB, 2 GB DIMM
	Minimum	512 MB (128 MB DIMM x 4)
	Maximum	24 GB (2 GB DIMM x 12)
	Bank size	4
	Bus Speed	100 MHz Address Bus, 200 MHz Data Bus
	Error Correction	ECC; chipkill
Baseboard	**Chipset**	ServerWorks Grand Champion HE ServerSet Memory Controller (CMIC x 1) PCI Bridge (CSB5 x 1) PCI-X Bus Bridge (CIOB30 x 2) Reliable Enhanced Memory Controller (REMC x 5)
	PCI BUS	Eight slots: Two PCI 32-bit, 33 MHz slots Four PCI-X 64-bit, 100 MHz Hot Plug slots Two PCI-X 64-bit, 100 MHz non-Hot Plug slots
	SCSI	Two Ultra320 ports on a single Adaptec*7902 controller.

IDE	ATA66, 1 channel, two devices total
LAN	1 x 10/100base-Tx (82550PM) 1 x 1000base-Tx (82544)
Graphics	ATI* Rage XL with 4 MB VRAM Resolutions: 640 x 480 to 1280 x 1024
Floppy Drive	3.5” (720 KB / 1.2 MB / 1.44 MB) three-mode
Legacy IO	National Semiconductor PC87417 I/O controller. Floppy disk controller Two serial ports Parallel port Keyboard and mouse Real-time clock
Video	ATI Rage XL with 4 MB VRAM
USB	Three Type “A” USB 1.1 (two rear pannel, one header)
Other	ICMB Header
Flash ROM	8 megabit
Backup RAM	8 KB

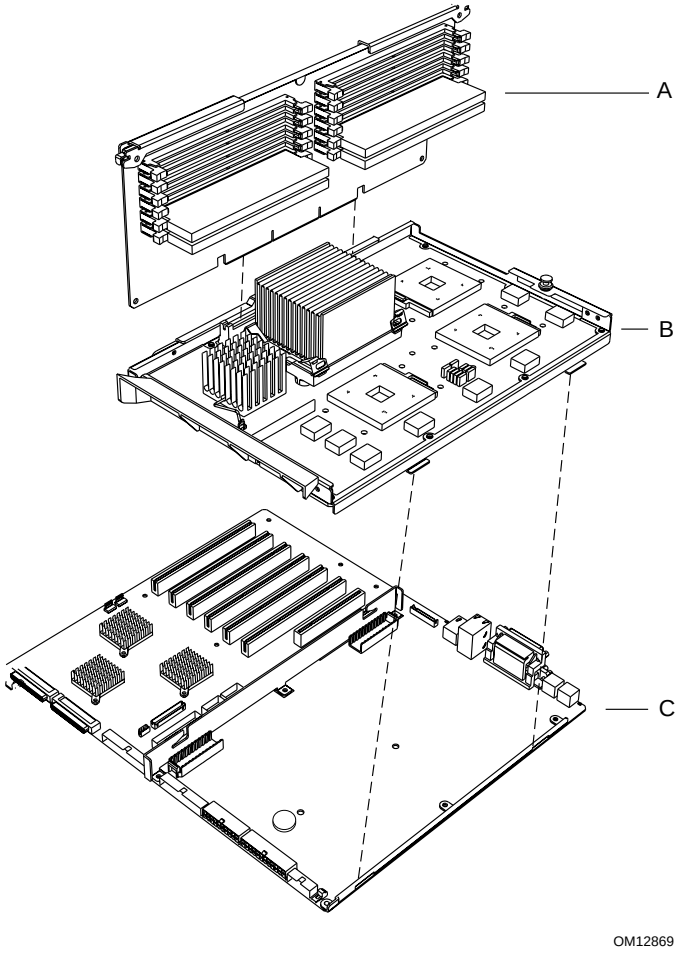
Table 2. Chipset Table

Component	Name	Model	Vendor	Features
Processor	Intel® Xeon™	–MP	Intel®	Up to 2.8 GHz
Host Bus Bridge	Grand Champion Chipset	CMIC	ServerWorks*	Memory controller
		REMC	ServerWorks	Memory address path and data path
PCI Bus Bridge		CSB5	ServerWorks	PCI Bridge. Includes: DMAC, Timer, 8259A-PIC, IDE, USB XIOAPIC
		CIOB30	ServerWorks	PCI-X bus Bridge
PCI Hot-Plug Controller	PCI Hot Plug Controller	PCI-X PHP	IBM*	PCI Hot Plug Controller (Xilinx* XCS20XL-VQ100)
PCI On-board peripherals	SCSI	AIC-7899W AIC-7902	Adaptec*	Ultra 320, two channels.
	Ethernet	I82550	Intel®	Ethernet Controller
		I82544	Intel®	Ethernet Controller (Gigabit)
	VGA	Rage XL	ATI*	Graphics controller
I/O	Super IO	PC87417	National Semiconducter*	KB/MS, serial port, parallel port, FDD, RTC
Server Management	BMC	BMC	Intel®	Server Management Controller

One megabyte of flash ROM is provided by an X-Bus interface to the CSB5. The Super I/O provides real-time clock (RTC) functionality.

The ServerWorks* Champion and Grand Champion chipset consists of four components: the CMIC, REMC, CSB5 and CIOB30. The CMIC is responsible for accepting access requests from the host (processor) bus, and if appropriate, directing those accesses to memory or to one of the I/O buses. The REMC, which is connected to the CMIC, provides the memory operation. The CIOB30, which is connected to the CMIC via IMBus, provides the interface to the 64-bit, 100-MHz PCI-X bus. The CSB5, which is connected to the CMIC via the Thin IMB Bus, provides the interface to the X-bus, the LPC bus, and I/O APICs.

Figure 1 provides a view of how the baseboard, processor board, and memory are connected.



A Memory Board
B Processor Board
C Baseboard

Figure 1. Baseboard, Processor Board, and Memory Board

2. Processor and Chipset

The Server System SSH4 processor/PCI bridge/memory subsystem consists of one to four identical Intel® Xeon™ processors, the Grand Champion HE chipset, a plug-in memory board, a processor board, and support circuitry. The processor board houses four surface mount zero insertion force (ZIF) processor sockets and two embedded VRMs.

The Grand Champion HE chipset provides the 36-bit address, 64-bit data processor host bus interface, operating at 100 MHz in the AGTL+ signaling environment. The Champion Memory and I/O Controller (CMIC) provides an integrated memory controller, a high-speed I/O connection to the CIOB through the IMB bus and a legacy PCI segment through the Thin IMB bus. The board set supports up to 24 GB of ECC memory, using DDR registered SDRAM DIMMs.

Additional descriptions and features include the following:

- Champion HE chipset providing an integrated I/O bridge and memory controller and a flexible I/O subsystem core (PCI) optimized for multiprocessor systems and standard high-volume (SHV) servers.
- Four processor sockets that accept Intel® Xeon™ processors.
- 330-pin connector interface to the memory expansion board.
- Processor host bus AGTL+ support circuitry, including termination power supply.
- Integrated APIC signals support.
- Miscellaneous logic for reset configuration, processor presence detection, ITP port, and server management.

2.1 Processor Support

The Server System SSH4 supports Intel® Xeon™ processor MP frequencies greater than 1.4 GHz. Processor speeds are automatically configured by the BMC, which automatically reads the processor data and sets the CPU speed setting necessary for the Intel Xeon processor(s). Therefore, processor speed setting jumpers are not necessary.

The processor is packaged in a 603-pin micro-PGA (Pin-Grid Array) and provides an Integrated Heat Spreader (IHS) for a heat sink attachment.

The Intel® Xeon™ processor socket conforms to the *603-pin Socket Design Guidelines* and is a surface mount technology (SMT), ZIF socket using solder ball attachment to the platform.

The Intel® Xeon™ processor MP contains a local APIC section for interrupt handling. When more than one processor is installed, all processors must be of identical revision, core voltage, cache voltage and bus/core speeds.

Note: If using a single processor in the system, it must be installed into the primary processor socket (processor1). The BMC will not allow DC power to be applied to the system unless the primary slot is populated with a processor. Processors must be populated in order by processor slot number.

The processor board consists of four processor sockets, a CMIC component, and a 300-pin connector for the memory board. The processor board sits parallel to the baseboard and is supported by a metallic skirt.

2.1.1.1 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc. through the CPUID instruction. The processor information is read at every system power-on. The requirements are as follows:

- **All processors in the system must operate at the same frequency and have the same cache sizes. No mixing of product families or speeds are supported.**
- **Processors run at a fixed speed as determined by the processor and BMC and cannot be programmed to operate at a lower or higher speed.**

2.1.1.2 Processor Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processors. The BMC checks the logic and will not turn on the system DC power until a processor is installed in the processor1 slot. Processors must be installed in sequential order according to the processor slot number. If processors are not installed in order, voltage rails will not be passed to the downstream processors and a system fault will be detected for the missing processor(s) or termination card.

2.1.2 APIC Bus

Interrupt notification and generation for the processors is done using the front side bus (FSB) between local APICs in each processor and the I/O APIC in the CSB5 located on the baseboard.

2.1.3 Server Management Registers and Sensors

The baseboard management controller manages registers and sensors associated with the processor/memory subsystem. For more information, refer to the Sahalee Baseboard Management Controller (BMC) section, beginning on page 56.

2.2 ServerWorks Grand Champion Chipset

The ServerWorks Grand Champion chipset provides an integrated I/O bridge and memory controller and a flexible I/O subsystem core (PCI), targeted for multiprocessor systems and standard high-volume servers based on the Intel® Xeon™ MP processor. The ServerWorks Grand Champion chipset used on the baseboard consists of the four components listed in the sections below.

2.2.1 CMIC: Champion Memory and I/O Controller

The CMIC is responsible for accepting access requests from the host (processor) bus and for directing those accesses to memory or to one of the PCI buses. The CMIC monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue for subsequent forwarding to the memory subsystem, or to an outbound request queue for subsequent forwarding to one of the PCI buses. The CMIC also accepts inbound requests from the CIOB and the legacy PCI bus. The CMIC is responsible for generating the appropriate controls to the REMC to control data transfer to and from the memory.

The Champion Memory and I/O Controller (CMIC) is the fourth generation product in ServerWorks Champion ServerSet Technology. The CMIC integrates two main functional units:

- An integrated high performance main memory subsystem
- An IMB bus interface that provides a high-performance data flow path between the processor bus and the I/O subsystem

In addition to the above-mentioned units, the CMIC incorporates a Thin-Intra Module Bus (Thin-IMB) Interface. Other features provided by the CMIC include the following:

- Full support of processor bus protocol with multiprocessor support
- Full support of ECC on the memory interface
- Twelve deep in-order queue
- Full support of registered DDR ECC SDRAM DIMMs
- Support for 24 GB of 4-way interleaved SDRAM
- Memory scrubbing
- ECC correction for 1-4 bits, multiple-bit error detection

2.2.2 CIOB30: Champion I/O Bridge

The CIOBs provide the interfaces for the 64-bit, 100-MHz Rev. 2.2-compliant PCI bus and the 64-bit, 100 MHz PCI-X addendum to Rev. 2.2-compliant PCI-X busses. The CIOBs are both master and target on the PCI buses.

The Champion I/O Bridge (CIOB) provides an integrated I/O bridge that provides a high-performance data flow path between the IMB and the 64-bit I/O subsystem. This subsystem supports peer 64-bit PCI segments. Having multiple PCI interfaces, the CIOB can provide large and efficient I/O configurations. The CIOB functions as the bridge between IMB and the multiple 64-bit PCI I/O segments.

The IMB interface is capable of supporting 1.6 GB/sec of data bandwidth in both the upstream and downstream direction simultaneously.

The internal PCI arbiter implements the Least Recently used algorithm to grant access to requesting masters.

2.2.3 CSB5: Champion South Bridge

The CSB5 controller has several components. It provides the interface for a 32-bit, 33-MHz Rev. 2.2-compliant PCI bus. The CSB5 can be both a master and a target on that PCI bus. The CSB5 also includes a USB controller and an IDE controller. The CSB5 is responsible for many of the power management functions, with ACPI control registers built in. The CSB5 also acts as a bridge between the PCI and the Low Pin Count (LPC) bus.

The CSB5 is a PCI device that provides multiple PCI functions in a single package: PCI-to-LPC bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the CSB5 has its own set of configuration registers; once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

The CSB5 is a 352-pin BGA device. On the SSH4 baseboard, the primary role of the CSB5 is to provide the gateway to all PC-compatible I/O devices and features. The SSH4 baseboard uses the following CSB5 features:

- PCI interface
- IDE interface, with Ultra DMA 66 capability
- USB interface
- PC-compatible timer/counters and DMA controllers
- Baseboard Plug and Play support
- General purpose I/O
- Power management
- APIC and 8259 interrupt controller
- Host interface for AT compatible signaling
- Internal-only ISA bus (no ISA expansion connectors) bridge for communication with Super I/O, BIOS flash, and BMC

2.2.4 REMC: Reliability Enhanced Memory Controller

The Server System SSH4 memory board has five REMC components. These devices are used to expand the SDRAM signaling environment to support up to 12 DDR Registered SDRAM DIMMs. These DIMMs can be up to 2 GB each.

2.2.5 ServerWorks Grand Champion HE Chipset Memory Architecture

The CMIC provides the memory controller for the system. The main memory interface consists of two channels, with 16-bit address channel running at 100 MHz and 144-bit CMDbus (data) running at 200 MHz.

These channels run to five REMC components (four data components and one address component) on the memory board to interface with DDR Registered ECC SDRAM DIMMs. The memory board provides 12 DIMM slots. Main memory sizes from 512 MB to 24 GB are supported with 144-bit, four-way interleaved DDR Registered SDRAM DIMMs. The ECC algorithm used during main memory accesses is capable of correcting single-bit errors and detecting all double-bit errors. The interface between the CMIC and the five REMC devices on the memory board provides 3.2 GB/sec bandwidth to/from main memory.

2.2.6 ServerWorks Grand Champion HE Chipset System I/O Architecture

The CMIC, CIOB, and CSB5 chips provide the pathway between the processor and I/O systems. The CMIC is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. I/O communications between the CMIC and PCI busses is conducted over one of two possible private interfaces called an IMB.

If the cycle is directed to one of the 64-bit PCI segments, the CMIC communicates with the CIOB through a private interface called the IMB bus. The IMB bus consists of two data paths, one upstream (to the CMIC from the CIOB) and one downstream (from the CMIC to the CIOB). The interface is 16 bits wide and operates at 200 MHz with double-pumped data, providing over 0.8 GB/sec of bandwidth in each direction or 1.6 GB/sec of bandwidth in both directions concurrently. The CIOB translates the IMB bus operation to a 64-bit PCI Rev. 2.2-compliant PCI-X addendum to PCI Rev. 2.2-compliant signaling environment, operating at 100 MHz.

If the cycle is directed to the 32-bit PCI segment or to the CSB5, the cycle is output on the private interface between the CMIC and the CSB5 called the Thin-IMB bus. The Thin-IMB a 16 bit wide bus (8 bits wide in each direction) and runs at 100 MHz with double pumped data. Throughput is 0.2 GB/sec of bandwidth in each direction or 0.4 GB/sec of bandwidth in both directions concurrently.

All I/O for the Server System SSH4 board set, including PCI, is directed through the CMIC and then either through the CIOB- or the CSB5-provided 32-bit, 33-MHz PCI bus.

- The CSB5 provides a 32-bit, 33-MHz PCI bus.
- The CIOB provides a 64-bit, 100-MHz PCI-X bus .

2.3 Super I/O

The National Semiconductor* PC87417 Super I/O device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The SSH4 baseboard supports the following features:

- GPIO
- Two serial ports
- Floppy
- Keyboard and mouse through PS/2 connectors
- Parallel port
- Real-time clock
- Wake-up control

2.3.1 GPIO

The National Semiconductor PC87417 Super I/O provides number of general-purpose input/output pins that the baseboard utilizes. Table 3 lists the pin, the signal name used in the schematic, and a brief description of its usage.

Table 3. Super I/O GPIO Usage Table (Preliminary)

Pin #	Signal Name	Description
1	IDES0-00	IDE Chip Select
9	SXRDY+00	Transmit ready signal from SIO to HPCs
10	BMC_SYSIRQ-00	System Interrupt Controller interrupt from BMC
13	SIO_CLK_40M_BMC	40 MHz clock output to BMC
14	IOR-00	Read from the HP controller
15	IOW-00	Write to the HP controller
16-18	SA+00<0-3>	4-bit Address bus
20	HPC4CS-00	Chip select for HP controller #1
21	HPC3CS-00	Chip select for HP controller #2
24-31	SD+10<0-7>	8-bit data bus
33	SXSTB1-00	Strobe signal for standard latched address mode
34	SXSTB0-00	Strobe signal for standard latched address mode
35	BMC_SWIN	Region 0 strapping option to determine 8-bit / 16-bit wide data path
36	BMC_PWRN	Power LED from BMC
37	EXTEV-00	External Event
38	SUPERSCI-00	SuperI/O Interrupt request to CSB5
45	SIO_CLK_RTC_BMC	Real Time Clock input to BMC
49	PCIX_PME	Power Management Event from PCI-X bus
50	HPCINT-10	Interrupt from HPC to SuperI/O
51	FP_PWR_LED	Power LED indicator to Front Panel
52	LAN_PME	Power Management Event from onboard LAN controller
53	BMC_SCIN	System Management Interrupt from BMC
125	KBCLK	Keyboard clock
126	KBDATA	Keyboard data
127	MSCLK	Mouse clock
128	MSDATA	Mouse data

2.3.2 Serial Ports

Two serial ports are provided on the baseboard, a 9-pin DB9 connector is located on the rear I/O to supply Serial Port A and a 10-pin header on the baseboard provides Serial Port B.

2.3.2.1 Serial Port A

Serial Port A is accessed through a 9-pin connector on the rear I/O panel. The Serial Port A interface follows the standard RS-232 pinout. The baseboard has a Serial Port A silkscreen label next to the connector and a location designator of P31. The Serial Port A connector is located below the parallel port connector, as shown in Figure 20.

2.3.2.2 Serial Port B

Serial Port B is provided via a header on the baseboard. See section 10.7 on page 74 for information about Serial Port B.

2.3.3 Floppy

The floppy disk controller in the SIO is functionally compatible with floppy disk controllers in the DP8473 and N844077. All the FDC functions are integrated into the SIO including analog data separator and 16-byte FIFO.

2.3.4 Keyboard and Mouse

Two PS/2 ports are provided for keyboard and mouse and are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector.

2.3.5 Parallel Port

The parallel port is supported on the baseboard through the rear I/O. The parallel port supports Bi-directional, EPP and ECP modes.

2.3.6 Real-time Clock

The SIO contains a real-time clock with external battery backup. The device also contains 242 bytes of general purpose battery-backed CMOS RAM.

2.3.7 Wake-up Control

The SIO contains functionality that allows various events to control the power-on and power-off of the system.

2.4 BIOS Flash

The baseboard incorporates a Fujitsu* 8176 8 megabit Flash ROM. The flash device is connected through the X-bus of the CSB5.

3. Baseboard PCI I/O Subsystem

The primary I/O bus for the Server System SSH4 MP baseboard is PCI, with one PCI bus segment and four PCI-X bus segments. Each PCI and PCI-X bus complies with the PCI Local Bus Specification, Rev 2.2 and the PCI-X addendum to the PCI local bus specification. The P32-A bus segment is directed through the CSB5 while the four 64-bit segments, P64-B, P64-C, P64-D, and P64-E are directed through the two CIOB30 I/O Bridges. Figure 2 illustrates the PCI bus layout. Table 4 lists the characteristics of the PCI and PCI-X bus segments.

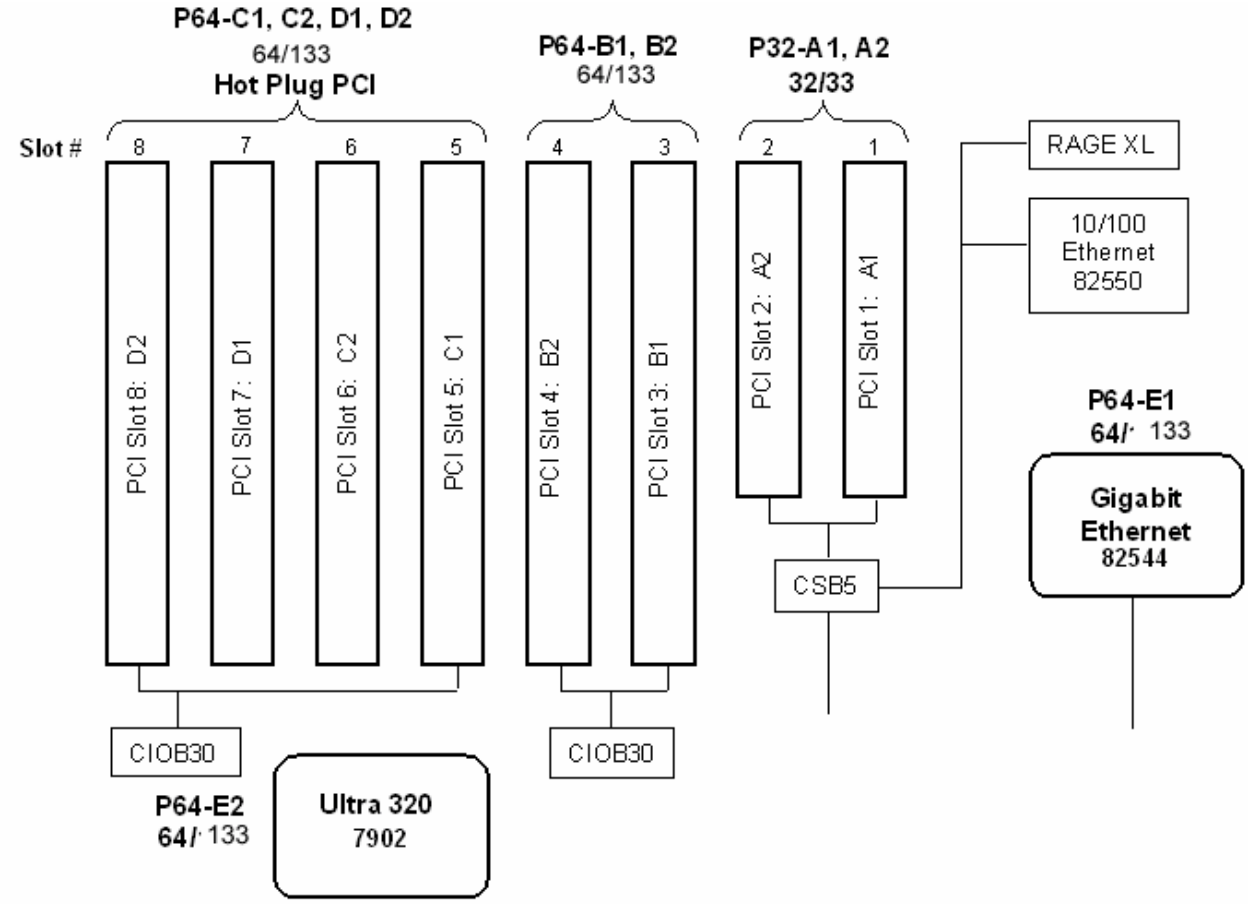


Figure 2. PCI Bus Layout

Table 4. PCI and PCI-X Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI Slots
PCI P32-A	5V	32 bits	33 MHz	Non-Hot Plug, Peer bus	Slots 1 and 2. Full-length system cable routing may interfere with insertion of some full-length PCI cards.
PCI-X P64-B	3.3V	64 bits	133/ 100 MHz	Non-Hot Plug, Peer bus	Slots 3 and 4. Full length
PCI-X P64-C	3.3V	64 bits	133/100 MHz	Hot Plug, Peer bus	Slots 5 and 6. Full length
PCI-X P64-D	3.3V	64 bits	1 33/100 MHz	Hot Plug, Peer bus	Slots 7 and 8. Full length
PCI-X P64-E	3.3 V	64 bits	133/100 MHz	Embedded Peer bus	N/A

3.1 32-bit, 33-MHz PCI Subsystem

All 32-bit (P32-A), 33-MHz PCI I/O for the baseboard is directed through the CSB5. The 32-bit, 33-MHz PCI segment created by CSB5 is called the P32-A segment. The P32-A segment contains the following embedded devices and connectors:

- 2D/3D graphics accelerator: ATI RAGE XL Video Controller
- One Network Interface Controller: Intel® 82550 Fast Ethernet Controller
- PCI Slots 1 and 2

Each of the embedded devices above will be allocated a GPIO to disable the device.

3.1.1 P32-A Slot Specifics

The PCI slots support the PME# and 3.3VAUX signals as described in the *PCI Bus Power Management Interface Specification*. The 3.3VAUX signal is a limited current 3.3 V supply maintained even when the system power is turned off.

Note: The baseboard supports only one slot consuming 375 mA of Standby current on the 3.3V AUX power line, although it can be any of the eight PCI slots. All other slots can consume a maximum of 20 mA each. The system will not operate correctly if this limit is exceeded.

3.2 64-bit, 133-MHz PCI-X Subsystem

P64 supports the following six 184-pin, 3.3 V, 64-bit PCI-X expansion connectors: Each embedded device is allocated a GPIO to disable the device.

- Slot 3 numbered P64-B1
- Slot 4 numbered P64-B2
- Slot 5 numbered P64-C1
- Slot 6 numbered P64-C2
- Slot 7 numbered P64-D1
- Slot 8 numbered P64-D2
- The P64-E segment supports the following embedded devices: One Ultra 320/m (Channel 0 and 1): AIC-7902W SCSI controller
- One Gigabit Network Interface Controller: Intel® 82544 Fast Ethernet Controller

3.2.1 PCI-X Bus Arbitration

P64-Bus segments 2 and 3 support five PCI-X masters (U-320 SCSI, Gigabit NIC, Slots P64-B1, P64-B2, and CIOB-1). P64-Bus segments 4 and 5 support five PCI-X masters (Slots P64-C1, P64-C2, P64-D1, P64-D2, and CIOB-2). All PCI-X masters must arbitrate for PCI-X access, using resources supplied by the CIOB. The host bridge PCI-X interface (CIOB) arbitration lines *REQx#* and *GNTx#* are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 5. PCI-X Arbitration Connections

Baseboard Signals	Device
P_REQ0#/P_GNT0#	PCI-X Slot P64-B1
P_REQ1#/P_GNT1#	PCI-X Slot P64-B2
P_REQ2#/P_GNT2#	PCI-X Slot P64-C1
P_REQ3#/P_GNT3#	PCI-X Slot P64-C2
S_REQ0#/S_GNT0#	PCI-X Slot P64-D1
S_REQ1#/S_GNT1#	PCI-X Slot P64-D2
S_REQ2#/S_GNT2#	PCI-X P64-E AIC-7902W SCSI controller
S_REQ3#/S_GNT3#	PCI-X P64-E Gigabit Network Interface Controller

3.2.2 P64 Slot Specifics

The PCI slots support the PME# and 3.3VAUX signals as described in the PCI Bus Power Management Interface Specification. The 3.3VAUX signal is a limited current 3.3 V supply maintained even when the system power is turned off.

Note: The baseboard only supports one slot consuming 375 mA of Standby current on the 3.3V AUX power line, although it can be any of the eight PCI slots. All other slots can consume a maximum of 20 mA each. The system will not operate correctly if this limit is exceeded.

3.3 PCI Hot Plug Support

Hot plug support is provided on four of the PCI-X slots on the 133/64-bit PCI bus segments (C and D). No hot plug support is provided on the 133/64-bit bus segments (B and E). Segment A operates at only 33 MHz and is not hot plug supported. The logic for powering-on and powering-off the slots is controlled by the PHP ASIC.

3.3.1 PCI Hot Plug Functionality

To support PCI Hot-plug, systems require hot-plug hardware, a hot-plug compatible operating system, and hot-plug capable adapter drivers. To ensure backward compatibility, any combination of hot-plug and conventional versions of each of these components is permitted, including mixing both hot-plug and conventional adapter drivers. If a conventional driver is loaded under a hot-plug capable operating system, or a hot plug driver is loaded under a conventional operating system, the driver will maintain the capability it had in the conventional environment.

3.3.2 Operating System Support

The initial steps involved in booting to an operating system are not impacted because of PHP support. After the operating system has booted, adapter drivers may be required to be installed or updated to get PHP functionality. Three terms that are commonly used to describe PCI Hot-plug operations are Hot Replace, Hot Add, and Hot Upgrade.

- **Hot Replace:** The process of removing an adapter card and then inserting an identical adapter into the same slot. The replacement adapter card will use the same PCI resources that were assigned to the previous card and its driver will not be updated. Hot Replace is also commonly referred to as “Like-for-Like Replacement.”

- **Hot Add:** The process of inserting an adapter card into a previously unoccupied slot. This operation requires that a driver also be loaded for the added adapter and that PCI resources have been reserved by the system BIOS for the added adapter card. Hot Add is also sometimes referred to as “Hot Expansion.”

- **Hot Upgrade:** The process of removing an adapter card and inserting an upgraded adapter (i.e., a new revision) that requires different PCI resources than the original card. The adapter’s driver may or may not use the same driver as the previous adapter.

“Hot Removal” and “Hot Insertion” refer to the sequence of steps involved in removing and inserting, respectively, a PCI card from a hot-pluggable PCI slot. Not all of these operations are supported by every hot-plug capable operating system. Each operating system may implement these operations in a different manner.

The following steps outline a typical enabling sequence for Windows NT* 4.0:

1. After booting, load the necessary drivers.

2. Enable the PHP graphical user interface (GUI) by clicking Start / Programs / PCI Hot Plug / PCI HP Utility on the Windows NT menu bar.

   This GUI provides the adapter status to the hot-plug user interface, and also allows the user to control hot-plug functionality. The initial screen lists *LED Condition* (Green, Amber), *Location* (logical slot number), *Board* (description, driver support), and *Status* (Normal/Not Ready). Logical slot numbering starts at 5 and ends at 8, in increments of 1. Only slots containing a card with hot-plug capable drivers can be controlled from the GUI. LED Control

Each slot has two LEDs. A green LED indicates the state of power on each slot. The amber LED is the slot attention indicator. The amber LED indicates an error condition with that slot. The following table summarizes typical LED states that may be encountered during operation.

Table 6. Slot State and Attention Indicators

LED States	Interpretation
Green On Amber Off	The slot is on and functioning normally
Green On Amber On	The slot is on and an attention condition exists (error)
Green Off Amber On	The slot is off and an attention condition exists (error)
Green Off Amber Off	The slot is off
Green On Amber blinking	The slot is on and an attention condition exists (Remove OK)
Green Off Amber blinking	The slot is off and an attention condition exists (Remove OK)

3.3.3 Interlock Switch Support

The baseboard does not support a mechanical interlock switch. The switch input is permanently grounded (enabled) on the baseboard.

3.3.4 Hot Plug Write Operations

Table 7 summarizes Hot Plug Write Operations. Table 8 defines the states of the slot status registers.

Table 7. Hot Plug Controller Write Operations

Command Encoding	Write to registers at offset:	Affects	Command	State Machine
00h	15	Controller	Enable IRQ	No
01h	15	Controller	Disable IRQ	No
02h	0-14	Slot	Turn Slot OFF	Yes
03h	0-14	Slot	Turn Slot ON	Yes
04h	0-14	Slot	Turn ATTENTION indicator OFF	No
05h	0-14	Slot	Turn ATTENTION indicator ON	No
06h	15	Controller	Clear IRQ	No
07h	15	Controller	Reset Controller	Yes
08h	15	Controller	IRQ Steering (SCI/SMI toggle)	No
09h	31-34	Bus	Set 33 MHz Conventional Bus Mode	Yes
0Ah	31-34	Bus	Set 66 MHz Conventional Bus Mode	Yes
0Bh	31-34	Bus	Set 66 MHz PCI-X Bus Mode	Yes
0Ch	31-34	Bus	Set 100 MHz PCI-X Bus Mode	Yes
0Dh	31-34	Bus	Set 133 MHz PCI-X Bus Mode	Yes
0Eh			Reserved	Yes
0Fh			Reserved	Yes
10h			Reserved	Yes
11h	15	All Slots	All Slots Off	Yes
12h	15	All Slots	All Slots On	Yes
13h	15	Slot	Activate ‘Locator’ (Blinking ATTN LED)	No
14h to FFh			Reserved	Reserved

Notes:

- Certain commands require time to complete. Device driver software must issue state machine commands using the pseudocode shown later in this document.
- Commands that do not require the state machine can be issued by waiting for a non-busy controller and then writing the command to the proper register.
- The current state of SCI/SMI is available using bit 6 of the controller status register. Disabling interrupts affects both SCI and SMI. SCI/SMI should be initialized to SCI.
- Interrupt steering is optional. If it is not implemented, the value of bit 6 in the controller status register will be 0 and will not change when command 08h is issued.
- Command 13h (Locator ON) causes the Attention indicator to blink at a rate of 2 Hz with 50% duty cycle until another command that affects the Attention indicator is written to the controller. (The Attention indicator is in one of three states (off, on, or blinking) and these three states are selected using commands 04 (Attention Off), 05h (Attention On), and 13h (Locator On).

Table 8. Slot Status Register Definitions (Read to Offsets 0-14)

Bit Position (0 is LSB)	Name	Description
0	Power	0 = Power off 1 = Power on to slot
1	Connect#	0 = Connected to PCI bus 1 = Disconnected
2	Attention	0 = Off 1 = On
3	PRSNT2#	PCI card Present signal 2; pulled up by system
4	PRSNT1#	PCI card Present signal 1; pulled up by system
5	PWRGD	From slot power module 0 = No power or power fault 1 = Power good
6	BusSpeed Mismatch	0 = Bus speed OK 1 = Bus speed mismatch (this slot)
7	Latch	0 = Tab latch is open 1 = Tab latch is closed

Notes:

- Allow one second to pass between the applying power and checking bit 5. If bit 5 indicates no power one second after power is applied to the slot, a power fault has occurred.
- If a hot-plug card insertion results in a bus speed mismatch (bit 6), the controller will decline all “Turn Slot On” commands (command 03h) addressed to the slot by returning “Command Failed” results in bits 2 and 3 of the command status register and asserting IRQ (if enabled). Commands to “Turn Slot Off” (command 02h), “Turn Attention Indicator On” (command 04h), and “Turn Attention Indicator Off” (command 05h) for the slot will be honored and, barring hardware faults, will complete successfully.
- Because M66EN may be used as an input on some adapters (and may, therefore, have clamping diodes on this signal line), M66EN should only be sampled when the adapter is powered up. The adapter may be powered up with PCIRST# asserted and the bus and clocks disconnected for the purpose of checking M66EN without affecting the bus, even if the card cannot operate at the current bus speed. The state of Bus Speed Mismatch (bit 6) must reflect the value of M66EN obtained while the adapter was powered and must be updated after each PCI bus reset operation involving this slot. (Bus speed mismatch [bit 6] must also take into account the state of the PCIXCAP bit (as reported in the Extended Slot Status register) versus the speed of the bus.

3.3.5 PCI Power Budgeting

The Server System SSH4 boardset is capable of supplying power to the eight PCI slots as identified in Table 9.

Table 9. PCI Power Consumption

Subsystem	Quantity of slots	+5 V Current	+3.3 V Current	+12 V Current	-12 V Current	+5 V Standby Current	Total Power (W)
64 bit PCI/PCI-X	6	9.00 A	13.64 A			0.31 A	91.56 W
32 bit PCI	2	6.00 A				0.03 A	30.15 W

3.4 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. Table 10 shows the bit to which each IDSEL signal is attached for PCI devices, and corresponding device description.

Table 10. PCI IDs

Device	Bus Number [23:16]	Device Number [15:11]	Slot ID Signal
CMIC	00h	00000b	
RageXL	00h	00010h	P32_AD18
82550 NIC	00h	00011b	P32_AD19
Slot #01(32)	00h	01000b	P32_AD24
Slot #02(32)	00h	01001b	P32_AD25
CSB5	00h	01111b	
CIOB30 #1	00h	10000b	
CIOB30 #2	00h	10001b	
82544	01h	00011b	1P64_AD19
AIC7902	01h (Note)	00100b	1P64_AD20
Slot #03 (64/PCI-X)	02h (Note)	01000b	2P64_AD24
Slot #04 (64/PCI-X)	02h (Note)	01001b	2P64_AD25
Slot #05 (64/PCI-X)	03h (Note)	01000b	3P64_AD24
Slot #06 (64/PCI-X)	03h (Note)	01001b	3P64_AD25
Slot #07 (64/PCI-X)	04h (Note)	01000b	4P64_AD24
Slot #08 (64/PCI-X)	04h (Note)	01001b	4P64_AD25

Note: The bus number will change if bridge cards are connected on the PCI bus.

3.5 Ultra 320 SCSI

The Server System SSH4 baseboard provides an embedded dual channel SCSI bus. The Adaptec AIC7902 controller contains two independent SCSI controllers that share a single 64-bit, 133-MHz PCI bus master interface as a multifunction device, packaged in a 456-pin BGA. Internally, each controller is identical, capable of operations using either 16-bit SE or LVD SCSI providing 40 MB/sec (Ultra-wide SE), 80 MB/sec (Ultra 2), 166 or 320 MB/sec (Ultra 320). Each controller has its own set of PCI configuration registers and SCSI I/O registers. The baseboard supports disabling of the onboard SCSI controller through the BIOS setup menu.

The baseboard provides active terminators, termination voltage, auto-resettable fuse, and protection diode for both SCSI channels. The BIOS setup menu allows the ability to enable/disable the onboard terminators.

3.6 Network Interface Controllers (NIC)

The SSH4 baseboard supports two network interface controllers:

- A 10Base-T/100Base-TX network subsystem based on the Intel® 82559 controller, a no data encryption NIC
- A 1000BASE-T, 100Base-TX, and 10Base-T network subsystem based on the Intel® 82544 NIC

3.6.1 82559 NIC

The 82559 is a highly integrated PCI LAN controller in a thin BGA 15 mm^2 package. The controller's baseline functionality is equivalent to that of the Intel 82559 with the addition of alert-on-LAN functionality. The baseboard supports disabling of the two NIC controllers using the BIOS setup menu. The 82559 supports the following features:

- 32-bit PCI, CardBus master interface
- Integrated IEEE 802.3 10Base-T and 100Base-TX compatible PHY
- IEEE 820.3u auto-negotiation support
- Chained memory structure similar to the 82558, 82557 and 82596
- Full duplex support at both 10 Mbps and 100 Mbps operation
- Low power +3.3 V device
- IP checksum off-loading

3.6.2 82544 NIC

The Intel® 82544GC Gigabit Ethernet Controller is an integrated, third-generation, Ethernet-LAN component, capable of supporting 1000 Mb/s, 100 Mb/s, and 10 Mb/s data rates. The single-chip device manages both the MAC and PHY layer functions, and is optimized for LAN on Motherboard (LOM) designs, enterprise networking, and Internet appliances that use the Peripheral Component Interconnect (PCI) or PCI-X bus. The controller provides a direct 32/64 bit, 33/66 MHz interface to the PCI bus that supports the PCI Local Bus Specification (revision 2.2), as well as the emerging PCI-X extension to the PCI Local Bus (revision 1.0a) at clock rates up to 133 MHz.

The Intel 82544GC Gigabit Ethernet Controller provides an interface to the host processors by using on-chip command and status registers and a shared host-memory area. The controller's descriptor ring management architecture is optimized to deliver both high performance and PCI/PCI-X bus efficiency. Using hardware acceleration, the controller can offload various tasks from the host processor, such as TCP/UDP/ IP checksum calculations and TCP segmentation. The Intel 82544GC Gigabit Ethernet Controller cache up to 64 packet descriptors in a single burst for efficient PCI-bandwidth usage while the large 64KB on-chip packet buffer maintains superior performance as available PCI bandwidth descriptors change.

Fully integrated physical-layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications (802.3ab, 802.3u, 802.3). And, with the addition of an appropriate serializer/deserializer (SERDES), the Intel 82544GC Gigabit Ethernet Controller alternatively provides an Ethernet interface for 1000Base-SX or LX applications (802.3z).

- Direct 32/64-bit 33/66-MHz PCI, 100/133 MHz PCI-X, CardBus master interface
- Integrated IEEE 802.3 10Base-T and 100Base-TX compatible PHY
- IEEE 820.3u auto-negotiation support
- Full duplex support for 10 Mbps, 100 Mbps, and 1000 Mbps operation
- Descriptor ring management architecture optimized to deliver both high performance and PCI/PCI-X bus efficiency
- Low power +3.3 V device
- IP and TCP/UDP checksum off-loading

3.6.3 Video Controller

The Server System SSH4 baseboard provides an ATI RAGE XL PCI graphics accelerator, along with 4 MB of video SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI RAGE XL chip contains a SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 2M x 32 SDRAM chip provides 4 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 3200 x 1200 resolution in 8/16/24/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors up to 100 Hz vertical refresh rate.

The baseboard provides a standard 15-pin VGA connector and supports disabling of the onboard video through the BIOS setup menu or when a plug in video card is installed in any of the PCI slots.

3.6.3.1 Video Modes

The RAGE XL chip supports all standard IBM VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD. Table 11 specifies the minimum memory requirement for various display resolution, refresh rates and color depths.

Table 11. Standard VGA Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	–
1280x1024	70, 72	Supported	–	Supported	–
3200x1200	60, 66	Supported	Supported	–	–
3200x1200	76, 85	Supported	Supported	–	–
3D Mode	**Refresh Rate (Hz)**	**3D Video Mode Support with Z Buffer Enabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	–	–
1280x1024	43,60,70,72	Supported	–	–	–
3D Mode	**Refresh Rate (Hz)**	**3D Video Mode Support with Z Buffer Disabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	–
1280x1024	43,60,70,72	Supported	Supported	–	–
3200x1200	60,66,76,85	Supported	–	–	–

3.6.3.2 VGA Connector

The following table shows the pinout of the VGA connector. For more information, see the ATI RAGE XL Technical Reference Manual.

Table 12. Video Port Connector Pinout

Pin	Name
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	(No Connect)
5	GROUND
6	GROUND
7	GROUND
8	GROUND
9	+5 VDC
10	GROUND
11	No connection
12	SDA
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	SCL

3.7 Interrupt Routing

Server System SSH4 interrupt architecture accommodates both PC-compatible Programmable Interrupt Controller (PIC) mode and APIC mode interrupts through use of the integrated I/O APICs in the CSB5. Figure 3 shows the PIC mode interrupt routing supported in the baseboard. Table 13 lists the symmetric mode interrupt routing for IRQ0-15 and PIQRQ0-24. Figure 4 shows the symmetric mode interrupt routing for PIRQ24-31.

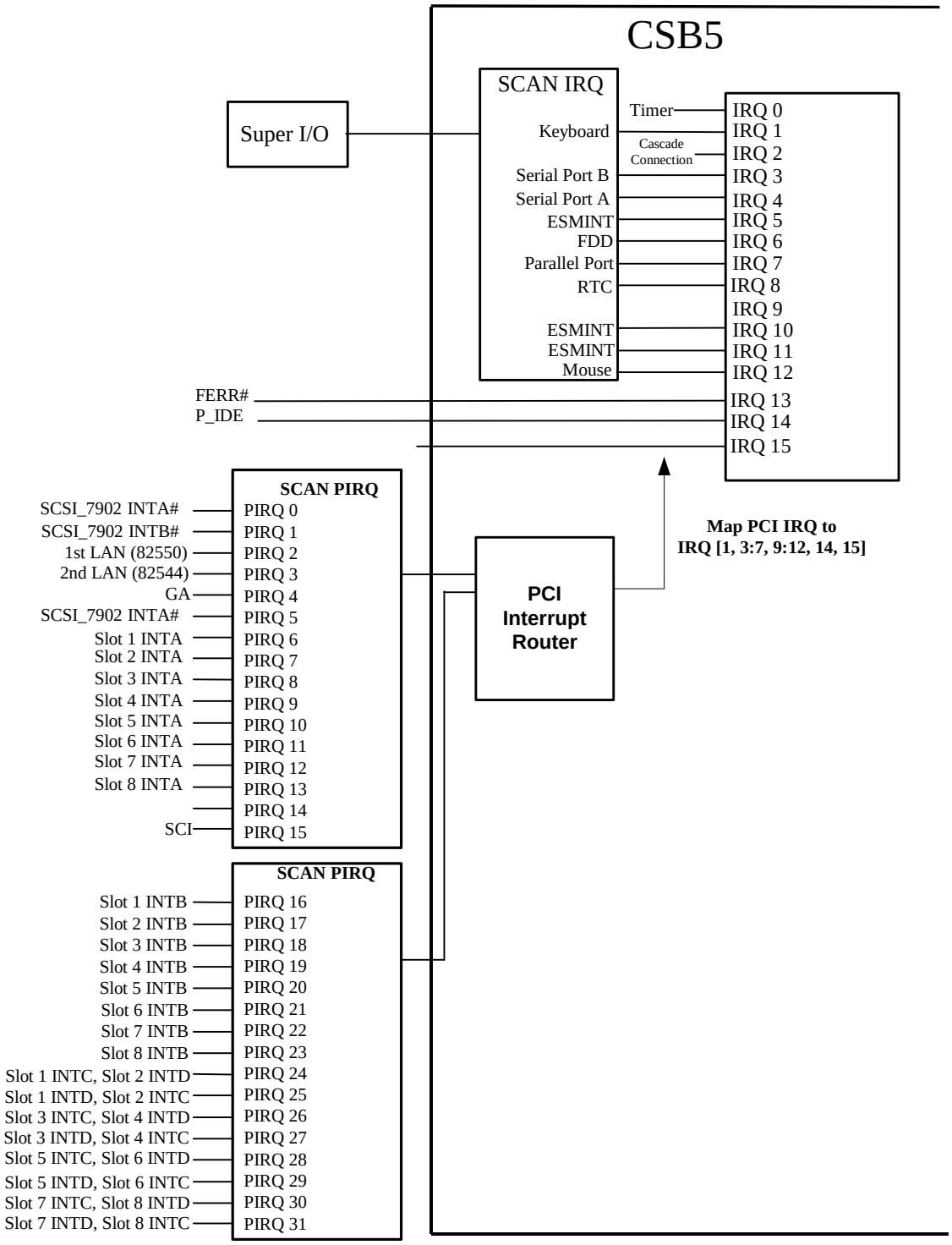


Figure 3. Interrupt Routing (PIC Mode)

Table 13. Interrupt Routing (Symmetric Mode)

Input	IRQx/PIRQx Connection
Timer	IRQ0
Keyboard	IRQ1
(Cascade connection)	IRQ2
Serial Port B	IRQ3
Serial Port A	IRQ4
ESMINT	IRQ5
Floppy	IRQ6
Parallel	IRQ7
RTC	IRQ8
	IRQ9
ESMINT	IRQ10
ESMINT	IRQ11
Mouse	IRQ12
Coprocessor Error	IRQ13
P_IDE	IRQ14
	IRQ15
SCSI (7902) Port A	PIRQ0
SCSI (7902) Port B	PIRQ1
LAN 1 (82550)	PIRQ2
LAN 2 (82544)	PIRQ3
VGA	PIRQ4
SCSI (7902) Port A	PIRQ5
Slot 01 INTA	PIRQ6
Slot 02 INTA	PIRQ7
Slot 03 INTA	PIRQ8
Slot 04 INTA	PIRQ9
Slot 05 INTA	PIRQ10
Slot 06 INTA	PIRQ11
Slot 07 INTA	PIRQ12
Slot 08 INTA	PIRQ13
	PIRQ14
SCI	PIRQ15
Slot 01 INTB	PIRQ16
Slot 02 INTB	PIRQ17
Slot 03 INTB	PIRQ18
Slot 04 INTB	PIRQ19
Slot 05 INTB	PIRQ20
Slot 06 INTB	PIRQ21
Slot 07 INTB	PIRQ22
Slot 08 INTB	PIRQ23

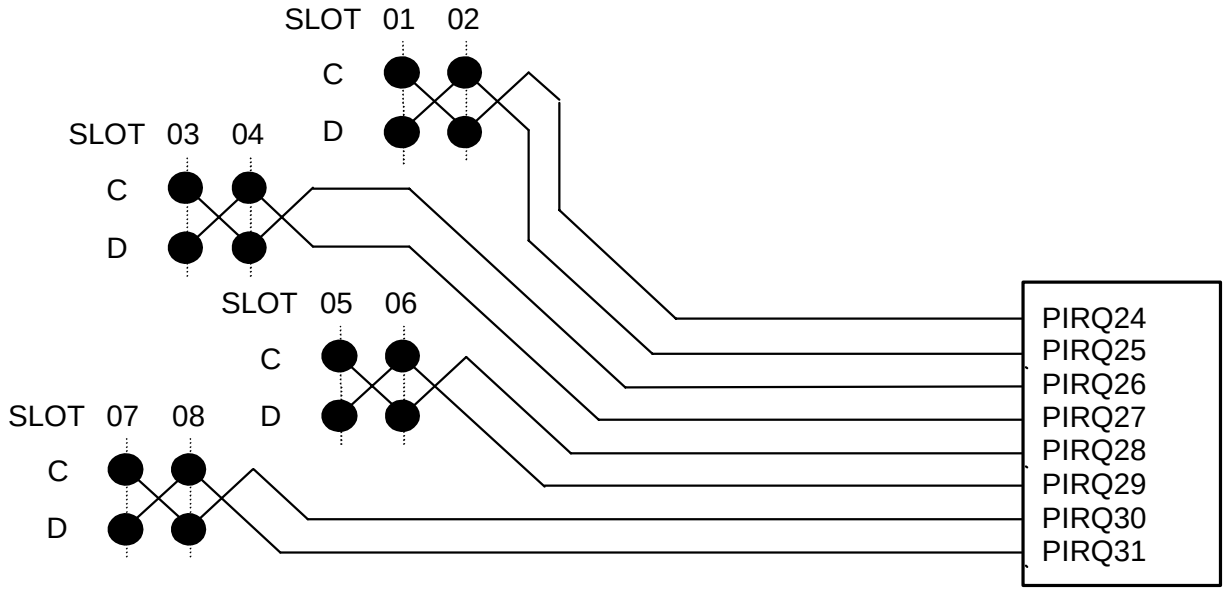


Figure 4. Interrupt Routing (Symmetric Mode)

The XIOAPIC logic inside the CSB5 has 48 entries, 16 of which are for legacy interrupts and 32 entries are for PCI interrupts. The 48 entries are implemented as three 16-entry XIOAPIC units. The basic building block for the XIOAPIC is 16-entry IOAPIC.

The Server System SSH4 baseboard supports mapping (redirection) of any of the 32 PCI interrupt sources to legacy interrupts. The legacy interrupt lines after mapping logic are connected to input of 82559 inside of CSB5.

3.7.1 Serialized IRQ support

The Server System SSH4 baseboard supports the serialized interrupt delivery mechanism. The serialized IRQ (SERIRQ) consists of a start frame, a minimum of 17 IRQ/ data channels, and a stop frame. Any slave device in quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

3.7.2 IRQ Scan for PCIIRQ

The IRQ/data frame structure includes the ability to handle up to 32 sampling channels with the standard implementation using the minimum 17 sampling channels. The baseboard has an external PCI interrupt serializer for PCIIRQ scan mechanism of CSB5 to support 32 PCIIRQs.

4. Server System SSH4 ACPI Implementation

This section documents the SSH4 Advanced Configuration and Power Interface (ACPI) implementation based on the ACPI Specification, Revision 1.0b.

The SSH4 platform supports the S0, S1, S4, and S5 states. When the system is operating in ACPI mode, the OS retains control of the system and OS policy determines the entry methods and wakeup sources for each sleep state—*sleep entry and wakeup event capabilities are provided by the hardware but are enabled by the OS*.

An ACPI-aware operating system generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by sending the appropriate command to the BMC to enable ACPI mode. The system automatically returns to legacy mode upon hard reset or power-on reset.

4.1 Front Panel Switches

The Server System SH4 baseboard supports up to five front panel buttons (via the front panel connector): the power button, the sleep button, the reset button, the ID button, and an NMI button.

The power button on the chassis is a request that is forwarded by the BMC to the power state machines in the National Semiconductor PC87417 Super I/O controller (SIO). The power button is monitored by the BMC and does not directly control power on the power supply.

The power button and the sleep button behave differently depending on whether or not the operating system supports ACPI. The sleep button has no effect unless an operating system with ACPI support is running. If the operating system supports ACPI and the system is running, pressing the sleep button causes an event. The operating system causes the system to transition to the appropriate system state depending on the user settings.

- **Power State Off to On:** The CSB5 and SIO may be configured to generate wakeup events for several different system events: Wake on LAN, PCI Power Management Interrupt, and Real Time Clock Alarm are examples of these events. The BMC monitors the power button and wakeup event signals from the SIO. A transition results in the BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The SIO receives power good and reset from the BMC and then transition to an ON state.
- **Power State On to Off (Legacy):** The SIO is configured to generate an SMI due to a power button event. The BIOS services this SMI and sets the state of the machine in the CSB5 and SIO to the OFF state. The BMC monitors power state signals from the SIO and deasserts PS_PWR_ON to the power supply.
- **Power State On to Off (ACPI):** If an ACPI operating system is loaded, the power button switch generates a request (via SCI) to the OS to shutdown the system. The OS retains control of the system and OS policy determines the entry methods and wakeup sources for the sleep state (if any) the system transitions into.

- **Power State On to Sleep (ACPI):** If an ACPI operating system is loaded, the sleep button switch generates a request (via SCI) to the OS to place the system in “sleep” mode. The OS retains control of the system and OS policy determines the entry methods and wakeup sources for the sleep state (if any) the system transitions into.
- **Power State Sleep to On (ACPI):** If an ACPI operating system is loaded, the sleep button switch generates a wake event to the CSB5 and a request (via SCI) to the OS to place the system in the “On” state. The OS retains control of the system and OS policy determines the entry methods and wakeup sources for the sleep state (if any) the system can wake from.

4.2 Wake Up Sources (ACPI and Legacy)

The Server System SSH4 hardware is capable of wake up from several sources under both ACPI and non-ACPI or legacy configurations, such as when the operating system does not support ACPI. The wake up sources for both configurations are defined in the table below. Under ACPI, the operating system programs the CSB5 and SIO to wake up on the desired event, but in legacy mode, the BIOS enables/disables wake up sources based on a switch in Setup. It is required that the operating system or a driver will clear any pending wake up status bits in the associated hardware, such as the Wake on LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI power management event (PME) status bit in a PCI device. The legacy wake up feature is disabled by default.

Table 14. Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
Sleep Button	S1	No
Ring indicate from Serial Port A	S1, S4	Yes
Ring indicate from Serial Port B	S1, S4	Yes
PME from PCI 32/33	S1, S4	Yes
PME from PCI 64/66, 64/33	S1, S4	Yes
RTC Alarm	S1, S4	Yes
Mouse	S1	No
Keyboard	S1	No
USB	S1	No

5. Server System SSH4 System Bus Error Monitoring

This section documents the types of system bus error conditions monitored by the board set and how they propagate to SMI# and NMI#.

One of the major requirements of server management is to correctly and consistently handle system errors. System errors, which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus
- Processor bus errors
- Memory single- and multi-bit errors
- IMB errors

On the server system SSH4, General Server Management sensors are managed by the BMC. See the “Sahalee Baseboard Management Controller (BMC)” section for specifics on these sensors.

5.1 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS (enabled by default).

5.2 Intel® Xeon™ Processor Bus Errors

The CMIC supports all the data integrity features supported by the Intel® Pentium® Pro bus including Address, Request and Response parity. The CMIC always generates ECC data while it is driving the processor data.

In the case of unrecoverable errors on the host processor bus, proper execution of SMI handler cannot be guaranteed and the SMI handler cannot be relied upon to log such conditions. The BIOS SMI handler will record the error to the system event log only if the system has not experienced a catastrophic failure that compromises the integrity of the SMI handler. The BIOS always enables the error correction and detection capabilities of the processors by setting appropriate bits in processor model specific register (MSR).

5.3 Memory Bus Errors

The CMIC provides two output pins for error reporting: ALERT# and FATAL#. ALERT# is used to report correctable memory errors like Correctable Memory Data bus errors. The reporting of correctable errors can be enabled/disabled by programming the SEMR register in the CMIC. The CMIC generates SMI on correctable ECC errors and the BMC records the errors as well as failing DIMM location in the SEL without halting the system. Uncorrectable ECC errors are logged in the SEL by the BMC and the system is halted. However, the BMC cannot determine the location of the failing DIMM.

5.4 IMB Bus Errors

The IMB bus supports parity protection on the IMBus. Communication integrity is checked with use of a parity bit for each direction. Error reporting and retry are supported using obligatory acknowledgement for all requests.

5.5 Error Escalation

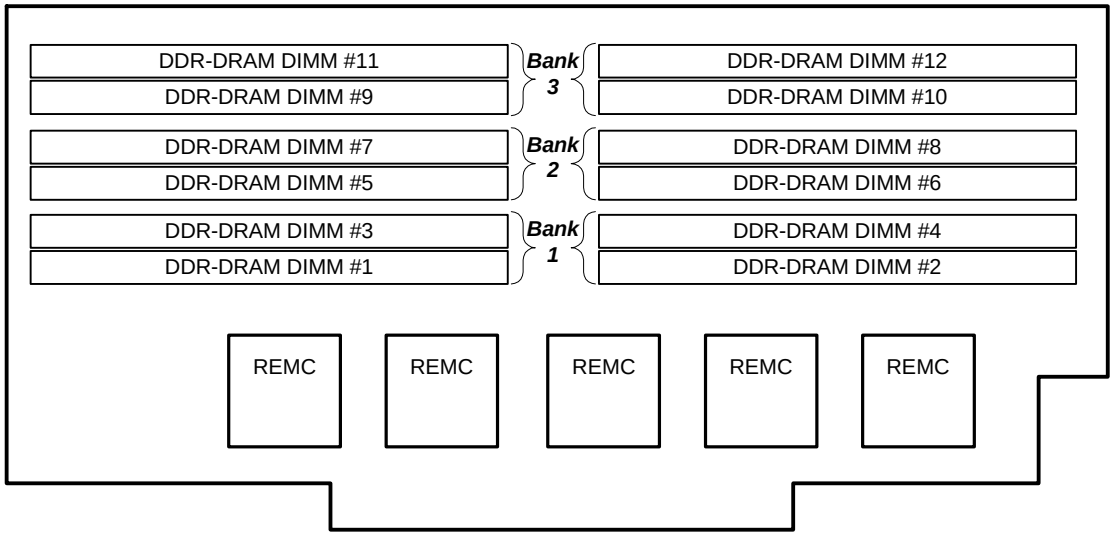
FATAL # is used to report fatal errors in the system, these errors include Uncorrectable ECC Errors, BUS protocol errors, ADDRESS and control PARITY errors, IMBus PROTOCOL and parity errors. The reporting of fatal errors can be enabled or disabled by programming the SEMR register in the CMIC.

6. Server System SSH4 DDR Memory Board

The memory board plugs into the memory riser connector on the processor board. The memory board contains five REMCs (Reliability Enhanced Memory Controllers), one clock buffer to provide 100-MHz clocks to the REMCs, voltage regulation circuits to provide power for the DIMMs, I^2C components to add server management features, and the 12 DIMM sockets. At least one bank of memory (four DIMM sockets) starting with bank 1 must be populated for the system to boot.

The memory board supports a minimum memory capacity of 512 MB using 128 MB DIMMs up to a maximum memory capacity of 24 GB of system memory using 2 GB DDR Registered DIMMs.

Figure 5 is a drawing of the memory board.



DIMM Loading Order
Bank 1: DIMMs 1, 2, 3, and 4
Bank 2: DIMMs 5, 6, 7, and 8
Bank 3: DIMMs 9, 10, 11, and 12

Figure 5. Memory Board Outline Diagram

6.1 Memory DIMM Support

The memory board supports only PC-200 or PC-266 compliant registered ECC SDRAM DIMMs. Only DIMMs tested and qualified by Intel or a designated memory test vendor are supported. All DIMMs are supported by design, but only fully qualified DIMMs will be supported. All supported DIMMs are listed in the Tested Memory List Summary Posted monthly on the Intel® Business Link and the Intel® Premier Support site.

- ECC single-bit errors will be corrected and multiple-bit error will be detected
- The maximum memory capacity is 24 GB
- The minimum DIMM size is 128 MB, memory capacity of 512 MB
- The maximum DIMM size is 2 GB, memory capacity of 24 GB

DIMM and memory configurations must adhere to the following:

- PC-200 or PC-266 compliant ECC SDRAM registered DIMM modules
- DIMM organization: x72 ECC
- Pin count: 184
- DIMM capacity: 128 MB, 256 MB, 512 MB, 1 GB, and 2 GB DIMMs
- Serial PD: JEDEC Rev 2.0
- Voltage options: 2.5 V (VDD/VDDQ)
- Interface: LVTTL
- Four DIMMs must be populated in a bank for a x288 wide memory data path

Note: The board set will support both stacked and un-stacked DDR compliant registered DIMMs, although thermal limitations of certain chassis may limit the configured system support. Conduct thermal testing to ensure your chassis provides adequate cooling to support the target memory configurations.

Note: The power dissipation of some un-stacked DIMMs exceeds that of some stacked DIMMs. Be sure to conduct thermal evaluations of all possible memory to be populated.

6.2 Memory Configuration

Data transfers occur between the CMIC and the DIMMs in a four-way interleaved fashion. This requires that four DIMMs be populated per bank in order for the system to operate. At least one bank must be populated in order for the system to boot. If additional banks have less than four DIMMs, the memory for that bank(s) will not be available to the system.

There are three banks of DIMMs, labeled 1, 2, and 3. Bank 1 contains DIMM sockets 1, 2, 3, and 4. Bank 2 contains DIMM sockets 5, 6, 7, and 8. Bank 3 contains DIMM sockets 9, 10, 11, and 12. DIMM sockets identifiers are marked with silkscreen next to each DIMM socket on the board.

The board’s signal integrity and cooling are optimized when memory banks are populated in order. Therefore, when installing memory, DIMMs should be installed starting with bank 1 and ending with bank 3.

6.3 DDR Memory Board Components

6.3.1 330-pin Edge Connector

The memory board plugs into the 330-pin edge connector on the processor board. The 100 MHz interface between the CMIC and the five REMCs goes through this connector. The interface includes control signals (RAS, CAS, CS, and Address), 144 bits of data and ECC, a 100-MHz clock to the clock buffer. One I^2C from the baseboard connects to a PCA9544 I^2C multiplexor for server management functions.

6.3.2 REMC

The REMC is designed such that it supports two modes of operation: Data Path (DP) mode and Address Path (AP) mode. Five REMCs facilitate a four-way interleaved memory sub-system. Four REMCs are used in DP mode and facilitate data multiplexing and buffering.

The fifth REMC is used in AP mode and generates multiple copies of address and control signals for memory sub-system. The fifth REMC is used to buffer the SDRAM address, control signals from the CMIC, and drive them to the SDRAM. Each provides four copies of address and control signals, so it can support up to four banks of DDR DRAM DIMM modules.

In four-way interleaved mode, all Data Path REMCs connect to the DIMMs by 72-bit interface and to the CMIC by a 144-bit interface. All REMCs utilize a core voltage of 2.5 V. This voltage is generated using a 2.5 V regulator on the memory board. The +12 V supply from the baseboard is used as the source to generate the 2.5 V core voltage for the REMCs.

6.3.3 I^2C Buses

An I^2C bus from the baseboard connects to a PCA9544 I^2C multiplexer. The multiplexer serves three distinct I^2C buses.

- One I^2C bus connects to the first six DIMM sockets (DIMMs 1 to 6)
- A second I^2C bus connects to next six DIMM sockets (DIMMs 7 to 12)
- A third I^2C bus connects to the REMCs and the I^2C EEPROM

The DIMM's I^2C buses are for the BIOS to retrieve SPD information from each DIMM such as type, size, etc. to program the CMIC memory registers accordingly to boot the system. The FRU EEPROM contains useful information for field services. Refer to

Table 15 for information on the I^2C addresses for the memory module SMB.

Table 15. I^2C Addresses for Memory Module SMB

Device	Address
DIMM 1, 7	0xA0
DIMM 2, 8	0xA4
DIMM 3, 9	0xA8
DIMM 4, 10	0xA2
DIMM 5, 11	0xA6

DIMM 6, 12	0xAA
EEPROM	0xE0
REMC	0xE2

6.3.4 Clocks

A clock buffer on the memory board generates zero delay, low skew, and low jitter for the REMCs and DIMMs. The CDCV850 is a zero-delay buffer that takes the 100-MHz input clock from the baseboard and generates two 100-MHz clocks to the five REMCs, and 12 clocks to the DIMMs.

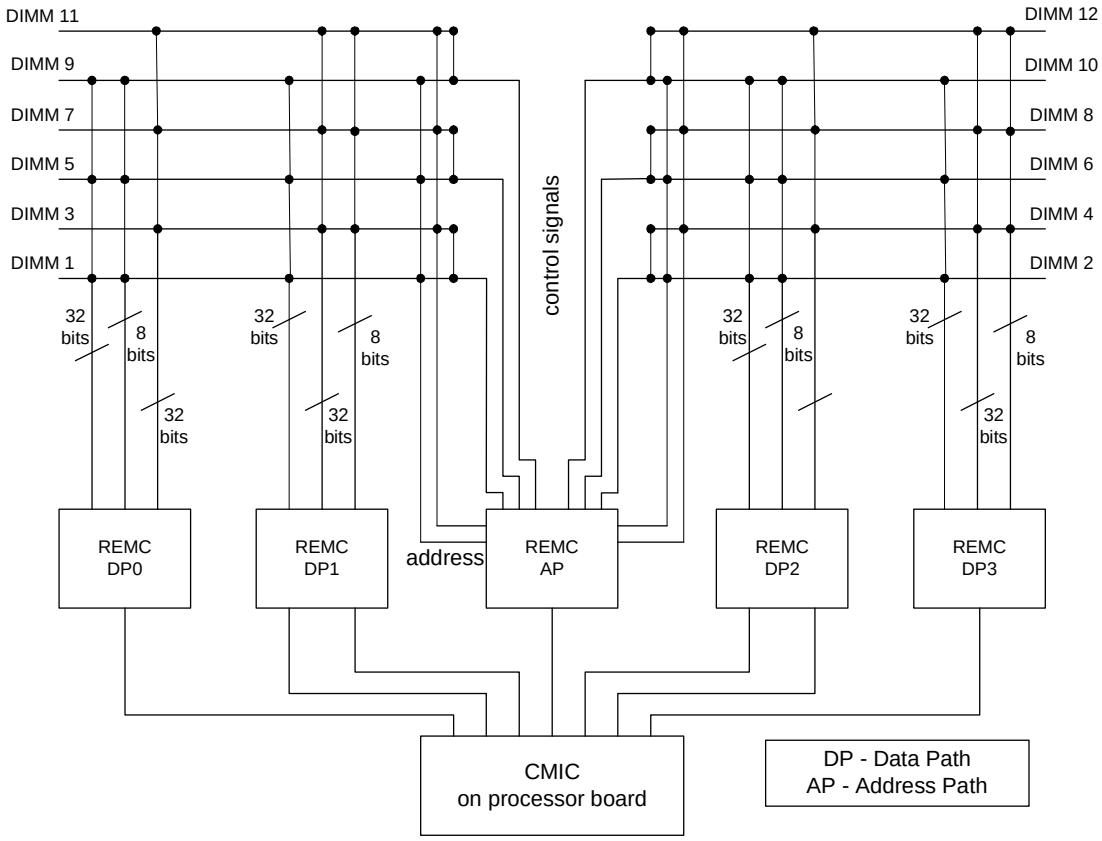


Figure 6. Memory Block Diagram

6.4 Advanced Memory Configuration

Intel provides Advanced Memory Configuration only for Shasta Server. There are two types of memory configurations: Single-Board Mirrored Memory and Online Spare Memory. The configuration should be done during BIOS setup and user needs to choose either Single Board Mirrored Memory or Online Spare Memory. Both can not co-exist.

6.4.1 Single Board Mirrored Memory

Single-Board Mirrored Memory uses mirrored banks on a single memory board to provide a high level of memory redundancy. This feature provides protection against multi-bit errors without degrading the performance of the memory system.

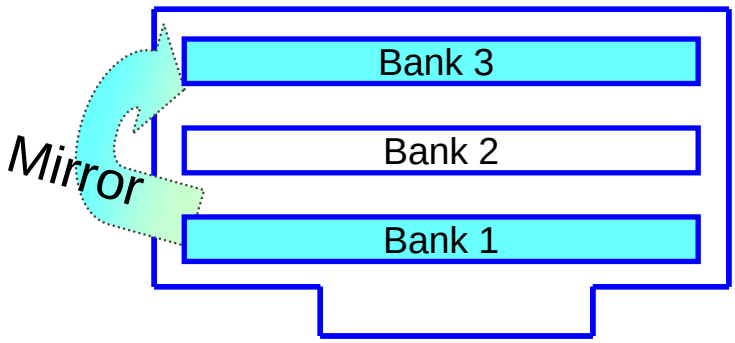


Figure 7 Advanced memory Configuration

DIMM Capacity and Configuration Requirements for Single-Board Mirrored Memory

- Memory is quad-interleaved and as a result the DIMMs must be installed in banks consisting of four DIMMs per bank.
- Mirrored banks must be configured identically. Corresponding banks must be populated with DIMMs of the same capacity.
- Banks must be installed in pairs. BANK 1 mirrors BANK 3.

Operation of Single Board Mirrored Memory

To configure this option, user needs to select “Mirroring” option in BIOS. After the system is properly configured for Mirrored Memory, the bank related information (healthy – green) is displayed in PIC for all the DIMMs. DIMMS configured for Online Spare/Mirror Memory Feature will have an additional tag of ‘<Spare/Mirror>’ to indicate that they are enabled for the Memory Management feature.

Currently BIOS does not provide sufficient information for PI to distinguish between Online Spare Memory and Mirror Memory, hence the tag will contain both options i.e. ‘<Spare/Mirror>’. This will convey to the user that the Shasta server has been configured for either of the Memory management features.

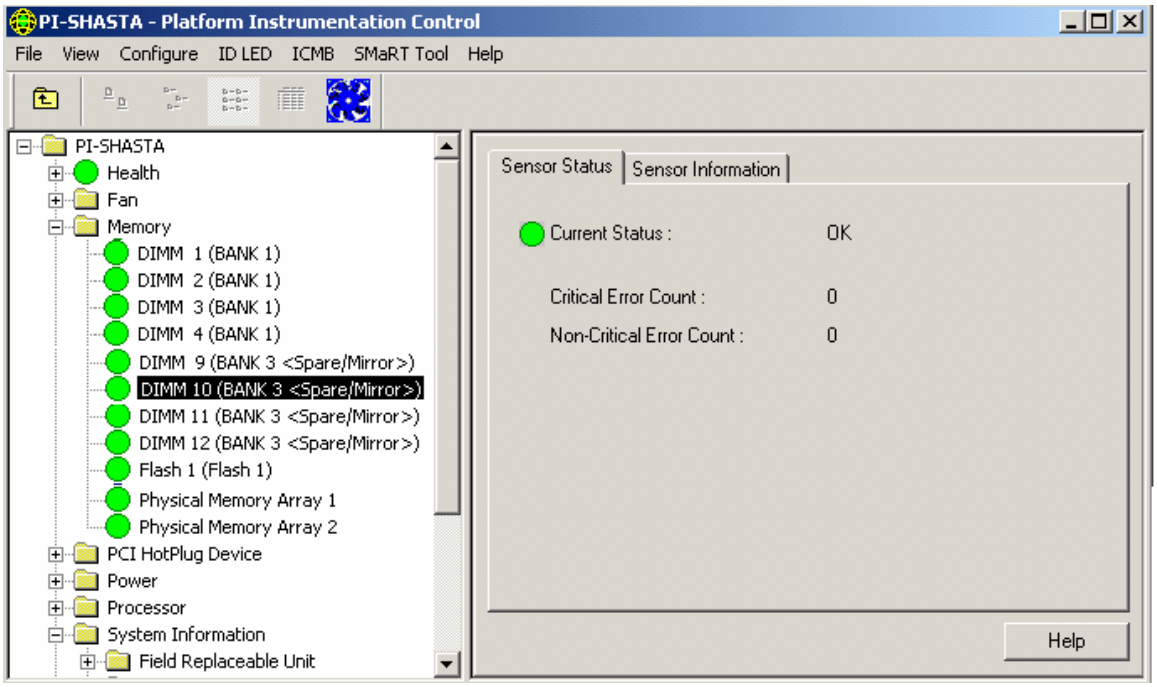


Figure 8 Advanced Mirror Memory Configuration status Tab (Normal

When configured for Single Board Mirrored Memory, the system is running a completely redundant set of DIMMs on mirrored memory banks. As the data is sent to memory, it is written by the memory controller to both banks of the mirrored pair simultaneously. During a memory read, if any DIMM in the master bank has a multi-bit error i.e. uncorrectable error, the system rereads the correct data from the redundant memory bank(s) and performs all future reads from the redundant memory bank(s). Since both sets of memory are being written to, there is no copying of data from one card to the other, and failover is immediate. As a result, the system can experience a non-correctable hard memory error, such as full DIMM failure, without interrupting service.

Failure Detection and Notification in Single-Board Mirrored Memory

Multi-bit errors

Multi-bit errors are identified only at the bank level. When a multibit error occurs in Single Board Mirror Memory, the system will fail-over to the redundant memory bank. If the system is configured for Single-Board Mirrored Memory, the memory controller will count single-bit errors, but will not fail-over. Fail-over in Single-Board Mirrored Memory occurs only when a multi-bit error is encountered.

If any one of the DIMM sensor associated with a bank encounters a multi-bit error, all the DIMMs in the bank will be displayed as critical in PIC GUI.

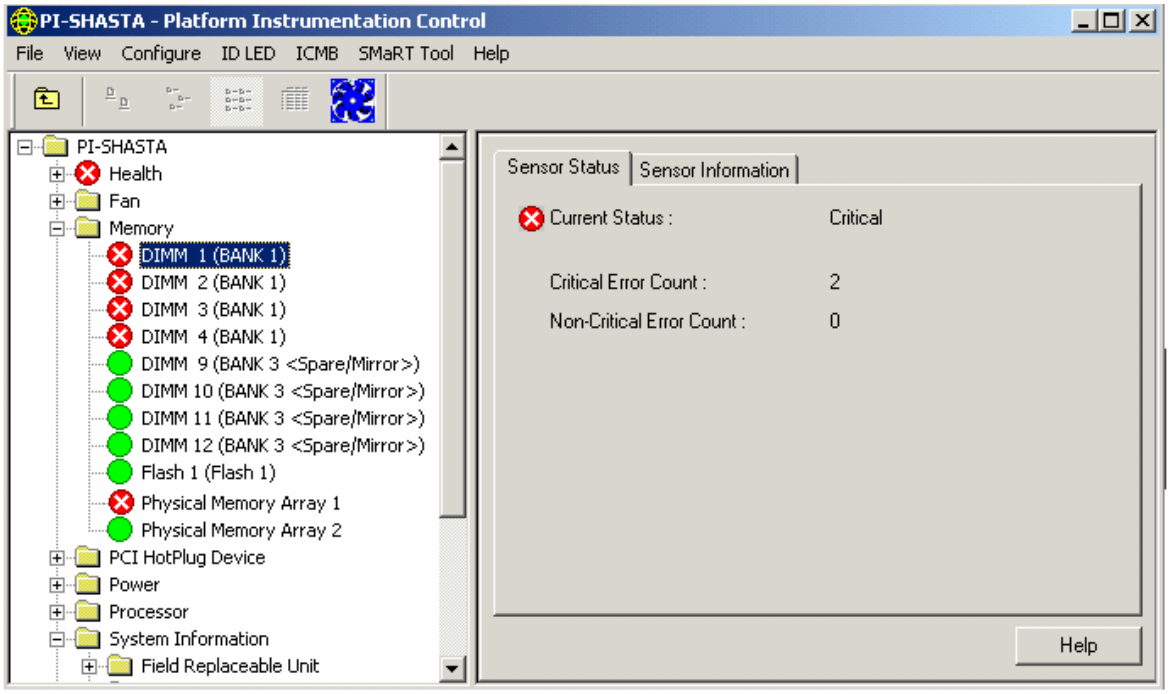


Figure 9 Advanced Mirrir Memory Configuration Sensor Status Tab (Critical)

6.4.2 Online Spare Memory

Online Spare Memory uses an online spare bank to provide DIMM failover capabilities when a pre-defined threshold of single-bit correctable errors is reached.

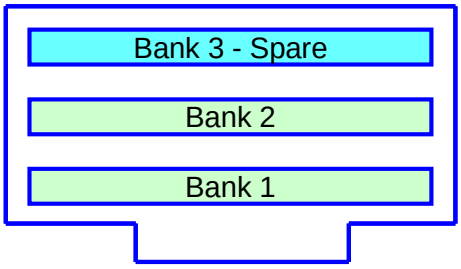


Figure 10 Advanced Spare Memory Configuration

DIMM Capacity and Configuration Requirements for Online Spare Memory

- Memory is quad-interleaved and as a result the DIMMs must be installed in banks consisting of 4 DIMMs per bank..
- The DIMMs in a bank must be of the same capacity. Manufacturer and have the same SPD characteristics.

Operation of Online Spare Memory

To configure this option, user needs to select “Sparing” option in BIOS. After the system is properly configured for Online Spare Memory, the following bank related information (healthy – green) is displayed in PIC for all the DIMMs.

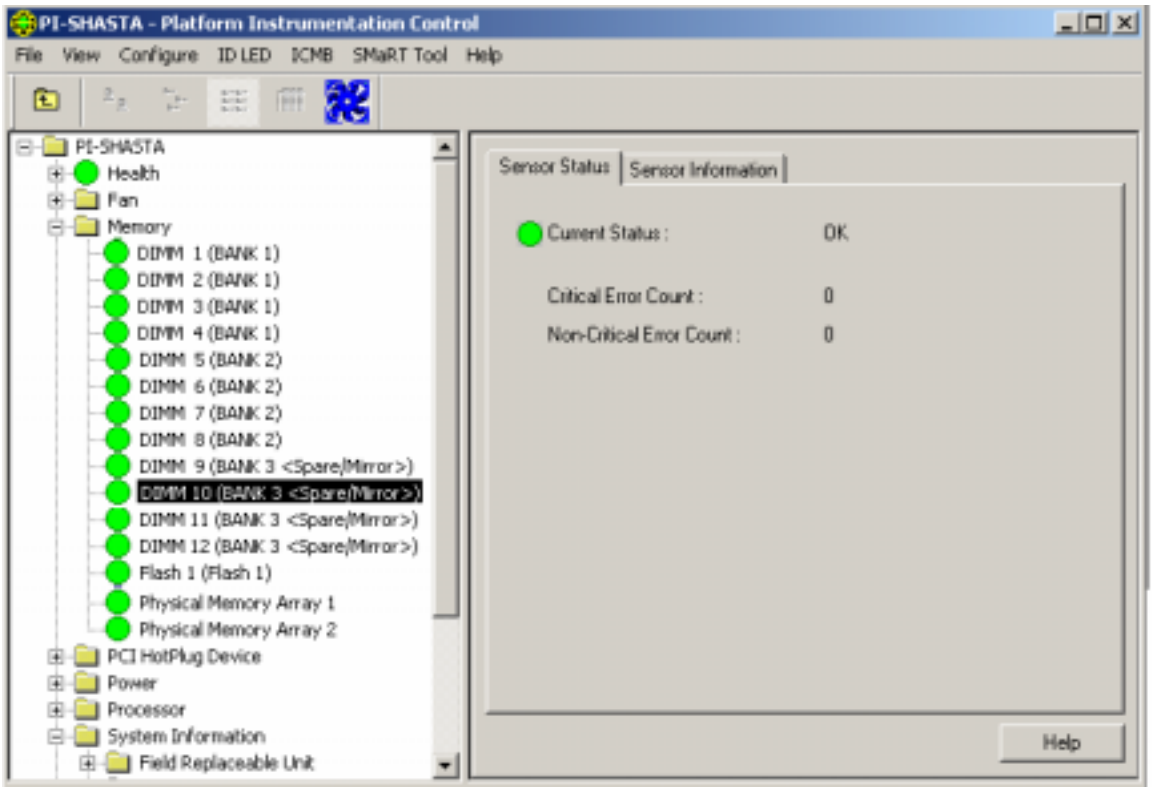


Figure 11 Advanced Spare Memory Configuration Sensor Status Tab (Normal)

In normal mode of operation, system reads/writes memory data to active bank (Bank#1/Bank#2). The system does not read/write memory data to spare bank (Bank#3).The Spare Bank (Bank#3) does not have memory data before memory data sparing begins.

Fail-over occurs when the correctable error count on a DIMM in the active bank reaches the pre-determined single-bit error threshold i.e. correctable error, which is set by BIOS at boot time. At the point of fail-over, the contents of the error bank will be copied to the spare bank, after which system degenerates error bank and records error log.
After the copy process is complete, all read and write requests will be serviced from the spare bank. If the correctable error count on the spare bank exceeds the threshold values, the system will assert fatal error.

If correctable error in any DIMM sensor associated with the Bank reaches the threshold value all the DIMMs in the BANK will be displayed as critical in PIC GUI.

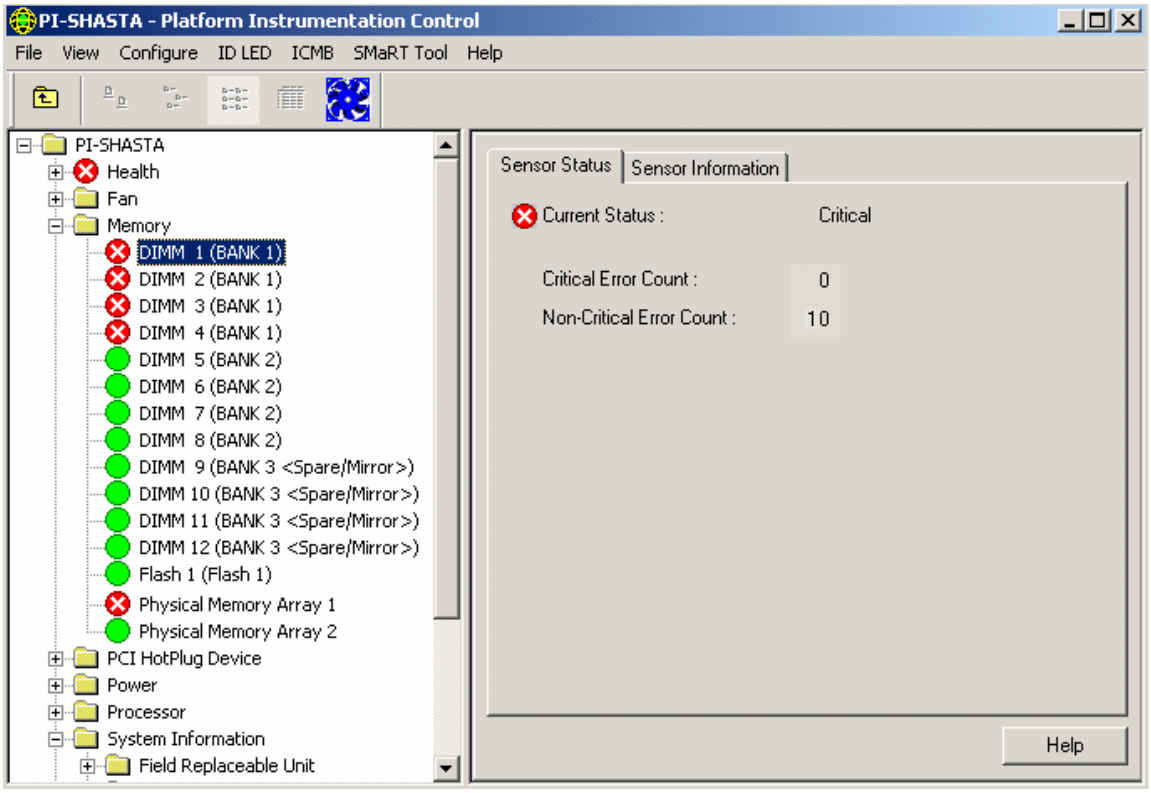


Figure 12 Advanced Spare Memory Configuration Status Tab (Critical)

Online Spare Memory does not recover uncorrectable error. Therefore, if system detects uncorrectable error, system will assert fatal error and the system will halt.

7. Server Management

The server management features are implemented using the Sahalee baseboard management controller chip. The Sahalee BMC is an ASIC packaged in a 156-pin BGA that contains a 32-bit RISC processor core and associated peripherals. Figure 13 illustrates the SSH4 server management architecture. A description of the hardware architecture follows the diagram.

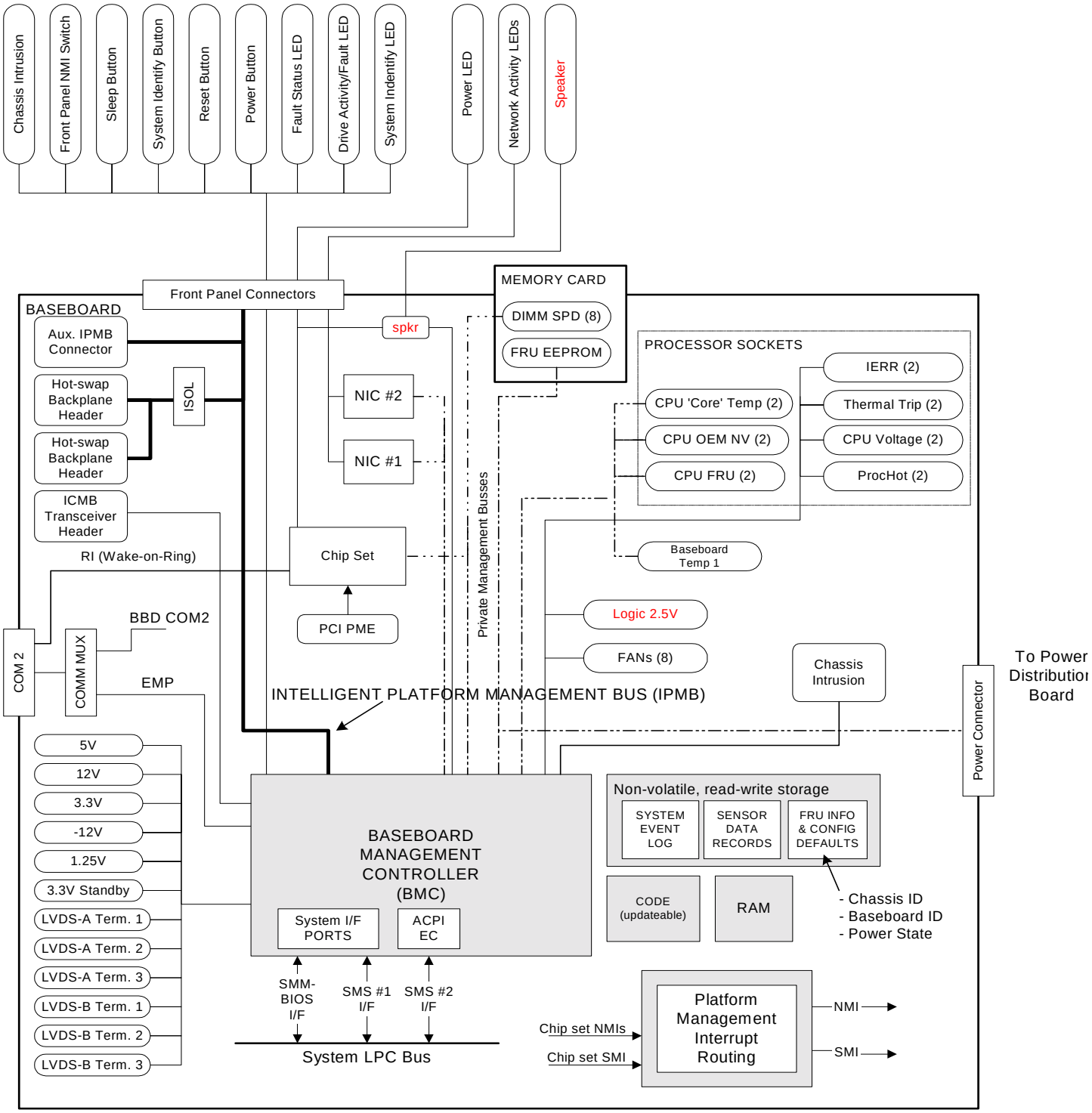


Figure 13. SSH4 Sahalee BMC Block Diagram

7.1 Sahalee Baseboard Management Controller (BMC)

The Sahalee BMC contains a 32-bit RISC processor core and associated peripherals used to monitor the system for critical events. The Sahalee BMC, packaged in a 156-pin BGA, monitors all power supplies, including those generated by the external power supplies and those regulated locally on the baseboard. The Sahalee BMC monitors SCSI termination voltage, fan tachometers for detecting a fan failure, and system temperature. Temperature is measured on each of the processors and at locations on the server board away from the fans. When any monitored parameter is outside of defined thresholds, the Sahalee BMC logs an event in the System Event Log (SEL).

Management controllers and sensors communicate on the I^2C^*-based Intelligent Platform Management Bus. Attached to one of its private I^2C bus is Heceta5, an ADM1026, which is a versatile systems monitor ASIC. Some of its features include:

- Analog measurement channels
- Fan speed measurement channels
- General-Purpose Logic I/O pins
- Remote temperature measurement
- On-chip temperature sensor
- Chassis intrusion detect

The table below details some of the inputs on the Heceta5 (ADM1026) as used on the Server System SSH4.

Table 16. ADM1026 Input Definition

Pin	ADM1026 Signal Name	Type	External Signal Name / Function
1	GPIO9	Digital Input	CPU2_IERR / CPU2 IERR
2	GPIO8	Digital Input	CPU1_IERR / CPU1 IERR
3	FAN0/GPIO0	Digital Output	ADM_DIS_CPU1_L / CPU1 Stop Clock
4	FAN1/GPIO1	Digital Output	ADM_DIS_CPU2_L / CPU2 Stop Clock
5	FAN2/GPIO2	Digital Input	Not connected / CPU2 VID [0]
6	FAN3/GPIO3	Digital Input	Not connected / CPU2 VID [1]
9	FAN4/GPIO4	Digital Input	ADM_INTR / CPU2 VID [2]
10	FAN5/GPIO5	Digital Input	ADM_NMI / CPU2 VID [3]
11	FAN6/GPIO6	Digital Input	ADM_A20MN / CPU2 VID [4]
12	FAN7/GPIO7	Digital Input	ADM_IGNNEN / CPU1 VID [0]
13	SCL	Digital Input	SM3_CLK / Open-drain Serial Bus Clock. Requires 2.2k pull-up resistor.
14	SDA	Digital I/O	SM3_DATA / Serial Bus Data. Open-drain output. Requires 2.2k pull-up resistor.
16	CI (Chassis Intrusion	Digital Input	FRONTOPEN+03 / An active high input which captures a Chassis Intrusion event in Bit 7 of Status Register 4. This bit will remain set until cleared, so long as battery voltage is applied to the VBAT input, even when the ADM1026 is powered off.
18	PWM	Digital Output	ADM_FAN_PWM / Pulse-width modulated output for control of fan speed. Open drain.

Pin	ADM1026 Signal Name	Type	External Signal Name / Function
19	RESET_STBY	Digital Output	RST_BMCRST_L / Power-on Reset 5 mA driver (open drain), active low output with a 200 ms minimum pulse width. This is asserted whenever 3.3VSTBY is below the reset threshold. It remains asserted for approximately 200 ms after 3.3VSTBY rises above the reset threshold.
30	P5VIN	Analog Input	VP50 / Monitors +5 V supply
31	N12VIN	Analog Input	XN12 / Monitors -12 V supply
32	P12VIN	Analog Input	XP12 / Monitors +12 V supply
33	VCCP	Analog Input	VCC_P / Monitors processor core voltage (0 to 3.0 V)
34	AIN7	Analog Input	ADM_VDD_CMIC / Monitors +2.5V supply
35	AIN6	Analog Input	VTT_IMB / Monitors VTT supply
43	GPIO15	Digital Input	CPU2_THERMTRIPN / CPU2 Thermal Trip
44	GPIO14	Digital Input	CPU1_THERMTRIPN / CPU1 Thermal Trip
45	GPIO13	Digital Input	CPU2_PROCHOTN / CPU1 VID [4]
46	GPIO12	Digital Input	CPU1_PROCHOTN / CPU1 VID [3]
47	GPIO11	Digital Input	STPWCTLA / CPU1 VID [2]
48	GPIO10	Digital Input	STPWCTLB / CPU1 VID [1]

8-bit ‘analog’ readings for the following system temperatures are provided:

Table 17. Temperature Sensors

Temperature Sensor	Description	Resolution	Accuracy
Primary Processor	Primary processor socket thermal sensor	8-bit	+/- 5°C or better
Secondary Processor	Secondary processor socket thermal sensor	8-bit	+/- 5°C or better

7.1.1 Fault Resilient Booting

The Sahalee BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If the default bootstrap processor (BSP) fails to complete the boot process, FRB attempts to boot using an alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a watchdog timeout during POST. The watchdog timer for FRB level 2 detection is implemented in the Sahalee BMC.
- FRB level 3 is for recovery from a watchdog timeout on hard reset or power-up. The Sahalee BMC provides hardware functionality for this level of FRB.

7.1.1.1 FRB-1

In a multiprocessor system, the BIOS registers the application processors in the MP table and the ACPI APIC tables. When started by the BSP, if an AP fails to complete initialization within a certain time, it is assumed to be nonfunctional. If the BIOS detects that an application processor has failed BIST or is nonfunctional, it requests the BMC disable that processor. The BMC then generates a system reset while disabling the processor; the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the Multi-Processor Specification, Rev. 1.4), nor in the ACPI APIC tables, and is invisible to the operating system.

If the BIOS detects that the BSP has failed BIST, it sends a request to BMC to disable the present processor. If there is no alternate processor available, the BMC beeps the speaker and halts the system. If BMC can locate another processor, BSP ownership is transferred to that processor via a system reset.

7.1.1.2 FRB-2

The second watchdog timer (FRB-2) in the BMC is set for approximately 6 minutes by BIOS and is designed to guarantee that the system completes BIOS POST. The FRB-2 timer is enabled before the FRB-3 timer is disabled to prevent an unprotected window of time. Near the end of POST, before the option ROMs are initialized, the BIOS disables the FRB-2 timer in the BMC.

If the system contains more than 1 GB of memory and the user chooses to test every DWORD of memory, the watchdog timer is disabled before the extended memory test starts, because the memory test can take more than 6 minutes under this configuration. If the system hangs during POST, the BIOS does not disable the timer in the BMC, which generates an asynchronous system reset (ASR) . For more details, refer to the SSH4 Server Management EAS and to the Baseboard Management Controller Interface Specification. Document # 10535

7.1.1.3 FRB-3

The first timer (FRB-3) starts counting down whenever the system comes out of hard reset, which is usually about 5 seconds. If the BSP successfully resets and starts executing, the BIOS disables the FRB-3 timer in the BMC by de-asserting the FRB_TIMER_HLT# signal (GPIO) and the system continues on with the POST.

If the timer expires because of BSP failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system continues to change the bootstrap processor until the BIOS POST gets past disabling the FRB-3 timer in the BMC. The BMC sounds beep codes on the speaker, if it fails to find a good processor. The process of cycling through all the processors is repeated upon system reset or power cycle.

7.2 System Reset Control

Reset circuitry on the baseboard looks at resets from the front panel, CSB5, ITP, and the processor subsystem to determine proper reset sequencing for all types of resets. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

The following subsections describe each type of reset.

7.2.1 Power-up Reset

When the system is disconnected from AC power, all logic on the baseboard is powered off. When a valid input (AC) voltage level is provided to the power supply, 3.3-volt standby power will be applied to the baseboard. A power monitor circuit on 3.3-volt standby will assert *BMCRST_L,* causing the BMC to reset. The BMC is powered by 3.3 volt standby and monitors and controls key events in the system related to reset and power control.

After the system is turned on, the power supply will assert the *PWRGD+00* signal after all voltage levels in the system have reached valid levels. The BMC receives *PWRGD+00* and after approximately 500 ms asserts *RST_P6_PWRGOOD,* which indicates to the processors and CSB5 that the power is stable. Upon *RST_P6_PWRGOOD* assertion, the CSB5 will toggle PCI reset.

7.2.2 Hard Reset

A hard reset can be initiated by resetting the system through the front panel switch. During the reset, the Sahalee BMC de-asserts *RST_P6_PWR_GOOD*. After 500 ms, it is reasserted, and the power-up reset sequence is completed.

The Sahalee BMC is not reset by a hard reset. It may be reset at power-up.

7.2.3 Soft Reset

A soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers. Soft resets can be generated by the keyboard controller located in the SIO, or by the CSB5. The output of the SIO (*KBD_PINITL*) is input to the CSB5.

7.3 Intelligent Platform Management Buses

Management controllers (and sensors) communicate on the I^2C-based Intelligent Platform Management Bus. A bit protocol, defined by the *I^2C Bus Specification*, and a byte-level protocol, defined by the *Intelligent Platform Management Bus Communications Protocol Specification*, provide an independent interconnect for all devices operating on this I^2C bus.

The IPMB extends throughout the baseboard and system chassis. An added layer in the protocol supports transactions between multiple servers on inter-chassis I^2C bus segments.

In addition to the "public" IPMB, the Sahalee BMC also has four private I^2C busses that are used on the baseboard. The Sahalee BMC is the only master on the private busses. The following table lists all baseboard connections to the Sahalee BMC private I^2C busses.

Table 18. Private I^2C Bus, One Devices

Function	Voltage	Address	Notes
PCI Slot 1	3VSB	TBD	
PCI Slot 2	3VSB	TBD	
PCI Slot 3	3VSB	TBD	
PCI Slot 4	3VSB	TBD	
PCI Slot 5	3VSB	TBD	
PCI Slot 6	3VSB	TBD	

Table 19. Private I^2C Bus, Two Devices

Function	Voltage	Address	Notes
Aux Power Connector	3VSB	0XBC	Power unit (PIC16C74)
ADM1026	3VSB	0x58	

Table 20. Private I^2C Bus, Three Devices

Function	Voltage	Address	Notes
CMIC	3.3V	0xC0	North Bridge
CIOB30	3.3V	0xC4	I/O Bridge
CSB5	3.3V	0xC1	South Bridge
REMC – AP	2.5V	0xE0	Address Path
REMC – DP	2.5V	0xE8	Data Path
REMC – DP	2.5V	0xEA	
REMC – DP	2.5V	0xEC	
REMC – DP	2.5V	0xEE	
DIMM 1	3.3V	0xA0	
DIMM 2	3.3V	0xA1	
DIMM 3	3.3V	0xA2	
DIMM 4	3.3V	0xA3	
DIMM 5	3.3V	0xA4	
DIMM 6	3.3V	0xA5	
DIMM 7	3.3V	0xA6	
DIMM 8	3.3V	0xA7	
PCA9559	3.3V	0xE2	EEMUX

Table 21. Private I^2C Bus, Four Devices

Function	Voltage	Address	Notes
NIC1	3VSB	0x84	
NIC2	3VSB	0x86	

Table 22. Private I^2C Bus, Five Devices

Function	Voltage	Address	Notes
PC87417	3VSB	0x60	
CPU Thermal sensor #1	3VSB	0x30	
CPU Information ROM	3VSB	0xA0	
CPU Thermal sensor #2	3VSB	0x32	
CPU Information ROM	3VSB	0xA2	

8. Clock Generation and Distribution

All buses on the baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz at 2.5 V logic levels: For Processor 1, Processor 2, Processor 3, and Processor 4, the CMIC, and the ITP port
- 66/100 MHz at 3.3 V logic levels: For CMIC and the CIOB PCI clock
- 33.3 MHz at 5 V logic levels: Reference clock for the PCI bus clock driver
- 14.318 MHz at 3.3V logic levels: CSB5, Super I/O, and video clocks

The synchronous clock sources on the baseboard are:

- 100 MHz host clock generator for processors, the CMIC, and the ITP
- 66/100 MHz clock for CIOB and 33-MHz clock for CSB5 PCI clocks
- 48 MHz clock for CSB5 USB
- 33.3 MHz PCI reference clock
- 14.318 MHz CSB5, Super I/O, and video clocks

For information on processor clock generation, see the *CK133-WS Synthesizer/Driver Specification*.

The Server System SSH4 baseboard also provides asynchronous clock generators:

- 40 MHz clock for the embedded SCSI controller
- 32 kHz clock for the BMC

The memory board has the following clocks:

- 100 MHz clock for memory clock buffer, to the five REMCs and 12 DIMMs

Spread-spectrum signals are distributed over a wide range of frequencies and then collected onto their original frequency at the receiver. They are unlikely to interfere with other signals, even those transmitted on the same frequencies. Intel enables Spread Spectrum on the Server System SSH4 boardset to reduce EMI.

Figure 14 illustrates clock generation and distribution on the baseboard.

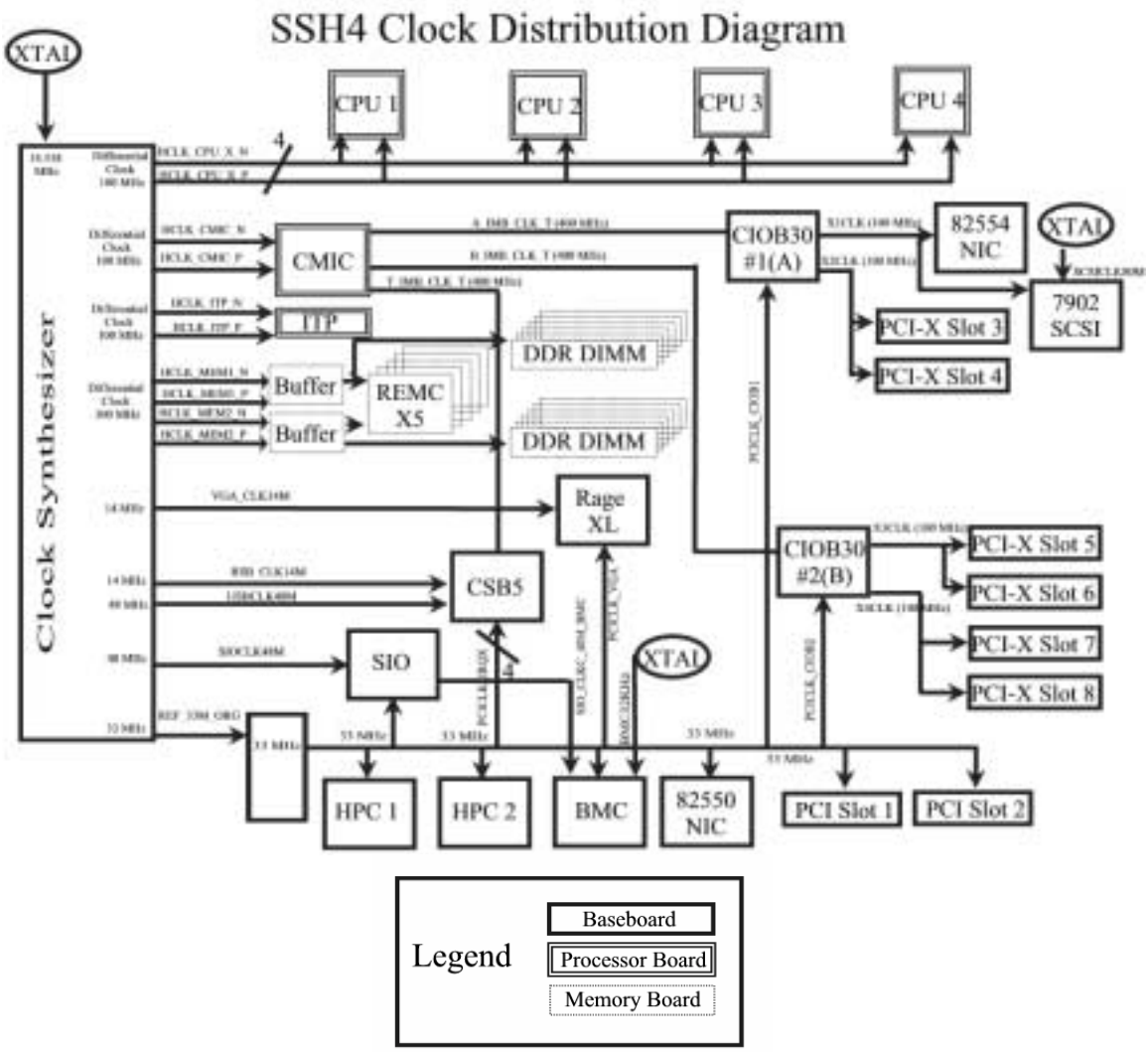
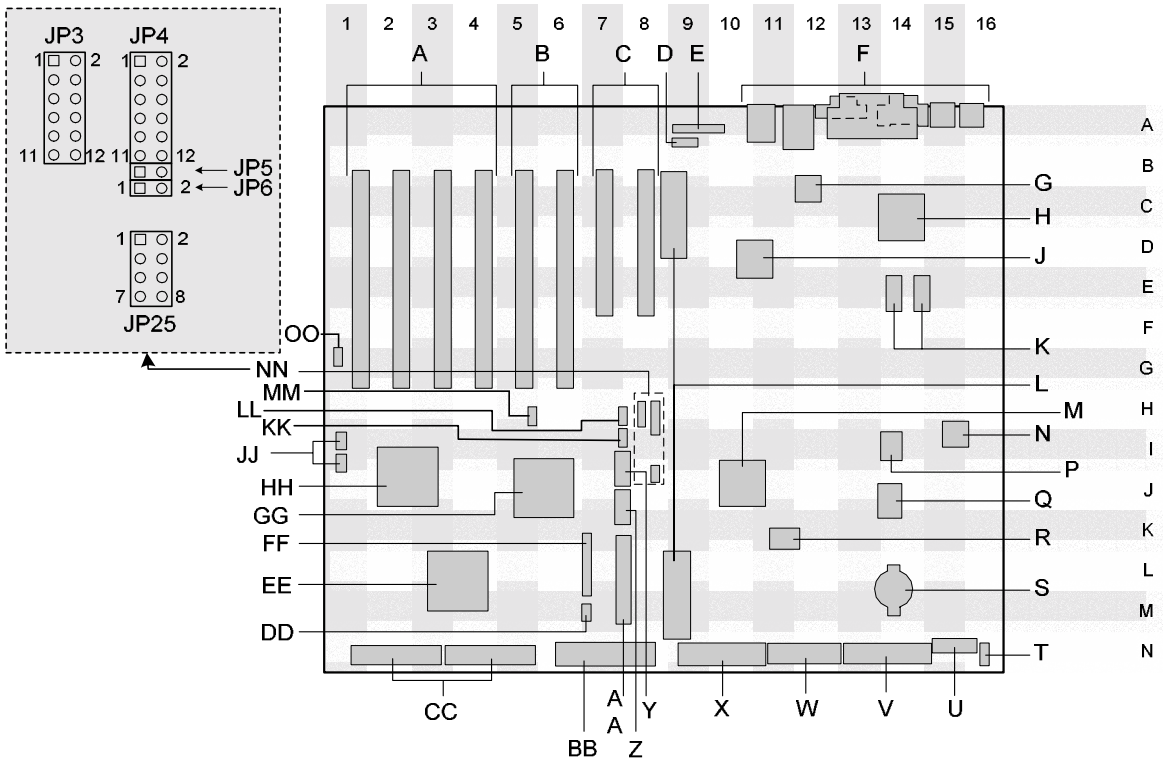


Figure 14. Baseboard and Memory Clock Distribution

9. Jumpers and Connectors

9.1 Baseboard Jumper, Connector, and Component Locations

This section describes jumper, connector, and component locations on the Server System SSH4 baseboard. Figure 15 shows the grid layout for the baseboard. The jumper blocks, onboard connectors, and header blocks are located using this grid layout. For example, the onboard battery is located at grid location 14M. The table below the figure identifies the connectors and major components on the SPSH4 baseboard.



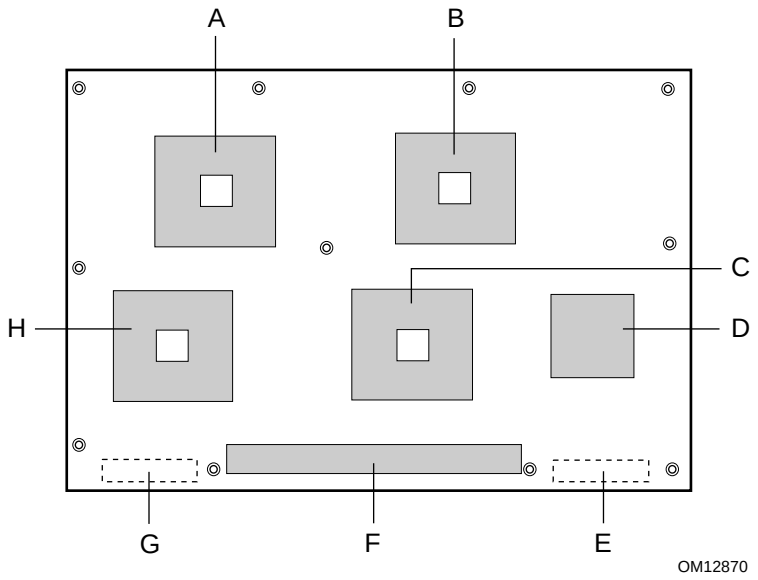
A	64-bit, 100-MHz, hot-plug PCI-X slots	U	14-pin Power Control connector (P35)
B	64-bit, 100-MHz, non-hot-plug PCI-X slots	V	24-pin Power connector (P32)
C	32 bit, 33-MHz, non-hot-plug PCI slots	W	20-pin Power connector (P28)
D	Intelligent Chassis Management Bus (ICMB) connector (P24)	X	Floppy disk drive connector (P25)
		Y	Serial port B connector (P17)
E	Hot-Plug Indicator Board (HPIB) connector (P23)	Z	USB #3 Header (P18)
		AA	Front Panel Header (P19)
F	Back Panel I/O connectors	BB	IDE Connector (P13)
G	Intel® 82550 Ethernet controller	CC	SCSI LVD connectors (P4 and P7)
H	ATI Rage XL 2D/3D graphics accelerator	DD	Intelligent Platform Management Bus (IPMB) connector (P12)
J	Intel® 82544 Ethernet controller		
K	Video RAM (VRAM) (4 MB total)	EE	Adaptec 7899 or 7902 SCSI controller (fab 704 baseboard
L	Processor board connectors (P21 and P22)	FF	Fan connector (P11)

M	ServerWorks South Bridge Controller (CSB5)	GG	ServerWorks PCI-X Bus Bridge Controller (CIOB30)
N	BMC component	HH	ServerWorks PCI-X Bus Bridge Controller (CIOB30)
P	BIOS Flash component	JJ	RAID LED connectors (P1 and P2)
Q	PC87417 Super I/O controller	KK	Hot-swap backplane (HSBP) connector (P16)
R	BMC Flash component	LL	Secondary HSBP connector (P15)
S	Battery	MM	Jumpers
T	Chassis Intrusion Detect connector (P36)		

Figure 15. Baseboard Connector and Component Locations

9.2 Processor Board Connector and Component Locations

The following figure shows the major features of the processor board identified by lettered callouts.

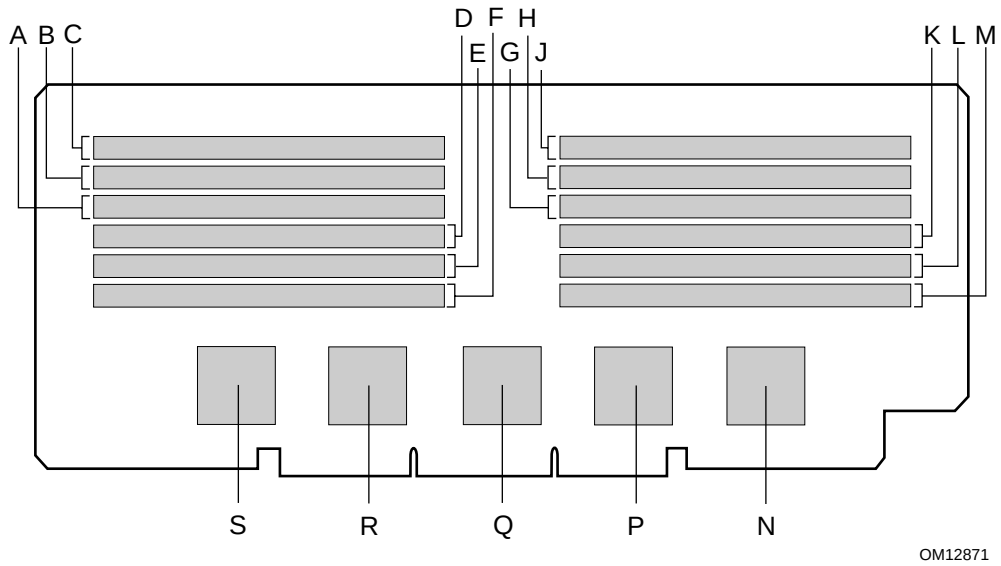


Key	Component	Key	Component
A	Procsesor Slot #3	E	Processor board to Baseboard connector (backside)
B	Procsesor Slot #4	F	Mempry Board Connector
C	Processor Slot #1 (Primary)	G	Processor board to Baseboard connector (backside)
D	CMIC	H	Procesor Slot #2

Figure 16. Processor Board Connector and Component Locations

9.3 Memory Board Connector and Component Locations

The following figure shows the major features of the memory board identified by lettered callouts.



Key	Component	Key	Component
A	DIMM Socket #7	K	DIMM Socket #6
B	DIMM Socket #9	L	DIMM Socket #4
C	DIMM Socket #11	M	DIMM Socket #2
D	DIMM Socket #5	N	REMC DP(3)
E	DIMM Socket #3	P	REMC DP(2)
F	DIMM Socket #1	Q	REMC Address Path
G	DIMM Socket #8	R	REMC DP(1)
H	DIMM Socket #10	S	REMC DP(0)
J	DIMM Socket #12		

Figure 17. Memory Board Connector and Component Locations

9.4 Primary Baseboard Jumpers

The configuration jumpers on the baseboard are shown in Figure 18 and are organized into three groups: boot block jumpers (JP3), main jumpers (JP4, JP5, and JP6), and serial port B jumpers (JP25). Figure 18 identifies the jumper blocks and pin numbers. The function of each pair of pins is described in the sections that follow.

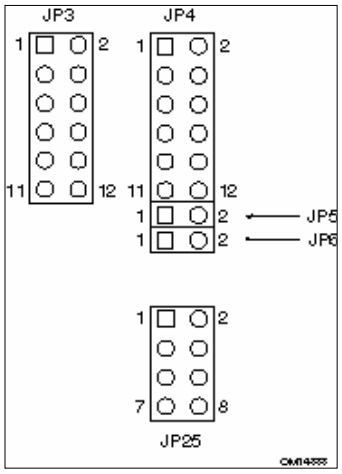


Figure 18. Baseboard Jumpers

9.4.1 Boot Block Jumpers (JP3)

The boot block jumpers are used when updating the BIOS or BMC firmware in the unusual event that the boot block area needs to be updated. These jumpers are not used for routine firmware updates. Use the boot block jumpers only when the instructions with a firmware update specifically say to do so. When you do need to enable either of these features, use one of the spares from JP4 pins 1 and 2 or JP25 pins 7 and 8. Table 23 identifies the function of each pin pair on JP3.

Table 23. Boot Block Jumper Descriptions

Jumper Block	Pins	Jumper Name—Effect when shorted.
JP3	1-2	INTR (Reserved)
	3-4	NMI (Reserved)
	5-6	IGNNE (Reserved)
	7-8	A20M (Reserved)
	9-10	BMC Boot Block Write Enable—Allows the BMC boot block to be overwritten when updating the BMC firmware.
	11-12	BIOS Boot Block Write Enable—Allows the BIOS boot block to be overwritten when updating the BIOS.

9.4.2 Main Jumpers (JP4, JP5, JP6)

Table 24 identifies the function of each pin pair on the main jumper blocks (JP4, JP5, and JP6). The BIOS Recover, Password Clear, and CMOS Clear jumpers are described in more detail elsewhere in this document (see the references in the above table). The FRB-3 Timer Disable jumper and the BMC Force Update jumper are special purpose jumpers that you should use only when instructed to do so by Intel support. When you do need to enable any of these features, use one of the spares from JP4 pins 1 and 2 or JP25 pins 7 and 8.

Table 24. Main Jumper Descriptions

JP4	1-2	Spare.
	3-4	BIOS Recovery—System will attempt to recover the BIOS at the next boot. .
	5-6	Reserved. Inspection Mode 2 (High speed)
	7-8	Reserved. Inspection Mode 1 (ignore voltage observation)
	9-10	Password Clear—User and administrator passwords are cleared at the next boot. For more information, see page 104.
	11-12	CMOS Clear—CMOS settings are cleared at the next boot.
JP5	1-2	FRB3 Timer Disable—Disables fault resilient boot timer 3.
JP6	1-2	BMC Force Update—Lets a system with corrupted BMC firmware boot for an update.

9.4.2.1 Serial Port B Jumpers (JP 25)

Table 25 identifies the function of each pin pair on the serial port B jumper block (JP25). By default, the serial port B connector is an RJ45, which has only eight pins and does not provide separate DCD and DSR signals. The serial port B jumpers let you configure the DSR and DCD signals passed from the port connector to the inputs of the UART. The default configuration has jumpers installed on pins 1 and 2 and on pins 3 and 4.

Note: Never install jumpers on pins 3 and 4 and on pins 5 and 6 at the same time. This would cause both the DCD and DSR signals from the connector to drive the DCD input on the UART, resulting in signal contention.

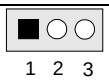
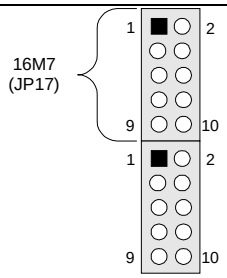
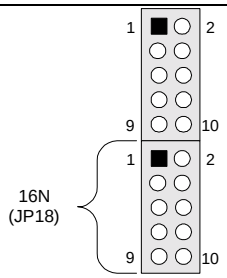
Table 25. Serial Port B Jumper Descriptions

JP25	1-2	DSR to DSR—DSR from connector is passed to DSR input on UART (RJ45 & DB9).
	3-4	DSR to DCD—DSR from connector is passed to DCD input on UART (RJ45 only).
	5-6	DCD to DCD—DCD from connector is passed to DCD input on UART (DB9 only).
	7-8	Spare.

9.5 Extended Baseboard Jumpers

Table 26 identifies additional jumper blocks used on the Server System SSH4 baseboard. These jumper blocks are typically only utilized for board level advanced diagnostics or similar functions.

Table 26. SSH4 Extended Baseboard Jumper Options

Key	Jumper Block and location	Function	Pin Description (Pins shorted = low; pins open = high)
L	14G9 (JP15) 	Expansion BMC Flash memory enable	1-2: short = normal 2-3: short = enable (for debugging)
	16M7 (JP17) 	X-bus debug port	
	16N (JP18) 	X-bus debug port	
	1G	PCI slot 5 & 6 speed (PCIXCAP) –603 baseboard only	1-2: short = 66MHz open = 100MHz
	5H11	PCI slot 7 & 8 speed (PCIXCAP) –603 baseboard only	1-2: short = 66MHz open = 100MHz

10. Connectors

10.1 Connector Locations

Refer to Figure 15. Baseboard Connector and Component Locations, for the location and description of the baseboard connectors.

10.2 ICMB Connector

The external Intelligent Management Bus (ICMB) provides external access to IMB devices within the chassis. This makes it possible to externally access chassis management functions, alert logs, post-mortem data, etc. The connector provides a mechanism for chassis power control. As an option the server can be configured with an ICMB adapter board to provide two SEMCONN 6-pin connectors to allow daisy chained cabling. Additional information about ICMB can be found in the External Intelligent Management Bus Bridge External Program Specification and in the SSH4 Intelligent Chassis Management Board (ICMB) External Product Specification.

Table 27. ICMB Connector Pinout, P24 (D)

Pin	Name
1	XP05S
2	ICMB_TX
3	ICMB_TX_ENB
4	ICMB_RX
5	GND

10.3 HPIB Connector

Table 28 lists the signal names for the hot plug indicator board (HPIB) connector.

Table 28. HPIB Connector Pinout, P23, (E)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V Standby	2	+5 VDC
3	GND	4	GND
5	No connect	6	No connect
7	No connect	8	No connect
9	SLT31SW-00	10	SLT32SW-00
11	SLT41SW-00	12	SLT42SW-00
13	No connect	14	No connect
15	No connect	16	No connect
17	ATTEN210-10	18	ATTEN211-10
19	ATTEN220-10	20	ATTEN221-10
21	ATTEN310-10	22	ATTEN311-10
23	ATTEN320-10	24	ATTEN321-10
25	ATTEN410-10	26	ATTEN411-10
27	ATTEN420-10	28	ATTEN421-10

10.4 Processor Board Connectors, P21, P22 (F)

Table 29 and Table 30 list the pins of the processor board connectors and the signal names that appear on the Server System SSH4 baseboard schematic diagram. Processor Board Connector A (P21) is the 144-pin (24 x 6) connector adjacent to PCI slot 1. Processor Board Connector B (P22) is the 144-pin (24 x 6) connector located near the IDE and floppy drive connectors.

Table 29. Processor Board Connector A Pinout, P21

Pin	Signal	Pin	Signal	Pin	Signal
A1	T_IMB_CLK_T	B1	T_IMB_CON_T	C1	GND
A2	T_IMB_PAR_T	B2	T_IMB_D_T<3>	C2	REMC_ALERTN
A3	GND	B3	GND	C3	ISOLATE_N
A4	T_IMB_D_T<1>	B4	T_IMB_D_T<2>	C4	GND
A5	T_IMB_CON_R	B5	T_IMB_D_T<0>	C5	No connect
A6	GND	B6	T_IMB_CLK_R	C6	No connect
A7	T_IMB_PAR_R	B7	GND	C7	GND
A8	T_IMB_D_R<1>	B8	T_IMB_D_R<3>	C8	RESETDLYN
A9	T_IMB_D_R<0>	B9	T_IMB_D_R<2>	C9	CMIC_ALERTN
A10	GND	B10	GND	C10	GND
A11	PCIRST_MEM	B11	SM3_DATA+20	C11	DPLLRST+10
A12	DBRSTL	B12	CMIC_PCIRST-0	C12	RSB_FERRN
A13	PWROK+00	B13	GND	C13	GND
A14	GND	B14	LA20ML_T	C14	IGNNEL_T
A15	MEMOFF-0	B15	LNMI_T	C15	INITN
A16	LINTR_T	B16	GND	C16	GND
A17	GND	B17	STPCLK-0	C17	CPU_SEL1
A18	CPU_PROCHOTIN	B18	CPU_SEL0	C18	GND
A19	CPU_IERRIN	B19	+3.3 VDC	C19	+3.3 VDC
A20	GND	B20	No connect	C20	+5 VDC
A21	+12 VDC	B21	+12 VDC	C21	+12 VDC
A22	+12 VDC	B22	+12 VDC	C22	+12 VDC
A23	+12 VDC	B23	+12 VDC	C23	+12 VDC
A24	+12 VDC	B24	+12 VDC	C24	+12 VDC
D1	GND	E1	HCLK_MEM2_N	F1	SM3_CLK+201
D2	GND	E2	HCLK_MEM2_P	F2	CMIC_FATALN
D3	GND	E3	GND	F3	GND
D4	GND	E4	HCLK_CPU3_N	F4	HCLK_CPU4_N
D5	GND	E5	HCLK_CPU3_P	F5	HCLK_CPU4_P
D6	GND	E6	GND	F6	GND
D7	GND	E7	HCLK_CPU1_N	F7	HCLK_CPU2_N
D8	GND	E8	HCLK_CPU1_P	F8	HCLK_CPU2_P
D9	+12 VDC	E9	GND	F9	VDD_CMIC
D10	+12 VDC	E10	+12 VDC	F10	+12 VDC
D11	+12 VDC	E11	+12 VDC	F11	+12 VDC

D12	SMS_CLK+00	E12	+12 VDC	F12	+12 VDC
D13	SMS_DATA+00	E13	CPU_SMALERTN	F13	+12 VDC
D14	RSB_SLPN	E14	GND	F14	+5 V STANDBY
D15	GND	E15	SMI1-0	F15	SMI4-0
D16	CPU_THERMTRIP1N	E16	SMI2-0	F16	VCCP
D17	GND	E17	SMI3-0	F17	+3.3 V STANDBY
D18	+3.3 VDC	E18	GND	F18	+3.3 VDC
D19	+3.3 VDC	E19	+3.3 VDC	F19	+3.3 VDC
D20	+5 VDC	E20	+5 VDC	F20	+5 VDC
D21	+12 VDC	E21	+12 VDC	F21	+12 VDC
D22	+12 VDC	E22	+12 VDC	F22	+12 VDC
D23	+12 VDC	E23	+12 VDC	F23	+12 VDC
D24	+12 VDC	E24	+12 VDC	F24	+12 VDC

Table 30. Processor Board Connector B Pinout, P22

Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	B1	A_IMB_D_R+10<0>	C1	A_IMB_D_R+10<1>
A2	A_IMB_D_R+10<2>	B2	A_IMB_D_R+10<3>	C2	GND
A3	A_IMB_D_R+10<4>	B3	GND	C3	A_IMB_D_R+10<5>
A4	GND	B4	A_IMB_D_R+10<6>	C4	A_IMB_D_R+10<8>
A5	A_IMB_D_R+10<10>	B5	A_IMB_D_R+10<7>	C5	GND
A6	A_IMB_D_R+10<9>	B6	GND	C6	A_IMB_D_R+10<11>
A7	GND	B7	A_IMB_D_R+10<14>	C7	A_IMB_D_R+10<12>
A8	A_IMB_D_R+10<13>	B8	A_IMB_D_R+10<15>	C8	GND
A9	A_IMB_CON_R+10	B9	GND	C9	A_IMB_PAR_R+10
A10	GND	B10	A_IMB_CLK_R+10	C10	A_IMB_D_T<1>
A11	A_IMB_D_T_<0>	B11	A_IMB_D_T_<3>	C11	GND
A12	A_IMB_D_T_<2>	B12	GND	C12	A_IMB_D_T<5>
A13	GND	B13	A_IMB_D_T_<4>	C13	A_IMB_D_T<7>
A14	A_IMB_D_T_<6>	B14	A_IMB_D_T_<8>	C14	GND
A15	A_IMB_D_T_<9>	B15	GND	C15	A_IMB_D_T<10>
A16	GND	B16	A_IMB_D_T_<11>	C16	A_IMB_D_T<12>
A17	A_IMB_CLK_T	B17	A_IMB_D_T_<14>	C17	GND
A18	A_IMB_D_T_<13>	B18	GND	C18	A_IMB_D_T<15>
A19	GND	B19	HCLK_CMIC_P	C19	A_IMB_PAR_T
A20	HCLK_ITP_P	B20	HCLK_CMIC_N	C20	A_IMB_CON_T
A21	HCLK_ITP_N	B21	GND	C21	+12 VDC
A22	+12 VDC	B22	+12 VDC	C22	+12 VDC
A23	+12 VDC	B23	+12 VDC	C23	+12 VDC
A24	+12 VDC	B24	+12 VDC	C24	+12 VDC
D1	GND	E1	B_IMB_D_R+10<9>	F1	HCLK_MEM1_P
D2	B_IMB_D_R+10<0>	E2	B_IMB_D_R+10<3>	F2	HCLK_MEM1_N
D3	B_IMB_D_R+10<1>	E3	GND	F3	GND
D4	GND	E4	B_IMB_D_R+10<4>	F4	B_IMB_D_R+10<2>
D5	B_IMB_D_R+10<5>	E5	B_IMB_D_R+10<6>	F5	GND

Pin	Signal	Pin	Signal	Pin	Signal
D6	B_IMB_D_R+10<8>	E6	GND	F6	B_IMB_D_R+10<7>
D7	GND	E7	B_IMB_CLK_R+10	F7	B_IMB_D_R+10<10>
D8	B_IMB_D_R+10<11>	E8	B_IMB_D_R+10<12>	F8	GND
D9	B_IMB_D_R+10<14>	E9	GND	F9	B_IMB_D_R+10<13>
D10	GND	E10	B_IMB_PAR_R+10	F10	B_IMB_D_R+10<15>
D11	B_IMB_D_T<8>	E11	B_IMB_CON_R+10	F11	GND
D12	B_IMB_D_T<7>	E12	GND	F12	B_IMB_D_T<9>
D13	GND	E13	B_IMB_D_T<1>	F13	B_IMB_D_T<0>
D14	B_IMB_D_T<4>	E14	B_IMB_D_T<2>	F14	GND
D15	B_IMB_D_T<6>	E15	GND	F15	B_IMB_D_T<3>
D16	GND	E16	B_IMB_D_T<10>	F16	B_IMB_D_T<5>
D17	B_IMB_D_T<12>	E17	B_IMB_D_T<11>	F17	GND
D18	B_IMB_D_T<14>	E18	GND	F18	B_IMB_D_T<13>
D19	GND	E19	B_IMB_CON_T	F19	B_IMB_PAR_T
D20	B_IMB_CLK_T	E20	B_IMB_D_T<15>	F20	+12 VDC
D21	+12 VDC	E21	+12 VDC	F21	+12 VDC
D22	+12 VDC	E22	+12 VDC	F22	+12 VDC
D23	+12 VDC	E23	+12 VDC	F23	+12 VDC
D24	+12 VDC	E24	+12 VDC	F24	+12 VDC

10.5 Front Panel Interface, P19, (J)

A 34-pin header is provided that attaches to the system front panel. The header contains reset, NMI, sleep, and power control buttons, and LED indicators. Table 31 summarizes the front panel signal pins, including the pin number, signal mnemonic, and a brief description.

Table 31. Front Panel Header Pinout, P19 (J)

Pin	Signal Name	Description
1	VP50 (VCC)	Power LED Anode (VDC)
2	Key	Pulled Pin – No Connect
3	FP_PWR_LED-10	Power LED Cathode (Low True)
4	VP50	HDD Activity LED Anode
5	HDD_LED-10	HDD Activity LED Cathode (Low True)
6	FP_POWERSW-00	Power Switch (Low True)
7	GND	Power Switch Ground
8	FP_RESETSW-00	Reset Switch (Low True)
9	GND	Reset Switch Ground
10	FP_SLEEPSW-00	ACPI Sleep Switch (Low True)
11	GND	ACPI Sleep Switch Ground
12	FP_DUMPSW-00	NMI to CPU Switch (Low True)
13	Key	Pulled Pin – No Connect
14	XP055	ID LED Anode (VDC)
15	IDLED-10	ID LED Cathode (Low True)
16	FP_IDSW-10	ID Switch (Low True)

Pin	Signal Name	Description
17	GND	ID Switch (GROUND)
18	XP055	+5V Standby
19	XP055	Fan Fail LED Anode (VDC)
20	FP_COOL_FLT_LED-10	Fan Fail LED Cathode (Low True)
21	XP055	Power Fault LED Anode (VDC)
22	FP_SYS_FLT_LED-10	Power Fault LED Cathode (Low True)
23	LAN1_ACTIVE_LED-FP	
24	LAN1_LINK_LED-FP	NIC #1 Activity LED Anode (VDC)
25	IPMB_DATA+10/+00	
26	IPMB_CLK+10/+00	
27	SIDE_CI / FP_CI	Side and Front Panel Chassis Intrusion
28	LAN1_ACTIVE_LED-FP	
29	LAN2_LINK_LED-FP	NIC #2 Activity LED Anode (VDC)
30	Key	Pulled Pin – No Connect
31	STATUS_LED_ANODE	
32	SYSRDY_LED-10	System Ready Cathode
33	VP50 (VCC)	HDD Fault Anode
34	HDD_FAULT_LED-10	HDD Fault Cathode

10.6 USB #3 Header

Table 32 lists the signal names of the USB #3 header.

Table 32. USB #3 Header, P18 (H)

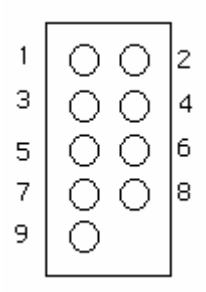
Pin	Name	Pin	Name
1	No connect	2	USBP2_VCC
3	No connect	4	USB_P2_N
5	No connect	6	USB_P2_P
7	No connect	8	USBP2_GND
9	Key (No pin)	10	GND

10.7 Serial Port B Header

Serial Port B can be used either as an emergency management port or as a normal serial port. As an emergency management port, Serial Port B is used as a communication path by the Server Management RS-232 connection to the Baseboard Management Controller. This provides a level of emergency management through an external modem. The RS-232 connection can be monitored by the BMC when the system is in a powered down (standby) state.

Table 33 lists the signals present on the Serial Port B header. If both DCD and DSR signals are required, leave jumper plugs on JP9 and JP10 jumper blocks (default). Refer to Table 26 for more information on these jumpers.

Table 33. Serial Port B Header, P17 (J)

Pin	Signal	Serial Port B Header
1	SIODCD + 00_2 (carrier detect)	
2	SIODSR + 00_2 (data set ready)	
3	SIORXD - 00_2 (receive data)	
4	SIORTS + 00_2 (request to send)	
5	SIOTXD - 00_2 (transmit data)	
6	SIOCTS + 00_2 (clear to send)	
7	SIODTR + 00_2 (data terminal ready)	
8	SIORI + 00_2 (ring indicator)	
9	GROUND	
10	KEY	

10.8 IPMB Connector

The baseboard provides a 3-pin auxiliary I^2C connector for OEM access to the IPMB. This connector is not isolated when power is off. Any devices connected must remain powered in this state or the BMC will not work properly.

Caution: A shorted I^2C connection at the auxiliary I^2C connector will prevent restoration of main power because the BMC needs the bus to boot the server from standby power.

Table 34. IPMB Connector Pinout, P12 (K)

Pin	Name
1	IPMB_DATA+10
2	GND
3	IPMB_CLK+10

10.9 Fan Connector

The Server System SSH4 baseboard provides a connector for eight fans. Each fan can be equipped with a sensor that indicates if the fan is operating. Four fan connectors are for processor cooling fans, two fan connectors are for front PCI boards and the remaining two connectors on the baseboard attach to chassis fans equipped with a sensor that indicates whether the fan is operating. The chassis fans can also be turned on and off from the Baseboard Management Controller. The sensor pins for all of these fans are routed to the BMC for failure monitoring

Table 35. Fan Connector, P11 (L)

Pin	Signal Name	Pin	Signal Name
1	FAN_CNCT1	2	FAN_CNCT2
3	FANLED4+0	4	FANLED8+0
5	FSPEED4+0	6	FSPEED8+0
7	FAN4_SENSE+0	8	FAN8_SENSE+0
9	GND	10	GND
11	FANLED3+0	12	FANLED7+0
13	FSPEED3+0	14	FSPEED7+0
15	FAN3_SENSE+0	16	FAN7_SENSE+0
17	GND	18	CABR-20
19	FANLED2+0	20	FANLED6+0
21	FSPEED2+0	22	FSPEED6+0
23	FAN2_SENSE+0	24	FAN6_SENSE+0
25	GND	26	GND
27	FANLED1+0	28	FANLED5+0
29	FSPEED1+0	30	FSPEED5+0
31	FAN1_SENSE+0	32	FAN5_SENSE+0
33	GND	34	+5 VDC

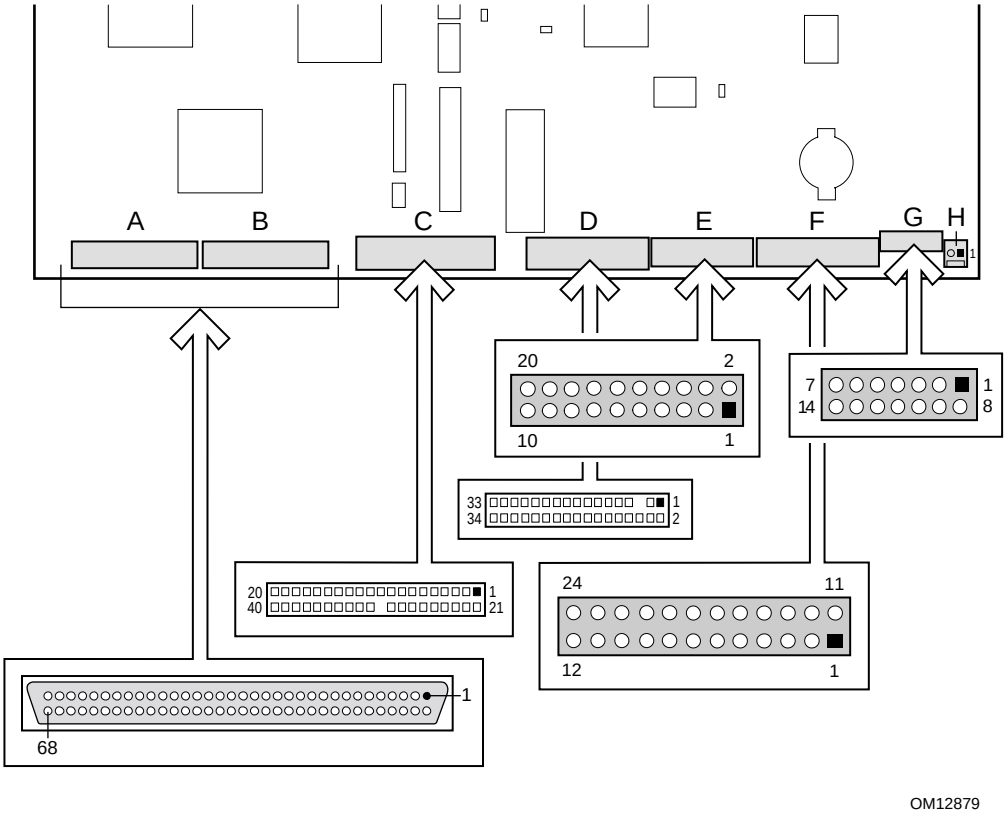
10.10 RAID LED Connector

Table 36. RAID LED Connectors, P1 and P2 (M)

Pin	Name
1	No connect
2	+5 VDC
3	+5 VDC
4	No connect

10.11 Power Distribution Board Interface Connectors (P10/11/29)

The following figure identifies the front edge connectors with key letters.



Key	Connector	Key	Connector
A	SCSI channel A LVD connector (P4)	E	20-pin power connector (P28)
B	SCSI channel B LVD connector (P7)	F	24-pin power connector (P32)
C	IDE connector (P13)	G	14-pin power control connector (P35)
D	Legacy Floppy connector (P23)	H	Chassis intrusion connector (P36)

Figure 19. Baseboard Front Edge Connectors

10.12 SCSI Connectors

The baseboard provides two SCSI connectors. The two connectors have the same pin-out. Table 37 details the pin-out of the SCSI connectors.

Table 37. 68-pin SCSI Connector Pin-out, P4, P7 (A)

Connector Contact Number	Signal Name	Signal Name	Connector Contact Number
1	+DB(12)	-DB(12)	35
2	+DB(13)	-DB(13)	36
3	+DB(14)	-DB(14)	37
4	+DB(15)	-DB(15)	38
5	+DB(P1)	-DB(P1)	39
6	+DB(0)	-DB(0)	40
7	+DB(1)	-DB(1)	41
8	+DB(2)	-DB(2)	42
9	+DB(3)	-DB(3)	43
10	+DB(4)	-DB(4)	44
11	+DB(5)	-DB(5)	45
12	+DB(6)	-DB(6)	46
13	+DB(7)	-DB(7)	47
14	+DB(P)	-DB(P)	48
15	GROUND	GROUND	49
16	GROUND	GROUND	50
17	RESERVED	RESERVED	51
18	RESERVED	RESERVED	52
19	RESERVED	RESERVED	53
20	GROUND	GROUND	54
21	+ATN	-ATN	55
22	GROUND	GROUND	56
23	+BSY	-BSY	57
24	+ACK	-ACK	58
25	+RST	-RST	59
26	+MSG	-MSG	60
27	+SEL	-SEL	61
28	+C/D	-C/D	62
29	+REQ	-REQ	63
30	+I/O	-I/O	64
31	+DB(8)	-DB(8)	65
32	+DB(9)	-DB(9)	66
33	+DB(10)	-DB(10)	67
34	+DB(11)	-DB(11)	68

10.13 IDE Connector, P13 (B)

Table 38 lists the pinout and signal names for the IDE connector.

Table 38. IDE 40-pin Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DDRQ0 (DDRQ1)	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Vcc pull-down
29	DDACK0 (DDACK1)#	30	Ground
31	IRQ14 (IRQ15)	32	Reserved
33	DAG1	34	Reserved
35	DAG0	36	DAG2
37	Chip Select 1P (1S)#	38	Chip Select 3P (3S)#
39	Activity#	40	Ground

10.14 Floppy Connector, P25 (C)

Table 39 details the pin-out of the Legacy 34-pin floppy connector.

Table 39. Legacy 34-pin Floppy Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index#
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	MSEN1	18	DIR#
19	Ground	20	STEP#

Pin	Signal Name	Pin	Signal Name
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	MSEN0	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

10.15 Power Connectors

The baseboard, processor board, and memory board receive their main power through two primary and one auxiliary power connector. The two main power connectors are identified as P32 and P28. The auxiliary power connector, identified as P35, provides server management communication with the power supply. Table 40 describes the 24-pin power connector.

Pin	Signal	Pin	Signal
1	+12 VDC	11	+5 VSB
2	GND	12	GND
3	GND	13	GND
4	GND	14	GND
5	GND	15	GND
6	+5 VDC	16	+5 VDC
7	+5 VDC	17	+5 VDC
8	+5 VDC	18	+5 VDC
9	+5 VDC	19	+5 VDC
10	+5 VDC	20	+5 VDC

Table 41 describes the 20-pin power connector. Table 42 describes the 14-pin power control connector.

Table 40. 20-Pin Power Connector, P28 (E)

Pin	Signal	Pin	Signal
1	+12 VDC	11	+5 VSB
2	GND	12	GND
3	GND	13	GND
4	GND	14	GND
5	GND	15	GND
6	+5 VDC	16	+5 VDC
7	+5 VDC	17	+5 VDC
8	+5 VDC	18	+5 VDC
9	+5 VDC	19	+5 VDC
10	+5 VDC	20	+5 VDC

Table 41. 24-Pin Power Connector, P32 (F)

Pin	Signal	Pin	Signal
1	+3.3 VDC	13	+3.3 VDC
2	+3.3 VDC	14	+3.3 VDC
3	+3.3 VDC	15	+3.3 VDC
4	GND	16	GND
5	GND	17	GND
6	GND	18	GND
7	GND	19	GND
8	GND	20	GND
9	+12 VDC	21	+12 VDC
10	+12 VDC	22	+12 VDC
11	+12 VDC	23	+12 VDC
12	+12 VDC	24	+12 VDC

Table 42. 14-Pin Power Control Connector P35 (G)

Pin	Signal	Pin	Signal
1	GND	8	+5VRS
2	+3.3VRS	9	Fan Speed Input*
3	I2C-SCL	10	I2C-SDA
4	GND	11	PS-GOOD
5	PS-ON	12	GND
6	-12V	13	No connection
7	+12VRS	14	Remote Sense Return

10.16 Chassis Intrusion Connector

Table 43 Describes the chassis intrusion connector.

Table 43. Chassis Intrusion Connector, P36 (H)

Pin	Signal
1	SIDE_CI
2	GND

10.17 Memory Board Riser Connector, P12 (P)

Table 44 lists the pins of the memory riser board connector and the signal name that appears on the Server System SSH4 baseboard schematic diagram.

Table 44. Memory Board Connector Pinout, P12 (6D)

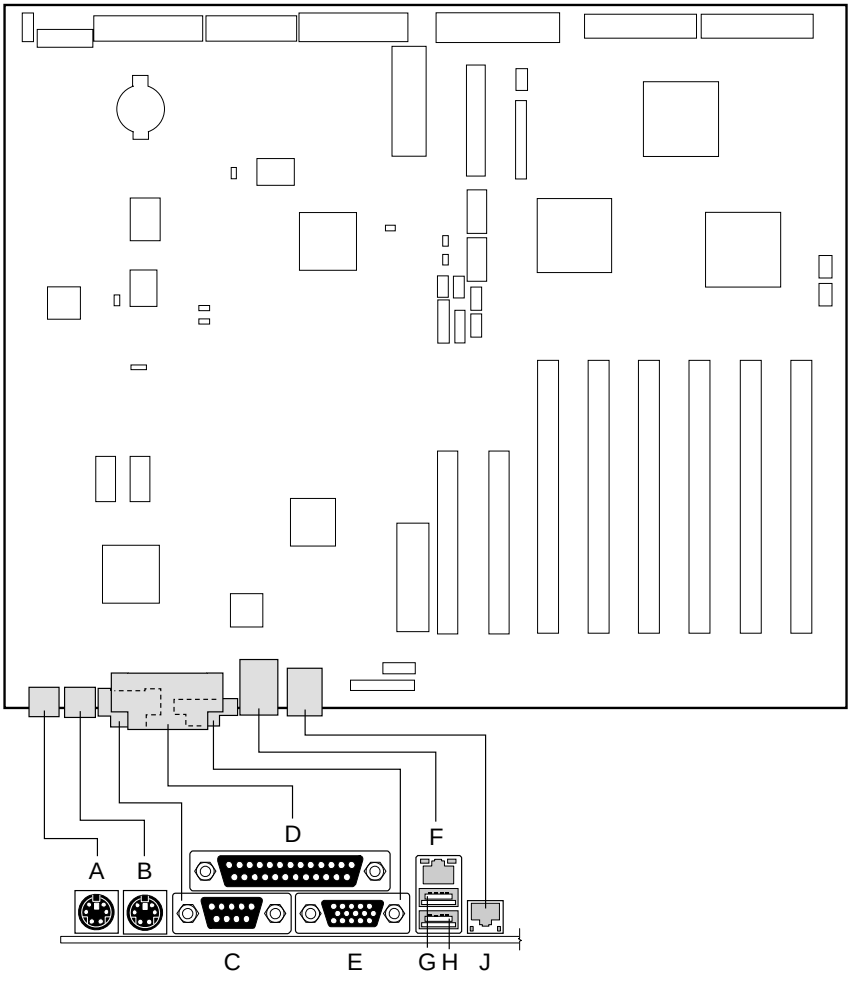
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A001	XP05S	B001	DPLLRST+10	A084	GND	B084	MA9
A002	ISOLATE_N	B002	GND	A085	MA6	B085	GND
A003	REMC_ALERTN	B003	HCLK_MEM1_N	A086	MA4	B086	MA12
A004	GND	B004	HCLK_MEM1_P	A087	GND	B087	MA7
A005	No Connect	B005	GND	A088	MA8	B088	GND
A006	CMD99	B006	CMD101	A089	MA0	B089	MA11
A007	GND	B007	CMD100	A090	GND	B090	MA2
A008	CMD98	B008	GND	A091	MA3	B091	GND
A009	CMD96	B009	CMD102	A092	CMD60	B092	MA1
A010	GND	B010	CMD97	A093	GND	B093	CMD63
A011	CSTRB6	B011	GND	A094	CMD62	B094	GND
A012	MECC0	B012	CMD103	A095	CMD56	B095	CMD57
A013	GND	B013	MECC6	A096	GND	B096	CMD61
A014	MECC7	B014	GND	A097	CMD59	B097	GND
A015	MECC5	B015	MECC4	A098	CMD50	B098	CMD58
A016	GND	B016	MECC3	A099	GND	B099	CSTRB3
A017	MECC2	B017	GND	A100	CMD53	B100	GND
A018	CMD117	B018	MECC1	A101	CMD55	B101	CMD52
A019	GND	B019	MSTRB0	A102	GND	B102	CMD54
A020	CMD116	B020	GND	A103	CMD49	B103	GND
A021	CMD118	B021	CMD113	A104	CSTRB2	B104	CMD46
A022	GND	B022	CMD115	A105	GND	B105	CMD51
A023	CMD114	B023	GND	A106	CMD47	B106	GND
A024	CMD106	B024	CMD119	A107	CMD44	B107	CMD42
A025	GND	B025	CMD112	A108	GND	B108	CMD46
A026	CMD105	B026	GND	A109	CMD41	B109	GND
A027	CMD104	B027	CMD108	A110	CMD45	B110	CMD40
A028	GND	B028	CMD111	A111	GND	B111	CMD43
A029	CMD107	B029	GND	A112	CMD32	B112	GND
A030	CMD127	B030	CMD109	A113	CMD33	B113	CMD39
A031	GND	B031	CMD110	A114	GND	B114	CMD38
A032	CMD121	B032	GND	A115	CMD37	B115	GND
A033	CMD122	B033	CMD126	A116	CMD34	B116	CMD36
A034	GND	B034	CMD123	A117	GND	B117	CMD35
A035	CMD120	B035	GND	A118	MECC13	B118	GND
A036	CSTRB7	B036	CMD125	A119	GND	B119	B_RCMD3
A037	GND	B037	CMD124	A120	MECC10	B120	GND
A038	CMD94	B038	GND	A121	MECC8	B121	MECC12

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A039	CMD89	B039	MSTRB1	A122	GND	B122	MECC14
A040	GND	B040	CMD91	A123	MECC15	B123	GND
A041	CMD95	B041	GND	A124	MSTRB3	B124	MECC9
A042	CMD90	B042	CMD88	A125	GND	B125	MECC11
A043	GND	B043	CMD93	A126	CMD28	B126	GND
A044	CMD87	B044	GND	A127	CMD30	B127	MSTRB2
A045	CMD82	B045	CMD92	A128	GND	B128	CMD26
A046	GND	B046	CMD83	A129	CMD25	B129	GND
A047	CMD81	B047	GND	A130	CMD27	B130	CMD24
A048	CMD85	B048	CMD84	A131	GND	B131	CMD31
A049	GND	B049	CMD86	A132	CSTRB1	B132	GND
A050	CSTRB5	B050	GND	A133	CMD18	B133	CMD29
A051	CMD74	B051	CMD80	A134	GND	B134	CMD21
A052	GND	B052	CMD73	A135	CMD17	B135	GND
A053	CMD76	B053	GND	A136	CMD19	B136	CMD16
A054	CMD78	B054	CMD79	A137	GND	B137	CMD22
A055	GND	B055	CMD75	A138	CMD23	B138	GND
A056	CMD77	B056	GND	A139	CMD14	B139	CMD20
A057	GND	B057	CMD72	A140	GND	B140	CMD13
A058	CMD69	B058	GND	A141	CMD11	B141	GND
A059	CMD66	B059	CSTRB4	A142	CMD8	B142	CMD15
A060	GND	B060	CMD67	A143	GND	B143	CMD12
A061	CMD65	B061	GND	A144	CMD9	B144	GND
A062	CMD71	B062	CMD68	A145	CMD0	B145	CMD10
A063	GND	B063	CMD64	A146	GND	B146	CMD1
A064	A_CKE	B064	GND	A147	CMD6	B147	GND
A065	A_CASN	B065	CMD70	A148	CMD7	B148	CMD2
A066	GND	B066	A_WEN	A149	GND	B149	CMD3
A067	A_RASN	B067	GND	A150	CMD4	B150	GND
A068	B_RCMD1	B068	BSDOEN	A151	GND	B151	CMD5
A069	GND	B069	A_RCMD0	A152	SM2_DATA+20	B152	CSTRB0
A070	B_RCMD2	B070	GND	A153	SM2_CLK+20	B153	GND
A071	A_RCMD2	B071	ASDOEN	A154	GND	B154	No Connect
A072	GND	B072	A_RCMD3	A155	No Connect	B155	No Connect
A073	B_RCMD0	B073	GND	A156	VP33 (+3.3V)	B156	GND
A074	AECSB2	B074	A_RCMD1	A157	IDLED-10	B157	No Connect
A075	GND	B075	AECSA2	A158	PCIRST-30	B158	VP50 (+5.0V)
A076	AECSB0	B076	GND	A159	No Connect	B159	No Connect
A077	AECSB1	B077	AECSA1	A320	XP12 (+12V_IO)	B320	XP12 (+12V_IO)
A078	GND	B078	AECSA0	A161	XP12 (+12V_IO)	B161	XP12 (+12V_IO)
A079	MA15	B079	GND	A162	XP12 (+12V_IO)	B162	XP12 (+12V_IO)
A080	MA5	B080	MEMPARN	A163	XP12 (+12V_IO)	B163	XP12 (+12V_IO)
A081	GND	B081	MA16	A164	XP12 (+12V_IO)	B164	XP12 (+12V_IO)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A082	MA10	B082	GND	A165	XP12 (+12V_IO)	B165	XP12 (+12V_IO)
A083	MA13	B083	MA14				

10.18 Back Panel Connectors

Figure 20 shows a graphical representation with identification of the physical connections at the I/O panel (also referred to as the back panel).



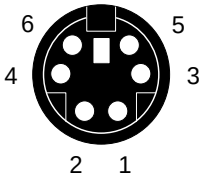
Key	Connector	Key	Connector
A	Keyboard (Mouse) connector	F	LAN1 connector
B	Mouse (Keyboard) connector	G	USB connector, port A
C	Serial port A connector	H	USB connector, port B
D	Parallel Port connector	J	LAN2 connector
E	VGA Video connector		

Figure 20. Back Panel I/O Connector Graphical Locations

10.18.1 Keyboard and Mouse Ports

Table 45 lists the signal names of the PS/2 keyboard and mouse ports.

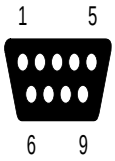
Table 45. Keyboard and Mouse Ports (A, B)

Mouse			Keyboard / Mouse Connector	Keyboard		
Pin	Signal	Description		Pin	Signal	Description
1	MSDATA	Mouse Data		1	KBDATA	Keyboard Data
2	GND	Ground		2	GND	Ground
3	GND	Ground		3	GND	Ground
4	MSFUSE	+5V		4	KBFUSE	+5V
5	MSCLK	Mouse clock		5	KBCLK	Keyboard clock
6	GND	Ground		6	GND	Ground

10.18.2 Serial Ports

The Server System SSH4 board provides one RS-232C serial port and a second serial port available through an onboard header. The back panel serial port is a D-subminiature 9-pin connector. Refer to page 75 for information on the Serial Port B connector.

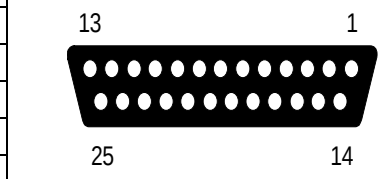
Table 46. Serial Port A Connector (C)

Pin	Signal	Serial Port A Connector
1	SIODCD + 00_1 (carrier detect)	
2	SIORXD – 00_1 (receive data)	
3	SIOTXD – 00_1 (transmit data)	
4	SIODTR + 00_1 (data terminal ready)	
5	GROUND	
6	SIODSR + 00_1 (data set ready)	
7	SIORTS + 00_1 (request to send)	
8	SIOCTS + 00_1 (clear to send)	
9	SIORI + 00_1 (ring indicator)	

10.18.3 Parallel Port Connector

The IEEE 1284-compatible parallel port, used primarily for a printer, sends data in parallel format. The parallel port is accessed through a D-subminiature 25-pin connector.

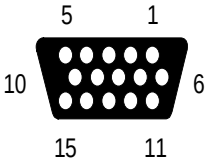
Table 47. Parallel Port Connector

Pin	Signal	Parallel Port Connector	Pin	Signal
1	STROBE_L		14	AUFDXT_L (auto feed)
2	Data bit 0		15	ERROR_L
3	Data bit 1		16	INIT_L (initialize printer)
4	Data bit 2		17	SLCTIN_L (select input)
5	Data bit 3		18	GND (ground)
6	Data bit 4		19	GND
7	Data bit 5		20	GND
8	Data bit 6		21	GND
9	Data bit 7		22	GND
10	ACK_L (acknowledge)		23	GND
11	BUSY		24	GND
12	PE (paper end)		25	GND
13	SLCT (select)			

10.18.4 Video Port

The video port interface is a standard VGA compatible 15-pin connector. Onboard video is supplied by an ATI RAGE XL video controller with 4 MB of onboard video SGRAM.

Table 48. Video Connector

Pin	Signal	Video Connector	Pin	Signal
1	GRED+10 (analog color signal R)		9	5 V
2	GGREEN+10 (analog color signal G)		10	GND
3	GBLUE+10 (analog color signal B)		11	No connection
4	No connection		12	SDA –10
5	GND		13	GHSYNC+10 (horizontal sync)
6	GND		14	GVSYNC+10 (vertical sync)
7	GND		15	SCL –10
8	GND			

10.18.5 Universal Serial Bus (USB) Interface

The baseboard provides two stacked USB ports (Port 0 on top, Port 1 on the bottom). The built-in USB ports permit the direct connection of three USB peripherals without an external hub. A third USB port is available through an on-board header (P18 near grid location 8J). If more devices are required, an external hub can be connected to either the back panel ports or the onboard header.

Table 49. Dual USB Connector

Pin	Signal
A1	Fused VCC (+5V /w over current monitor of both port 0 and 1)
A2	DATAL0 (Differential data line paired with DATAH0)
A3	DATAH0 (Differential data line paired with DATAL0)
A4	GND
B1	Fused VCC (+5V /w over current monitor of both port 0 and 1)
B2	DATAL1 (Differential data line paired with DATAH1)
B3	DATAH1 (Differential data line paired with DATAL1)
B4	GROUND

10.18.6 Ethernet Connectors

The system supports two 10/100 Mbps TX based on board Ethernet connectors. These Ethernet connectors are each single RJ-45 connectors with activity LEDs and integrated magnetics.

Table 50. LAN1 Connector

Pin	Signal
1	GND
2	TX+
3	TX-
4	RX+
5	RX-
6	GND
7	LAN1_SPEED_LED
8	+3.3V standby (for LED)
9	LAN1_LINK_LED
10	LAN1_ACTIVE_LED

Table 51. LAN2 Connector

Pin	Signal
1	TR0+00
2	TR0-00
3	TR1+00
4	TR1-00
5	GBVCC25
6	GBVCC25
7	TR2+00
8	TR2-00
9	TR3+00
10	TR3-00

The 82550PM drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, a valid link to the LAN, and 10- or 100-Mbps operation. The green LED indicates network connection when on and TX/RX activity when blinking. The yellow LED indicates 100-Mbps operation when lit.

The 82544PM drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, a valid link to the LAN, and 10- or 100-Mbps operation. The green LED indicates network connection when on and TX/RX activity when blinking. The yellow LED indicates 100-Mbps operation when lit.

10.19 Connector Manufacturers and Part Numbers

The following table shows the quantity and manufacturers' part numbers for connectors on the baseboard. Item numbers reference the circled numbers on the mechanical drawing. Refer to manufacturers' documentation for more information on connector mechanical specifications.

Table 52. Baseboard Connector Manufacturer Part Numbers

Interface Definition	Description / Manufacture	Item Number	Qty	Unit of Measure
SSI Main Power	CONN, HDR, 2 X 12, PLG, VT, 0.165, 093ST, KP P		1	1.0000 EA
	Molex Connector Corporation	0442060001		
	Foxconn Electronics, Inc.	HM91120-P2		
P2 +12V Power	CONN, HDR, 2 X 4, PLG, VT, 0.165, 093ST, KP PG		1	1.0000 EA
	Molex Connector Corporation	39-29-9082		
	Tyco Electronics Corporation	794305-1		
	Foxconn Electronics, Inc.	HM25040-P2		
P3 Signal Connector	Molex Connector Corporation	70541-0004		
VESA Video	CONN, I/O, 15P, DSUB, RA, 0.05, 062ST, SHIELDE		1	1.0000 EA
	Foxconn Electronics, Inc.	DZ11A36-R9		

Interface Definition	Description / Manufacture	Item Number	Qty	Unit of Measure
Serial #1 Comm	CONN, I/O, 9P, DSUB, RA, .109, 062ST		1	1.0000 EA
	Foxconn Electronics, Inc.	DT10126-R9		
Parallel Comm	CONN, I/O, 25P, DSUB, RA, .109, 093ST		1	1.0000 EA
	Foxconn Electronics, Inc.	DM11356-R1		
NIC #1 with integrated Activity LED"	CONN, I/O, 16P, RJ45/USB, RA, 0.1, 062ST		1	2.0000 EA
	Tyco Electronics Corporation	1116151-2		
Stacked Keyboard and Mouse	CONN, I/O, 12P, DIN, RA, 0.1, 093ST		1	1.0000 EA
	Tyco Electronics Corporation	84405-1		
	Foxconn Electronics, Inc.	MH11067-D5		
PCI 1 and PCI 2	CONN, CEDG, 120P, PCI, VT, 0.05, 093ST		1	2.0000 EA
	Foxconn Electronics, Inc.	EH06011-PC-W		
	Foxconn Electronics, Inc.	EH06013-GC-W		
PCI 3 and PCI 4	CONN, CEDG, 184P, PCI, VT, 0.05, 062ST		1	2.0000 EA
	Tyco Electronics Corporation	145169-4		
	Foxconn Electronics, Inc.	EH09211-R4-W		
PCI 5 and PCI 6	CONN, CEDG, 184P, PCI, VT, 0.05, 062ST		1	2.0000 EA
	Tyco Electronics Corporation	145168-4		
	Foxconn Electronics, Inc.	EH09211-R3-W		
Memory Riser	CONN, CEDG, 330P, SLOT2, VT, 0.03, 062ST		1	1.0000 EA
	Molex Connector Corporation	0711095005		
	Foxconn Electronics, Inc.	PC33013-20		
Serial #2 Comm Header	CONN, HDR, 2 X 5, PLG, VT, 0.1, 062ST, KP 10, P		1	1.0000 EA
	Tyco Electronics Corporation	111950-1		
Floppy	CONN, HDR, 2 X 17, PLG, VT, 0.1, 062ST, KP 5, S		1	1.0000 EA
	Foxconn Electronics, Inc.	HL09177-P4		
	Tyco Electronics Corporation	111972-7		
	Foxconn Electronics, Inc.	HL13178		
	Tyco Electronics Corporation	111685-7		
	Molex Connector Corporation	0872563456		
Primary and Secondary ATA	CONN, HDR, 2 X 20, PLG, VT, 0.1, 062ST, KP 20		1	2.0000 EA
	Foxconn Electronics, Inc.	HL09207-D2		
	Tyco Electronics Corporation	111971-8		
	Foxconn Electronics, Inc.	HL13208		
	Tyco Electronics Corporation	111685-8		
	Molex Connector Corporation	0872564056		
SCSI 320 Internal and External,	CONN, HDR, 2 X 34, RCP, VT, 0.1, 093ST, KP SHR		1	2.0000 EA
	Foxconn Electronics, Inc.	QA01343-P4		
	Molex Connector Corporation	0743051302		
SSI Front Panel	CONN, HDR, 2 X 12, PLG, VT, 0.1, 062ST, KP 3		1	1.0000 EA
	Foxconn Electronics, Inc.	HC1912G-D5		
Extended Front Panel	CONN, HDR, ST, PLRZ, 2X(4)P		1	1.0000 EA
	Foxconn Electronics, Inc.	HC1904G-D0		

Interface Definition	Description / Manufacture	Item Number	Qty	Unit of Measure
	Tyco Electronics Corporation	2-146220-1		
Intrusion Switch Header	CONN, HDR, 1 X 2, PLG, VT, 0.1, 093ST, KP PG		1	1.0000 EA
	Foxconn Electronics, Inc.	HF06021-P1		
Stacked USB Port 1 and 2				
ICMB, Four Position version				
Bay A Hot Swap Drive I2C				
Bay B Hot Swap Drive I2C	CONN, HDR, 1 X 4, PLG, VT, 2MM, 093ST, KP PG		1	3.0000 EA
	Foxconn Electronics, Inc.	HF55040-C1		
All Eight Fans	CONN, HDR, 1 X 3, PLG, VT, 0.1, 093ST, KP 1, SH		1	8.0000 EA
	Foxconn Electronics, Inc.	HF08030-P1		
Speaker	AUDIO XDCR, 80OHM, 2400HZ, 85DB, THM, 5V		1	1.0000 EA
	Challenge Electronics	DBX-05A		
	RDI Electronics, Inc.	DMT-1206[I]		
Retention Mechanisms	ASSY, MECH PRC-RET, LIF, MULTI, TUFL, PLASTI> 1 4.000 EA		1	
	ITW Fastex	8026-00-9909		

11. Electrical and Thermal Specifications

This chapter specifies the operational parameters and physical characteristics for the Server System SSH4 baseboard. This is a board-level specification only. System specifications are beyond the scope of this document.

11.1 Absolute Maximum Electrical and Thermal Ratings

Operation of the Server System SSH4 board set at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 53. Absolute Maximum Electrical and Thermal Specifications

Operating Temperature	5°C to +55°C 1
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to Vdd + 0.3V 2
3.3V supply voltage with respect to ground	-0.3 to +3.63V
5V supply voltage with respect to ground	-0.3 to +5.5V
Notes: Chassis design must provide proper airflow to avoid exceeding Intel Xeon processor IHS maximum case temperature. VDD means supply voltage for the device.	

Table 54 lists the maximum component case temperatures for baseboard components that could be sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect component case temperatures. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

Caution: An ambient temperature that exceeds the board's maximum operating temperature by 5°C to 10°C can cause components to exceed their maximum case temperature. In determining system compliance, consideration should be given to maximum rated ambient temperatures.

Table 54. Thermal Specification for Key Components

Component	Maximum Temperature
Intel® Xeon™ processor, rating to meet Flexible Motherboard (FMB) guidelines.	72 °C (case)
82550PM Ethernet Controller	85 °C (case)
CSB5	80 °C (case)
CIOB30	97 °C (case)
CMIC	85 °C (case)
REMC	90 °C (case)
Lithium battery	70 °C (case)
Note: The Intel Xeon processor uses an integrated heat spreader (IHS). Thermal specifications relate to processor operation under maximum power dissipation conditions with the HIS installed.	

11.2 Electrical Specifications

DC and AC specifications for the Server System SSH4 are summarized below.

11.2.1 Power Budget

The following tables list the power consumed on each supply line for the Server System SSH4 boardset configured with four Intel Xeon processors, 12 DIMMs, and six fans. Table 55 lists power consumption for use with the Intel® SR4100 chassis. Table 56 lists power consumption for use with the Intel® SR7000 chassis.

Note: The following numbers are provided as an example. Actual power consumption will vary depending on the exact server configuration.

Table 55. Power Budget for SRSH4 Chassis

Devices	3.3V	+5V	+12V	-12V	5V Standby	Total Wattage
Processors	-	-	30.85 A	-	-	370.20 W
DIMMs	1.97 A	-	6.10A	-	-	79.70 W
Baseboard	10.76 A	4.36A	1.15 A	0.01 A	0.38 A	73.13 W
Fans	-	-	5.00 A	-	-	60.00 W
PCI / PCI-X slots	13.64 A	15.00 A	-	-	0.34 A	121.71 W
Peripherals	-	6.91A	4.90A	-	-	93.35 W
Total Current	26.37 A	26.27 A	48.00 A	0.01 A	0.72 A	Total
Total Power						798.09 W

Table 56. Power Budget for SPSH4 Chassis

Devices	3.3V	+5V	+12V	-12V	5V Standby	Total Wattage
Processors	-	-	30.85 A	-	-	370.20 W
DIMMs	1.97 A	-	6.10 A	-	-	79.70 W
Baseboard	10.76 A	4.36 A	1.15 A	0.01 A	0.38 A	73.13 W
Fans	-	-	5.58 A	-	-	66.96 W
PCI / PCI-X slots	13.64 A	15.00 A	-	-	0.34 A	121.71 W
Peripherals	-	13.18 A	10.5 A	-	-	191.9 W
Total Current	26.37 A	26.27 A	48.00 A	0.01 A	0.72 A	Total
Total Power						903.6 W

For a specific system or configured calculations, add the power consumed by all devices plugged into the board set.

11.2.2 Power Supply Specifications

This section provides power supply design guidelines for the server system SSH4, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 57. Static Power Supply Voltage Specification

Parameter	Min	Nom	Max	Units	Tolerance
+3.3 V	+3.25	+3.30	+3.35	Vrms	+1.5/-1.5%
+5 V	+4.90	+5.00	+5.10	Vrms	+2/-2%
+12 V	+11.76	+12.00	+12.24	Vrms	+2/-2%
-12 V	-11.40	-12.20	-13.08	Vrms	+9/-5%
+5 VSB	+4.85	+5.00	+5.20	Vrms	+4/-3%

Table 58. Dynamic Power Supply Voltage Specification

Output	Min	Max	Tolerance
+3.3 V	3.20 V	3.46 V	+5 / -3 %
+5 V	4.80 V	5.25 V	+5 / -4 %
+12 V	11.52 V	12.6 V	+5 / -4 %
+5 VSB	4.80 V	5.25 V	+5/-4%

11.2.3 Power Timing

This section discusses the timing requirements for single power supply operation.

The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 5 to 200 ms. The +3.3 V, +5 V and +12 V output voltages start to rise approximately at the same time. All outputs must rise monotonically. The +5 V output must be greater than the +3.3 V output during any point of the voltage rise, however, never by more than 2.25 V. Each output voltage shall reach regulation within 100 ms (Tvout_on) of each other and begin to turn off within 100 ms (Tvout_on) of each other. The following table shows the output voltage timing parameters.

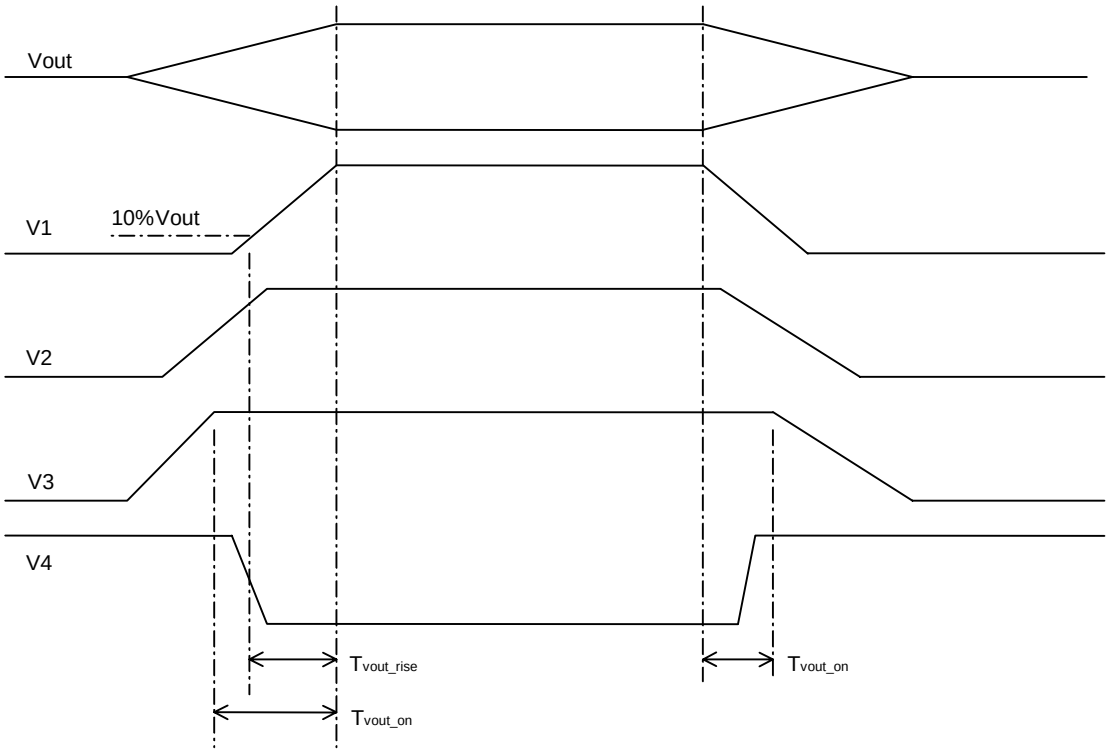


Figure 21. Output Voltage Timing

Table 59 shows the timing requirements for a single power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied. The ACOK# signal is not being used to enable the turn on timing of the power supply. Table 60 describes the required turn on/off timing parameters.

Table 59. Voltage Timing Parameters

Item	Description	Min	Max	Units
Tvout_rise	Output voltage rise time from each main output.	5	200	ms
Tvout_on	All main outputs must be within regulation of each other within this time.		100	ms

Table 60. Turn On / Off Timing

Item	Description	Min	Max	Units
Tsb_on_delay	Delay from AC being applied to 5 VSB being within regulation.			ms
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltages, including 5 VSB, stay within regulation after loss of AC.	21		ms
Tpwok_holdup	Delay from loss of AC to deassertion of PWOK.	20		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T pson_pwok	Delay from PSON# deactive to PWOK being deasserted.		50	ms
Tacok_delay	Delay from loss of AC input to deassertion of ACOK#.	20		ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	ms
T pwok_off	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V, 5VSB) dropping out of regulation limits.	1	200	ms
Tpwok_low	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal.	100		ms

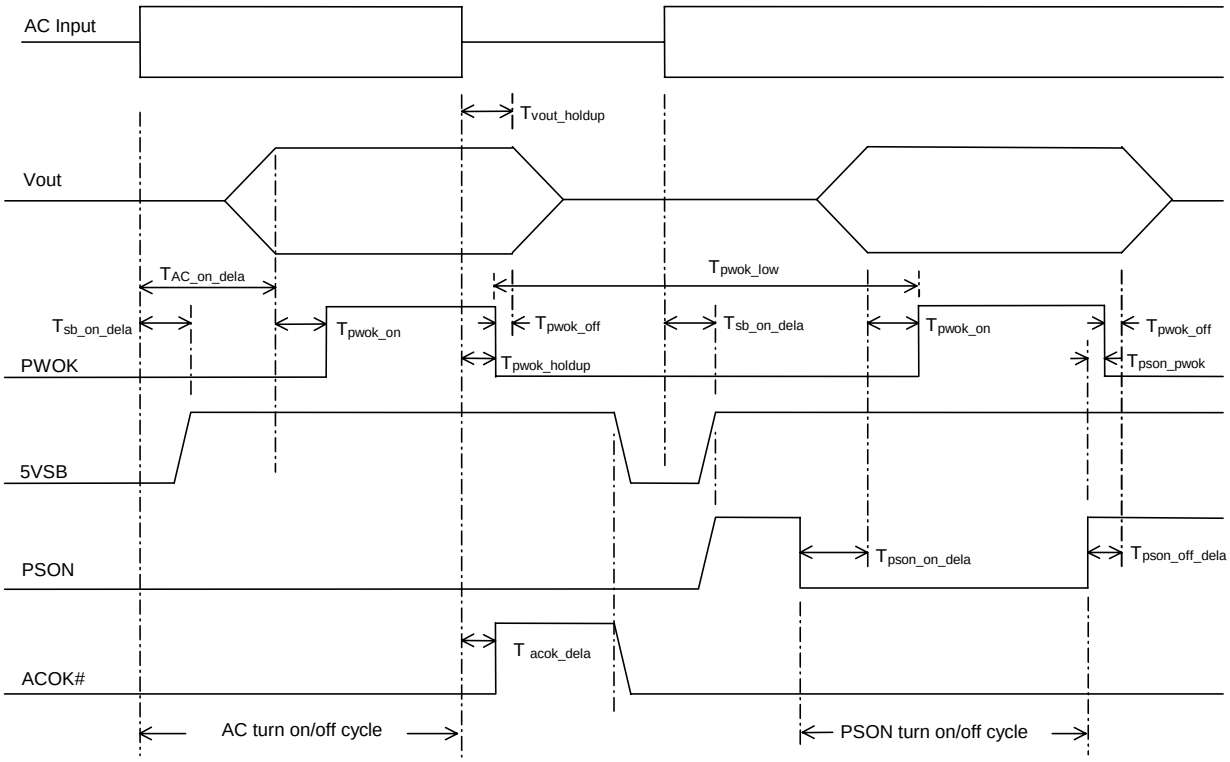


Figure 22 Turn On Turn Off Timing

11.2.4 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

Voltage shall remain within +/- 5% of the nominal set voltage on the +5 V, +12 V, 3.3 V, -5 V and –12 V output, during instantaneous changes in load shown in the following table.

Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.

Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50 Hz to 5 kHz. The load slew rate shall not be greater than 0.2 A/µs.

Table 61. Transient Load Requirements

Output	Step Load Size	Starting Level	Finishing Level	Slew Rate
+3.3 V	8.0 A	Min. Load	Min. load + 8.0 A and step up to max. load	0.50 A/µs
+5 V	6.0 A	Min. Load	Min. load + 6.0 A and step up to max. load	0.50 A/µs
+12 V	7.0 A	Min. Load	Min. load + 7.0 A and step up to max. load	0.50 A/µs
+5 VSB	150 mA	Min. Load	Min. load + 150 mA and step up to max. load	0.1 A/µs
-12 V	250 mA	Min. Load	Min load +250 mA and step up to max. load	0.1 A/µs

12. Mechanical Specifications

The following diagrams show the mechanical specifications of the Server System SSH4 baseboard. All dimensions are given in inches, and are dimensioned per ANSI Y15.4M. Connectors are dimensioned to pin 1.

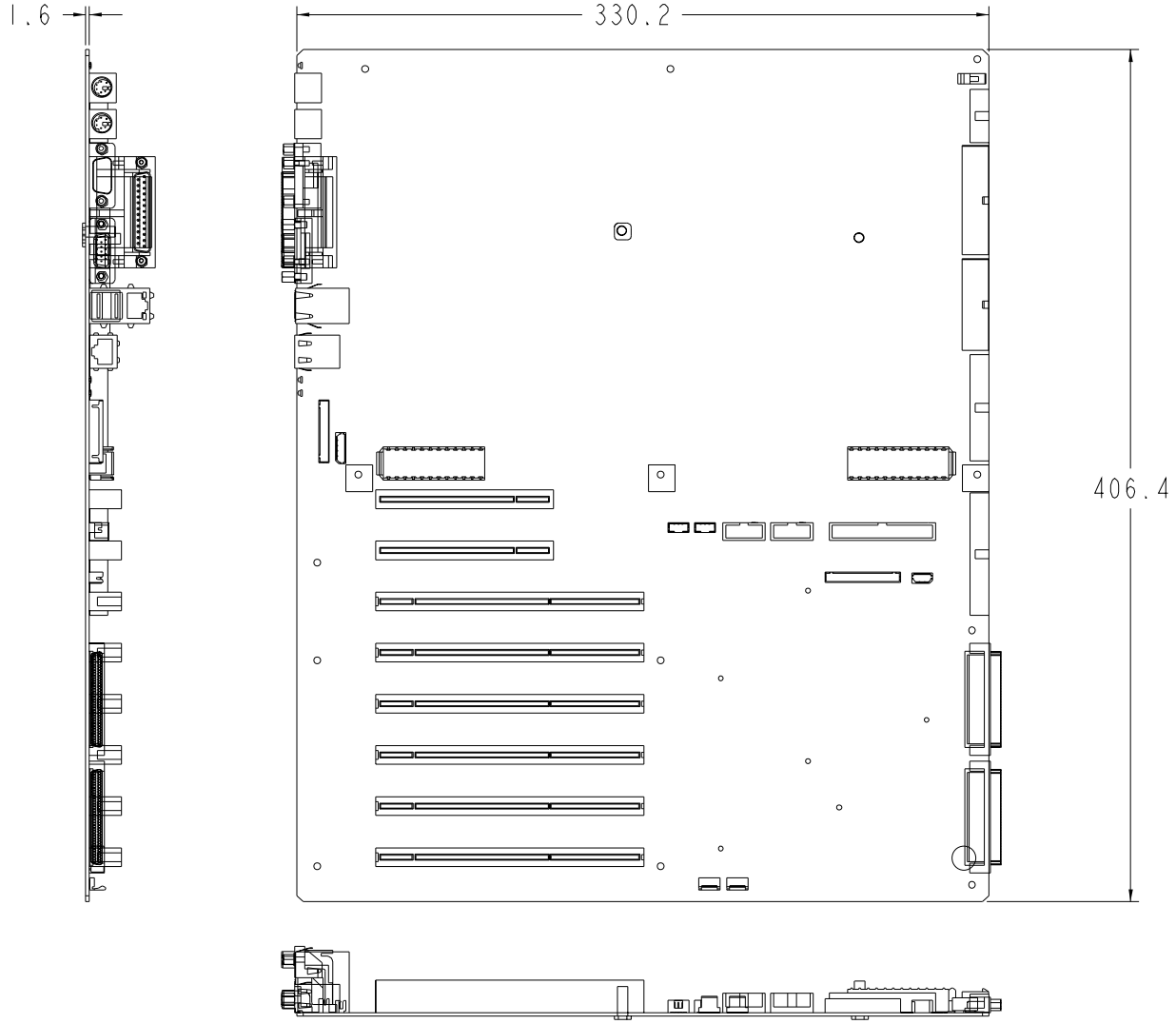


Figure 23. Baseboard Mechanical Diagram

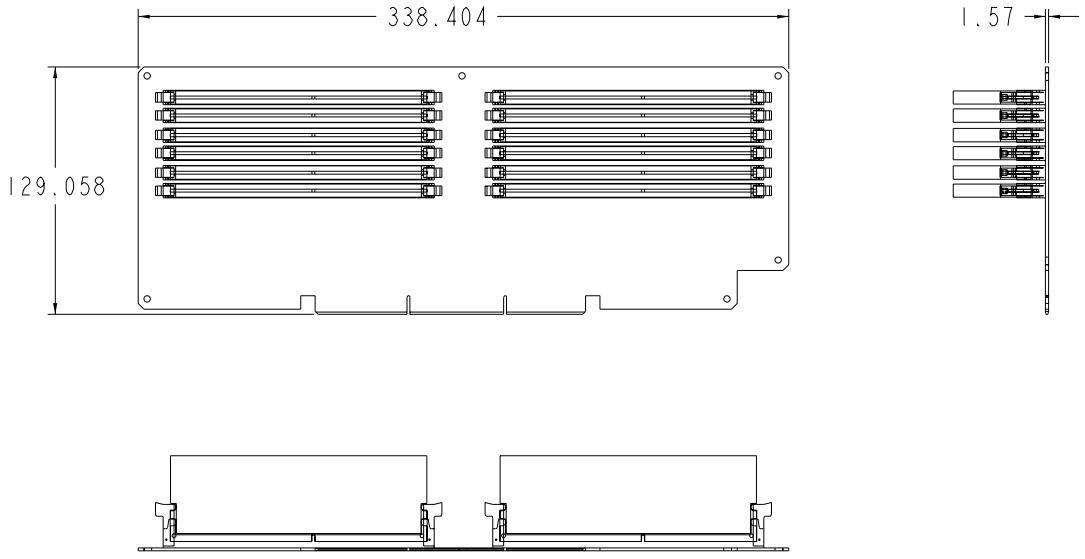


Figure 24. Memory Board Mechanical Diagram

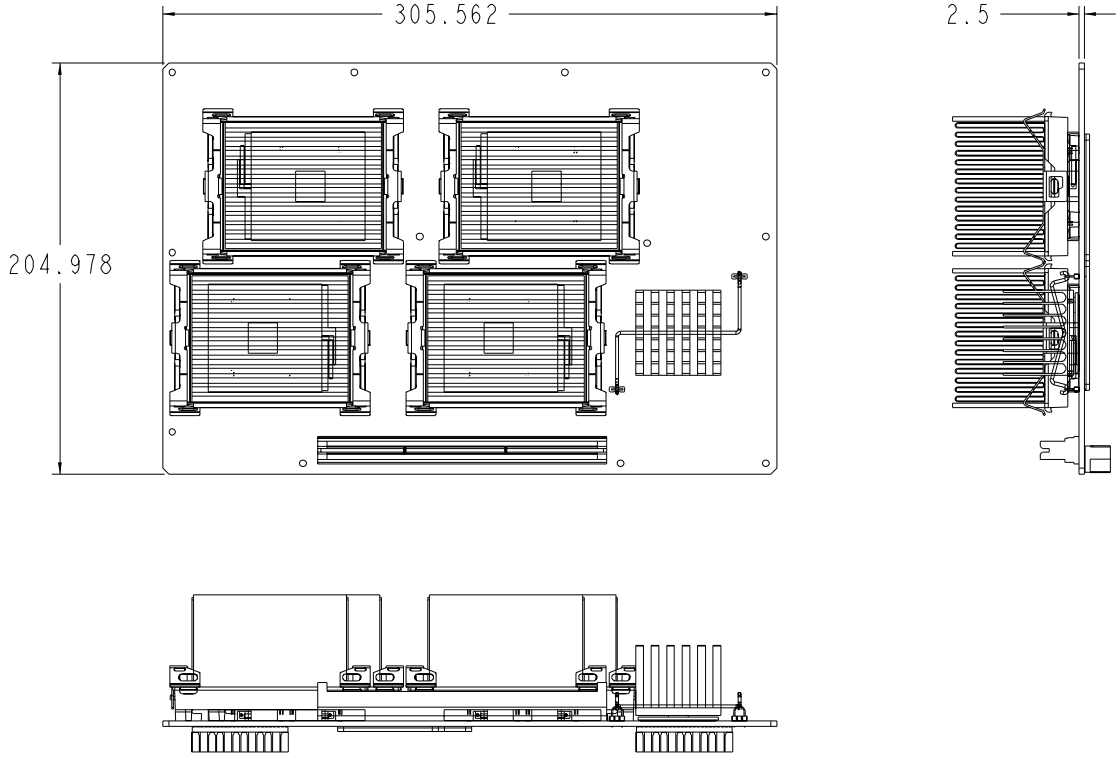


Figure 25. Processor Board Mechanical Diagram

13. System BIOS

This section describes basic features of the system BIOS. System BIOS features that are specific to error handling are described in Section 14, Error Handling. For a complete specification of standard PC-BIOS functions, refer to the appropriate reference document such as the *System BIOS for IBM PCs, Compatibles, and EISA Computers, Second Edition ISBN 0-201-57760-7*). The following groups of system BIOS features are described here:

- Security features
- Auto-configuration features
- System services

13.1 BIOS Overview

The term BIOS, as used in the context of this document, refers to the system BIOS, the BIOS Setup, and option ROMs for on-board peripheral devices that are contained in the system flash. The system BIOS controls basic system functionality using stored configuration values. The terms flash ROM, system flash, and BIOS flash may be used interchangeably in this document.

BIOS Setup (Setup) is a flash ROM-resident configuration utility that provides the user with control of configuration values stored in battery-backed CMOS configuration RAM. BIOS Setup provides the means to configure on-board hardware devices and add-in cards. BIOS options can also be set utilizing the System Setup Utility (SSU). The operation of the System Setup Utility is discussed in a separate document. BIOS Setup is closely tied with the system BIOS and is considered a part of BIOS.

Intel® iFlash(iFlash.exe) are used to load areas of flash ROM with Setup, BIOS, and other code/data.

The following is the breakdown of the product ID string:

BIOS string **SSH40.86B.0061.B.0206071510** (sample)

- 4-byte board ID, ‘SSH4’
- 1-byte board revision, starting from ‘0’
- 3-byte OEM ID, ‘86B’ for standard BIOS
- 4-byte build number
- 1-3 bytes describing build type (D for development, A for Alpha, B for Beta, Pxx for production version xx)
- 6-byte build date in yymmdd format
- 4-byte time in hhmm format

13.1.1 System BIOS

The system BIOS is the core of the flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services and support for industry standards, such as the *Advanced Configuration and Power Interface Specification*, Revision 1.0b and the *Wired for Management Baseline Specification*, Revision 2.0.

In addition, the system BIOS supports the following features.

- Security
- MPS support
- Server management and error handling
- CMOS configuration RAM management
- OEM customization
- PCI and Plug and Play (PnP) BIOS interface
- Console redirection
- Resource allocation support

13.1.2 Flash Update Utility

The system BIOS and the setup utility are resident in partitioned flash ROM. The device is in-circuit reprogrammable. On the Server System SSH4, 1 MB of flash ROM is provided. iFlash and Phoenix PHLASH can be used to reprogram the BIOS operational code located in the flash ROM. A BIOS image is provided in the form of a binary file or files that is/are read by the flash utilities. Baseboard revisions may create hardware incompatibilities and may require different BIOS code.

For more information, refer to Section 16: Flash Update Utilities.

13.1.2.1 System Flash ROM Layout

The flash ROM contains system initialization routines, BIOS strings, BIOS Setup, and run-time support routines. A 16 KB user block is available for user ROM code and an additional 128 KB block is available for custom logos. The flash ROM also contains compressed initialization code for on-board peripherals such as SCSI, NIC, and video controllers. The BIOS image contains all of the BIOS components at appropriate locations. The Flash Update Utilities can be used to reprogram the BIOS operational code areas.

At run time, none of the flash blocks are visible at the aliased addresses below 1 MB due to shadowing. Intel reserves the right to change the flash map without notice.

A 64 KB parameter block in the flash ROM is dedicated to storing configuration data that controls extended system configuration data (ESCD), on-board SCSI configuration, OEM configuration areas, etc. The block is partitioned into separate areas for logically different data. Application software must use standard flash device advanced programming interfaces (APIs) to access the ESCD areas and may not access the data directly.

13.2 Security Features

The BIOS provides a number of security features. This section describes the operating model of the security features implemented on the Server System SSH4.

13.2.1 Operating Model

The following table summarizes the operation of security features supported by the BIOS.

Note: The “Supervisor” password is not a superset of the “User” password. The User password unlocks I/O devices, enables boot, and allows access to a minimal amount of BIOS Setup. The Supervisor password only controls access to the complete BIOS Setup.

Table 62. Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Runtime activation of PS/2 keyboard controller Hotkey	User password enabled in Setup	• On-board video goes blank (if enabled in Setup). • Floppy writes are disabled (if selected in setup). • All switches on the front panel except NMI and ID are disabled • No PS/2 mouse or PS/2 keyboard input is accepted except password. • Keyboard LEDs flash	User Password	• Video is restored. • Floppy writes are enabled. • Front panel switches are enabled. • Keyboard and mouse inputs are accepted.
Secure boot	Power On/Reset	User password and Secure Boot Enabled in Setup	• Prompts for Password, if booting from drive A • Enter Secure Mode just before scanning option ROMs and before “F2” keyboard option. • Keyboard LEDs flash • Floppy writes are disabled (if programmed in setup). • All the switches (including the power switch) on the front panel are disabled except NMI and ID • No input from PS/2 mouse or PS/2 keyboard is accepted except password; however, the mouse driver is allowed to load before a password is required.	User Password	• Floppy writes are re-enabled. • Front panel switches are re-enabled. • PS/2 Keyboard and PS/2 mouse inputs are accepted. • System attempts to boot from drive A. If the user enters correct password, and drive A is bootable, the system boots normally • Video is restored.

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
			• If booting from a floppy, the system will pause and wait for the User password before booting. If the user enters a correct password, the system boots normally.		
Password on boot	Power On/Reset	User password set, Password on Boot enabled and Secure Boot disabled in Setup	• Front panel switches are disabled. • System halts for user password before scanning option ROMs. The system is not in secure mode. • No mouse or keyboard input is accepted except the password.	User Password	• Front panel switches are re-enabled. • PS/2 keyboard and PS/2 mouse inputs are accepted. • The system boots normally. Boot sequence is determined by setup options.
Fixed disk boot sector	Power On/Reset	Write Protect enabled in Setup	Write protects the master boot record of the IDE hard drives, only if the system has been booted from a floppy. The BIOS will also write protect the boot sector of the drive C: if it is an IDE drive.	Set feature to Normal in Setup	Hard drive will behave normally.

13.2.2 Password Protection

The BIOS uses passwords to prevent unauthorized tampering with the system. Once Secure Mode is entered, access to the system is allowed only after the correct password(s) has been entered. Both user and administrator passwords are supported by the BIOS. Each password can be independently set or cleared during system configuration using Setup. The maximum length of the password is seven characters, the minimum length is one character. The password uses only alphanumeric characters a-z, A-Z, 0-9. The user and administrator passwords are not case sensitive. When entering a password, the backspace key is accepted as a character of the password. Entering the backspace key will result in a wrong password. Once set, a password can be cleared by changing it to a null string.

Access to specific Setup fields is controlled through the User password. These Setup fields are: time, date, language, user password, secure mode timer, and secure mode hot-key setup fields. The remaining Setup fields can be modified only if the Supervisor password is entered. If only one password is set, that password is required to enter Setup. The Administrator has control over all fields in the setup including the ability to clear the User password.

The user password also allows the system to boot if secure boot is enabled.

If three wrong passwords are entered consecutively when the system is booting or when entering BIOS setup, the system will be placed into a halt state and a message will be displayed to the operator stating that the system has been disabled. Once in this mode, the only way to clear the system disabled state is to power cycle the system. This feature makes it difficult to

break the password by “trial and error” method. If an operating system is running there is no check for the number of incorrect password attempts.

The emergency management port password is only utilized by the BMC and does not affect the BIOS security in any way, nor does the BIOS security engine provide any validation services for this password. EMP security is handled through the BMC and EMP utilities.

13.2.3 Secure Mode Timer

If the Secure Mode Timer function is enabled and no keyboard or mouse action has occurred during the specified time-out period (preset time periods are provided as options in BIOS Setup), the system enters Secure Mode. The following occurs until the user password is entered:

- PS/2 Keyboard and PS/2 mouse input is disabled. PS/2 keyboard lights start blinking.
- On-board video is blanked (if selected in Setup).
- The floppy drive is write-protected (if selected in Setup).
- The front panel reset, power, and sleep (ACPI OS only) buttons are locked.

13.2.4 Hot Key Activation

A hot-key combination allows the user to activate Secure Mode immediately, instead of waiting for the Secure Mode Timer time-out to expire. The hot-key combination is configured in Setup. Valid hotkeys are Ctrl-Alt <A-Z, 0-9>; the alpha characters are not case-sensitive. The hot-key works only with PS/2 keyboards.

13.2.5 Password Clear Jumper

If the user or administrator password(s) is lost or forgotten, both passwords can be cleared by moving the Password Clear Jumper into the “clear” position. The BIOS determines if the Password Clear Jumper is in the “clear” position during BIOS POST and clears any passwords. The Password Clear Jumper must be restored to its original position before a new password can be set. EMP passwords are not affected by password clear jumper. The location of the Password Clear Jumper is described in *Appendix A: Jumper Locations*.

13.2.6 Secure Mode

Secure Mode refers to a system state in which many of the external inputs and outputs are disabled to prevent tampering. These include PS/2 ports, floppy drives, and the on-board video. Secure mode is temporarily disabled by entering the User password.

13.2.7 Floppy Write Protection

If enabled in Setup, writes to the floppy disk are blocked when the system is in Secure Mode. This feature prevents copying data from a machine that has been secured. When the Floppy Write Protection feature is disabled, the floppy diskette drive operates normally regardless of the Secure Mode.

13.2.8 Front Panel Lock

The power, sleep, and reset buttons on the front panel are always disabled when in Secure Mode.

13.2.9 Video Blanking

If enabled in Setup and if a monitor is attached to embedded VGA controller, the display will be blanked upon entering Secure Mode. The display will be restored after the user password has been successfully entered. This feature prevents unauthorized users from viewing the screen while the system is in Secure Mode. Monitors attached to add-in video adapters will not be blanked, regardless of the setting of the video blanking feature.

13.2.10 PS/2 Keyboard and Mouse Lock

The PS/2 keyboard and mouse are unavailable while the system is in secure mode. The keyboard controller will not pass any keystrokes or mouse movements to the system until the correct user password is entered.

Note: A USB keyboard and mouse are not affected by secure mode keyboard and mouse lock and will continue to work.

13.2.11 Secure Boot (Unattended Start)

Secure Boot allows the system to boot and run the operating system without requiring the user password even if a user password is configured. Until the user password is entered, mouse input, keyboard input, and activation of the enabled secure mode features described above are not accepted.

In Secure Boot mode, if the BIOS detects a floppy diskette in the A: drive at boot time, it displays a message and waits for the user password before booting. After the password is entered, the system can boot from the floppy and secure mode is disabled. If the secure mode timer expires or the secure mode hot-key is pressed, the system will return to secure mode.

If no diskette is in drive A, the system will boot from the next boot device and will be placed in secure mode automatically. The PS/2 keyboard and mouse are locked before option ROMs are scanned. If Secure Boot mode is enabled, the user cannot enter option ROM setup unless the user password is entered. This prevents the user from entering the configuration utilities in the option ROMs, where it is possible to format, etc. The on-board video is not blanked until the end of POST.

13.2.12 Fixed Disk Write Protect

When the Fixed Disk Write Protect option is enabled, it will prevent writes to the fixed IDE disk only when the system is booted to a floppy. This feature works only with IDE drives (SCSI drives are not affected) and only the boot drive is write-protected.

13.2.13 Power Switch Inhibit

The Power Switch Inhibit option enables and disables the power switch. If enabled, the system power cannot be turned off with the power switch after booting the operating system nor can the system be powered off when the power switch is held down for more than four seconds. In this mode, to shut down the system the operator will need to enter the User password to unlock the keyboard and then shut the system down from the operating system.

13.3 Auto-configuration Features

The BIOS provides support for auto-configuration of the following:

- Plug and Play
  - Resource allocation
  - PCI auto-configuration
  - Automatic detection of video adapters
- Multiple processor support
- Memory configuration
- Multi boot
- Boot drive selection
- PS/2 mouse and keyboard swapping
- Boot without keyboard and mouse
- USB keyboard and mouse
- Processor micro-code update
- CMOS reset
- Boot splash screen

13.3.1 Plug and Play

13.3.1.1 Resource Allocation

The system BIOS identifies, allocates, and initializes resources. The BIOS scans for the following (in order):

1. ISA devices: Add-in ISA devices are not supported on the baseboard. However, some standard PC peripherals may require ISA-style resources. Resources for these devices are reserved as needed.

2. Add-in video graphics adapter (VGA) devices: If found, the BIOS initializes and allocates resources to these devices (precedence over on-board video).

3. PCI Devices: The BIOS allocates resources according to the parameters configured through the Setup Menu.

The system BIOS Power-on Self Test (POST) guarantees there are no resource conflicts prior to booting the system. Note that PCI device drivers must support sharing IRQs, which should not be considered a resource conflict. Only four legacy IRQs are available for use by PCI

devices. Therefore, most of the PCI devices share legacy IRQs. In SMP mode, the I/O APICs are used instead of the legacy “8259-style” interrupt controller. There is very little interrupt sharing in SMP mode.

13.3.1.2 PnP ISA Auto-configuration

The BIOS provides the following support:

- Supports relevant portions of the Plug and Play ISA Specification, Revision 1.0a and the *Plug and Play BIOS Specification*, Revision 1.0A.
- Assigns I/O, memory, direct memory access (DMA) channels, and IRQs from the system resource pool to the embedded PnP Super I/O device.
- Does not support add-in PnP ISA devices.

13.3.1.3 PCI Auto-configuration

The system BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the *PCI Local Bus Specification*, Revision 2.2.

Beginning at the lowest device, the BIOS uses a “depth-first” scan algorithm to enumerate the PCI buses. Each time a bridge device is located, the bus number is incremented and scanning continues on the secondary side of the bridge until all devices on the current bus are scanned.

The BIOS then scans for PCI devices using a “breadth-first” search. All devices on a given bus are scanned from lowest to highest before the next bus number is scanned.

The system BIOS POST maps each device into memory[1] and/or I/O space, and assigns IRQ channels[2] as required. The BIOS programs the PCI-ISA interrupt routing logic in the chipset hardware to steer PCI interrupts to compatible ISA IRQs.

The BIOS dispatches any option ROM code for PCI devices to the DOS compatibility hole (C0000h to E7FFFh[3]) and transfers control to the entry point. The DOS compatibility hole is a limited resource. Therefore, system configurations with a large number of PCI devices may result in a shortage of this resource. If the BIOS runs out of option ROM space, some PCI option ROMs may not be executed and a POST error is generated. Scanning PCI option ROMs can be controlled on a slot-by-slot basis in the BIOS setup.

Drivers and/or the operating system can detect the installed devices and determine resource consumption using the defined PCI, legacy PnP BIOS, and/or ACPI BIOS interface functions.

13.3.1.4 Legacy ISA Configuration

The baseboard does not support legacy ISA add-in devices.

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[1] The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space due to PCI architectural limitations (refer to the *PCI-to-PCI Bridge Architecture Specification*).

[2] PCI IRQ assignments may be overridden using the System Setup Utility.

[3] Note that the BIOS size may increase thereby limiting the area used by option ROMs to 0C0000h – 0E0000h.

13.3.1.5 Automatic Detection of Video Adapters

The BIOS detects video adapters in the following order:

1. Add-in PCI
2. On-board PCI

The on-board video or add-in video BIOS is shadowed, starting at address C0000h, and is initialized after memory initialization but before memory tests begin in POST. Precedence is always given to add-in devices.

13.3.2 Multiple Processor Support

The BIOS supports up to four identical Intel® Xeon™ processors. Processors must be populated starting with the first processor socket. Populating processors in any other order may result in system error messages, including system beep codes indicating a missing processor and failure to boot.

13.3.2.1 Multiprocessor Specification Support

The BIOS complies with all requirements of the *Multi-Processor Specification* (MPS), Revision 1.4, for symmetric multiprocessor support.[4] The base MP Configuration Table contains the following entries:

- MP table header
- Processor entries
- PCI bus entries
- I/O APIC entries
- I/O interrupt entries
- Local interrupt entries
- System address space mapping entries
- Bus hierarchy descriptor
- Compatibility bus address space modifier entries

13.3.2.2 Multiple Processor Support

Intel® Xeon™ processors have a microcode-based MP initialization protocol. On reset, each processor competes to become the bootstrap processor (BSP) . If a serious error is detected during the Built-in Self Test (BIST), the processor on which the error occurred does not participate in the initialization protocol. A single processor that successfully passes BIST is automatically selected by the hardware as the BSP and begins executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an application processor (AP).

The BSP is responsible for executing POST and preparing the machine to boot the operating system. The BIOS performs several other tasks in addition to those required for MPS support,

[4] MPS Revision 1.1 is no longer supported.

as described in Revision 1.4 of the MP specification. These tasks are part of fault resilient booting algorithm and are discussed in this document in Section 13.5: Reliability Features. At the time of booting, the system is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR driven by programmable interrupt controller (PIC) and non-maskable interrupt (NMI)).

As a part of the boot process, the BSP wakes each AP. When awakened, an AP programs its memory type range registers (MTRRs) to be identical to those of the BSP. All APs execute a halt instruction with their local interrupts disabled. To ensure that an AP can respond to an SMI, any agent that wakes an AP must ensure that the AP is left in the halt state, not the “wait for startup IPI” state. The waking agent must also ensure that the code segment containing the halt code executed by an AP is protected and does not get overwritten. Failure to comply with these guidelines results in a system hang during the next SMI.

13.3.2.3 Multiple Processor Speed Support

The processor speed is configured by the BMC and is not user selectable. BIOS Setup reports the type and current speed of all detected and enabled processors. Mixing different speed processors is not supported. If the BIOS detects a configuration in which there are mismatched speed-locked processor, the BIOS disables all but the lowest featured and lowest speed processor(s). The BIOS sends the POST error codes to the BMC to log in the SEL. The BIOS displays a POST error message and pauses the boot process. BIOS displays the <F1> to continue and <F2> to go to Setup message on bottom of screen (this behavior is dependent on the setting of the “POST Error Pause” Setup value).

13.3.2.4 Unsupported Processor Steppings

If the system BIOS detects a processor for which a microcode update is not available, the BIOS displays an POST error message and pauses the boot process (this behavior is independent of the setting of the “POST Error Pause” Setup value). The BIOS displays the <F1> and <F2> messages on the bottom of the screen. The BIOS sends the POST error codes to the BMC for logging in the system event log.

13.3.3 Memory Sizing

During POST, the BIOS:

- Tests and sizes memory
- Configures the memory controller

The Server System SSH4 baseboard supports only 2.5 V, 100 MHz Address Bus, 200 MHz Data Bus, DDR200 or DDR266 -compliant registered ECC DDR DIMMs. 12 DIMM slots are provided.

The minimum supported memory configuration is 512 MB using four DIMMs. The maximum configurable memory size is 24 GB using 12 DIMMs.

Memory must be populated starting with the lowest numbered bank of four DIMMs first and filling banks of DIMMs in consecutive order. Empty memory banks between DIMMs are not supported. Various sizes and vendors of DIMMs can be used but the banks must be filled with identical DIMMs. Memory sizing and configuration are guaranteed only for qualified DIMMs approved by

Intel. The BIOS gathers all type, size, speed, and memory attributes from the Serial Presence Detect (SPD) on the memory DIMM.

The memory-sizing algorithm determines the size of each row of DIMMs. The BIOS reads the DIMM speed information and programs the memory controller. The BIOS is capable of detecting, sizing, and testing any amount of RAM, up to a maximum of 24 GB. The total amount of configured memory can be found using using INT 15h, AH = 88h;[5] INT 15h, function E801h;[6] INT 15h, function E820h.[7]

Because the system supports up to 24 GB of memory, the BIOS creates a hole just below 4 GB to accommodate the system BIOS flash, APIC memory, and memory-mapped I/O located on 32-bit PCI devices. The size of this hole depends upon the number of PCI cards and the memory mapped resources requested by them. It is typically less than 128 MB.

13.3.3.1 ECC Memory Initialization

The system BIOS handles ECC memory initialization. All memory locations, including system management RAM (SMRAM) and the shadow memory region, are unconditionally initialized during POST (set to '0'). ECC errors are ignored while ECC memory is initialized to prevent false errors caused by uninitialized memory bytes. If hard errors are detected during the memory test, the memory partition containing the errors is resized to eliminate the failing locations.

Note: ECC memory initialization cannot be aborted and may result in a noticeable delay depending on the amount of memory in the system.

13.3.4 Boot Device Selection

The BIOS conforms to the *BIOS Boot Specification (BBS)*, Revision 1.01, which describes a method by which the BIOS identifies all initial program load (IPL) devices in the system, prioritizes them in the order selected in Setup, and then sequentially attempts to boot from each device.

If more than one non-BBS compliant device exists in the system, determination of which device will be the boot device is based on the option ROM scan order. Option ROMs residing lower in memory are scanned first and option ROMs higher in memory are scanned last. In some cases, control of the non-BBS compliant device from which the system is booted may be achieved by moving adapter cards to different slots in the system. It is possible to boot from a non-BBS complaint device, but the BIOS cannot selectively boot from one of several non-BBS compliant devices in a system.

BIOS Setup presents boot order options including floppy, CD-ROM, hard drive, and removable ATAPI (Advanced Technology Attachment Packet Interface) drives, such as the LS-120. The system BIOS tries to boot from devices in the order specified by BIOS Setup. BIOS Setup also allows the boot drive to be any hard drive that is controlled by a *BIOS Boot Specification* compliant option ROM BIOS, including drives attached to the on-board SCSI controller or on-board IDE. Some BBS compliant option ROMs may present all the drives as a single device, and may not allow the user to manipulate the order on a drive-by-drive basis.

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[5] INT 15h, AH=88h can report a maximum of 64 MB of contiguous memory.

[6] INT 15h, function E801h can report a maximum of 4096 MB of contiguous memory.

[7] INT 15h, function E820h can report up to 2^{65} –1 bytes of memory including non-contiguous memory regions.

A boot device selection menu can be invoked before booting by pressing the ESC key during POST. This allows the user to select the boot device (e.g., to a CDROM) for the current boot without entering Setup. Available selections on this menu are similar to the boot device menu described in Section 15.1.3.5.

User selections made in this menu are temporary and are not saved in non-volatile memory. The system can boot from a SCSI CD-ROM or SCSI DVD-ROM drive if the corresponding SCSI option ROM provides appropriate support.

13.3.5 PS/2 Mouse and Keyboard Swapping

The BIOS allows the keyboard and PS/2 mouse connectors to be swapped. The BIOS detects attached devices during POST and the keyboard controller is programmed accordingly. Hot plugging the mouse and keyboard is not supported by the baseboard and may have unpredictable results.

13.3.6 Boot without Keyboard and/or Mouse

The system can boot with or without a keyboard and/or mouse. The presence of the keyboard and mouse is detected automatically during POST, and, if present, the keyboard is tested. The BIOS displays the message "Keyboard Detected" if it detects a keyboard during POST and displays the message "Mouse Initialized" if it detects a mouse during POST. The system does not halt on errors if the keyboard is not detected.

13.3.7 Universal Serial Bus

The Server System SSH4 baseboard supports Universal Serial Bus devices that have run-time device drivers, the system BIOS supports only the following USB devices.

- USB keyboard
- USB Mouse
- Legacy USB

During POST, the system BIOS initializes and configures and enables the root hub ports, keyboards, mice, and USB hubs. The BIOS implements legacy USB keyboard support. The system BIOS does not support the ability to boot from a USB attached devices such as a floppy disk, hard drive or CD-ROM.

13.3.8 Processor Microcode Update API

The Intel® Xeon™ processor has the capability of correcting specific errata through the loading of an Intel-supplied data block (also called the “microcode update.”) The BIOS is responsible for storing the update in a non-volatile memory block and loading it into each Intel® Xeon™ processor during POST sequence. The *Willamette/Foster Processor BIOS Writer’s Guide* defines the interface for incorporating future releases of such updates into a system BIOS. This interface can be accessed from real mode by executing INT 15 with AX=0xD042. The BIOS performs all the recommended security checks before validating an update.

13.3.9 CMOS Reset

The CMOS configuration RAM is cleared by using one of the following methods:

- Placing a jumper on the CMOS clear jumper location. The location of the CMOS clear jumper is described in *Appendix A, Jumper Locations*.
- CMOS clear button sequence being pressed on the front panel (BMC detected). With the system off, press the Reset button and hold it down for four seconds or more; while holding down the reset button, press the power button. Release both buttons at the same time.
- BMC receiving the Set Front Panel CMOS Clear Options command with setCMOSClear indicated.

When the BMC requests a CMOS Clear, it sets the CMOS Clear signal. BIOS clears that signal using the Set Front Panel CMOS Clear Options command.

13.3.10 Processor Speed Settings

The BIOS does not participate in the determination or configuration of the correct processor speed. BIOS Setup reports the type and current speed of all detected and enabled processors.

Note: All production Intel® Xeon™ processors are speed-locked

13.3.11 Boot Logo

The BIOS includes a default Intel® server logo that is displayed by default during POST. If the POST diagnostic screen is disabled and a valid logo is detected, the BIOS will display the logo during the entire POST process except during option ROM scanning. When the logo is displayed, the BIOS displays a message showing the available hot-keys at the bottom of the screen.

The <Esc> key or the setup hot-key are used to switch to the POST diagnostic screen from the logo screen. The BIOS provides a Setup option to enable the POST diagnostic screen instead of the logo. Since serial console redirection cannot redirect screen if the display is in a graphics mode, serial console redirection does not work while the logo is being displayed. It is not possible use BIOS Setup to enable the logo and serial console redirection at the same time. If a service partition boot is requested, the BIOS turns off the logo for the current boot, then it restores the setting during the subsequent normal boot. The BIOS will temporarily remove the logo when the user is prompted for password during POST.

The logo remains on during option ROM initialization. The option ROM screen can be displayed if the user presses the <ESC> key. The option ROM screen is restored if the BIOS detects any key combination that includes the <CTRL> or <ALT> keys during option ROM scan because many option ROMs use such a key combination to enter their setup applications. The BIOS displays a progress meter at the top of the screen to provide visual indication of the percentage of POST completed. The BIOS measures the amount of time required for completing POST during every boot and uses that information to update the progress meter during the next boot.

The OEM boot splash logo implementation follows the guidelines specified in *Server Design Guide,* revision 2.0. The logo can be customized by OEMs. Section 13.9.2: OEM Logo Screen describes how to customize this logo.

13.4 Performance Features

For enhanced performance, the BIOS sets up the L2/L3 cache controller for the Intel® Xeon™ processor and performs option ROM shadowing.

13.4.1 Cache State on Boot

The cache controllers in all Intel® Xeon™ processors are initialized in a consistent manner with each other and the chip set.

13.4.2 Option ROM Shadowing

All on-board adapter option ROMs (stored in compressed form in the system flash ROM), and PCI adapter option ROMs are shadowed into RAM in the ISA-compatible ROM adapter memory space between C0000h and E7FFFh.[8] No external controls are provided for selecting the state of shadowing for a given region of ISA-compatible ROM space. PCI adapter option ROMs are always shadowed.[9] If enabled, the on-board video BIOS is always shadowed at C0000h.

13.5 Reliability Features

The BIOS supports several features to create a robust computing environment, including the following:

- ECC memory and defective DIMM handling
- Memory test
- Fault resilient booting
- Logging of critical events
- Boot monitoring

13.5.1 Defective DIMM Detection and Memory Reconfiguration

Memory reconfiguration allows a DIMM that has generated a Multi-bit error (MBE) or a Memory Read/Write error to be excluded from the POST process and it remaps the memory access to another DIMM. If a DIMM is disabled, the entire DIMM bank will be unavailable (bank size is determined by the Memory Interleave). The effect of this is to reduce the amount of memory available to the system but to have the addresses of the available memory to be continguous.

If by disabling all failing DIMMs there would be no DIMMs left enabled in the system, the BIOS will display a POST error message and display the message “Press <F1> to resume, <F2> to enter setup” message instead of continuing POST. If the user chooses to continue, the BIOS will attempt to use only 64 MB of memory on one DIMM by setting the DRAM row boundary

[8] Note that the BIOS size may increase thereby limiting the area used by option ROMs to 0C0000h – 0E0000h.

[9] ISA-compatible ROM space is a limited resource. If more than 128KB of PCI option ROMs are in the system, some PCI option ROMs will not be shadowed or executed.

registers. The BIOS will continue through each DIMM bank until 64 MB of useable memory can be located. If the BIOS cannot locate a block of memory to use, the system will halt.

During POST, the BIOS sends a Get DIMM State command to the BMC to check the DIMM status. If the Memory Retest option is selected in BIOS Setup, the BIOS will send a ReArm DIMMs command to the BMC. This will cause the BMC to clear the failure state of all DIMMs. See Section 15.1.3.2: Advanced Menu Selections, for details on how this is to be presented in BIOS Setup.

13.5.1.1 BIOS Behavior

- The BIOS will configure and test system memory. Any errors generated during this phase will be detected by the BIOS.
- The BIOS will configure the memory subsystem to enable BMC notification of memory errors.
- The BIOS will enable BMC memory error monitoring when memory testing has completed, at which point the BMC will start monitoring memory errors.
- The BIOS will synchronize with the BMC for access to the SMBus.
- The BIOS will use BMC stored DIMM failure and disabled states to determine if a DIMM should be disabled.

13.5.1.2 Memory Error Handling

The BMC is responsible for monitoring and logging memory errors. The BIOS configures the hardware to notify the BMC on single-bit and multi-bit memory errors. The BMC will query the hardware for error information when notified of an error.

Correctable and uncorrectable memory errors cause a BMC input signal to generate a BMC interrupt. The BMC then reads the current memory error state from the memory controller via the I^2C bus and generates IPMI sensor events.

Correctable memory errors are invisible to the BIOS and the operating system. The BMC will count the number of correctable memory error that occur on each DIMM over time. If more than ten errors occurs on a DIMM within an hour, an Event Logging Disabled event will be generated and logging of correctable errors on that DIMM will be stopped until the next reset or power-on.

If the BMC detects an uncorrectable error, it will generate an Uncorrectable ECC event against the memory sensor and set the failed offset in the associated DIMM sensor (if a failing DIMM can be determined).

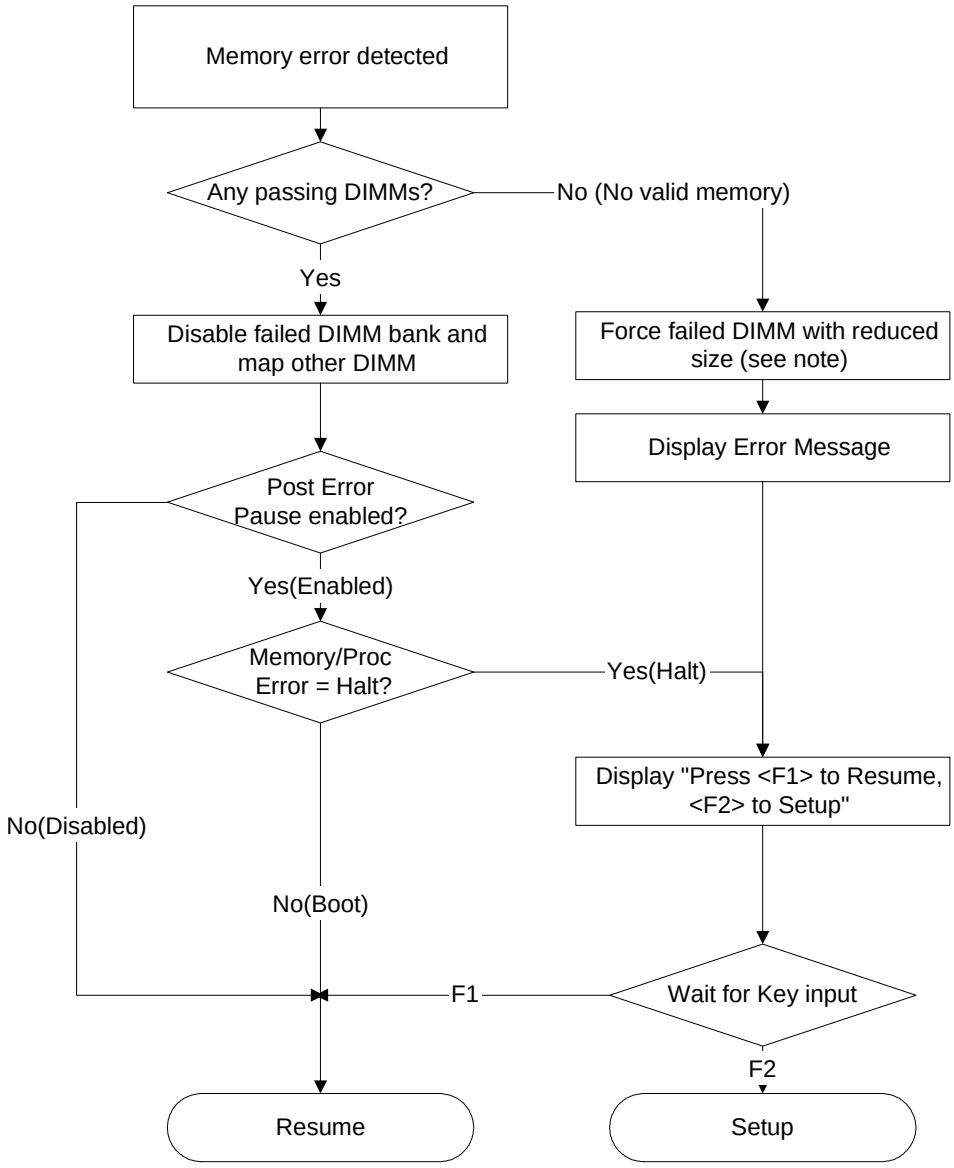

Figure 26. Memory Reconfiguration Flow Chart

Notes:

- POST halts at POST code 28h when there are no DIMMs or BIOS does not read any SPD data on DIMMs. In this case, speaker beeps are generated. (see Table 77)
- POST halts at POST code 2Ch when the 512 KB memory test fails. In this case, speaker beeps are generated. (see see Table 77)
- If all DIMMs are reconfigured by memory error, POST proceeds to the following steps:
    1. Enable the available DIMM which has least significant number. Usually DIMM0 will be selected at first.
    2. Examine default minimum size (512MB) of memory
    3. If step 2 passes successfully, POST displays a message that indicates F1 is the hot key to force a boot. If the user presses the F1 key, then BIOS tries to boot. If step 2 failed, POST stores in CMOS that this DIMM is unusable. When POST returns to step 1, this DIMM will be not used.
    4. If all DIMMs are marked unusable, the system halts and beeps (See Table 77).

13.5.2 Memory Test

The base memory test is performed before video initialization and covers the first 8 MB of memory. The extended memory test covers the remaining memory and is performed after video initialization. Note that the entire ECC memory is always initialized during POST.

13.5.3 Fault Resilient Booting (FRB)

Fault resilient booting (FRB) is a set of BIOS and BMC algorithms and hardware support that allow a multiprocessor system to boot in case of failure of the bootstrap processor (BSP) under certain conditions. There are three FRB timers; detailed explanation of the different FRB timers can be found in the following sections. The FRB algorithm detects BSP failure and takes steps to disable that processor and reset the system so another processor will run as the BSP. The BMC relies on BIOS to assert the FRB timer halt signal to indicate that the system has successfully started executing code.

The BMC is responsible for retaining non-volatile FRB-3 history and the disable status for each processor. This history tracks whether the processor has failed FRB-3 at least once before and whether the BIOS has disabled the processor. Some of the other processor status sensors also have their values stored in non-volatile memory. Non-volatile sensor offsets retain their values across system AC power cycles.

When the BMC detects that a processor socket/slot inventory state has changed (e.g., empty/terminated slot, new processor), the BMC clears the processor status sensor state and enables / disables the processor as appropriate.

If the BMC detects a processor-related hardware configuration error, it produces a beep code through the system speaker and will not power the system on.

In a multiprocessor system, the BIOS registers the application processors in the MP table and in the ACPI APIC tables. If an application processor fails to complete initialization within a certain time upon being started by the BSP, it is assumed to be nonfunctional. If the BIOS detects that an application processor has failed FRB-1 or is nonfunctional, it requests the BMC to disable the processor.

The BMC then generates a system reset while disabling the processor. The BIOS will not see the failed processor on the next boot. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification,* Rev. 1.4) nor in the ACPI APIC tables, and is invisible to the OS.

13.5.3.1 FRB-3

FRB-3 refers to the FRB algorithm that detects whether the BSP is executing instructions. The FRB-3 timer is started when the system is powered up or hard reset. The BIOS stops this timer during POST by asserting the FRB-3 timer halt signal to the BMC. This requires that the BSP executes the BIOS code. If the timer is not stopped and it expires, the BMC disables the BSP, logs an FRB-3 error event, chooses another BSP (from the set of non-failed processors), and resets the system. This process repeats either until the system boots without an FRB-3 timeout, or until all of the remaining processors have been disabled. If all the processors have been disabled, the BMC will attempt to boot the system on one processor at a time, irrespective of processor error history. This is called Desperation Mode.

The BMC always starts the FRB-3 timer regardless of processor number.

The FRB-3 disable jumper located on the baseboard can disable FRB-3. The location of FRB-3 disable jumper is described in *Appendix A Jumper Locations*. The FRB-3 disable jumper should be available on the baseboard to aid in early BIOS debug.

13.5.3.2 FRB-2

FRB-2 refers to the level of FRB in which the BIOS uses the BMC watchdog timer to monitor its operation during POST. The BIOS configures the Watchdog Timer for approximately 6-10 minutes.

After the BIOS has identified the BSP and saved that information, it sets the Watchdog Timer FRB-2 timer use bit, loads the Watchdog Timer with the new timeout interval, and disables FRB-3 using the FRB-3 timer halt signal. This sequence ensures that no gap exists in Watchdog Timer coverage between FRB-3 and FRB-2.

If the Watchdog Timer expires, the BMC logs a watchdog expiration event showing an FRB-2 timeout. It then hard resets the system.

The BIOS is responsible for disabling the FRB-2 timeout before initiating the option ROM scan, prior to displaying a request for a boot password or prior to an extensive memory test. The BIOS will re-enable the FRB-2 timer after the extensive memory test. The BIOS provides a user-configurable option to change the FRB-2 response behavior. These three options shall be:

- Disable on FRB2
- Never Disable
- Disable after 3 consecutive FRB2

The option of “Disable on FRB2” will do the following: If the FRB-2 timer expires (in other words, a processor has failed FRB-2), the BMC resets the system. As part of its normal operation, the BIOS obtains the watchdog expiration status from the BMC. If this status shows an expiration of the FRB-2 timer, the BIOS logs an FRB-2 event with the event data being the last ASF Progress code or Post Code issued in the previous boot. The BIOS also issues a Set Processor State command to the BMC, telling it to disable the BSP and reset the system. The BMC then disables the processor that failed FRB-2 and resets the system, causing a different processor to become the BSP.

The option of “Never Disable” will perform all the same functions as “Disable on FRB2” with the exception that the BIOS will not send a Set Processor State command to the BMC. The BIOS will still log the FRB-2 event in the system event log.

The option of “Disable after 3 consecutive FRB2” will perform all the same functions as “Disable on FRB2” with the following exception: The BIOS maintains a failure history of the successive boots. If the same BSP fails three concecutive boots with an FRB-2, the processor is disabled. If the system successfully boots to a BSP, the failure history maintained by the BIOS is cleared.

13.5.3.3 FRB-1

FRB-1 is implemented by the BIOS to detect the failure of the BSP by examining a processor's built-in self test (BIST) results. If a BIST failure occurs, the BIOS records the event so it can be logged later. The BIOS then disables the processor by sending a Set Processor State command to the BMC.

In checking for a FRB-1 error, the BIOS does the following:

1. The BIOS reads the processor BIST results and determines if a failure occurred.

2. The BIOS saves the FRB-1 (BIST) failure status for the processor to CMOS.

3. The BIOS attempts to identify the BSP and force a switch to another processor as the BSP. This can be accomplished by sending a Set Processor State command to the BMC. If this is successful, the BIOS sends an FRB-1 (BIST) Failure event message to the BMC and stops the FRB-3 timer by asserting the FRB-3 timer halt signal. Otherwise, the FRB-3 timer times out.

4. BMC disables the processor and resets the system.

13.5.4 Boot Inhibit

After all POST tasks have finished but before booting the operating system, the BIOS checks the system temperature and voltage. If the temperature exceeds a limit value and / or if the system has an abnormal voltage, POST will display the message "Press <F1> to override boot suppression, <F2> to enter Setup". The BIOS will continue to poll the temperature sensor. If the sensor returns to the acceptable range, the POST process will automatically continue and will allow the operating system to boot. If the user presses <F2>, the system will enter SETUP. If user presses <F1>, the system will continue to boot.

13.5.4.1 Thermal Sensor

After all POST tasks have finished but before booting the operating system, the BIOS checks the system temperature. If the temperature exceeds lower or upper limit, POST will display the message "Press <F1> to override boot suppression, <F2> to enter Setup" and it polls the temperature sensor. If the temperature returns to normal, POST will resume automatically and boot the system. If the user presses <F2>, the system will enter SETUP. If user presses <F1>, the system will continue to boot. The Thermal Sensor option is enabled/disabled Setup (see Table 94). If Thermal Sensor is disabled in Setup, the BIOS will not check the temperature and will not halt the boot if the temperature thresholds are exceeded. If "POST Error Pause" is disabled in Setup, the system will continue to boot regardless of the Thermal Sensor setting or error state.

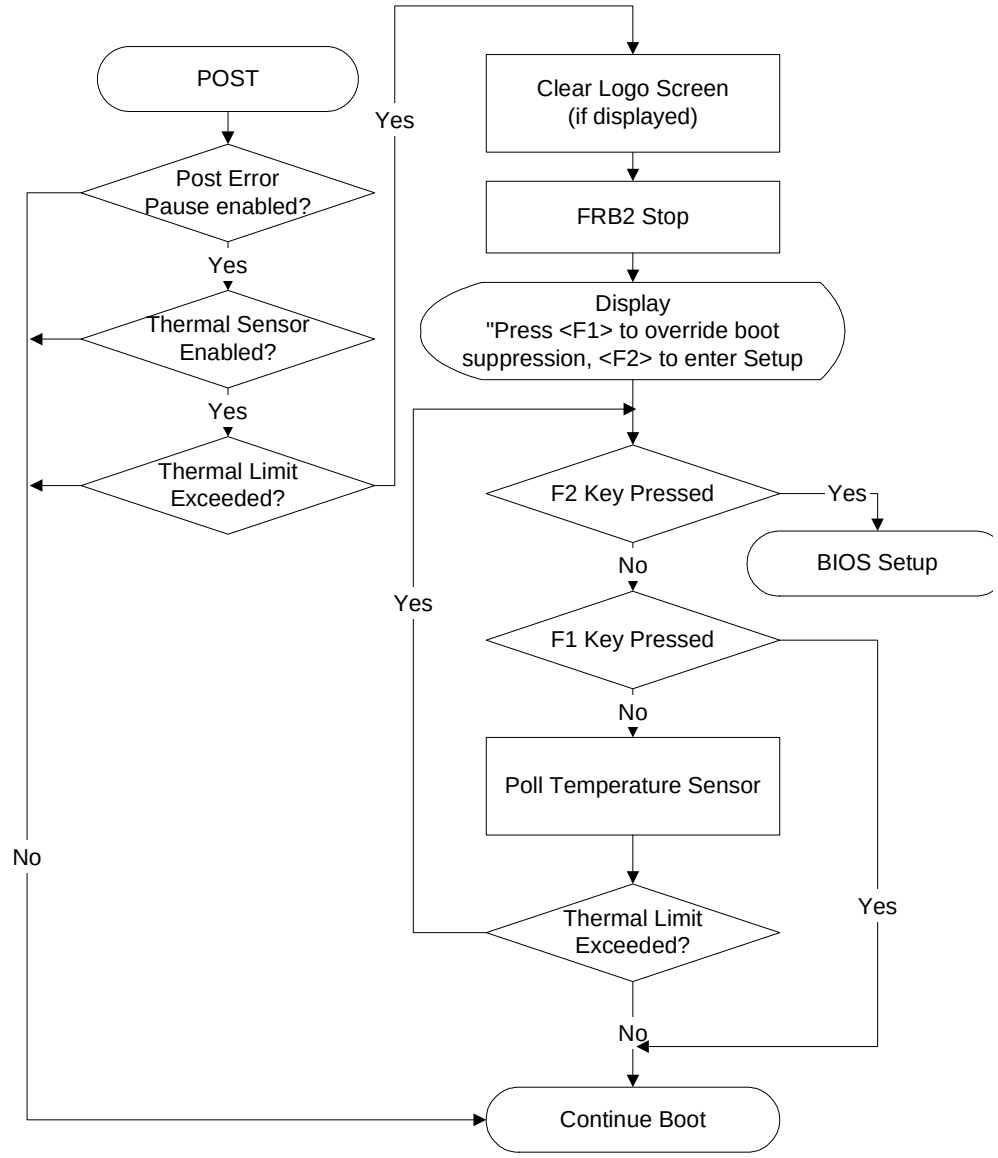

Figure 27. Thermal Sensor

13.5.4.2 Voltage Sensor

After all POST tasks are finished but before booting to the operating system, the BIOS checks the system voltages. If the voltage exceeds lower/upper limit and “POST Error Pause” is enabled in Setup, POST will display the message “Press <F1> to override boot suppression, or <F2> to enter Setup”. If the user presses <F2>, the BIOS will enter Setup. If the user presses <F1>, the BIOS will resume the POST process. If “POST Error Pause” is disabled in Setup, the BIOS does not monitor the system voltages and will not stop the boot process.

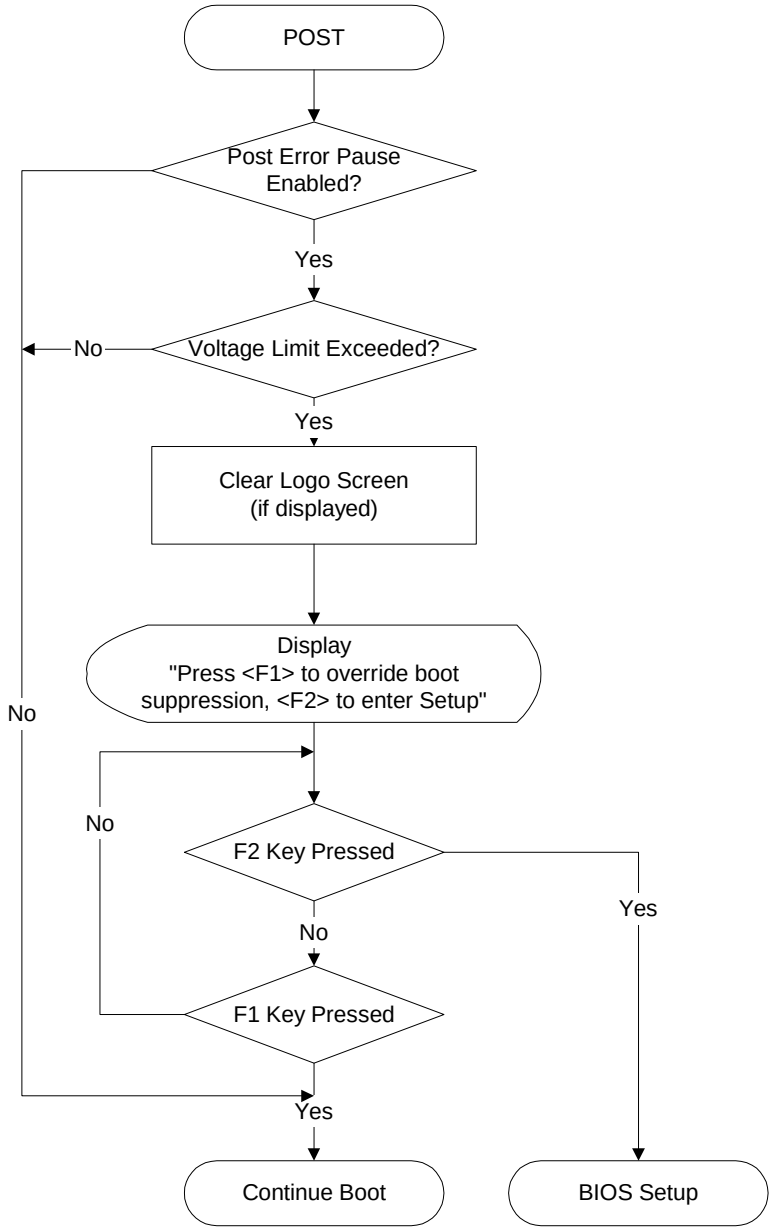

Figure 28. Voltage Sensor

13.6 Wired for Management (WFM)

Wired for Management (WFM) is an industry-wide initiative to increase overall manageability and reduce the total cost of ownership. WFM allows a server to be managed over a network. The BIOS sets up the SYSID table as described in the *Network PC System Design Guidelines, Revision 1.0*. This table contains the globally unique ID (GUID) of the baseboard.

13.6.1 System Management BIOS (SMBIOS)

The BIOS provides the SMBIOS structures via a table-based method. The table convention, provided as an alternative to the calling interface, allows the SMBIOS structures to be accessed under 32-bit protected-mode operating systems such as Windows* NT*. This convention provides a searchable entry point structure that contains a pointer to the packed SMBIOS structures residing somewhere in 32-bit physical address space.

Application software can locate the SMBIOS entry-point structure described below by searching for the anchor-string on paragraph (16-byte) boundaries within the physical memory address range 000F0000h to 000FFFFFh. This entry point encapsulates an intermediate anchor string, which is used by some existing DMI browsers.

The total number of structures can be obtained from the SMBIOS entry-point structure. The system information is presented to an application as a set of structures that are obtained by traversing the SMBIOS structure table referenced by the SMBIOS entry-point structure. The following table describes the types of SMBIOS structures supported by the BIOS:

Table 63. SMBIOS Header Structure

Structure Type	Supported?	Comments
BIOS Information (Type 0)	Yes	One record for the system BIOS. SMBIOS 2.3 does not allow the use of type 0 records to describe the option ROMs.
System Information (Type 1)	Yes	
Baseboard Information (Type 2)	Yes	Shasta has three records; Server board, Memory board and processor board.
Chassis Information (Type 3)	Yes	
Processor Information (Type 4)	Yes	One for every processor socket.
Memory Controller Information (Type 5)	No	
Memory Module Information (Type 6)	No	
Cache Information (Type 7)	Yes	One record for each level of cache for every processor. One record describes L1 cache and the second one describes L2 cache and the third one describes L3 cache. The disabled bit in the cache configuration field is set if the corresponding processor is absent or disabled.
Port Connector Information (Type 8)	Yes	Describes all internal and external baseboard connectors including IDE, floppy, SCSI, keyboard, mouse, COM ports, parallel port, USB port, Network, ICMB, video, etc.
System Slots (Type 9)	Yes	One record for each PCI slot. Also includes memory module slots.
On-board Device Configuration (Type 10)	Yes	One for each on-board device, i.e. SCSI controller, video controller, and Lan controllers.
OEM Strings (Type 11)	Yes	Comes from OEM GPNV area. This area can be re-written by the OEM. The HWID is stored in this location.
System Configuration Options (Type 12)	Yes	Describes the baseboard jumper settings.

Structure Type	Supported?	Comments
BIOS Language Information (Type 13)	Yes	Use “ISO 639 Language Name | ISO 3166 Territory Name | Encoding Method”. Supported languages is English, French, German, Spanish, Italian.
Group Association (Type 14)	No	
Event Log (Type 15)	No	
Physical Memory Array (Type 16)	Yes	Offset 0Bh contains either 0FFFFh(if no error was detected) or the handle of the error information structure(Type18). Offset 0Dh should contain the number of memory device slots in the system.
Memory Device (Type 17)	Yes	One record for each memory device slot. DIMM capacity is reported as a function of the physical capacity rather than the current configured capacity. No support for mapping out bad memory.
Memory Error Information (Type 18)	Yes	One record for each memory device slot. Error Type, Error Granularity and Error operation are set to “Unknown” for unpopulated memory device slots.
Memory Array Mapped Addresses (Type 19)	Yes	The field “Partition Width” is set equal to the number of DIMMs that comprise a bank. I.e. the interleave.
Memory Device Mapped Addresses (Type 20)	Yes	One structure for each memory device slot.
Built-in Pointing Devices (Type 21)	No	
Portable Battery (Type 22)	No	
System Reset (Type 23)	No	
Hardware Security (Type 24)	Yes	Dynamically set to match current BIOS and BMC security settings.
Probe Information (Type 26-29, 34-36)	No	
Out-of-band Remote Access (Type 30)	No	
BIS Entry Point (Type 31)	Yes	
System Boot Information (Type 32)	Yes	Boot Status field is linked to Bootup State Field in Type 3 structure.
64-bit Memory Error Information (Type 33)	No	
IPMI Device Information (Type 38)	Yes	BMC interrupt type is set in this structure.
Structure Not In Effect (Type 126)	Optional	Indicates software should ignore this structure.
End of Table (Type 127)	Yes	Indicate end of table.

Table 64. System Information (Type 1)

Offset	Name	Length	Value	Description
00h	Type	BYTE	1	Component ID Information Indicator
01h	Length	BYTE	19h	
02h	Handle	WORD	Varies	
04h	Manufacturer	BYTE	String	Number of Null terminated string. Comes from FRU Field “Product Manufacturer”.
05h	Product Name	BYTE	String	Number of Null terminated string. Comes from FRU Field “Product Name” and “Product Part Number”.
06h	Version	BYTE	String	Number of Null terminated string. Comes from FRU Field “Product Version”.
07h	Serial Number	BYTE	String	Number of Null terminated string. Comes from FRU Field “Product Serial Number”.
08h	UUID	16 BYTEs	Varies	From value stored in FLASH or from ID generated at boot time..
18h	Wake-up type	BYTE	ENUM	See SMBIOS 2.3 Spec section 3.3.2.1 for meaning.

Table 65. Base Board Information (Type 2)

Offset	Name	Length	Value	Description
00h	Type	BYTE	2	Base Board Information Indicator
01h	Length	BYTE	08h	
02h	Handle	WORD	Varies	
04h	Manufacturer	BYTE	String	Number of Null terminated string. Comes from FRU Field “Board Manufacturer”.
05h	Product	BYTE	String	Number of Null terminated string. Comes from FRU Field “Board Product Name”.
06h	Version	BYTE	String	Number of Null terminated string. Comes from FRU Field “Board Version”.
07h	Serial Number	BYTE	String	Number of Null terminated string. Comes from FRU Field “Board Serial Number”.

Table 66. System Chassis or Enclosure (Type 3)

Offset	Name	Length	Value	Description
00h	Type	BYTE	3	System Enclosure Indicator
01h	Length	BYTE	09h	No OEM-defined
02h	Handle	WORD	Varies	
04h	Manufacturer	BYTE	String	Number of Null terminated String.
05h	Chassis Type	BYTE	Varies	Bit 7: 1 – Chassis lock present. 0 - Lock not present or unknown Bits 6:0 – See SMBIOS 2.3 Section 3.3.4.1 Chassis Type info comes from FRU Field “Chassis Type” and “Chassis Characteristics”.
06h	Version	BYTE	String	Number of Null terminated string. Comes from FRU Field “Chassis Part Number / Code”.
07h	Serial Number	BYTE	String	Number of Null terminated string. Comes from FRU Field “Chassis Serial Number”.
08h	Asset Tag Number	BYTE	String	Number of Null terminated string. Comes from FRU Field “Product Asset Tag”.
09h	Bootup State	BYTE	ENUM	See SMBIOS 3.3.4.2
0Ah	Power Supply State	BYTE	ENUM	See SMBIOS 3.3.4.2
0Bh	Thermal State	BYTE	ENUM	See SMBIOS 3.3.4.2
0Ch	Security Status	BYTE	ENUM	See SMBIOS 3.3.4.2

13.6.2 UUID

The utility generates the UUID that complies with the requirements set forth in *Wired For Management Baseline Specification*, Version 2.0. The UUID is stored in the BMC NVRAM area.

13.7 Post Memory Manager

The POST Memory Manager specification allows external clients, such as option ROMs, to request memory buffer during initialization and release it later. Without the POST memory manager, the option ROMs may destroy buffers used by the system BIOS or other clients.

13.8 ACPI

The primary role of the ACPI BIOS is to supply the ACPI tables. POST initializes the ACPI tables and relocates them to extended memory. INT 15h, function E820h reports memory that is used by the ACPI BIOS as reserved. An ACPI aware OS generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by sending the appropriate command to the BMC to enable ACPI mode. The system automatically returns to legacy mode upon hard reset or power-on reset.

There are three run time components to ACPI:

- **ACPI Tables:** These tables describe the interfaces to the hardware. ACPI tables can make use of a p-code type of language, the interpretation of which is performed by the OS. The OS contains and uses an ACPI machine language (AML) interpreter that executes procedures encoded in AML and stored in the ACPI tables; AML is a compact, tokenized, abstract machine language. The tables contain information about power management capabilities of the system, APIC information, and bus structure. The tables also describe control methods that the OS uses to change PCI interrupt routing, enable/disable devices in server I/O, and find out the cause of a wakeup event.
- **ACPI Registers:** The ACPI registers are the constrained part of the hardware interface, described (at least in location) by the ACPI tables.
- **ACPI BIOS:** This code boots the machine and implements interfaces for sleep, wake, and some restart operations. The ACPI Description Tables also are provided by the ACPI BIOS.

The SSH4 baseboard supports the S0, S1, S4, and S5 states. The behavior and valid wakeup sources of each sleep state are defined in the ACPI specification. When the system is operating in ACPI mode, the OS retains control of the system and OS policy determines the entry methods and wakeup sources for each sleep state. Sleep entry and wakeup sources are not controlled by the BIOS on an ACPI-enabled system.

The ASL supports the following ASL functions.

- Use the _PTS method to notify the EC of sleep state changes
- The BIOS sets the sleep button as a wake event in the BMC
- COM2 can be enabled/disabled based on the results of the device check function
- Supports the thermal zone which implements the critical trip point

13.8.1 Front Panel Switches

The SSH4 baseboard supports up to five front panel buttons: power, reset, sleep, NMI, and ID. Since a sleep button may not be present on a specific front panel design, the BIOS provides a setup option (see Table 91) to configure the system accordingly. The BIOS updates the ACPI tables to indicate the presence or absence of sleep button. Removal of the sleep button feature does not prevent an ACPI OS from entering a sleep state.

The power button on the chassis is a request that is forwarded by the BMC to the power state machines in the National Semiconductor* PC87417 Super I/O (SIO.) It is monitored by the BMC and does not directly control power on the power supply.

The power button and the sleep button behave differently, depending on whether the operating system supports ACPI. The sleep switch has no effect unless an operating system with ACPI support is running. If the operating system supports ACPI and the system is running, pressing the sleep switch causes an event. The operating system causes the system to transition to the appropriate system state, depending on the user settings.

Power Switch Off to On: The CSB5 and SIO may be configured to generate wakeup events for several different system events: Wake on LAN*, PCI Power Management Interrupt, and

Real Time Clock Alarm are examples of these events. The BMC monitors the power button and wakeup event signals from the SIO. A transition results in the BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The SIO receives power good and reset from the BMC and then transition to an ON state.

On to Off (Legacy): The SIO is configured to generate an SMI due to a power button event. The BIOS services this SMI and sets the state of the machine in the CSB5 and SIO to the OFF state. The BMC monitors power state signals from the SIO and deasserts PS_PWR_ON to the power supply.

On to Off (ACPI): If an ACPI operating system is loaded, the power button switch generates a request (via SCI) to the OS to shutdown the system. The OS retains control of the system and OS policy determines into which sleep state (if any) the system transitions.

On to Sleep (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a request via *System Control Interrupt* (SCI) to the OS to place the system in “sleep” mode. The OS retains control of the system and OS policy determines into which sleep state (if any) the system transitions.

Sleep to On (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a wake event to the CSB5 and a request (via SCI) to the OS to place the system in the “On” state. The OS retains control of the system and OS policy determines from which sleep state (if any) the system can wake.

13.8.2 Legacy Wakeup Features

The BIOS is also capable of configuring the system to wake up from several sources under a non-ACPI configuration, such as when the operating system does not support ACPI. The wakeup sources are the same as the ones specified in *Section 2.7.1: Front Panel Switches*. Under ACPI, the operating system programs the CSB5 and SIO to wake up on the desired event, but in legacy mode the BIOS enables / disables wakeup sources based on a switch in Setup. It is required that the operating system or a driver clear any pending wakeup status bits in the associated hardware (such as the Wake on LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI power management event (PME) status bit in a PCI device). The BIOS enables and clears the PME# functionality of the on-board NIC (no driver required.) The legacy wakeup feature is disabled by default.

Table 67. Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported via Legacy Wake
Power Button	Always wakes system	Always wakes system
Sleep Button	S1	No
Ring indicate from COMA	S1, S4	Yes
Ring indicate from COMB	S1, S4	Yes
PME from PCI 32/33	S1, S4	Yes
PME from Onboard NICs	S1, S4	Yes

Wake Event	Supported via ACPI (by sleep state)	Supported via Legacy Wake
PME from add-in NIC	S1, S4	Yes
RTC Alarm	S1, S4	Yes
Mouse	S1	No
Keyboard	S1	No
USB	S1	No

13.9 OEM Customization

System OEMs can differentiate their products by customizing the BIOS. The extent of customization is limited to that what is stated in this section.

The user binary capability of the system BIOS allows system vendors to change the look and feel of BIOS and to manage OEM-specific hardware by executing custom code during POST. Custom code should not hook critical interrupts, reprogram the chipset, or take any other action that affects the correct functioning of system BIOS.

13.9.1 User-supplied BIOS Code Support

A 16 KB region of flash ROM is available to store a user binary. The iFlash utility allows the OEM or end user to update the user binary region with OEM supplied code and/or data. At several points throughout POST, control is passed to this user binary. Intel provides tools and reference code to help OEMs create a user binary. The user binary must adhere to the following requirements:

1. To allow detection by BIOS and protection from run time memory managers, the user binary must have an option ROM header (i.e., 55AAh, size).

2. The system BIOS performs a scan of the user binary area at predefined points during POST. Mask bits must be set within the user binary to inform the BIOS which entry points exist.

3. System state must be preserved by the user binary (all registers, including extended and Intel® MMX™ technology, stack contents, and nonuser binary data space, etc.).

4. The user binary code must be relocatable. The user binary is located within the first 1 MB of memory. The user binary code must not make any assumptions about the value of the code segment.

5. The user binary code is always executed from RAM and never from flash.

6. The user binary must not hook critical interrupts, must not reprogram the chip set, and must not take any action that affects the correct functioning of the system BIOS.

7. The user binary ROM must be checksummed. The checksum byte must be placed in the last byte position of the 16 KB ROM.

The BIOS copies the user binary into system memory before the first scan point. If the user binary reports that it does not contain run time code, it is located in conventional memory (0-640 KB). Reporting that the user binary has no run time code has the advantage of not using limited option ROM space (therefore, more option ROMs may be executed in a large system configuration). If user binary code is required at run time, it is copied into and executed from option ROM space (0C8000H – 0E7fffH). At each scan point during POST, the system BIOS determines if the scan point has a corresponding user binary entry point to transfer control to the user binary. Presence of a valid entry point in the user binary is determined by examining the bitmap at byte 4 of the user binary header; each entry point has a corresponding “presence” bit in this bitmap. If the bitmap has the appropriate bit set, an entry point ID is placed in the “AL” register and execution is passed to the address computed by (ADR(Byte 5)+5*scan sequence #).

During execution, the user binary may access 11 bytes of extended BIOS data area RAM (EBDA). The segment of EBDA can be found at address 40:0e. Offset 18h through offset 22h is available for the user binary. The BIOS also reserves 8 CMOS bits for the user binary. These bits are in an unchecksummed region of CMOS with default values of zero, and is always be located in the first bank of CMOS. These bits are contiguous, but are not in a fixed location. Upon entry into the user binary, DX contains a ‘token’ that points to the reserved bits. This token is of the following format:

MSB LSB

15			12	11											0
# of bit available –1				Bit offset from start of CMOS of first bit											

The most significant four bits are equal to the number of CMOS bits available minus one. This field is equal to seven, since there are eight CMOS bits available. The 12 least significant bits define the position of the CMOS bit in the real-time clock (RTC). This is a bit address rather than a byte address. The CMOS byte location is 1/8th of the 12-bit number, and the remainder is the starting bit position within that byte. For example, if the 12-bit number is 0109h, user binary can use bit 1 of CMOS byte 0108h/8 or 021h. It should be noted that the bits available to the user binary may span more than one byte of CMOS (i.e., a value of 07084h indicates that the upper nibble of byte 10h and the lower nibble of byte 11h are reserved for the user binary).

The following code fragment shows the header and format for a user binary:

```
            db     55h, 0AAh, 20h      ; 16 KB USER Area

MyCode      PROC   FAR                 ; MUST be a FAR procedure
            db     CBh                 ; Far return instruction
                                       ;
            db     04h                 ; Bit map to define call points, a 1
                                       ; in any bit specifies
                                       ; that the BIOS is called at that
                                       ; scan point in POST
            db     CBh                 ; First transfer address used to
                                       ; point to user binary extension
                                       ; structure
            dw     ?                   ; Word Pointer to extension
                                       ; structure
            dw     0                   ; Reserved
```

```
JMP    ErrRet              ; This is a list of 7 transfer
                           ; addresses, one for each
JMP    ErrRet              ; bit in the bitmap.
                           ; 5 Bytes must be used for each
JMP    Start               ; JMP to maintain proper offset for
                           ; each entry. Unused entry JMP's
                           ; should be filled with 5 byte
                           ; filler or JMP to a RETF
JMP    ErrRet              ;
JMP    ErrRet
JMP    ErrRet
JMP    ErrRet
```

13.9.1.1 Scan Point Definitions

The table below defines the bitmap for each scan point, indicating when the scan point occurs and which resources are available (RAM, stack, binary data area, video, and keyboard).

Table 68. User Binary Area Scan Point Definitions

Scan Point	Mask	RAM / Stack / BDA	Video / Keyboard
Near pointer to the user binary extension structure, mask bit is 0 if this structure is not present. Instead of a jump instruction the scan address (offset 5) contains an 0CB followed by a near pointer.	01h	N/A	N/A
Obsolete. No action taken.	02h	NA	NA
This scan occurs immediately after video initialization.	04h	Yes	Yes
This scan occurs immediately before video initialization.	08h	Yes	No
This scan occurs on POST error. On entry, BX contains the number of the POST error.	10h	Yes	Yes
This final scan occurs immediately prior to the INT 19 for normal boot and allows one to completely circumvent the normal INT 19 boot if desired.	20h	Yes	Yes
This scan occurs immediately before the normal option ROM scan.	40h	Yes	Yes
This scan occurs immediately following the option ROM area scan.	80h	Yes	Yes

Table 69. Format of the User Binary Information Structure

Offset	Bit Definition
0	Bit 0 = 1 if mandatory user binary, 0 if not mandatory. If a user binary is mandatory, it will always be executed. If a platform supports a disabling of the user binary scan through Setup, this bit overrides the Setup setting. Bit 1= 1 if runtime presence required (other than SMM user binary portion, SMM user binary will always be present in runtime irrespective of setting of this bit). 0, if not required in runtime, and can be discarded at boot time. Bit 7:2 – reserved for future expansion.
1 - 0fh	Reserved for future expansion.

If this structure is not present (bit 0 of the scan point structure is not set), the system BIOS assumes that the user binary is not mandatory (bit 0 in User Binary Information Structure assumed cleared), and it is required in run time (bit 1 in User Binary Information Structure assumed set).

13.9.2 OEM Logo Screen

A 128 KB region of Flash ROM is available to store the OEM logo in compressed format. The BIOS contains the standard Intel logo. Using the iFlash utility, this region can be updated with OEM supplied logo image. The OEM logo must fit within 640 X 384 size. If an OEM logo is flashed into the system, it overrides the built in Intel logo. A file is included with the BIOS update to restore the default logo.

13.10 Serial Console Redirection

The BIOS supports redirection of both video and keyboard through a serial link on either of the physical serial ports in the system. On COM2, the BIOS supports baud rate settings as specified by the BMC. When console redirection is enabled, local (Host Server) keyboard input and video output is passed both to the local keyboard and video connections, and to the remote console through the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Setup and any other text-based utilities can be accessed via console redirection until the system is switched to protected mode or an extended memory manager is loaded.

13.10.1 Operation

When redirecting through a modem (as opposed to a Null modem cable), the modem needs to be configured with the following:

- Auto-answer (for example, ATS0=2, to answer after two rings) if emergency management port is not enabled on the COM port that is used by redirection.
- Modem reaction to DTR set to return to command state (for example, AT&D1). Failure to provide this causes the modem to either drop the link when the Server reboots (as in AT&D0), or make the modem unresponsive to Server baud rate changes (as in AT&D2).

The Setup option for handshaking must be set to CTS/RTS + CD for optimum performance. (CD = Carrier Detect.) If emergency management port is sharing the COM port with serial redirection, the handshaking must be set to CTS/RTS + CD. In selecting this form of handshaking, the server is prevented from sending video updates to a modem that is not connected to a remote modem. If this is not selected, video update data being sent to the modem inhibits many modems from answering an incoming call. Carrier Detect should not be used if a modem is not used and the Carrier Detect line is not connected.

Once console redirection is selected in Setup, redirection is loaded into memory and activated during POST. Although redirection cannot be “removed” without rebooting, it can be inhibited and restarted. When inhibited, the serial port is released from redirection and it can be used by another application. Restarting reclaims the serial port and continues redirection.

Inhibiting or restarting is accomplished through the following INT 16h mechanism. The standard INT 16h (Keyboard handler) function AH=05h places a keystroke in the key buffer, just as if an actual key had been pressed. Keystrokes buffered in this way are examined by redirection, and if a valid command string has been sent, it is executed. The following commands are supported in this fashion:

- Esc-CDZ0 Inhibit Console Redirection
- Esc-CDZ1 Restart Console Redirection

In order to inhibit redirection, the software must call INT 16h, function AH=05h five times to place the five keys into the key buffer. Keystrokes sent to the INT 16h buffers to invoke a command are buffered, and is removed through the normal INT 16h calls to prevent these keystrokes from being passed on to another application.

13.10.2 Keystroke Mappings

During console redirection, the remote terminal (which may be a dumb terminal or a system with a modem running a communication program, such as ProComm) sends keystrokes to the local server. The local server passes video back over this same link. For keys that have an ASCII mapping, such as A and Ctrl-A, the remote sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote terminal must send a string of characters, as defined in the tables below. The strings are based on the ANSI terminal standards. Since the ANSI terminal standard does not define all the keys on the standard 101 key U.S. keyboard, mappings for these keys were created, such as F5 – F12, Page Up, and Page Down.

Alt key combinations are created by sending the combination ^[} followed by the character to be alt modified. Once this Alt key combination is sent (^[}), the next keystroke sent will be translated into its alt-key mapping (that is, if ^[} is mapped to Shift-F1, then pressing Shift-F1 followed by ‘a’ would send an Alt-a to the server). The remote terminal can force a refresh of its video by sending ^[{.

Unusual combinations outside of the ANSI mapping and not in the table below, are not supported (for example, Ctrl-F1).

Table 70. Non-ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
ESC	^[	NS	NS	NS
F1	^[OP	NS	NS	NS
F2	^[OQ	NS	NS	NS
F3	^[OR	NS	NS	NS
F4	^[OS	NS	NS	NS
F5	^[OT	NS	NS	NS
F6	^[OU	NS	NS	NS
F7	^[OV	NS	NS	NS
F8	^[OW	NS	NS	NS
F9	^[OX	NS	NS	NS
F10	^[OY	NS	NS	NS
F11	^[OZ	NS	NS	NS

Key	Normal	Shift	Ctrl	Alt
F12	^[O1	NS	NS	NS
Print Screen	NS	NS	NS	NS
Scroll Lock	NS	NS	NS	NS
Pause	NS	NS	NS	NS
Insert	^[[L	NS	NS	NS
Delete	(7Fh)	NS	NS	NS
Home	^[[H	NS	NS	NS
End	^[[K	NS	NS	NS
Pg Up	^[[M	NS	NS	NS
Pg Down	^[[2J	NS	NS	NS
Up Arrow	^[[A	NS	NS	NS
Down Arrow	^[[B	NS	NS	NS
Right Arrow	^[[C	NS	NS	NS
Left Arrow	^[[D	NS	NS	NS
Tab	(09h)	NS	NS	NS

NS = Not supported
(xxh) = ASCII character xx

Table 71. ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
Backspace	(08h)	(08h)	(7Fh)	^[](08h)
(accent) `	`	(tilda) ~	NS	^[]`
1	1	!	NS	^[]1
2	2	@	NS	^[]2
3	3	#	NS	^[]3
4	4	$	NS	^[]4
5	5	%	NS	^[]5
6	6	^	NS	^[]6
7	7	&	NS	^[]7
8	8	*	NS	^[]8
9	9	(	NS	^[]9
0	0	)	NS	^[]0
(dash) -	-	(under) _	(1Fh)	^[]-
=	=	+	NS	^[]=
a to z	a to z	A to Z	(01h) to (1Ah)	^[]a to ^[]z
[	[	{	(1Bh)	^[]{
]	]	}	(1Dh)	^[]]
\	\	|	(1Ch)	^[]\
(semi-colon) ;	;	(colon) :	NS	^[];
(apostrophe) '	‘	(quote) "	NS	^[]'
(comma) ,	,	<	NS	^[],
(period) .	.	>	NS	^[].
/	/	?	NS	^[]/
(space)	(20h)	(20h)	(20h)	^[](20h)

NS = Not supported
(xxh) = ASCII character xx

13.10.3 Limitations

Console redirection is a real mode BIOS extension and only operates in real mode. Console redirection does not work once the OS or a driver such as EMM386* takes the processor into protected mode. Video is redirected by scanning and sending changes in text video memory. Thus, console redirection is unable to redirect video in graphics mode. Keyboard redirection functions via the BIOS INT 16h handler. Software bypassing this handler does not receive redirected keystrokes.

13.10.4 Console Redirection Menu Synchronization with BMC

The communication parameters for console redirection are synchronized between BIOS and BMC. The BIOS uses IPMI 1.5 serial/Modem configuration commands for this purpose.

13.10.4.1 BMC to BIOS Setup

The BIOS reads the BMC communication parameters at the beginning of POST. The parameters are copied to the corresponding CMOS items. When “COM2 port” bits show “no use” in BMC emergency management port information area, the BIOS does not copy the communication parameters to CMOS.

13.10.4.2 BIOS Setup to BMC

The BIOS saves the communication parameters to BMC when CMOS is updated (when exiting Setup and saving changes). BIOS controls whether or not the communication parameters are saved into the BMC based on the COM2 port settings. When the “COM2 port” bits shows “no use”, the BIOS does not save the parameters to the BMC emergency management port information area.

13.11 LAN Console Redirection

LAN console redirection uses the UDP/IP protocol connection-less packets to connect to the remote side. The Host machine will use DHCP to either discover an IP address for itself or it can use information stored in the BMC for this purpose. Protocols used include DHCP, ARP and UDP. The state of LAN redirection after INT19h can be controlled by sending an ‘Open’ or ‘Close’ command early in POST but after redirection is established. The current default behavior is to send the ‘Close’ command.

LAN Console redirection should not inhibit the ability to boot to a PXE server while redirection is occurring. During a LAN Console session, the system shall support the ability to remotely boot from a floppy over the LAN. The BIOS will query the BMC and find out if a remote DPC session is in place. If yes, then the BIOS will find out which NIC was being used for the DPC session (BMC has the info). LAN console redirection is only supported on one NIC at a time, so BIOS disables the other NIC from doing LAN console redirection.

13.12 Service Partition Boot

The BIOS supports a service partition boot. The service partition is installed as a separate file system partition on one of the local hard drives. It hosts the DOS operating system and Diagnostics agents and tests. The service partition can communicate with the remote console applications, and it can transfer files between the service partition over LAN, serial port, or a modem. The BIOS provides setup options for setting up the Service Partition Type (default: 12h).

A service partition boot can be initiated by three methods:

- A remote agent can direct BMC firmware to set the service partition boot request and reboot the system
- A local user can directed the BIOS to perform a one-time boot from the service partition
- Three unsuccessful operating system boots occur in a series

A service partition boot is attempted once per request. The service partition boot option is disabled upon each boot attempt. During POST, the system BIOS checks for a service partition boot request. On finding a boot request, the system will search for the Service Partition Type, starting from the highest disk number in the scan order. If a service partition was found, then the system will boot from that partition.

The drive numbers of all other drives will be incremented by one, except for the drive that has a scan order that is higher than the Service partition drive.

The BIOS will implement the service partition boot flag in BMC as specified by IPMI 1.5. IPMI 1.5 defines flags for requesting scan of the service partition and requesting service partition boot.

Before attempting to boot from a service partition, the BIOS will set the BMC watchdog timer. This timer will be disabled upon booting of the service partition by an application. If the system hangs on booting, a reset will bring system out of the service partition boot. An error will be logged upon failed service partition boot. If the service partition boot is not successful, BIOS re-tries it three times.

The BIOS will also start serial console redirection on COM2 for a Diagnostic boot. Any reboot after a Diagnostic Boot will revert the serial console redirection to the previous settings. For example, if console redirection was turned off before the service boot, it will revert to disabled.

The BIOS supports invoking the service partition boot via F4 hot key during POST. The hot-key message will be displayed indicating that this option is available when a service partition is installed. If the service partition boot is invoked by F4 key and an administrator password is set, the BIOS will check for that password before booting to service partition. If the service partition boot is invoked from remote console, no password check is needed because the remote console has already checked the password. If the ’password on boot’ feature is enabled, and the user password is set, but admin password is not set, the BIOS will check the user password.

13.13Warm Reset Processing

The system BIOS processes all resets as cold resets.

13.14 Hot Key

The system BIOS supports the following hot keys during the POST process.

- F1 Resume after POST error display
- F2 Enter BIOS Setup
- F4 Service Partition boot
- F12 PXE Boot
- Space Skip memory test
- ESC Clear Boot Logo, if enabled. Also display Multiboot Menu at the end of POST.

13.15 HWID

The system BIOS has the following unique ID referred to as the HWID. This ID is hardcoded into BIOS and stored in Type 11 SMBIOS structure.

- SSH4 HWID (Intel® Chassis SR7100): 0258h
- SSH4 HWID (Intel® Chassis SR4100):028Eh

13.16 Localization

The BIOS supports multiple languages to address various geographies. The BIOS support English, Spanish, French, German and Italian. The language can be selected using BIOS Setup.

13.17 BMC Initialization

13.17.1 BMC Self Test

The BIOS checks the status of the BMC Self Test results as early as possible during POST to verify that the BMC is functional. Additionally, the BIOS checks the status of the BMC on each command sent to the BMC. If the BMC has failed, the BIOS reports the failure to the POST screen and send a POST error code to the BMC to log a SEL entry. The BIOS will not send further commands to the BMC during this boot. The system will continue to boot but require user interaction to complete POST (i.e. – “Press <F1> to continue”). The failure status is cleared for any subsequent boots.

13.17.2 BMC Initialization Sequence

The following describes the sequence of interactions between the BMC and BIOS on system power up and hard resets.

1. System powers up or is hard reset (BMC detects a hard reset by detecting that the FRB3_TIMER_HLT signal has become deasserted. The BMC does this by polling the state of the FRB3_TIMER_HALT signal once every ~10ms).
2. The BMC initializes.

3. The BMC disables event logging during initialization. BMC timestamp clock is cleared to 0. The BMC restores Global Enable defaults. The default is for system event logging to be enabled after sensor initialization completes.
4. The BMC enables/disables processors based on FRB-3, IERR and Thermal Trip history.
5. The BMC reads all DIMM SPD FRU devices and initializes DIMM sensor states based on presence and persistent fault information.
6. The BMC starts 5-second FRB-3 timer and releases reset.
7. The BIOS starts. The BMC is ready to accept commands through the SMIC interface, including event messages.
8. The BIOS checks BIST results for BSP.
9. If no BIST failure is indicated, the system continues to boot. If a BIST failure is indicated, BIOS:
   - Determines which processor is BSP
   - Sends the Set Processor State command to the BMC to indicate FRB-1 failure, disable the BSP, and reset the system
   - Halts the BSP
10. If the BIOS disables the FRB-3 timer within 6 seconds, the system continues to boot. If the BIOS fails to disable the FRB-3 timer within 6 seconds, the BMC:
    - Disables the BSP
    - Resets the system
11. The BIOS sets the timestamp as early as possible.
12. The BIOS arms the FRB-2 timer and disables the FRB-3 timer.
13. In order for the BIOS to access the SMBus, it needs to perform the following operations in order:
    - Reprogram the FRB-2 timer to a value long enough to complete the memory configuration plus some padding.
    - Issue a SyncSMBus command
    - Access memory SPDs or any other device on the I^2C bus (i.e., clock generator, I^2C mux, etc.).
14. The BIOS detects and configures memory. The BIOS will query the BMC via a Get DIMM State command to determine if a DIMM has been previously disabled due to a fault. Any DIMMs that are marked as failed will not be utilitized. Any DIMMs that fail to properly configure are marked offline and a Set DIMM Failure State command is issued.
15. When the BIOS completes its I^2C transaction, it needs to perform the following operation in order:
    - Relinquish control of SMBus by issuing a SyncSMBus command.
    - Reprogram the FRB-2 timer to a value between 6-10 minutes.

16. BIOS tests memory. Any DIMM failures are communicated to the BMC via a Set DIMM State command.
17. BIOS sends a Control Memory Monitoring command upon completion of the memory test. In response, the BMC will begin monitoring memory errors.
18. BIOS POST continues as normal.
19. BIOS sends GUID/UUID to BMC by issuing a Set System GUID OEM command.
20. At the end of POST, BIOS sends an Enable NMI command to BMC and then disables the FRB-2 timer.

13.18 PCI-X Hot-plug Support

A PCI adapter can be added or replaced without shutting down the system. The BIOS provides ACPI hot-plug methods for operating systems that support them and generates the Hot plug Resource Table in EBDA. The HRT is required for NetWare* and Linux. The BIOS provides a method of adjusting the memory resource padding for the hot pluggable devices via BIOS setup.

The hardware provides an interlocking switch on each hot-plug slot. Opening this switch automatically powers off the slot. The hardware also provides green and amber lights to indicate the status of each PCI slot. The green light indicates that power is applied to that PCI slot; adapters should not be added or removed from a slot while the green light is on. The amber light acts as an attention indicator. When the amber light is on, the system has detected a slot power fault, a slot bus speed mismatch, or a slot command failure.

The ACPI hot plug methods check the frequency and PCI/PCI-X capabilities of the adapter. The ACPI hot plug methods do not allow less capable adapters to be connected to a bus segment that is currently operating in a more capable mode. In this situation, the hot plug controller turns off power to the adapter and the ACPI hot plug methods turn on the amber light.

13.18.1 PCI/PCI-X Speed and Capabilities Determination

Hot-plug PCI bus segments(slots 5 through 8) support 66MHz and 100MHz PCI-X adapters, as well as 33MHz and 66MHz PCI adapters. Prior to starting POST, the BIOS determines the capabilities of adapters located in these bus segments. If a bus segment is empty, the BIOS sets the capabilities based on an associated option in BIOS setup. The default for this BIOS Setup option is to set these buses to run in PCI mode at 33MHz. Otherwise, BIOS sets the bus segment to the highest capabilities supported by the installed cards. The capabilities of segments are set independently of each other.

14. Error Handling

This section defines how errors are handled by the system BIOS on the Server System SSH4 baseboard. Also discussed is the role of the BIOS in error handling, and the interaction between the BIOS, platform hardware and server management firmware with regard to error handling. In addition, error-logging techniques are described and beep codes for errors are defined.

14.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors that can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus
- Memory correctable- and uncorrectable errors
- Sensors
- Processor internal error, bus/address error, thermal trip error, temperatures and voltages, and GTL voltage levels

Sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and logging system events.

14.2 Handling and Logging System Errors

This section describes actions taken by the SMI handler with respect to the various categories of system errors. It covers the events logged by the BIOS and the format of data bytes associated with those events. The BIOS is responsible for monitoring and logging certain system events. The BIOS sends a platform event message to the BMC to log the event. Some of the errors, such as processor failure, are logged during early POST and not through the SMI handler.

14.2.1 Logging Format Conventions

The BIOS complies with the *Intelligent Platform Management Interface Specification, Revision 1.5*. The BIOS always uses system software ID within the range 00h-1Fh to log errors. As a result, the generator ID byte is an odd number in the range 01h-3fh. OEM user binary should use software IDs of 1. The software ID allows external software to find the origin of the event message.

The BIOS logs the following system event log entries. The sensor numbers for each sensor type in the table below are specified in the Server System SSH4 Baseboard Management Controller External Product Specification.

Table 72. BIOS Logging SEL List

Sensor Type	Sensor Type Code	Sensor-Specific Offset	Event
Processor	07h	02h	FRB-1/BIST Failure
POST Memory Resize	0Eh	–	POST Memory Resize
POST Error	0Fh	–	POST Error
Event Logging Disabled	10h	00h	Correctable Memory Error Logging Disabled
		01h	Event 'Type' Logging Disabled
System Event	12h	00h	System Reconfigured
		01h	OEM System Boot Event (Hard Reset)
Critical Interrupt	13h	04h	PCI PERR
		05h	PCI SERR
		08h	Bus Uncorrectable Error This event is handled by Sahalee.
System Boot Initiated	1Dh	00h	Initiated by power up
		03h	User requested PXE boot
		04h	Automatic boot to diagnostic
Boot Error	1Eh	00h	No bootable media
		02h	PXE Server not found
		03h	Invalid boot sector
Sensor Failure	F6h	00h	I2C Bus Device Address Not Acknowledged
		01h	I2C Bus Device Error Detected
		02h	I2C Bus Timeout
Chipset Specific Critical Interrupt	F4h		
		08h	CIOB30 #0 Errors
		09h	CIOB30 #1 Errors
		0Ah	REMC Errors

Table 73. Event Data 3 Definitions for Optional OEM SEL Entries

Specific Error Code (Event Data3)	
CIOB30 #0, #1	(Func0: X=0, Func2: X=1) X0h=IMB Error Data Phase error X1h=IMB Error Command Phase error X2h=IMB Error Parity error X3h=IMB Error Bus error X4h=IMB Error Sequence error received during ACK X5h=IMB Error Parity error received during ACK X6h=IMB Error Timeout error received during ACK X7h=IMB Error Retry response received during ACK X8h=PCI-X SCE Sampled X9h=PCI-X Unexpected Spilt Completion XAh=PCI-X SCM Generated XBh=PCI-X Split Completion Discarded XCh=PCI-X Split Response Timer Expired XDh=Reserved XEh=Reserved XFh=PCI-X PLL lock

The table below describes the various fields in the event request message sent by the BIOS.

Table 74. Event Request Message Event Data Field Contents

Event Trigger Class	Event Data
Discrete	7:6 00 = Unspecified byte 2 01 = Previous state and/or severity in byte 2 10 = OEM code in byte 2 11 = Sensor specific event extension code in byte 2 5:4 00 = Unspecified byte 3 01 = Reserved 10 = OEM code in byte 3 11 = Sensor specific event extension code in byte 3 3:0 Offset from Event Trigger for discrete event state
	Event Data 2 7:4 Optional offset from ‘Severity’ Event Trigger. (0Fh if unspecified). 3:0 Optional offset from Event Trigger for previous discrete event state. 0Fh if unspecified.

14.3 SMI Handler

The SMI handler is used to handle and log system level events that are not visible to the server management firmware. All system errors are preprocessed by the SMI handler, even those that are normally considered to generate an NMI. The SMI handler sends:

- A command to the BMC to log the event and provides the data to be logged,
- A Set NMI Source command to indicate BIOS as the source of the NMI
- A BIOS LCD command to display the LCD and LED message(s).

A correctable memory error does not generate an SMI. Correctable and uncorrectable memory errors are handled and logged by the BMC.

14.3.1 PCI Bus Error

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively.

14.3.2 Intel® Xeon™ Processor Bus Error

In the case of irrecoverable errors on the host processor bus, proper execution of SMI handler cannot be guaranteed and SMI handler cannot be relied upon to log such conditions. The BIOS SMI handler records the error to the system event log only if the system has not experienced a catastrophic failure that compromises the integrity of the SMI handler. The BIOS always enables the error correction and detection capabilities of the processors by setting appropriate bits in processor model specific register (MSR).

14.3.3 Memory Bus Error

The BMC monitors and logs memory errors. The BIOS will configure the hardware to notify the BMC on correctable and uncorrectable memory errors.

14.3.4 System Limit Error

The BMC monitors system operational limits. It manages the A/D converter, defining voltage and temperature limits as well as fan sensors and chassis intrusion. Any sensor values outside of specified limits are fully handled by BMC and there is no need to generate an SMI to the host processor.

14.3.5 Processor Failure

The BIOS detects processor BIST failure and logs this event. The failed processor can be identified by the first OEM data byte field in the log. For example, if processor 0 fails, the first OEM data byte is 0. The BIOS depends upon BMC to log the watchdog timer reset event. Refer to Section 13.5.3 Fault Resilient Booting (FRB) for details.

14.3.6 Boot Event

The BIOS downloads the system date and time to the BMC during POST and logs a boot event. This does not indicate an error, and software that parses the event log should treat it as such.

14.3.7 Chipset Failure

The BIOS detects the chipset (REMIC and CIOB30) failures and logs these events. The chipset error generates an SMI.

14.4 Firmware (BMC)

The BMC implements the logical system event log device as specified in the *Intelligent Platform Management Interface Specification, Version 1.5.* The system event log is accessible via all BMC transports. This allows the system event log information to be accessed while the system is down, via out-of-band interfaces.

14.4.1 SEL Full

The BIOS generates a POST warning message when the system event log is full. This warning will not inhibit the system from booting.

14.4.2 Timestamp Clock

The BMC maintains a four-byte internal timestamp clock used by the system event log and sensor data record subsystems. This clock is incremented once per second and is read and set using the Get SEL Time and Set SEL Time commands, respectively. The Get SDR Time command can also be used to read the timestamp clock.

The BMC has direct access the system RTC. This allows the BMC to automatically synchronize the SEL/SDR timestamp clock to the RTC time on BMC startup. The BMC periodically reads the RTC to maintain synchronization even when software asynchronously changes the value. In addition to this, the BIOS sends a timestamp to the BMC using Set SEL Time command during POST.

14.5 Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Before video initialization, beep codes inform the user of errors. POST error codes are logged in the event log. The BIOS displays POST error codes on the video monitor.

14.5.1 ASF Progress Codes

The Alert Standard Forum (ASF) events that the BIOS supports are shown in the following table.

Table 75. Event Request Message Event Data Field Contents

ASF Code	Description	Comment
01h	Memory initialization.	At beginning of ECC initialization or memory test.
02h	Hard-disk initialization	At beginning of IDE device detection.
03h	Secondary processor(s) initialization	At beginning of MP Init
04h	User authentication	When waiting for User/Supervisor password
05h	User-initiated system setup	When Setup is invoked
06h	USB resource configuration	When USB devices scan/initialization begins
07h	PCI resource configuration	At beginning of configuring PCI devices in system.
08h	Option ROM initialization	At beginning of Option ROM scan
09h	Video initialization	At beginning of initialization primary video controller (if present)
0Ah	Cache initialization	At beginning of setting up processor cache
0Bh	SM Bus initialization	At beginning of configuring SMBus to communicate with BMC
0Ch	Keyboard controller initialization	At keyboard discovery scan
0Dh	Embedded controller/management controller initialization	When first checking for functional BMC
12h	Calling operating system wake-up vector	When waking from Wake-On-LAN, Wake-On-Ring, Magic Packet, etc.
13h	Starting operating system boot process, e.g. calling Int 19h	Immediately prior to calling INT19h

14.5.2 POST Codes

The BIOS indicates the current testing phase to I/O location 80h and to LCD on front panel during POST after the video adapter has been successfully initialized. If a Port-80h card (Postcard*) is installed, it displays this 2-digit code on a pair of hex display LEDs.

Table 76. Port-80h Code Definition

Code	Meaning
CP	Phoenix* check point POST code

The following table contains the POST codes displayed during the boot process. A beep code is a series of individual beeps on the PC speaker, each of equal length. The following table describes the error conditions associated with each beep code and the corresponding POST checks point code as seen by a ‘port 80h’ card and LCD. For example, if an error occurs at checkpoint 22h, a beep code of 1-3-1-1 is generated. The “-“ indicates a pause between the sequence that delimits the sequence.

Some POST codes occur before the video display is initialized. To assist in determining the fault, a unique beep-code is derived from these checkpoints as follows:

- The 8-bit test point is divided into four 2-bit groups.
- Each group is made one-based (1 through 4)
- One to four beeps are generated based on each group's 2-bit pattern.

Example:

Checkpoint 4Bh is divided into: 01 00 10 11
The beep code is: 2 – 1 – 3 – 4

Table 77. Standard BIOS POST Codes

CP	Beeps	Reason
01		Initialize BMC
02		Verify Real Mode
03		Test BMC
04		Get Processor type
06		Initialize system hardware
08		Initialize chipset registers with initial POST values
09		Set in POST flag
0A		Initialize Processor registers
0B		Enable Processor cache
0C		Initialize caches to initial POST values
0E		Initialize I/O
0F		Initialize the local bus IDE
10		Initialize Power Management
11		Load alternate registers with initial POST values
12		Restore Processor control word during warm boot
13		Initialize PCI Bus mastering devices
14		Initialize keyboard controller
16	1-2-2-3	BIOS ROM checksum
17		Initialize external cache before memory autosize
18		8254 timer initialization
1A		8237 DMA controller initialization
1C		Reset Programmable Interrupt Controller
20	1-3-1-1	Test DRAM refresh
22	1-3-1-3	Test 8742 Keyboard Controller
24		Set ES segment register to 4GB
28	1-3-3-1	Autosize DRAM, system BIOS stops execution here if the BIOS does not detect any usable memory DIMMs
29		Initializes the POST Memory Manager
2A		Clear 8 MB base RAM
2C	1-3-4-1	Base RAM failure, BIOS stops execution here if entire memory is bad
2E		Test the first 4MB of RAM
2F		Initialize external cache before shadowing

CP	Beeps	Reason
32		Test Processor bus-clock frequency
33		Initializes the Phoenix Dispatch Manager
34		Test CMOS
35		RAM Initialize alternate chipset registers
36		Warm start shut down
37		Reinitialize the chipset
38		Shadow system BIOS ROM
39		Reinitialize the cache
3A		Autosize cache
3C		Configure advanced chipset registers
3D		Load alternate registers with CMOS values
40		Set Initial Processor speed new
41		Check unsupported processor
42		Initialize interrupt vectors
44		Initialize BIOS interrupts
45		POST device initialization
46	2-1-2-3	Check ROM copyright notice
47		Initialize manager for PCI Option ROMs
48		Check video configuration against CMOS
49		Initialize PCI bus and devices
4A		Initialize all video adapters in system
4B		Display QuietBoot screen
4C		Shadow video BIOS ROM
4E		Display copyright notice
4F		Allocate memory for the multiboot data
50		Display Processor type and speed
52		Test keyboard
54		Set key click if enabled
55		USB initialization
56		Enable keyboard
58	2-2-3-1	Test for unexpected interrupts
59		Initialize the POST display service
5A		Display prompt "Press F2 to enter SETUP"
5B		Disable L1 cache during POST
5C		Test RAM between 512 and 640k
60		Test extended memory
62		Test extended memory address lines
64		Jump to UserPatch1
66		Configure advanced cache registers
67		Quick init of all AP’s early in post
68		Enable external and processor caches
69		Initialize the SMM handler
6A		Display external cache size
6B		Load custom defaults if required
6C		Display shadow message

CP	Beeps	Reason
6E		Display non-disposable segments
70		Display error messages
72		Check for configuration errors
74		Test real-time clock
76		Check for keyboard errors
7A		Test for key lock on
7C		Set up hardware interrupt vectors
7D		Intelligent system monitoring
7E		Test coprocessor if present
81		POST device initialization routine
82		Detect and install external RS232 ports
83		Configure non-MCD IDE controllers
84		Initialize parallel ports
85		Initialize PC-compatible PnP ISA devices
86		Re-initialize on board I/O ports
87		Configure motherboard configurable devices
88		Initialize BIOS Data Area
89		Enable Non-maskable Interrupts
8A		Initialize Extended BIOS Data Area
8B		Test and initialize PS/2 mouse
8C		Initialize floppy controller
90		Initialize hard disk controller
91		Initialize local bus hard disk controller
92		Jump to UserPatch2
93		Build MPTABLE for multi-processor boards
94		Disable A20 address line
95		Install CD-ROM for boot
96		Clear huge ES segment register
97		Fixup Multi Processor table
98	1-2	Search for option ROMs. One long, two short beeps on checksum failure
9A		Shadow option ROMs
9C		Set up Power Management
9D		Initialize security engine
9E		Enable hardware interrupts
A0		Set time of day
A2		Check key lock
A4		Initialize typematic rate
A8		Erase F2 prompt
A9		Prepare boot
AA		Scan for F2 key stroke
AC		Enter SETUP
AE		Clear in-POST flag
B0		Check for errors
B2		POST done – prepare to boot Operating System
B4	1	One short beep before boot

CP	Beeps	Reason
B5		Display MultiBoot menu
B6		Check password, password is checked before option ROM scan
B7		ACPI initialization
B8		Clear global descriptor table
B9		Prepare boot
BA		SMBIOS configuration
BC		Clear parity checkers
BD		Display Boot Menu
BE		Clear screen (optional)
C0		Try to boot with INT 19
C1		Initialize the POST Error Manager
C2		Invoke End of POST Error Logging
C3		Invoke End of POST Error Message Display
C6		Initialize Console Redirection
C7		Control Console Port
C8		Forced shutdown
C9		Flash recovery
DO		Interrupt handler error
D2		Unknown interrupt error
D4		Pending interrupt error
D6		Initialize option ROM error
D8		Shutdown error
DA		Extended Block Move
DC		Shutdown 10 error

Table 78. Recovery BIOS POST Codes

CP	Beeps	Reason
E0		Initialize chip set
E1		Initialize bridge
E2		Initialize processor
E3		Initialize timer
E4		Initialize system I/O
E5		Check forced recovery boot
E6		Validate checksum
E7		Go to BIOS
E8		Initialize processors
E9		Set 4 GB segment limits
EA		Perform platform initialization
EB		Initialize PIC and DMA
EC		Initialize memory type
ED		Initialize memory size
EE		Shadow boot block
F0		Test system memory
F1		Initialize interrupt services

CP	Beeps	Reason
F2		Initialize real time clock
F3		Initialize video
F4		Initialize beeper
F5		Initialize boot
F6		Restore segment limits to 64 KB
F7		Boot mini DOS

14.5.3 POST Error Codes and Messages

The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. Some error messages are preceded by the string "Error" to indicate that the system may be malfunctioning. All POST errors and warnings are logged in the system event log unless it is full.

Table 79. POST Error Messages and Codes

Code	Error Message	Failure Description
0200:	Failure Fixed Disk	hard disk error
0210:	Stuck Key	Keyboard connection error
0211:	Keyboard error	Keyboard failure
0212:	Keyboard Controller Failed	Keyboard Controller Failed
0213:	Keyboard locked – Unlock key switch	Keyboard locked
0220:	Monitor type does not match CMOS – Run SETUP	Monitor type does not match CMOS
0230:	System RAM Failed at offset	System RAM error Offset address
0231:	Shadow RAM Failed at offset	Shadow RAM Failed Offset address
0232:	Extend RAM Failed at address line	Extended RAM failed Offset address
0250:	System battery is dead – Replace and run SETUP	NVRAM battery dead
0251:	System CMOS checksum bad – Default configuration used	CMOS checksum error
0252:	Password checksum bad - Passwords cleared	
0260:	System timer error	System timer error
0270:	Real time clock error	RTC error
0271:	Check date and time setting	RTC time setting error
02B0:	Diskette drive A error	
02B1:	Diskette drive B error	
02B2:	Incorrect Drive A type – run SETUP	Incorrect Drive A type
02B3:	Incorrect Drive B type – run SETUP	Incorrect Drive B type
02D0:	System cache error – Cache disabled	CPU cache error
02D1:	System Memory exceeds the CPU's caching limit	
0B28	Unsupported Processor detected on Processor 1	
0B29	Unsupported Processor detected on Processor 2	
0B2A	Unsupported Processor detected on Processor 3	

Code	Error Message	Failure Description
0B2B	Unsupported Processor detected on Processor 4	
0B30	Fan 1 Alarm occured	
0B31	Fan 2 Alarm occured	
0B32	Fan 3 Alarm occured	
0B33	Fan 4 Alarm occured	
0B34	Fan 5 Alarm occured	
0B35	Fan 6 Alarm occured	
0B50:	Processor 1 with error taken offline	Failed Processor 1 because an error was detected.
0B51:	Processor 2 with error taken offline	Failed Processor 2 because an error was detected.
0B52:	Processor 3 with error taken offline	Failed Processor 3 because an error was detected.
0B53:	Processor 4 with error taken offline	Failed Processor 4 because an error was detected.
0B5F:	Forced to use CPU with error	An error detected in the entire CPU.
0B60:	DIMM bank 1 has been disabled	Memory error, memory bank 1 failed
0B61:	DIMM bank 2 has been disabled	Memory error, memory bank 2 failed
0B62:	DIMM bank 3 has been disabled	Memory error, memory bank 3 failed
0B6F:	DIMM bank with error is enabled	An error detected in all the memory
0B70:	The error occurred during temperature sensor reading	Error while detecting a temperature failure.
0B71:	System temperature out of the range	Temperature error detected.
0B74:	The error occurred during voltage sensor reading	Error while detecting voltage
0B75:	System voltage out of the range	System voltage error
0B7C:	The error occurred during redundant power module confirmation.	The error occurred while retrieving the power information.
0B7D:	The normal operation can't be guaranteed with use of only one PSU	
0B80:	BMC Memory Test Failed	BMC device (chip) failed
0B81:	BMC Firmware Code Area CRC check failed	
0B82:	BMC core Hardware failure	
0B83:	BMC IBF or OBF check failed	Access to BMC address failed
0B8A:	BMC SEL area full	
0B8B:	BMC progress check timeout	
0B8C:	BMC command access failed	
0B8D:	Could not redirect the console –BMC Busy -	
0B8E:	Could not redirect the console –BMC Error -	
0B8F:	Could not redirect the console –BMC Parameter Error -	
0B90:	BMC Platform Information Area corrupted.	BMC device(chip) failed
0B91:	BMC update firmware corrupted.	
0B92:	Internal Use Area of BMC FRU corrupted.	SROM storing chassis information failed (Available for use except for FRU command and emergency management port function)
0B93:	BMC SDR Repository empty.	BMC device (chip) failed
0B94:	IPMB signal lines do not respond.	SMC(Satellite Management Controller) failed (Available for use except for the access function to SMC via IPMB)

Code	Error Message	Failure Description
0B95	BMC FRU device failure.	SROM storing chassis information failed (Available for use except for FRU command and emergency management port function.)
0B96	BMC SDR Repository failure.	BMC device (chip) failed
0B97	BMC SEL device failure.	
0B98:	BMC RAM test error.	BMC RAM error
0B99:	BMC Fatal hardware error.	BMC hardware error
0B9A:	BMC not responding	
0B9B:	Private I2C bus not responding	SMBus Error
0B9C:	BMC internal exception.	
0B9D:	BMC A/D timeout error.	
0B9E:	SDR repository corrupt.	
0B9F:	SEL corrupt.	
0BB0:	SMBIOS – SROM data read error	SROM data read error
0BB1:	SMBIOS – SROM data checksum bad	Bad checksum of SROM data
0BC0:	POST detected startup failure of 1st Processor.	
0BC1:	POST detected startup failure of 2 nd Processor.	
0BC2:	POST detected startup failure of 3 rd Processor.	
0BC3:	POST detected startup failure of 4 th Processor.	
0BD0:	1st SMBus device address not acknowledged.	1 st SMBus device (chip) failed
0BD1:	1st SMBus device Error detected.	
0BD2:	1st SMBus timeout.	
0BD3:	2 nd SMBus device address not acknowledged.	2 nd SMBus device (chip) failed
0BD4:	2 nd SMBus device Error detected.	
0BD5:	2 nd SMBus timeout.	
0BD6:	3 rd SMBus device address not acknowledged.	3 rd SMBus device (chip) failed
0BD7:	3 rd SMBus device Error detected.	
0BD8:	3 rd SMBus timeout.	
0BD9:	4 th SMBus device address not acknowledged.	4 th SMBus device (chip) failed
0BDA:	4 th SMBus device Error detected.	
0BDB:	4 th SMBus timeout.	
0BDC:	5 th SMBus device address not acknowledged.	5 th SMBus device (chip) failed
0BDD:	5 th SMBus device Error detected.	
0BDE:	5 th SMBus timeout.	
0BE8:	IPMB address not acknowledged.	IPMB device (chip) failed
0BE9:	IPMB device Error detected.	
0BEA:	IPMB timeout.	
8100:	Memory Error detected in DIMM group #1.	
8101:	Memory Error detected in DIMM group #2.	
8102:	Memory Error detected in DIMM group #3.	
8120:	Unsupported DIMM detected in DIMM group #1.	
8121:	Unsupported DIMM detected in DIMM group #2.	
8122:	Unsupported DIMM detected in DIMM group #3.	
8130:	Mismatch DIMM Type detected in DIMM group #1.	
8131:	Mismatch DIMM Type detected in DIMM group #2.	

Code	Error Message	Failure Description
8132:	Mismatch DIMM Type detected in DIMM group #3.	
8140:	DIMM group #1 with error is enabled.	
8141:	DIMM group #2 with error is enabled.	
8142:	DIMM group #3 with error is enabled.	
8150:	NVRAM Cleared By Jumper	
8320:	Mismatch Processor Speed detected on Processor 1	
8161:	Mismatch Processor Speed detected on Processor 2	
8162:	Mismatch Processor Speed detected on Processor 3	
8163:	Mismatch Processor Speed detected on Processor 4	
8170:	Processor 1 not operating at intended frequency	
8171:	Processor 2 not operating at intended frequency	
8172:	Processor 3 not operating at intended frequency	
8173:	Processor 4 not operating at intended frequency	
817F	All Processor not operating at intended frequency	
8180:	Processor #1 Error	
8181:	Processor #2 Error	
8182:	Processor #3 Error	
8183:	Processor #4 Error	
	Expansion ROM not initialized.	PCI Expansion ROM card not initialized
	Invalid System Configuration Data	System configuration data destroyed
	System Configuration Data Read Error	System configuration data read error
	Resource Conflict	PCI card resource is not mapped correctly.
	System Configuration Data Write error	System configuration data write error
	Warning: IRQ not configured	PCI interrupt is not configured correctly.
	PCI System Error on Bus/Device/Function	PCI SERR
	PCI Parity Error on Bus/Device/Function	PCI PERR

14.5.4 LCD Display

The LCD display can be accessed by BMC, BIOS, and software. In some cases, more than one of these may be using the LCD simultaneously.

14.5.4.1 BIOS Usage

The BIOS uses the first line of the LCD for messages related to failures and other conditions. The BIOS generates an LCD message during POST and as a result of errors handled by the BIOS SMI handler. Unless the LCD has been forcibly reserved by software via the LCD Display Control command, a BIOS message will override a software message written to the BIOS area.

Normally, the BIOS will use the BIOS LCD Message command that will cause the BMC to display a BMC stored message in the BIOS message area (first line) of the LCD.

14.5.4.2 Message Format

During POST, the LCD panel displays the following:

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0	A	A		P	P		S	S	H	4				X	X	X
1																

Where:

- AA = ASF Progress Code
- PP = Port 80h Code
- SSH4 = Platform Code
- XXX = BIOS Build Number

During POST task hootPrepareToBootJ (TP B9h), the following message is displayed:

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0	P	r	e	p	a	r	e		T	O		B	o	o	t	
1																

When a POST Error occurs, the following message is displayed. It displays up to six messages as shown below starting on Row0, Column0:

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0	N	N	N	N	,	N	N	N	N	,	N	N	N	N	,	
1	N	N	N	N	,	N	N	N	N	,	N	N	N	N	,	

14.5.4.3 Virtual LCD

The BMC implements a virtual LCD that provides LCD command functionality even if a physical LCD is not present in the chassis. This allows BIOS messages to be retrieved by a remote console independently of chassis configuration.

14.5.4.4 OEM Extensibility

To allow OEMs to provide LCD functionality in their own chassis, the BIOS provides LCD Control Services via INT15. These will automatically be directed to a satellite intelligent IPMI controller at slave address 22h on the IPMB.

15. Setup Utility

This section describes the ROM resident Setup utility that provides a way to configure the platform. The Setup utility is part of the system BIOS and allows limited control over on-board resources such as parallel port and mouse. The following topics are covered here:

- Setup utility operation
- Configuration CMOS RAM definition
- Function of CMOS clear jumper

Configuration of on-board devices is done using the Setup utility embedded in flash ROM. Setup provides enough configuration functionality to boot a system diskette or CD-ROM. Setup is always provided in flash for basic system configuration.

The configuration utilities modify CMOS and NVRAM under direction of the user. The actual hardware configuration is accomplished by the BIOS POST routines and the BIOS Plug-N-Play Auto-configuration Manager. The configuration utilities always update a checksum for both areas, so any potential data corruption is detectable by the BIOS before actual hardware configuration takes place. If the data is corrupted, the BIOS loads the default configuration and requests that the user reconfigure the system and reboot.

15.1 Setup Utility Operation

The ROM-resident Setup utility configures only on-board devices. The Setup utility screen is divided into four functional areas. Table 80 describes each area:

Table 80. Setup Utility Screen

Keyboard Command Bar	Located at the bottom of the screen. This bar displays the keyboard commands supported by the Setup utility.
Menu Selection Bar	Located at the top of the screen. Displays the various major menu selections available to the user. The server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, System Menu, Boot Menu, and the Exit Menu.
Options Menu	Each Option Menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Option Menu drops you into submenus.
Item Specific Help Screen	Located at the right side of the screen is an item-specific Help screen.

15.1.1 Entering Setup Utility

During POST operation, the user is prompted to enter Setup using the F2 function key as follows:

```
Press <F2> to enter Setup
```

A few seconds might pass before Setup is entered while POST completes the test and initialization functions. When Setup is entered, the Main Menu options page is displayed.

15.1.2 Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used for navigating the Setup utility. These commands are displayed at all times, for every menu and submenu.

Each Setup menu page contains a number of features. Except those used for informative purposes, each feature is associated with a value field. This field contains user-selectable parameters. Depending on the security option chosen and in effect via password, a menu feature's value can be changeable or not. If a value is nonchangeable due to insufficient security privileges (or other reasons), the feature's value field is inaccessible. The Keyboard Command Bar supports the following:

F1	Help	Pressing F1 on any menu invokes the general Help window. This window describes the Setup key legend. The up arrow, down arrow, Page Up, Page Down, Home, and End keys scroll the text in this window.
Enter	Execute Command	The Enter key is used to activate submenus when the selected feature is a submenu, or to display a pick list if a selected feature has a value field, or to select a subfield for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.
ESC	Exit	The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed in any submenu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded.
↑	Select Item	The up arrow is used to select the previous value in a pick list, or the previous feature in a menu item's option list. The selected item must then be activated by pressing the Enter key.
↓	Select Item	The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.
↔	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a submenu or pick list is displayed.
-	Change Value	The minus key or the F5 function key is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.
+	Change Value	The plus key or the F6 function key is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboard, but it has the same effect.
F9	Setup Defaults	Pressing F9 causes the following to appear: **Setup Confirmation** **Load default configuration now?** **[Yes] [No]** If "Yes" is selected and the Enter key is pressed, all Setup fields are set to their default values. The User binary and custom splash screen are not affected by pressing F9. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values.

F10	Save and Exit	Pressing F10 causes the following message to appear: **Setup Confirmation** **Save Configuration changes and exit now?** **[Yes] [NO]** If “Yes” is selected and the Enter key is pressed, all changes are saved and Setup is exited. If “No” is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.

15.1.3 Menu Selection Bar

The Menu Selection Bar is located at the top of the screen. It displays the various major menu selections available to the user:

- Main Menu
- Advanced Menu
- Security Menu
- Server Menu
- Boot Menu
- Exit Menu

These and associated submenus are described below.

15.1.3.1 Main Menu Selections

The following tables describe the available functions on the Main Menu, and associated submenus. Default values are highlighted.

Table 81. Main Menu Selections

Feature	Option	Description
System Time	HH:MM:SS	Set the System Time.
System Date	MM/DD/YYYY	Set the System Date.
Legacy Floppy A	Disabled 1.2Mb 5.25” 720Kb 3.5”**1.44 / 1.25 MB 3½”** 2.88Mb 3.5”	
Legacy Floppy B	Disabled 1.2Mb 5.25” 720Kb 3.5” **1.44 / 1.25 MB 3½”** 2.88Mb 3.5”	

Feature	Option	Description
Hard Disk Pre-delay	**Disabled** 3 seconds 6 seconds 9 seconds 12 seconds 15 seconds 21 seconds 30 seconds	Allows slower spin-up drives to come ready.
Primary IDE Master		Selects sub-menu
Primary IDE Slave		Selects sub-menu
Processor Settings		Selects sub-menu
Language	**English (US)** Spanish Italian French German	Selects the language BIOS displays.

Table 82. Primary Master and Slave IDE Submenu Selections

Feature	Option	Description
Type	**Auto** None CD-ROM User ATAPI Removable IDE Removable Other ATAPI	Select the byte of device that is attached to the IDE. Channel. If User is selected, the user will need to enter the parameters of IDE device (cylinders, head and sectors).
CHS format Cylinders	1 to 2048	Number of cylinders on drive. This field is changeable only for Type User. This field is informational only, for Type Auto.
CHS format Heads	1 to 16	Number of read/write heads on Drive. This field is available only for Type User. This field is informational only, for Type Auto.
CHS format Sectors	1 to 64	Number of Sectors per Track. This field is available only for Type User. This field is informational only, for Type Auto.
CHS format Maximum Capacity	See description	Computed size of drive from cylinders, heads, and sectors entered. This field is only available for Type User. This field is informational only for Type Auto.
Multi-Sector Transfer	**Disabled** 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Specifies the number of sectors that are transferred per block during multiple sector transfers. This field is informational only for Type Auto.
LBA Mode Control	**Disabled** Enabled	Enable/Disable LBA instead of cylinder, head, sector, addressing. This field is informational only for Type Auto.
32 Bit I/O	**Disabled** Enabled	Enabling allows 32 bit IDE data transfers. This field is informational only for Type Auto.

Feature	Option	Description
Transfer Mode	Standard FPIO 1 FPIO 2 FPIO 3 **FPIO 4** FPIO 3 / DMA 1 FPIO 4 / DMA 2	Select the method for moving data to/from the drive. This field is informational only for Type Auto. This field is updated to display only the modes supported by the attached device.
Ultra DMA Mode	**Disabled** Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	Select the Ultra DMA mode This field is informational only for Type Auto.

Table 83. Processor Settings Submenu Selections

Feature	Option	Description
Processor Retest	**No**, Yes	If yes, BIOS will clear historical processor status and retest all processors on the next boot.
Processor POST speed setting	Information Only	Displays measured processor speed.
Processor 1 CPUID	CPUID Not installed Disabled	Reports CPUID for Processor 1, if present. If empty, reports Vacant. If disabled by BMC, reports Disabled.
Processor 1 L2/L3 Cache Size	Information Only	Displays L2/L3Cache Size for Processor 1.
Processor 2 CPUID	CPUID Not installed Disabled	Reports CPUID for Processor 2, if present. If empty, reports Vacant. If disabled by BMC, reports Disabled.
Processor 2 L2/L3 Cache Size	Information Only	Displays L2/L3Cache Size for Processor 2.
Processor 3 CPUID	CPUID Not installed Disabled	Reports CPUID for Processor 3, if present. If empty, reports Vacant. If disabled by BMC, reports Disabled.
Processor 3 L2/L3 Cache Size	Information Only	Displays L2/L3Cache Size for Processor 3.
Processor 4 CPUID	CPUID Not installed Disabled	Reports CPUID for Processor 4, if present. If empty, reports Vacant. If disabled by BMC, reports Disabled.
Processor 4 L2/L3 Cache Size	Information Only	Displays L2/L3Cache Size for Processor 4.
Hyper-Threading Technology	**Enabled** Disabled	Sets state of Hyper-Threading Technology*support in all installed processors.

15.1.3.2 Advanced Menu Selections

The following tables describe the menu options and associated submenus available on the Advanced Menu. Please note that MPS 1.4/1.1 selection is no longer configurable. The BIOS always builds MPS 1.4 tables.

Table 84. Advanced Menu Selections

Feature	Option	Description
Memory Configuration		Select sub-menu
PCI Configuration		Selects sub-menu.
I/O Device/peripheral Configuration		Selects sub-menu.
Advanced Chipset Control		Select sub-menu
Boot-time Diagnostic Screen	Disabled **Enabled**	If enabled, the BIOS will display the OEM logo during POST. This option is hidden if the BIOS does not detect a valid logo in the flash area reserved for this purpose.
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the System Configuration Data during next boot. Automatically reset to 'No' in next boot.
Installed O/S	**Other** PnP O/S	If PnP O/S is selected, only the devices required to boot the system are configured. If Other is selected, all devices are configured.
Numlock	On **Off**	Sets power on Numlock state.
Memory/Processor Error	**Boot** Halt	Selects the behavior of the system in response to a memory or processor reconfiguration. If set to Boot, the system will attempt to boot. If set to Halt, the system will require user intervention to complete booting.

Table 85. Memory Configuration Menu Selections

Feature	Option	Description
DIMM Group #1 Status	Normal **Not Installed** Disabled	Displays the current status of the memory bank. Disabled indicated that a DIMM in the bank has failed and the entire bank has been disabled.
DIMM Group #2 Status		
DIMM Group #3 Status		
Memory Retest	**No** Yes	Causes BIOS to retest all memory on next boot.
Extended RAM Step	**Disabled** 1 MB 1 KB Every Location	Selects the size of step to use during Extended RAM tests.

Table 86. PCI Configuration Menu Selections

Feature	Description
Hot plug PCI Control	Selects sub-menu
Embedded SCSI	Selects sub-menu
Embedded NIC 1	Selects sub-menu
Embedded NIC 2	Selects sub-menu
Embedded Video Controller	Selects sub-menu
PCI slot1	Selects sub-menu
PCI slot2	Selects sub-menu
PCI slot3	Selects sub-menu
PCI slot4	Selects sub-menu
PCI slot5	Selects sub-menu
PCI slot6	Selects sub-menu
PCI slot7	Selects sub-menu
PCI slot8	Selects sub-menu

Table 87. Hot Plug PCI Control Submenu Selections

Feature	Option	Description
Reserving memory space for PHP	**Disabled** Minimum Middle Maximum	Determines the amount of memory and I/O address space that is reserved for each hot-plug PCI device.
Empty Bus Default Speed PCI Slots 5-6: PCI Slots 7-8:	**PCI 33MHz** PCI 66MHz PCI-X 66MHz PCI-X100 MHz PCI-X 133 MHz	If a Hot-plug PCI bus is empty, this option controls the speed at which the bus will be configured to operate. (Fab 704 Base board.)

Table 88. Embedded SCSI, LAN and VGA Submenu Selections

Feature	Option	Description
SCSI ControllerLAN Controller 1 LAN Controller 2 VGA Controller	**Enabled** Disabled	If Disabled, the BIOS will hold the embedded chip in reset. In this configuration, the controller HW is completely disabled, and will be invisible to the PnP operating systems.
Option ROM Scan	**Enabled** Disabled	If Enabled, initialize device expansion ROM.

Table 89. PCI Slot Submenu Selections

Feature	Option	Description
PCI Slotn (n:1-8) Option ROM Scan	**Enabled** Disabled	Enable option ROM scan of the selected device.

Table 90. I/O Device Configuration Submenu Selections

Feature	Option	Description
Serial Port 1	Disabled **Enabled** Auto	If set to “Auto,” BIOS configures the port. If set to “OS Controlled,” OS configures the port.
Base I/O Address	**3F8h** 2F8h 3E8h 2E8h	Selects the base I/O address for COM port 1.
Interrupt	**IRQ 4** IRQ 3	Selects the IRQ for COM port 1.
Serial Port 2	Disabled **Enabled** Auto	If set to “Auto”, BIOS configures the port. If set to “OS Controlled”, OS configures the port.
Base I/O Address	3F8h **2F8h** 3E8h 2E8h	Selects the base I/O address for COM port B.
Interrupt	IRQ 4 **IRQ 3**	Selects the IRQ for COM port B.
Parallel Port	Disabled **Enabled** Auto	If set to “Auto,” BIOS configures the port. If set to “OS Controlled,” OS configures the port.
Mode	Output only Bi-Directional EPP **ECP**	Selects Parallel Port Mode.
Base I/O Address	**378h** 278h	Selects the base I/O address for LPT port.
Interrupt	IRQ 5 **IRQ 7**	Selects the IRQ for LPT port.
DMA channel	**DMA1** **DMA** 3	Selects the DMA for LPT port.
Legacy USB support	Disabled **Enabled**	If disabled, legacy USB support is turned off at the end of the BIOS POST.
PS/2 Mouse	Disabled **Enabled**	If disabled, the PS/2 mouse port will not function. Should make IRQ12 available for other devices.

Table 91. Advanced Chipset ControlSubmenu Selections

Feature	Option	Description
PCI Device		Selects sub-menu
Wake On LAN	Enabled **Disabled**	Only controls legacy wake up. May not be present if not supported.
Wake On Ring	Enabled **Disabled**	Only controls legacy wake up. May not be present if not supported.
Sleep Button	**Present** Absent	Selects the sleep button of the platform.

Table 92. PCI Device Submenu Selections

Feature	Option	Description
PCI IRQ line 1-14 : PCI IRQ line 17-32	Disable **Auto Select** IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ14 IRQ15	Select the IRQ for PCI IRQ

15.1.3.3 Security Menu Selections

Table 93. Security Menu Selections

Feature	Option	Description
User password is	**Clear** Set	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Administrator Password is	**Clear** Set	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set User password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set Administrative Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Password on boot	**Disabled** Enabled	If enabled, requires password entry before boot.
Fixed disk boot sector	**Normal** Write protect	Will write protect the boot sector of the hard drive to prevent viruses from corrupting the drive under DOS if set to write protect.

Feature	Option	Description
Secure Mode Timer	2 minutes 5 minutes 10 minutes 20 minutes 1 hour **2 hours**	Period of key/PS/2 mouse inactivity specified for Secure Mode to activate. A password is required for Secure Mode to function. Has no effect unless at least one password is enabled.
Secure Mode Hot Key (Ctrl-Alt-)	[ ], [A, B, ..., Z], [0-9]	Key assigned to invoke the secure mode feature. Cannot be enabled unless at least one password is enabled. Can be disabled by entering a new key followed by a backspace or by entering delete.
Secure Mode Boot	**Disabled** Enabled	System boots in Secure Mode. The user must enter a password to unlock the system. Cannot be enabled unless at least one password is enabled.
Video Blanking	**Disabled** Enabled	Blank video when Secure mode is activated. A password is required to unlock the system. This cannot be enabled unless at least one password is enabled. This option is only present if the system includes an embedded video controller.
Floppy Write Protect	**Disabled** Enabled	When Secure mode is activated, the floppy drive is write protected. A password is required to re-enable floppy writes. Cannot be enabled unless at least one password is enabled.
Power Switch Inhibit	**Disabled** Enabled	Determines whether power switch function from front panel.

15.1.3.4 Server Menu Selections

Table 94. Server Menu Selections

Feature	Option	Description
System Management		Selects sub-menu.
Console Redirection		Selects sub-menu.
Service Partition Type	12	Displays the partition type of the service partition
Clear Event Log	Press Enter	If selected, the System Event log will be cleared immediately.
Assert NMI on PERR	**Disabled** Enabled	If enabled, PCI bus parity error (PERR) is enabled and is routed to NMI.
Assert NMI on SERR	**Enabled** Disabled	If enabled, PCI bus system error (SERR) is enabled and is routed to NMI.
FRB-2 Policy	**Disable BSP** Don't Disable Retry 3 Times	Controls the policy of the FRB-2 timeout. This option determines when the Boot Strap Processor (BSP) should be disabled if FRB-2 error occur and it detemines when FRB-2 stops.
Thermal Sensor	Disabled **Enabled**	Determines wheter Thermal Sensor monitoring function
BMC IRQ	**11** 5 10 Disabled	Determines BMC IRQ.
Post Error Pause	Disabled **Enabled**	If enabled, the boot is stopped when Post error occurs.
AC Link	Power On **Last State** Stay off	Selects system power state after AC loss.

Table 95. System Management Submenu Selections

Feature	Description
BIOS Version	Information field only
Board Part #	Information field only
Board Serial #	Information field only
System Part #	Information field only
System Serial #	Information field only
Chassis Part #	Information field only
Chassis Serial #	Information field only
BMC Device ID	Information field only.
BMC Device Rev	Information field only.
BMC Firmware Rev	Information field only.
BMC BBFirmware Rev	Information field only.
IPMI Rev	Information field only.
SDR Revision	Information field only.
PIA Revision	Information field only.
Primary HSBP Revision	Information field only, hidden if not detected
Secondary HSBP Revision	Information field only, hidden if not detected

Table 96. Console Redirection Submenu Selections

Feature	Option	Description
Serial Port Address	**Disabled** On-board COM A On-board COM B	When enabled, console redirection uses the I/O port specified. Choosing “Disabled” completely disables Console Redirection.
Baud Rate	**9600** 19.2 KB 38.4 KB 57.6 KB 115.2 KB	When console redirection is enabled, use the baud rate specified. When emergency management port is sharing the COM port as console redirection, the baud rate must be set to 19.2 k to match emergency management port baud rate, unless auto-baud feature is used.
Flow Control	None CTS / RTS XON / XOFF **CTS / RTS + CD**	• None = No flow control. • CTS/RTS = Hardware based flow control. • XON/XOFF = Software flow control. • CTS/RTS +CD = Hardware based + Carrier Detect flow control. When the emergency management port is sharing the COM port as console redirection, the flow control must be set to CTS/RTS or CTS/RTS+CD depending on whether a modem is used.

15.1.3.5 Boot Menu Selections

Boot Menu options allow the user to select the boot device. The following table is an example of a list of devices ordered in priority of the boot invocation. Items can be re-prioritized by using the up and down arrow keys to select the device. Once the device is selected, the plus (+) key moves the device higher in the boot priority list and the minus (-) key moves the device lower in the boot priority list.

Table 97. Boot Device Priority Selections

Boot Priority	Device	Description
1	Removable Devices	Attempt to boot from a legacy floppy A: or removable media device such as the LS-120.
2	Hard Drive	Attempt to boot from a hard drive device.
3	ATAPI CD-ROM Drive	Attempt to boot from an ATAPI CD-ROM drive.
4	PXE UNDI	Attempt to boot from a network. This entry will appear if there is a network device in the system that is controlled by a PXE compliant option ROM.

Table 98. Hard Drive Selections

Option	Description
Drive #1 (or actual drive string) Other bootable cards Additional entries for each drive that has a PnP header	To select the boot drive, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list or the minus key (–) to move it down. Other bootable cards cover all the boot devices that are not reported to the system BIOS through BIOS Boot specification mechanism. It may or may not be bootable, and may not correspond to any device. If BIOS boot spec. support is set to limited, this item covers all drives that are controlled by option ROMs (like SCSI drives). Press ESC to exit this menu.

Table 99. Removable Drive Selections

Feature	Option	Description
Lists Bootable Removable Devices in the System	+ _	Use +/– keys to place the removable devices in the boot order you want. Includes Legacy 1.44 MB floppy, 120 MB floppy etc.

15.1.3.6 Exit Menu Selections

The following menu options are available on the Exit menu. Use the up and down arrow keys to select an option, then press the Enter key to execute the option.

Table 100. Exit Menu Selections

Option	Description
Exit Saving Changes	Exit after writing all modified Setup item values to NVRAM.
Exit Discarding Changes	Exit leaving NVRAM unmodified. User is prompted if any of the setup fields were modified.
Load Setup Defaults	Load default values for all SETUP items.
Load Custom Defaults	Load values of all Setup items from previously saved Custom Defaults. NOTE: This is hidden if custom defaults are not valid or present.
Save Custom Defaults	Stores Custom Defaults in NVRAM.
Discard Changes	Read previous values of all Setup items from NVRAM.
Save Changes	Write all Setup item values to NVRAM.

15.2 CMOS Memory Definition

The CMOS map is available in the NVRAM.LST file generated for every BIOS release. The CMOS map is subject to change without notice.

15.3 Clearing CMOS

The BIOS detects CMOS clear request via the CMOS jumper or BMC request. If the BIOS detects “CMOS Clear” prior to power-on or a hard reset, the BIOS changes the CMOS and NVRAM settings to a default state. This guarantees the system’s ability to boot from floppy.

Password settings, user binary, and custom splash screens are unaffected through CMOS clear. The BIOS clears the ESCD parameter block and loads a null ESCD image. The boot order information is also cleared when CMOS is cleared via jumper. The configuration data for the on-board SCSI controllers is not cleared during a clear CMOS event as each device controls its own default settings.

If the Reset Configuration Data option is enabled in Setup, ESCD data and BIOS Boot specification data is cleared and reinitialized in next boot.

16. Flash Update Utilities

Note: The Intel® iFlash utility must be run without the presence of a 386 protected mode control program, such as Microsoft* Windows or EMM386*. The flash update utilities use the processor's flat addressing mode to update the flash ROM.

16.1 Loading System BIOS via iFlash

The new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the flash part. The number of files is constrained by the fact that the image and the utilities fit onto a single, 1.44 MB DOS-bootable floppy. These files are named as follows:

- xxxxxxxx.BIO
- xxxxxxxx.BI1
- xxxxxxxx.BI2

The first eight letters of each filename can be any value, but the files cannot be renamed. Each file contains a link to the next file in the sequence. iFlash does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent filenames must remain unchanged.

The user binary area is also updated during a system BIOS update. The user binary can be updated independently from the system BIOS. CMOS is not cleared when the system BIOS is updated in normal or recovery mode. Configuration information like ESCD is not overwritten during BIOS flash update. The user is prompted to reboot after a BIOS update completes.

16.2 User Binary Area

The BIOS flash ROM includes a 16 KB area in flash for implementation-specific OEM add-ons. The user binary area can be saved and updated exactly as described above in the System BIOS section. Only one file is needed. The valid extension for user files is .ROM.

For more information on using this area, refer to Section 13.9.1.

16.3 Language Area

The system BIOS language area can be updated only by updating the entire BIOS. The BIOS supports English, Spanish, French, German, and Italian. These languages are selected through Setup.

16.4 OEM Logo Screen

A 128 KB region of Flash ROM is available to store the OEM logo in compressed format. The BIOS contains the standard Intel logo. Using the Phoenix* PHLASH utility, this region can be updated with an OEM supplied logo image. The OEM logo must fit within 640 X 384 size. If an OEM logo is flashed into the system, it overrides the built in Intel logo.

For more information on using this area, refer to Section 13.9.2: OEM Logo Screen.

16.5 Recovery Mode

The Server System SSH4 baseboard supports a method for performing a BIOS recovery in order to restore the system from a failed flash. This utilizes a jumper on the baseboard. The system beeps throughout the process. The recovery BIOS boots from a 1.44 MB floppy diskette inserted into a 1.44 MB floppy drive or LS-120/240 drive only. Nothing is displayed to the video screen during the recovery process.

Note: The user must make the recovery floppy diskette following the instructions included in the release notes. Failure to do so will cause the process to fail.

16.5.1 Performing BIOS Recovery

The following procedure boots the recovery BIOS and flashes the normal BIOS.

1. Prepare a BIOS recovery diskette by following the instructions included with the BIOS release.
2. Turn off the system power.
3. Move the BIOS recovery jumper to the recovery position.
4. Insert the BIOS recovery diskette.
5. Turn on the system power.

The system boots from the recovery diskette. The BIOS will beep twice when the update process starts. The system will continue to beep while updating the BIOS. When the BIOS update completes successfully, the system will stop beeping. If the update fails, the system will sound an alternating pattern of a buzz and a beep.

When the flash update completes:

1. Turn off the system power.
2. Remove the recovery diskette.
3. Restore the recovery jumper to its original position.
4. Turn on the system power.
5. Flash any custom blocks such as user binary.

The system should boot normally using the updated system BIOS.

Appendix A: Obsolete BIOS Features

The following obsolete BIOS features are not supported by the Server System SSH4 BIOS.

- Multi Processor Specification 1.1: All Priority 1 operating systems support MPS 1.4
- Add-in ISA devices: No ISA slots on baseboard (no support for PCI-ISA bridge).
- Add-in ISA PnP devices: No ISA slots on baseboard (no support for PCI-ISA bridge).
- Offboard AGP video: No AGP slot on baseboard.
- 360 KB, drives plus associated setup options: These floppy drives are obsolete.
- Backup Reminder
- Virus Check Reminder
- BIOS Boot Support Disable: Problem related to maximum of eight drive supports. Resolved.
- Independently updateable BIOS strings: BIOS supports five languages by default. Feature unused on previous products.

Appendix B: Specifications Supported

The following specifications are supported by the SSH4 Server Platform:

Specification	Revision	Information
POST Memory Manager Specification	1.01	
Advanced Configuration and Power Interface Specification	1.0b	http://www.teleport.com/~acpi
Wired for Management Baseline Specification	2.0	
System Management BIOS Reference Specification	2.3.1	
Hardware Design Guide for Microsoft Windows NT	2.0	
System BIOS for IBM PCs, Compatibles, and EISA Computers	Second Edition	ISBN 0-201-57760-7
Plug and Play ISA Specification	1.0A	Relevent sections only.
Plug and Play BIOS Specification	1.0A	
Extended System Configuration Data Specification	1.03	
PCI Local Bus Specification	2.2	
PCI-X Addendum to the PCI Local Bus Specification		
USB Specification	1.1	
PXE (Preboot eXecution Environment) Specification	2.1	As outlined in the WFM baseline specification using an embedded WFM-compliant network device.
BBS (BIOS Boot Specification)	1.01	
Network PC System Design Guildlines	1.0	
ASF Specification	1.0a	

Glossary

Hexadecimal numbers are represented by appending an "h" at the end.

Term	Definition
ACPI	Advanced Configuration & Power Interface
AGP	Advanced Graphics Port
AP	Application Processor
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
ASF	Alert Standard Forum. A sub-committee of the DMTF.
BIOS	Basic Input/Output System
BIST	Built-in Self Test
BMC	Baseboard Management Controller
BSP	Bootstrap Processor
Byte	An 8-bit quantity
CHS	Cylinder Head Sector
CIOB20	Champion* I/O bridge
CNB2.0HE-SL	Champion* north bridge
CMOS	Complementary metal-oxide semiconductor
CSB5	Open South Bridge
DIMM	Dual Inline Memory Module
DMTF	Distributed Management Task Force
DRAM	Dynamic Random Access Memory
DTR	Data Terminal Ready
DWORD	Double word. A 32-bit quantity
EBDA	Extended BIOS Data Area
EC	ACPI Embedded Controller
ECC	Error Correction Code
ESCD	Extended System Configuration Data
GB	1024 megabytes
GUID	Globally Unique ID
I/O	Input/Output
I^2C	Inter Integrated Circuit
I_2O	Intelligent I/O
ID	Identifier
IDE	Integrated Drive Electronics
IMB	Intelligent Management Bus
IMB	Intra Module Bus
IOP	I/O Platform
IPI	Inter Processor Interrupt
IPL	Initial Program Load
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ISA	Industry Standard Architecture
KB	1024 bytes

Term	Definition
KBC	Keyboard Controller
LBA	Logical Block Address
MB	1024 kilobytes
MBE	Multi-bit Error
MBCE	Memory Data Bus Correctable Error
MBUE	Memory Data Bus Ubcorrectable Error
MHz	Megahertz
MPS	Multi-processor Specification
MPS	Multi-processor System
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OEM	Original Equipment Manufacturer
OS	Operating System
PC	Personal Computer
PCI	Peripheral Component Interconnect
PEP	Platform Event Paging
PHP	PCI Hot-plug
PIC	Priority Interrupt Controller
PnP	Plug and Play
POR	Plan of Record
POST	Power-on-Self Test
PXE	Preboot Execution Environment
QWORD	Quad word. A 64-bit quantity.
RAM	Random Access Memory
ROM	Read-only Memory
RTC	Real-time Clock
SBE	Single-bit Error
SCSI	Small Computer Systems Interface
SEL	System Event Log
SM	System Management
SMBIOS	System Management BIOS
SMI	System Management Interrupt.
SMM	Server Management Module
SMP	Symmetric Multi-processing
SSU	System Setup Utility
SVGA	Super Video Graphics Array
USB	Universal Serial Bus
WFM	Wired for Management
Word	A 16-bit quantity

Reference Documents

Refer to the following documents for additional information.[10]

Server System SSH4 Baseboard Specifications:

- SSH4 Baseboard EPS, Revision 1.0
- SSH4 BIOS EPS
- SSH4 Baseboard Management Controller EPS
- Sahalee Core BMC EPS for IPMI v1.5
- SSH4 Server Management EAS
- Platform Instrumentation EPS
- Direct Platform Control EPS
- FRU/SDR Load EPS
- LAN Alert Viewer EPS

Chip Set, On-board Hardware and Processor Specifications:

- Willamette/Foster BIOS Writer's Guide, Revision 1.0
- Extensions to the Intel® Pentium® Pro Processor BIOS Writer's Guide, Revision 3.7
- Extensions to the Intel® Pentium® Pro Processor BIOS Writer's Guide Specification Update, Revision 2.0
- ATI* Rage IIC and ATI VT-4 Graphics Controller Specification Technical Reference Manual, Revision 1.02
- National Semiconductor* PC87417LPC Super I/O for Servers and Workstations
- Adaptec* AIC-7992 ULTRA 320 SCSI Controller Data Book
- *Intel® Xeon™ Processor Electrical, Mechanical, and Thermal Specifications (EMTS).* Rev. No. 1.4.
- *Willamette/Xeon Processor BIOS Writer's Guide* (Intel Corp)
- *Multiprocessor Specification* version 1.4 (Intel Corp)
- *RCC/ServerWorks Champion 1.5 South Bridge (CSB5) Specification.*
- *RCC/ServerWorks Champion I/O Bridge 3.0 (CIOB30) Specification.*
- *RCC/ServerWorks Grand Champion AC/DC Specifications, Version 0.3.*
- *RCC/ServerWorks Reliability Enhanced Memory Controller 1.0 (REMC) Specification.*
- *Serverworks Champion Memory and I/O Controller 1.13 (CMIC) Specification.*
- *PCI Local Bus Specification, Revision 2.2.*
- *PCI-X addendum to the PCI Local Bus Specification.*
- *USB Specification, Revision 1.0.*
- *5 Volt Flash File (28F008SAx8) Datasheet.*
- *PCI Bus Power Management Interface Specification.*
- *AIC-7902 PCI-Dual Channel SCSI Multi-function Controller Data Manual.*

[10] The URLs are accurate as of July 2000. These addresses are provided only for reference and are not kept up to date.

- *ATI RAGE I2C Technical Reference Manual.*
- *I^2C Bus Specification.*
- *Intelligent Platform Management Bus Communications Protocol Specification.*
- *VRM 9.1 DC-DC Converter Specification.*
- *Adaptec AIC-7902 PCI Bus Master Dual-Channel Ultra 320/M SCSI Host Adapter Chip Data Book.*
- *Intel® 82550PM Fast Ethernet Multifunction PCI/CardBus Controller Advance Information Datasheet.*
- *Pentium® Pro Family Developer's Manual*
- *Intel Architecture Software's Developer's Manual*
- *Plug and Play BIOS Specification 1.0a*
- *PC87417 LCP SuperI/O for Servers and Workstations* (National Semiconductor)
- *BIOS Porting Guide for LPC SuperI/O PC87417*
- *Rage XL/XC Register Reference Guide*
- *System Management Bus Specification Revision1.1*
- *Adaptec AIC7902 ULTRA 320/m SCSI Controller Data Book*
- *Analog Devices ADM1026 Technical Data*
- *Low Pin Count (LPC) Interface Specification, Revision 1.0*
- *ATI Rage XL Register Reference Guide*

Industry Standards and Related Documentation:

- PCI Local Bus Specification, Revision 2.1
- PCI Local Bus Specification, Revision 2.2
- PCI BIOS Specification, Revision 2.1
- PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0
- PCI-to-PCI Bridge Architecture Specification, Revision 1.0
- Plug and Play ISA Specification, Revision 1.0a (*http://www.microsoft.com/hwdev/tech/pnp/default.asp*)
- Plug and Play BIOS Specification, Revision 1.0a (*http://www.microsoft.com/hwdev/tech/pnp/default.asp*)
- Extended System Configuration Data Specification 1.03
- APIC External Architecture Specification, Revision 4.0
- Intel Multi-processor Specification, Revision 1.4 (*http://developer.intel.com/design/pro/datashts/242016.htm*)
- Intelligent I/O (I2O) Architecture Specification, Revision 1.5
- System Management BIOS Reference Specification, Version 2.3
- Wired For Management Baseline Specification, Revision 2.0 (*http://www.intel.com/ial/wfm/wfmspecs.htm*)
- SYSID Programming Interface Specification, Version 1.2
- SYSID BIOS Support Interface Requirement Specification, Version 1.2
- Preboot Execution Environment (PXE) Version 2.1 (*http://www.intel.com/ial/wfm/wfmspecs.htm*)

- Preboot Execution Environment BIOS Support Specification, Version 1.1 *(http://developer.intel.com/ial/wfm/design/bibliog.htm)*
- Hardware Design Guide for Microsoft Windows NT, Version 2.0 *(http://www.microsoft.com/hwdev/serverdg.htm)*
- "El Torito" Bootable CD-ROM Format Specification, Version 1.0 *(http://www.phoenix.com/products/specs.html)*
- System BIOS for IBM PCs, Compatibles, and EISA Computers, Second Edition ISBN 0-201-57760-7
- ACPI Specification, Revision 1.0b *(http://www.teleport.com/~acpi/)*
- ACPI Implementer's Guide, Revision 0.50 *(http://www.teleport.com/~acpi/)*
- BIOS Boot Specification, Revision 1.01 *(http://www.phoenix.com/techs/specs.html)*
- POST Memory Manager Specification, Revision 1.01 *(http://www.phoenix.com/techs/specs.html)*
- Intelligent Platform Management Interface (IPMI) Specification V1.0 *(http://developer.intel.com/design/servers/ipmi/spec.htm)*
- Intelligent Platform Management Bus (IPMB) Specification V1.0 *(http://developer.intel.com/design/servers/ipmi/spec.htm)*

Other Specifications:

- Phoenix* BIOS 4.0 Users Manual
- Phoenix* PCI Information Storage Specification, Version 1.0
- Phoenix* NVRAM Storage API V1.03
- DMTF Systems Standard Groups Definition
- Intelligent Platform Management Interface Specification v1.0, rev 1.1

The SSH4 server board supports the Intel® Server Management Version 5.1 server management software. Several additional EPS documents are available to provide technical detail on the feature set of the server management software. These include:

- Client System Setup Utility EPS
- ISC Console EPS
- ISC Customization Guide
- ISC Install EPS
- Service Partition EPS

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