CK25 Clock Driver / Synthesizer Design Guidelines

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CONTENTS

FIGURES

TABLES

1.0. INTRODUCTION

With the introduction of processors powered by less than 3.3 volts, components and I/O will again shift power and signaling levels. New transistor feature sizes dictate that interfaces move to a new 2.5V level.

A key difference in this specification from that of previous processor clock driver specifications is that this device requires that the I/O be operated from multiple power supplies e.g. 3.3V and 2.5V. The 3.3V power supply is used to power a portion of the I/O and the core, and 2.5V is used to power the remaining outputs. Because the two power supplies are independent and because current PC technology does not control the power sequencing for turning on or turning off the system, latch-up and potentially damaging conditions can exist during these power sequencing phases. Your design is required to operate properly and make no requirement of the system to sequence the power supplies.

This 2.5V signaling specification follows the JEDEC standard 8-X. The 3.3V signaling specification follows the JEDEC standard for LVTTL signaling. The 3.3V power delivery specification follows the JEDEC standard range 3.3V ±5%.

This specification provides a baseline of development for the Pentium® II processor desktop platform clock driver requirements. It is not the only solution that can be arrived at, but is generic enough to provide solutions for most desktop platforms.

This specification is also intended to aid computer OEMs in defining and using the clock synthesis components for all desktop system level clocking requirements.

1.1. Clock Synthesizer Overview

Clock synthesizers are expected to source multiple clock types, e.g. Host clock, PCI clock, system clock, and others as defined by system requirements. This specification deals with the CPU clock, other Host bus clocks, PCI clocks, IOAPIC clocks, Floppy clock, Serial Bus Clock, Keyboard controller clock and the Reference clocks.

There are no references to the number of clocks or the types of clocks any given clock driver chip will supply in the main body of the specification. An example of a clock driver design is located in Appendix A. The number of clocks and the types of clocks, package type and load conditions are specified.

Timing and electrical requirements for all of the above mentioned clocks are provided. Information about the PCI CLK reflects the requirements as specified in the PCI specification Chapter 4. Examples of routing topologies, loading and signal quality specifications are outlined in Section 5

Appendix A provides a sample design implementation of this specification. This sample can also be used as a reference when developing a custom clock synthesizers.

1.2. Applicable Documents

The latest revision of the following are used as reference documents:

JEDEC Standard No. 8-1A, Interface Standard for 3.3±0.3 V Power Supply & Digital Integrated Circuits.

JEDEC Standard No. 8-X, 2.5V(0.2V (normal range), and 1.8V to 2.7V (wide range) Power supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuit.

PCI Specification 2.1

IBIS Modeling Specification

See Section 6 on how to obtain copies of PCI and IBIS specifications.

1.3. Drive Specification

The primary motivation for this document is to specify all of the issues associated with split I/O voltage and the effects of it on system power delivery, signaling, timing and test. The signaling, timing, and test characteristics change with the different supply voltages and need to be thoroughly worked through for optimal system performance.

The Clock driver output buffers are specified in terms of their AC switching characteristics and their DC drive characteristics as such, the primary electrical parameters are the voltage to current relationship (V/I), the rise and fall time (Trise/Tfall) of the driver through its active switching range, and critical timing parameters.

2.0. ELECTRICAL REQUIREMENTS

This section details the electrical parameters for two 2.5V clock output buffers, two 3.3V clock output buffers and a 5.0V compatible 3.3V PCI clock driver output buffer. Two types of 2.5V and 3.3V drivers are needed to compensate for corresponding board layout topologies.

Due to the new low voltages (<3.0V) now required by CPUs normal TTL voltage levels are no longer feasible to produce. A new signaling level to support 2.5V is being used for that portion of the design. The JEDEC standard called "2.5V±0.2V (normal range), and 1.8V to 2.7V (wide range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuit", hereafter referred to as 2.5V signaling, and a 2.5V supply is being used.. The 3.3V clocking requirements still support the TTL-level compatible requirements and will be called by their appropriate name, LVTTL, even though they are TTL signaling levels.

A clock driver designed to operate in the Pentium II processor signaling environment will not necessarily operate correctly in the 3.3V LVTTL or the 5.0V PCI I/O bus signaling environment. Great care must be taken in this design environment to properly support the extremely tight timing requirements between clocks.

The clock driver for all clocks must generate monotonic edges through the threshold regions as specified for each signaling environment. Many conditions exist in the design of clock chips and the system that can affect the monotonic operation of the clock driver. Power supply noise, pin inductance and capacitance, ratio of clock signals to Vddq and Vss pins (SSO), and routing topology will affect the monotonicity of these clocks. The electrical requirements outlined here ensure components connect directly together without any external buffers or other "glue" logic. Series terminating resistors may be required to keep noise within limits on strong drivers under lightly loaded conditions. Components should be designed to operate within the "commercial" range of environmental parameters. However, this does not preclude the option of other operating environments at the vendor's discretion.

Clock driver output buffers are specified in terms of their V/I curves and Trise/Tfall times. Limits on acceptable V/I curves provide for a maximum output impedance that can achieve acceptable timing in typical configurations, and for a minimum output impedance that keeps the reflected wave within reasonable bounds for signal quality. It is important to understand that drive strength and layout topology go hand in hand. Point-to-point or multiple stubs at the receiver end will work with a weaker driver, whereas a route that splits at the driver requires a stronger buffer. The signal quality problems of a strong driver under light loads can be negated somewhat with a series termination resistor placed as close to the driver as possible. See Section 5 for more detail.

An example of a clock driver design is contained in Appendix A. This is not the only solution that can be achieved, however it is a good starting point to design a component to meet specific design requirements.
Due to the mixed power supplies now required for proper system operation, it is very important to understand that specific power supply sequencing is not supported. The clock synthesizer CAN NOT require power sequencing requirements in the system.

2.1. DC Specifications (Clock Driver)

DC parameters must be sustainable under steady state (DC) conditions.

Table 1. Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	-0.5	4.6	V	
V_{DDQ2}	2.5V I/O Supply Voltage	-0.5	3.6	V	
V_{DDQ3}	3.3V I/O Supply Voltage	-0.5	4.	V	
Ts	Storage Temperature	-65	150	(C	

Table 2. Absolute Maximum DC I/O

Symbol	Parameter	Min	Max	Units	Notes
Vih3	3.3V Input High Voltage	-0.5	4.6	V	1
Vil3	3.3V Input Low Voltage	-0.5		V	
ESD prot.	Input ESD protection	2		kV	

1. Max Vih is not to exceed maximum VDD.

Table 3. DC Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{DDQ3}	3.3V I/O Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{DDQ2}	2.5V I/O Supply Voltage	2.5 ±5%	2.375	2.625	V	4
V_{DD} = 3.3±5%						
V_{ih3}	3.3V Input High Voltage		2.0	V_{DDQ3} +0.3	V	
V_{il3}	3.3V Input Low Voltage		VSS-0.3	0.8	V	
I_{il}	Input Leakage Current	$0 < V_{in} < V_{DDQ3}$	-5	+5	µA	3
V_{DDQ2} = 2.5±5%						
V_{oh2}	2.5V Output High Voltage	Ioh = -1 mA	2.0		V	1
V_{ol2}	2.5V Output Low Voltage	Iol = 1 mA		0.4	V	1
V_{DDQ3}= 3.3±5%						
V_{oh3}	3.3V Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{ol3}	3.3V Output Low Voltage	Iol = 1 mA		0.4	V	1
V_{DDQ3}= 3.3±5%						
V_{poh}	PCI Bus Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{pol}	PCI Bus Output Low Voltage	Iol = 1 mA		0.55	V	5

Table 3. DC Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
C_{in}	Input Pin Capacitance			5	pF	2
C_{out}	Output Pin Capacitance			6	pF	2
L_{pin}	Pin Inductance			7	nH	2
Ta	Ambient Temperature	No Airflow	0	70	°C	

NOTES:

1. Signal edge is required to be monotonic when transitioning through this region.
2. This is a recommendation, not an absolute requirement as the package size and type are not being specified. The actual value should be provided with the component data sheet.
3. Input Leakage Current does not include inputs with Pull-up or Pull-down resisters. Inputs with resistors should state current requirements.
4. No power sequencing is implied or allowed to be required in the system.
5. V_{pol} limit is consistent with 5 Volt PCI specification.

2.2. Buffer Specifications: 2.5V / 3.3V Clocks, and PCI Clocks

The V/I curves, and Trise/Tfall specifications are targeted at achieving acceptable switching behavior under the load conditions as described in section 5 of this specification. Pull-up and pull-down sides for each of the buffers have separate V/I curves which are provided in section 2.2. The DC drive curve specifies steady state conditions that must be maintained, but does not indicate real output drive strength. The shaded areas on the V/I curves shown in this section define the allowable range for output driver characteristics.

AC parameters must be guaranteed under transient switching (AC) conditions. The sign on all current parameters (direction of current flow) is referenced to a ground inside the component; i.e. positive currents flow into the component while negative currents flow out of the component.

Buffer Name	VCC Range (V)	Impedance (Ohms)	Buffer Type
CPU	2.375 - 2.625	13.5 - 45	Type 1
IOAPIC	2.375 - 2.625	9- 30	Type 2
KBC, FD, USB, REF1, REF2	3.135 - 3.465	20 - 60	Type 3
REF0	3.135 - 3.465	10 - 30	Type 4
PCI	3.135 - 3.465	12 - 55	Type 5

2.2.1. TYPE 1: CPU (2.5V) BUFFER CHARACTERISTICS

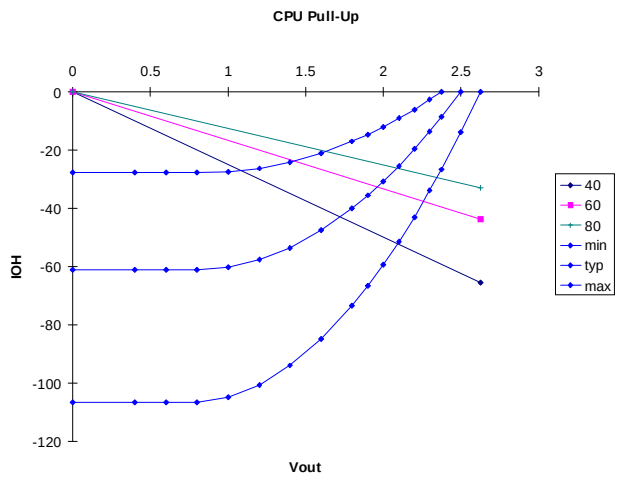
Table 4. TYPE 1: CPU Clock Buffer Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	V_{out} = 1.0 V	-27			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 2.375 V			-27	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.2 V	27			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.3 V			30	mA	1
t_{rh}	2.5V Type 1 Output Rise Edge Rate	2.5V ±5% @ 0.4V - 2.0V	1/1		4/1	V/ns	2
t_{fh}	2.5V Type 1 Output Fall Edge Rate	2.5V ±5% @ 2.0V - 0.4V	1/1		4/1	V/ns	2

NOTES:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 13 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are V_{il}=0.7 and V_{ih}=1.7 Volts.
5. Ron 13.5-45 Ohm with a 29 Ohm nominal driver impedance.
6. Ron = V_{out}/I_{oh}, V_{out}/I_{ol} measured at $V_{CC}/2$.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-28	-61	-107
0.4	-28	-61	-107
0.6	-28	-61	-107
0.8	-28	-61	-107
1	-27	-60	-105
1.2	-26	-58	-101
1.4	-24	-53	-94
1.6	-21	-48	-85
1.8	-17	-40	-73
1.9	-15	-36	-67
2	-12	-31	-59
2.1	-9	-25	-51
2.2	-6	-20	-43
2.3	-3	-14	-34
2.375	0	-9	-27
2.5		0	-14
2.625			0

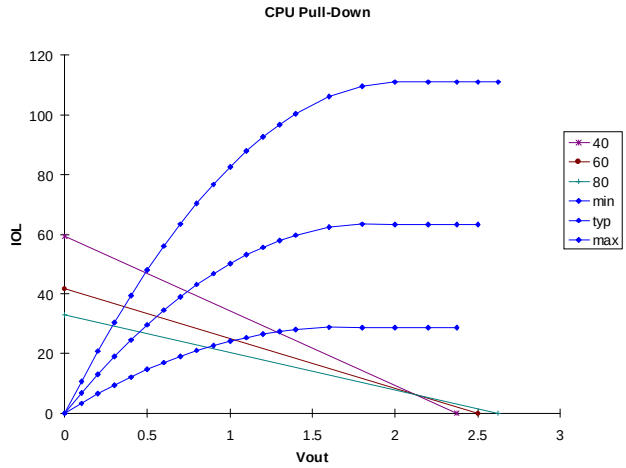


NOTES:

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 4.

Figure 1. TYPE 1: CPU Clock Output Buffer Pull-Up Characteristics

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.1	3	7	11
0.2	6	13	21
0.3	9	19	30
0.4	12	24	40
0.5	15	30	48
0.6	17	35	56
0.7	19	39	63
0.8	21	43	70
0.9	23	47	77
1	24	50	83
1.1	25	53	88
1.2	27	56	93
1.3	27	58	97
1.4	28	60	100
1.6	29	62	106
1.8	29	63	110
2	29	63	111
2.2	29	63	111
2.375	29	63	111
2.5		63	111
2.625			111



NOTES:

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 4.

Figure 2. TYPE 1: CPU Clock Output Buffer Pull-Down Characteristics

2.2.2. TYPE 2: IOAPIC (2.5V) BUFFER CHARACTERISTICS

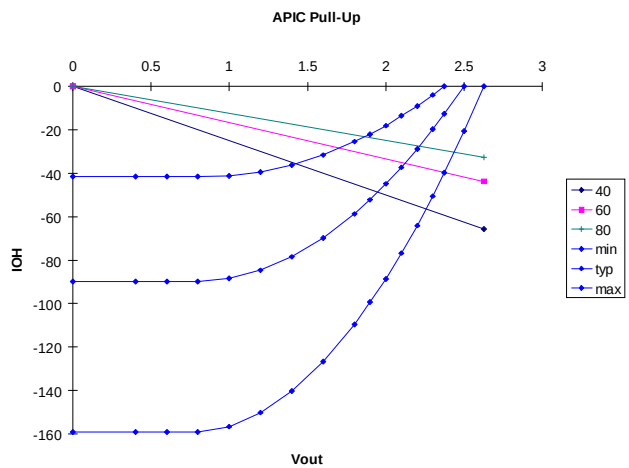
Table 5. TYPE 2: IOAPIC Clock Buffer Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	V_{out} = 1.4 V	-36			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 2.5V			-21	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.0 V	36			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.2 V			31	mA	1
t_{rh}	2.5V Type 2 Output Rise Edge Rate	2.5V ±5% @ 0.4V - 2.0V	1/1		4/1	V/ns	2
t_{fh}	2.5V Type 2 Output Fall Edge Rate	2.5V ±5% @ 2.0V - 0.4V	1/1		4/1	V/ns	2

NOTES:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 13 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across V_{CC} , process and temperature range.
4. Receiver logic thresholds are V_{il}=0.7 and V_{ih}=1.7 Volts.
5. Ron 9-30 Ohm with a 20 Ohm nominal driver impedance.
6. Ron = V_{out}/I_{oh}, V_{out}/I_{ol} measured at $V_{CC}/2$.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-42	-90	-159
0.4	-42	-90	-159
0.6	-42	-90	-159
0.8	-42	-90	-159
1	-41	-88	-157
1.2	-39	-85	-150
1.4	-36	-78	-140
1.6	-32	-70	-127
1.8	-25	-59	-109
1.9	-22	-52	-99
2	-18	-45	-89
2.1	-14	-37	-77
2.2	-9	-29	-64
2.3	-4	-20	-50
2.375	0	-13	-40
2.5		0	-21
2.625			0

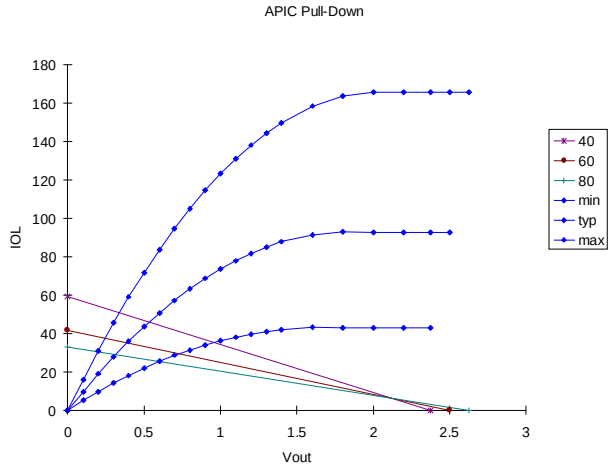


NOTES:

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 5.

Figure 3. TYPE 2: IOAPIC Clock Output Buffer Pull-Up Characteristics

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.1	5	10	16
0.2	10	19	31
0.3	14	28	45
0.4	18	36	59
0.5	22	44	72
0.6	25	51	84
0.7	29	57	95
0.8	31	63	105
0.9	34	69	114
1	36	73	123
1.1	38	78	131
1.2	40	82	138
1.3	41	85	144
1.4	42	88	150
1.6	43	91	158
1.8	43	93	163
2	43	93	165
2.2	43	93	165
2.375	43	93	165
2.5		93	165
2.625			165



NOTES:

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 5.

Figure 4. TYPE 2: IOAPIC Clock Output Buffer Pull-Down Characteristics

2.2.3. TYPE 3: KBC, FD, USB, REF1, REF2 (3.3V) BUFFER CHARACTERISTICS

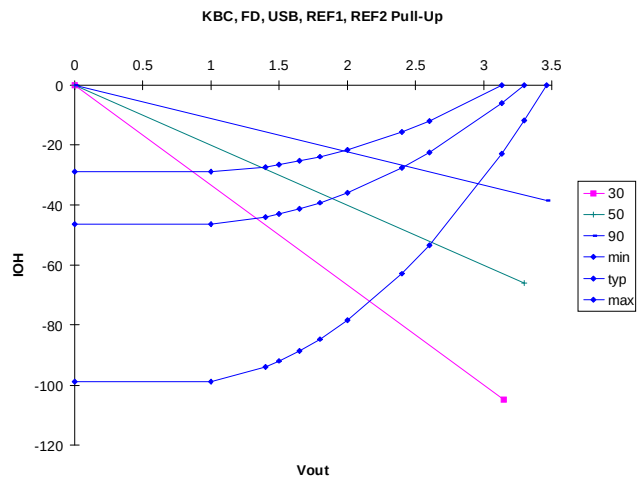
Table 6. 3.3V Clock Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	V_{out} = 1.0 V	-29			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-23	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95V	29			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			27	mA	1
t_{rh}	3.3V Type 3 Output Rise Edge Rate	3.3V @ 0.4V - 2.4V	0.5		2.0	V/ns	2
t_{fh}	3.3V Type 3 Output Fall Edge Rate	3.3V @ 2.4V - 0.4V	0.5		2.0	V/ns	2

NOTES:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 13 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across V_{CC} , process and temperature range.
4. Receiver logic thresholds are V_{il}=0.8 and V_{ih}=2.0 Volts.
5. Ron 20-60 Ohm with a 40 Ohm nominal driver impedance.
6. Ron = V_{out}/I_{oh}, V_{out}/I_{ol} measured at $V_{CC}/2$.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-29	-46	-99
1	-29	-46	-99
1.4	-27	-44	-94
1.5	-27	-43	-92
1.65	-25	-41	-89
1.8	-24	-39	-85
2	-22	-36	-79
2.4	-16	-28	-63
2.6	-12	-22	-53
3.135	0	-6	-23
3.3		0	-12
3.465			0

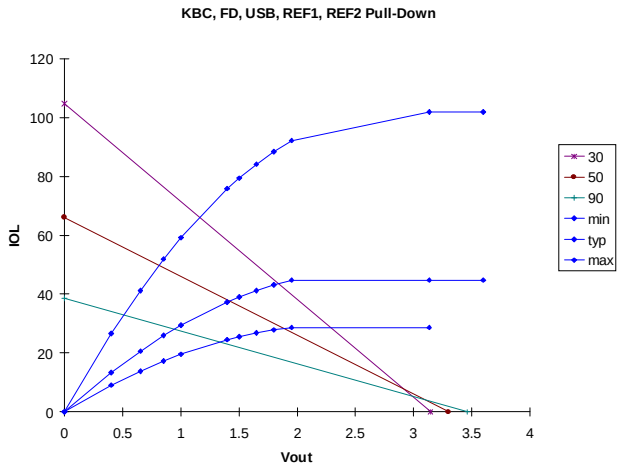


NOTES:

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 6 3.3V Clock Operating Requirements.

Figure 5. TYPE 3: 3.3V Clock Output Buffer Pull-Up Characteristics

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.4	9	13	27
0.65	14	21	41
0.85	17	26	52
1	20	29	59
1.4	25	37	76
1.5	26	39	79
1.65	27	41	84
1.8	28	43	88
1.95	29	45	92
3.135	29	45	102
3.6		45	102



NOTES:

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 6 3.3V Clock Operating Requirements.

Figure 6. TYPE 3: 3.3V Clock Output Buffer Pull-Down Characteristics

2.2.4. TYPE 4: REF0 (3.3 V) CLOCK BUFFER CHARACTERISTICS

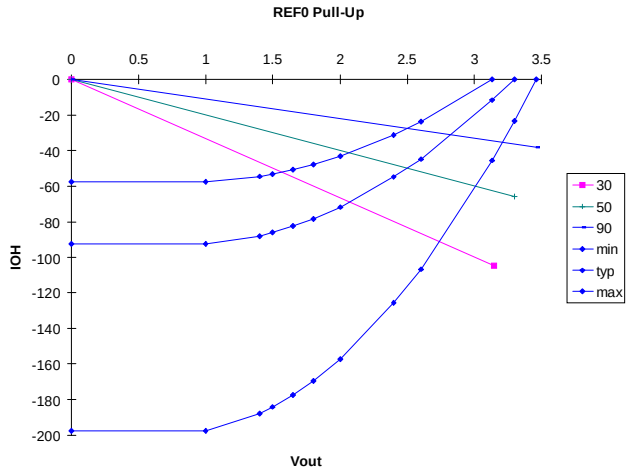
Table 7. REF0 Clock Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	V_{out} = 1.65 V	-51			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-46	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.65V	54			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			53	mA	1
t_{rh}	3.3V Type 4 Output Rise Edge Rate	3.3V @ 0.4V - 2.4V	1/1		4/1	V/ns	2
t_{fh}	3.3V Type 4 Output Fall Edge Rate	3.3V @ 2.4V - 0.4V	1/1		4/1	V/ns	2

NOTES:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 13 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across V_{CC} , process and temperature range.
4. Receiver logic thresholds are V_{il}=0.8 and V_{ih}=2.0 Volts.
5. Ron 10-30 Ohm with a 20 Ohm nominal driver impedance.
6. Ron = V_{out}/I_{oh}, V_{out}/I_{ol} measured at $V_{CC}/2$.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-58	-93	-198
1	-58	-93	-198
1.4	-55	-88	-188
1.5	-53	-86	-184
1.65	-51	-83	-177
1.8	-48	-78	-170
2	-43	-72	-157
2.4	-31	-55	-126
2.6	-24	-45	-107
3.135	0	-12	-46
3.3		0	-23
3.465			0

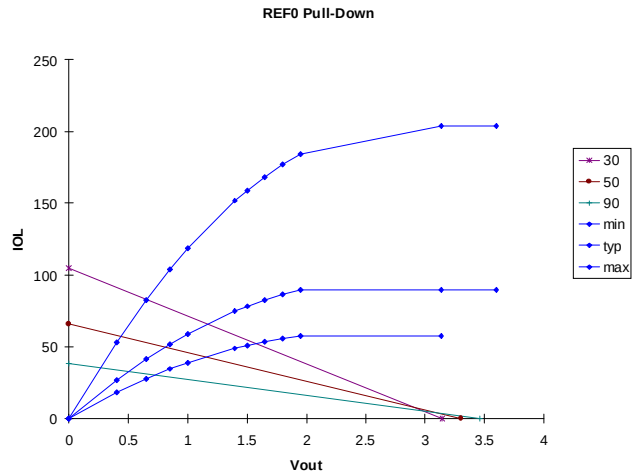


NOTES:

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 7 REF0 Clock Operating Requirements.

Figure 7. TYPE 4: REF0 Clock Output Buffer Pull-Up Characteristics

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.4	18	27	53
0.65	28	41	83
0.85	34	52	104
1	39	59	118
1.4	49	75	152
1.5	51	78	159
1.65	54	83	168
1.8	56	86	177
1.95	57	89	184
3.135	57	89	204
3.6		89	204



NOTES:

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 7 REF0 Clock Operating Requirements.

Figure 8. TYPE 4: REF0 Clock Output Buffer Pull-Down Characteristics

2.2.5. TYPE 5: PCI CLOCK BUFFER CHARACTERISTICS

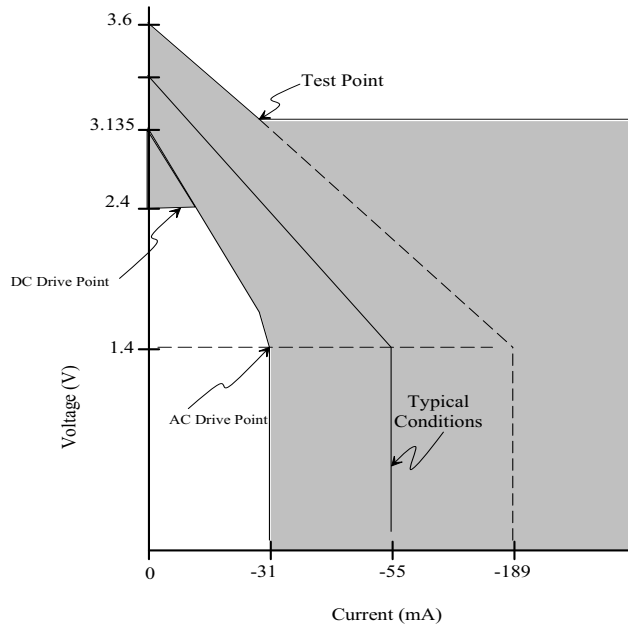
Table 8. PCI Clock AC Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	V_{out} = 1.0 V	-33			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-33	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95V	30			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			38	mA	1
t_{rh}	3.3V Type 4 Output Rise Edge Rate	3.3V @ 0.4V - 2.4V	1/1		4/1	V/ns	2
t_{fh}	3.3V Type 4 Output Fall Edge Rate	3.3V @ 2.4V - 0.4V	1/1		4/1	V/ns	2

NOTES:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 13 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across V_{CC} , process and temperature range.
4. Receiver logic thresholds are V_{il}=0.8 and V_{ih}=2.0 Volts.
5. Ron 12-55 Ohm with a 30 Ohm nominal driver impedance.
6. Ron = V_{out}/I_{oh}, V_{out}/I_{ol} measured at $V_{CC}/2$.
7. See PCI specification for additional PCI details.

	Pull-Up		
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-34	-59	-195
1	-33	-58	-194
1.4	-31	-55	-189
1.5	-30	-54	-184
1.65	-28	-52	-172
1.8	-25.5	-50	-159
2	-22	-46	-140
2.4	-14.5	-35	-100
2.6	-11	-28	-83
3.135	0	-6	-33
3.3		0	-19
3.6			0

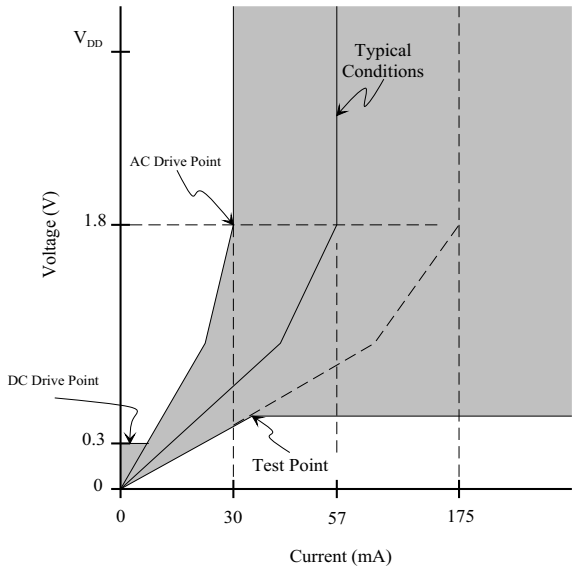


NOTES:

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements.
2. This drawing is not to scale. Comparisons should be made to the data provided in the table.

Figure 9. TYPE 5: PCI Clock Output Buffer Pull-up Characteristics

Pull-Down			
Voltage (V)	I (mA) min	I(mA) typ	I (mA) max
0	0	0	0
0.4	9.4	18	38
0.65	14	30	64
0.85	17.7	38	84
1	20	43	100
1.4	26.5	53	139
1.5	28	55	148
1.65	29	56	163
1.8	30	57	175
1.95	30	58	178
3.135	31	59	187
3.6	32	59	188



NOTES:
1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table.

Figure 10. TYPE 5: PCI Clock Output Buffer Pull-Down Characteristics

2.2.6. VENDOR PROVIDED SPECIFICATIONS

Vendors should make the following information available in their data sheets:

- Pin capacitance for all pins (min and max).
- Pin inductance for all pins (min and max).
- Output V/I curves under switching conditions. Two graphs / tables should be given for each output type used: one for driving high, the other for driving low. Both should show best-worst case conditions.
- Loaded rise/fall times for each output type for loads as specified in the test section of this specification.
- Absolute maximum data, including operating and non-operating temperature, DC maximums, etc.

It is strongly recommended that component vendors make the following information electronically available in the IBIS model format. Include the following minimum information:

- Output V/I curves under switching conditions. Two curves should be supplied one for driving high, the other for driving low. Both should show best-typical-worst curves.
- Unloaded rise/fall times for each output type as specified by IBIS.
- Package Resistance (R_pkg [min, max]); Package Inductance (L_pkg [min, max]); Package Capacitance (C_pkg [min, max]); Component Capacitance (C_comp [min, max]).

3.0. AC TIMING

3.1. Timing Requirements

Table 9. AC Timing Requirements

		66 MHz		60 MHz			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
tHKP	Host CLK period	15		16.7		ns	
tHKH	Host CLK high time	5.2		6.0		ns	1,5
tHKL	Host CLK low time	5.0		5.8		ns	1,6
tHRISE	Host CLK rise time	0.4	1.6	0.4	1.6	ns	8
tHFALL	Host CLK fall time	0.4	1.6	0.4	1.6	ns	8
tJITTER	Host CLK Jitter (cycle-cycle)		250		250	ps	2
Duty Cycle	Measured at 1.25V	45	55	45	55	%	
tHSKW	Host Bus CLK Skew		250		250	ps	2
tHSTB	Host CLK Stabilization from power-up		3		3	ms	7
tPKP	PCI CLK period	30.0	∞	33.3	∞	ns	3
tPKPS	PCI CLK jitter		500		500	ps	2
tPKH	PCI CLK high time	12		13.3		ns	1
tPKL	PCI CLK low time	12		13.3		ns	1
tPSKW	PCI Bus CLK Skew		500		500	ps	2
tHPOFFSET	Host to PCI Clock Offset	1.0	4.0	1.0	4.0	ns	2,4
tPSTB	PCI CLK Stabilization from power-up		3		3	ms	7

NOTES:

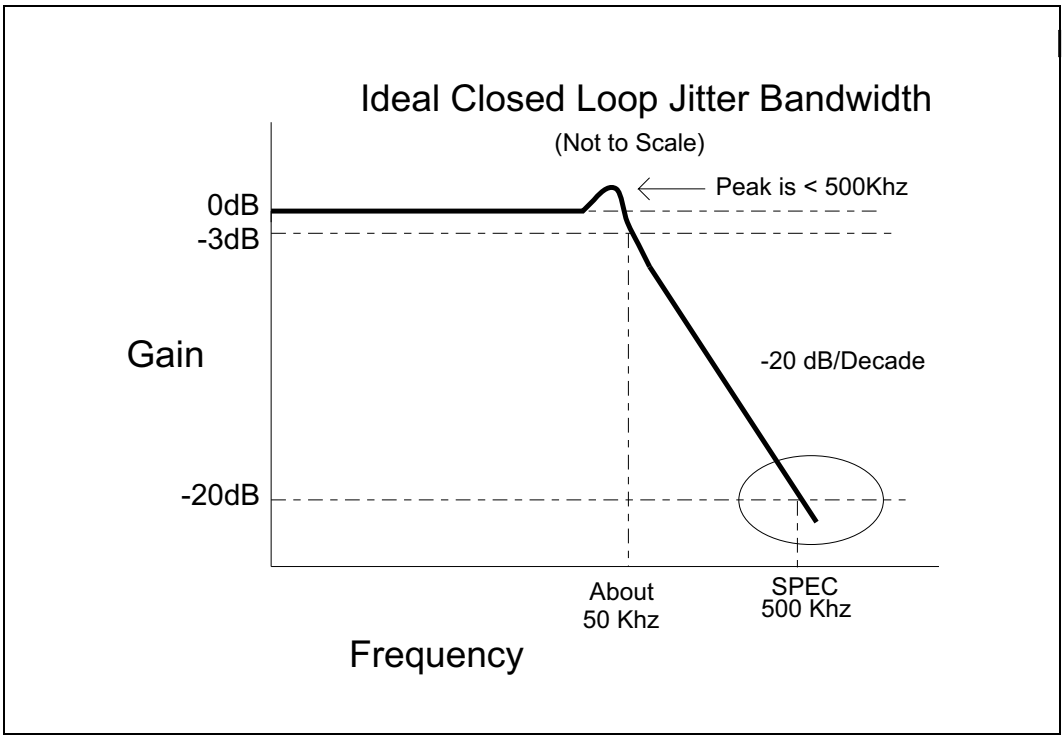
1. Output drivers must have the characteristics noted in Section 2 above.
2. Jitter, skew and offset are measured on the rising edge of CLKs at 1.25V for the 2.5V clocks and at 1.5V for the 3.3V clocks. Duty cycle is measured at 1.25V for the 2.5 V clocks and 1.5V for the 3.3V clocks.
3. PCI Clock is the host clock divided by two.
4. The Host CLK must always lead the PCI CLK as shown in Figure 12. This must be guaranteed by design under loaded conditions. This is a function of drive strength as well as routing topologies. This is a combined CLK driver requirement and a layout requirement.
5. tHKH is measured at 2.0V as shown in Figure 13.
6. tHKL is measured at 0.4V as shown in Figure 13.
7. The time specified is measured from when Vddq achieves its nominal operating level (typical condition Vddq = 3.3V) till the frequency output is stable and operating within specification.
8. tHRISE and tHFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.0V (1mA) JEDEC Specification.

3.2. Multiple PLL Jitter Tracking Specification.

The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. This 1:1 relationship is critical when the clock driver drives two or more PLLs. A worst case timing issue would occur if one PLL attenuated the jitter and another device (PLL or nonPLL) tracked the jitter completely. To reduce the possibility of this we require that the -20dB attenuation point be less than or equal to 500Khz. Most clock vendors do not specify their jitter bandwidth characteristics or specify it only at the -3dB level. To allow for greatest flexibility in loop design we require the vendor to provide the -20dB point. This specification may be guaranteed by design and/or measured with a spectrum analyzer.

This specification is intended to replace/clarify previous specifications which were stated as:

> "To ensure a 1:1 jitter frequency relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 Khz and 1/3 of the clock operating frequency."



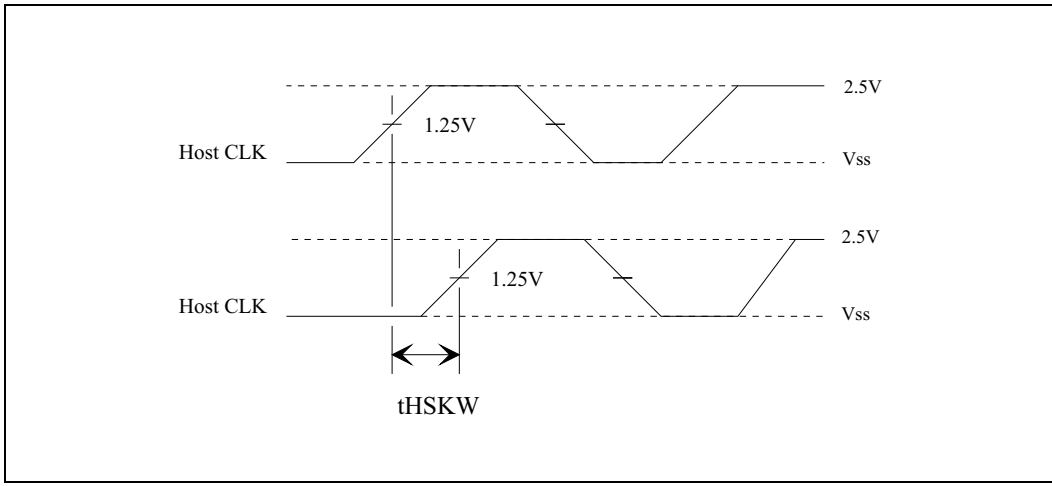


Figure 11. Host CLK to Host CLK Skew

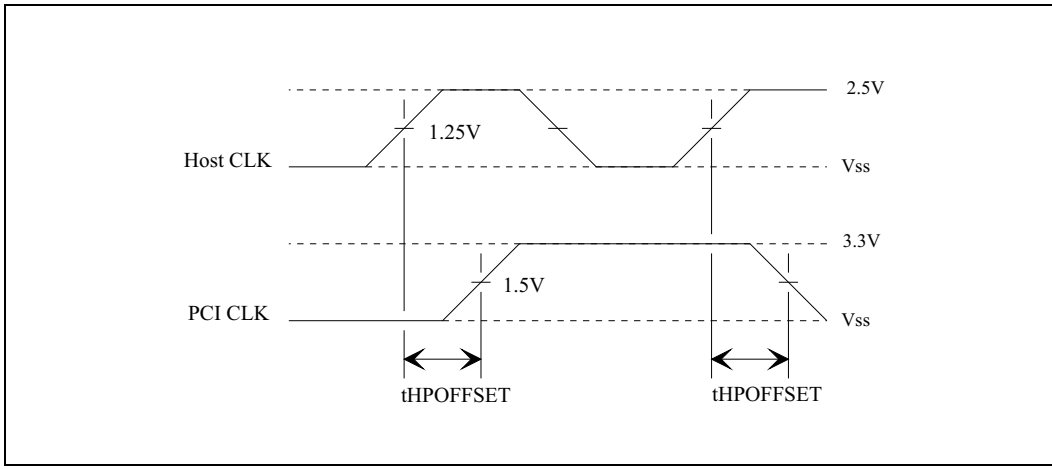


Figure 12. Host CLK to PCI CLK Offset

4.0. TEST AND MEASUREMENT

Ideally this measurement would be made under a no load condition and derating tables provided for skew and jitter under loaded conditions. It is understood that this is not possible and a load will exist when taking a measurement. Data obtained by measurement should be derated back to 0 pf for reporting purposes and tables provided for skew and jitter.

Table 10. Minimum and Maximum Expected Capacitive Loads

Clock	Min Load	Max Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads.
PCI Clocks (PCLK)	- - -	30	pF	Must meet PCI 2.1 requirements
24 MHz Clock	10	20	pF	1 device load
48 MHz Clock	10	20	pF	1 device load
Ref0	20	45	pF	3 - 4 device loads
Ref1	10	20	pF	1 device load
Ref2	10	20	pF	1 device load
IOAPIC	10	20	pF	2 device loads

NOTES:

1. Maximum rise/fall times are to be guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are to be guaranteed at minimum specified load for each type of output buffer

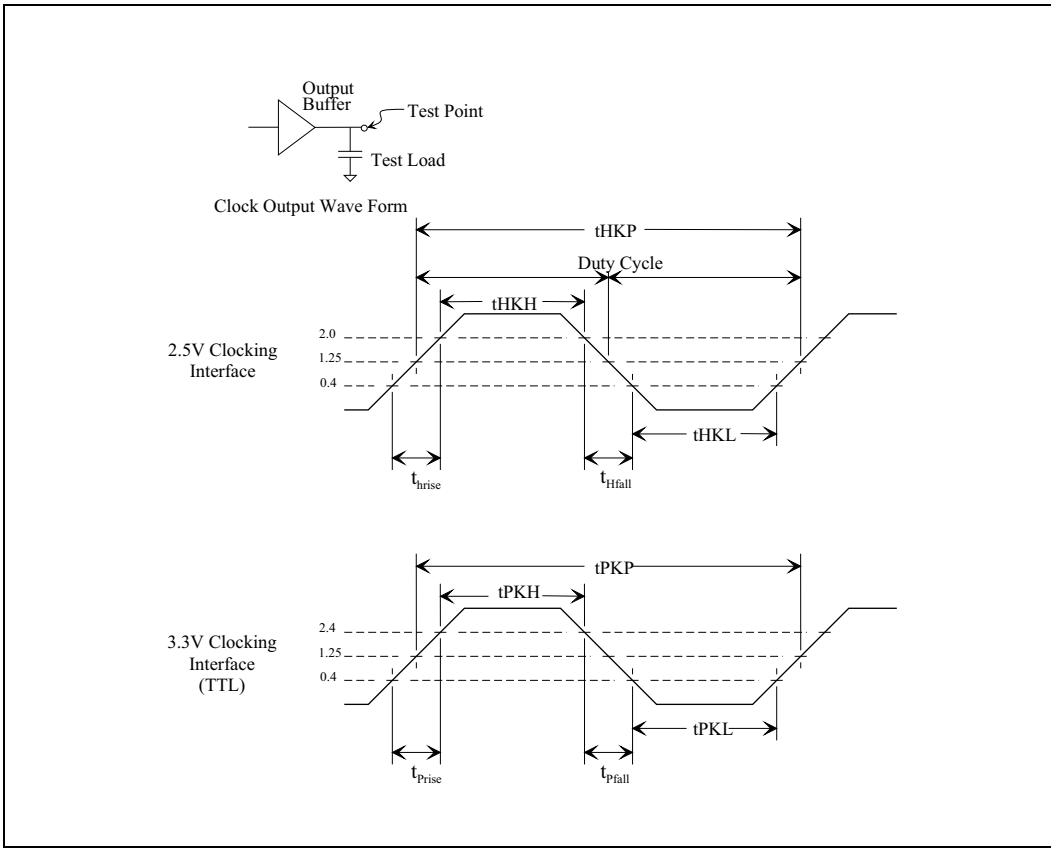


Figure 13. Clock Waveform

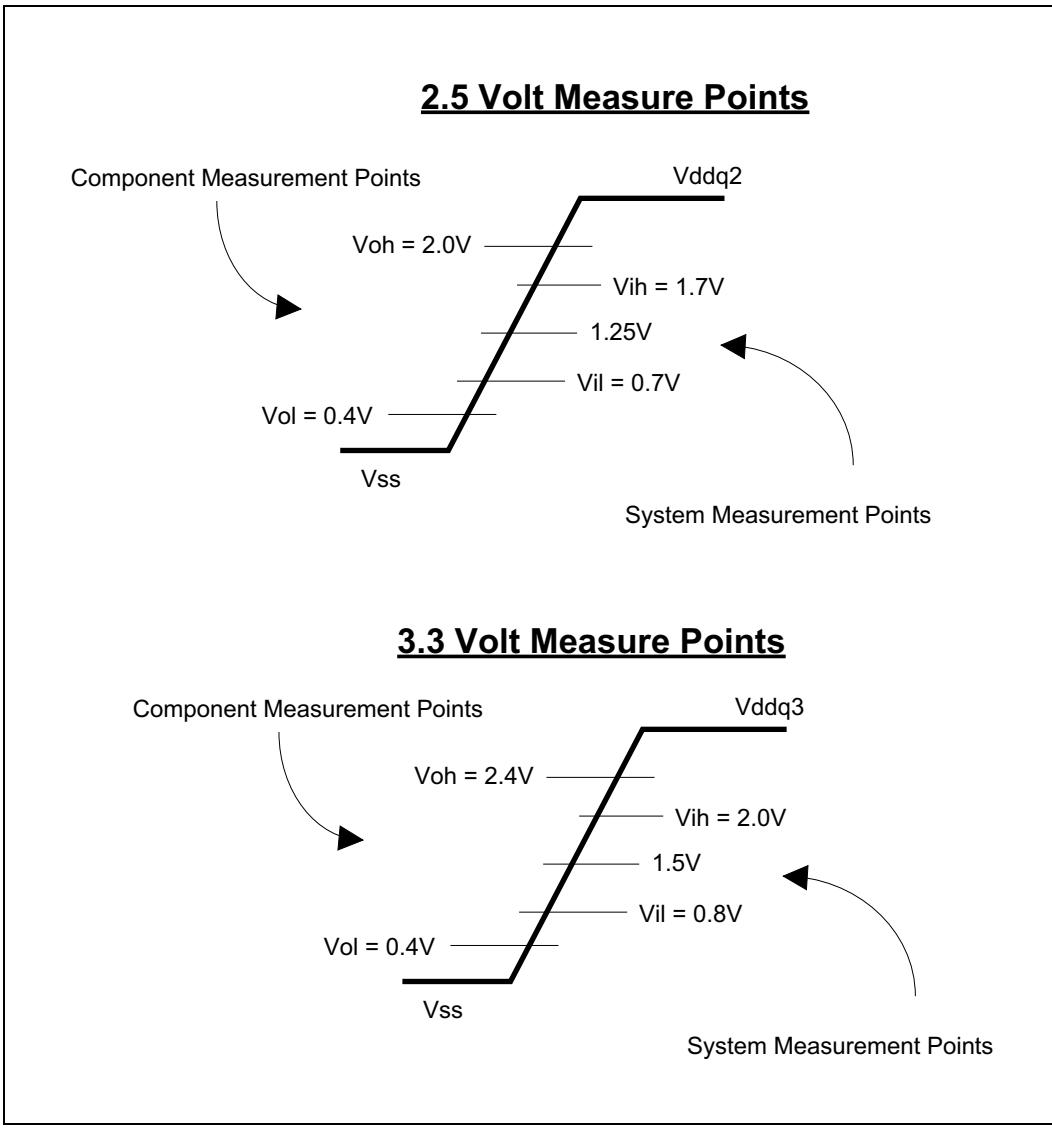


Figure 14. Clock Platform and Component Measure Points

5.0. SYSTEM CONSIDERATIONS

The diagrams shown below are typical clock routing topologies for Pentium II processor-based desktop platforms. And are meant as an aid to the OEM in laying out clocks for PC Desktop platforms. It is also meant as an aid to clock driver vendors to simulate and check their buffers.

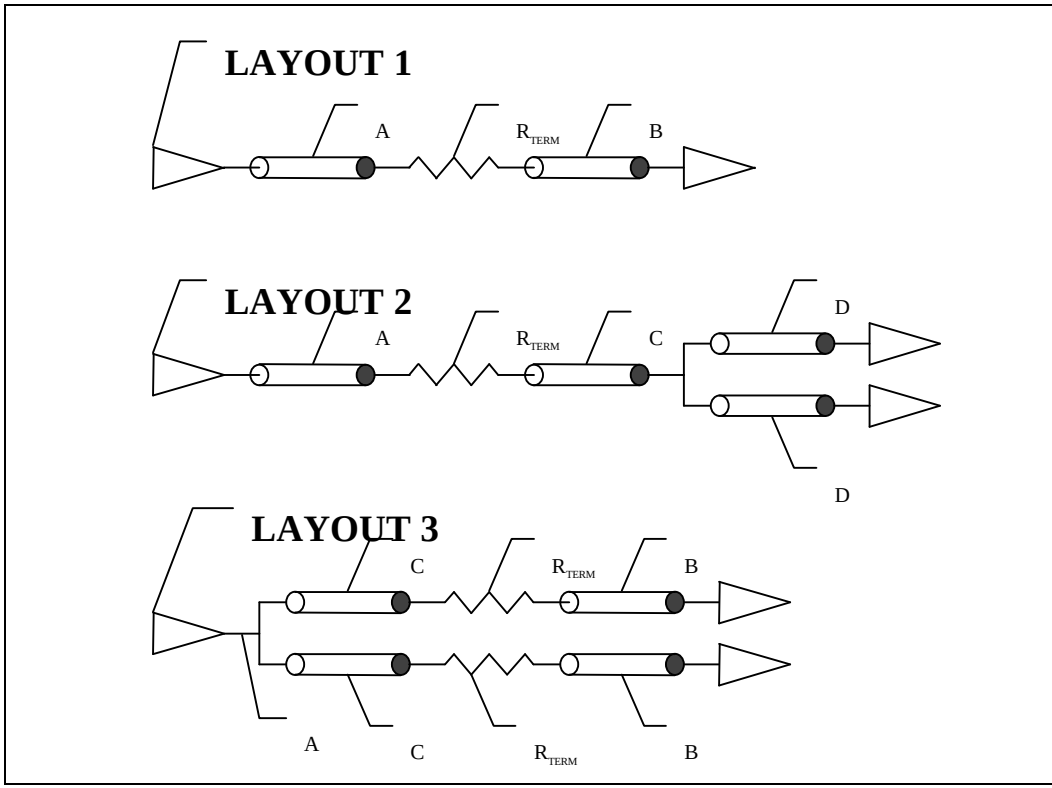


Figure 15. Standard Clock Layout Topologies

Table 11. Layout Dimensions

CLK	Topology	A	B	C	D	R_{TERM}	Notes
CPU	LAYOUT 1	0.25"- 0.5 "	3" - 7"	n/a	n/a	33	1
CPU	LAYOUT 2	0.25"- 0.5"	n/a	3" - 6"	0.25"- 0.5"	33	2
IOAPIC	LAYOUT 3	0.25"- 0.5"	3" - 7"	0.25"- 0.5"		33	3
48MHz, 24MHz, REF1, REF2	LAYOUT 1	0.25"- 0.5"	3" - 7"	n/a	n/a	22	4
REF0	LAYOUT 2	0.25" - 0.5"	n/a	1" - 3"	3" - 7"	22	5

NOTES:

1. Primary topology for CPU outputs. One load.
2. Secondary topology for CPU outputs. Two loads.
3. REQUIRED to drive two loads, split at receiver.
4. Primary topology. One loads.
5. Similar to layout #2. Drives three to four ISA slots.

Table 12. Board Level Simulation Conditions

Symbol	Parameter	Slow	Typ	Fast
Z_O	Line Impedance	55 Ω	70 Ω	85 Ω
S	Line Velocity	2.4 ns/ft	2.2 ns/ft	1.9 ns/ft
V_{DD}	Core Supply Voltage	3.135 V	3.30V	3.465 V
V_{DDQ}	I/O Supply Voltage	2.375 V	2.5 V	2.625 V
T	Ambient Temperature (no airflow)	70°C	25° C	0° C

The topologies listed above in Figure 15 are standard topologies for Desktop PC clock routings. The parameters listed in Table 11 above give the minimum and maximum dimension ranges to be used for clock buffer driver simulation.

Series termination resistors will be required to control the output driver variation from platform to platform. Series termination should be placed as close to the driver as possible for best signal quality results.

The low impedance outputs for the IOAPIC and the REF0 clocks are required to reduce the sensitivity of the topologies to output buffer edge-rate variation in the non point-to-point layout topologies shown in Figure 15.

Table 13. Characteristics at Clock Destination

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{ih2}	2.5V Input High Voltage		1.7	V_{DDQ} +0.3	V	1
V_{il2}	2.5V Input Low Voltage		-0.3	0.7	V	1
V_{ih3}	3.3V Input High Voltage		2.0	V_{DDQ} +0.3	V	1
V_{il3}	3.3V Input Low Voltage		-0.3	0.8	V	1
C_{in}	Input Pin Capacitance			6	pF	

NOTES:

1. Signal edge is required to be monotonic when transitioning through this region.

The clock input to the processor and the chip-set must meet signal quality specifications to guarantee the clock signal is sensed properly and to ensure the clock signal does not affect the long term reliability of the components. There are two signal quality parameters defined: Overshoot/Undershoot and Ringback. Both signal quality parameters are shown in Figure 16 below.

Table 14. AC Signal Quality Requirement at Destination

Symbol	Parameter	Min	Max	Units	Notes
t_{over}	Overshoot/Undershoot Voltage Duration		0.2*tCY	ns	1
t_{ring}	Ring back		Vih / Vil	V	
$t_{settling}$	Overshoot/Undershoot Settling Time		0.8*tCY	ns	2

NOTES:

1. The duration must be less than 20% of maximum clock period specified.
2. The duration must be less than 80% of maximum clock period specified.
3. Settling time is defined at the point at which the output voltage remains within 10% of the clocks steady-state quiescent voltage.

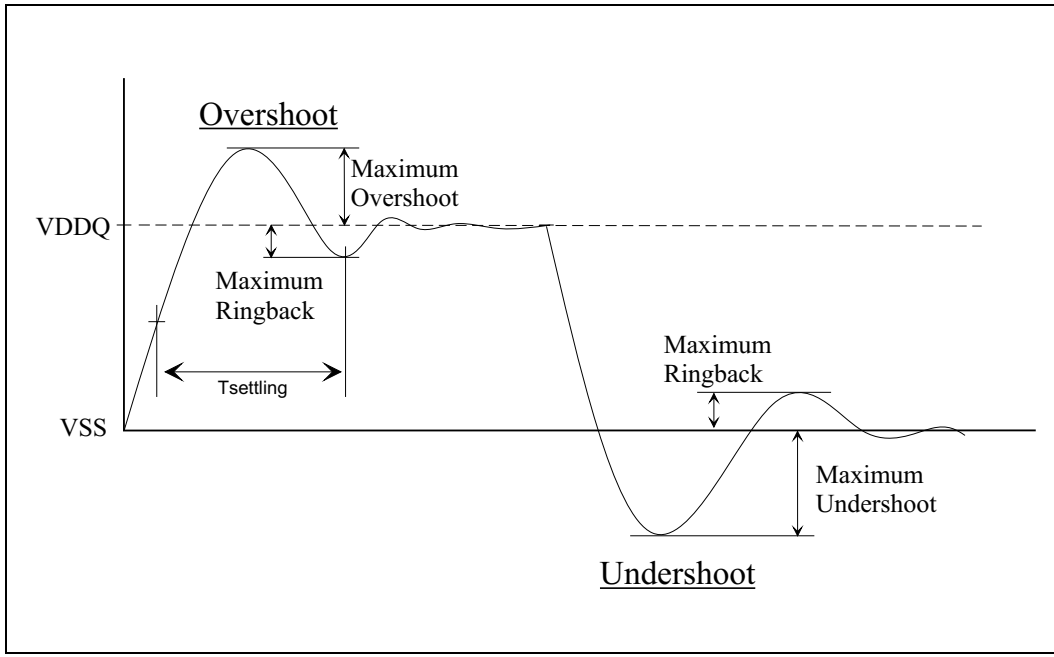


Figure 16. Overshoot & Undershoot

6.0. HOW TO OBTAIN REFERENCE MATERIAL

6.1. PCI Reference

The PCI Special Interest Group is an industry-wide group that controls the official PCI specification. You can obtain the latest copies of the PCI specification by contacting the PCI Special Interest Group at the following numbers:

(800) 433-5177 - USA
(503) 797-4297 - International
(503) 234-6762 - Fax

There is a nominal fee for obtaining this specification.

6.2. IBIS Reference

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are on-line at "vhdl.org". To join in the email discussions, send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

To download a copy of the specification, the golden parser, various public-domain models, the IBIS Overview in PostScript, and other information, either phone in by modem or use FTP.

FTP: (IP address 198.31.14.3)
login as "anonymous"
password is your email address

Modem: (408) 945-4170
login as "guest"
password is your email address

IBIS-related files are in the directory "/pub/ibis" and its sub-directories.

To get documents by email, send an email message to "archive@vhdl.org" with the following commands in the message body:

path <your_email_address>
send docs <name_of_document>

For direct modem access, dial-up to the vhdl.org system at (408) 945-4170. You can use any baud rate up to 14,400, any parity, start and stop bits, and any v.* settings. Log in using the "guest" account. Simple UNIX commands such as "cd", "ls", and "cat" are available and you can download files using "kermit", "zmodem", or "sz" (another zmodem application).

For Internet access, use "ftp vhdl.org" (or "ftp 198.31.14.3") and log in as user "anonymous". The gopher utility is available and highly recommended. Gopher to "vhdl.org". Set "binary" mode for transferring binary files (*.doc, *.fm, *.xls).

The IBIS specification and overview are also available from Intel's AMO APPS BBS, via modem dial-up to (916) 356-3600.

The IBIS home page can be found at **http://www.eia.org/eig/ibis/ibis.htm**

7.0. APPENDICES

7.1. Appendix A: Suggested pinout requirements

The following Addendum defines a generic pinout and base requirements for Pentium® II processor-based desktop platforms and mobile systems. This addendum can also be used as an example for development of other custom clock synthesizer/driver components. This is not the only solution that can be derived.

Features (48 pin Package):

- Four Copies of CPU Clock @ 66.66MHz, 60MHz - selectable
- Eight Copies of PCI Clock (Sync. CPU Clock/2)
- One Copy of IOAPIC Clock @14.31818 Mhz (Shared CPU / IOAPIC)
- One 24 Mhz (3.3V TTL)
- Two 48 Mhz (3.3V TTL)
- Three copies of Ref. Clock @14.31818 Mhz
- Ref. 14.31818MHz Xtal Oscillator Input
- PCICLK_EN, CPUCLK_EN and PWR_DWN# modes for Mobile support
- Test Mode support
- Package Type SSOP: 48 pin

CLK Synth Symbol:

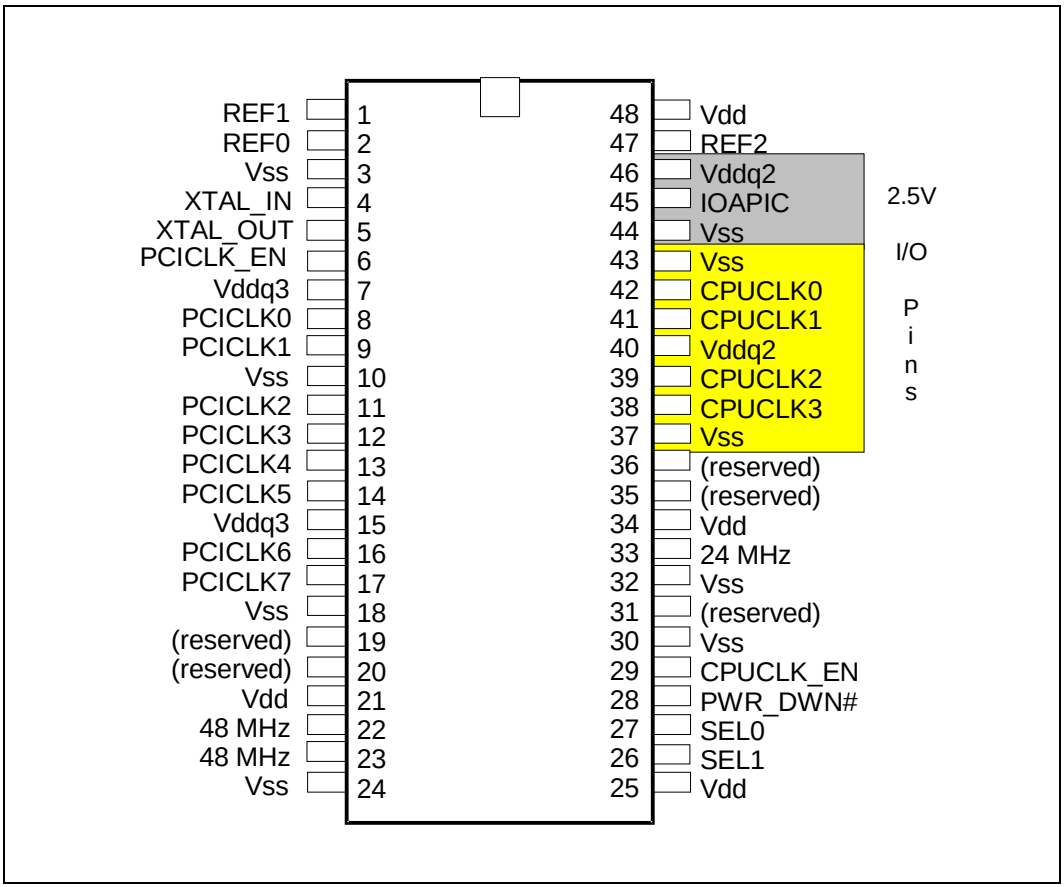


Table 15. Pin Description Table

Pin	Type	Qty	Symbol	Description
2, 1, 47	output	3	REF0, REF1, REF2	14.318 Mhz Clock outputs
8, 9, 11, 12, 13, 14, 16, 17	output	8	PCICLK	PCI Clock outputs TTL compatible 3.3V.
33	output	1	24 MHz	24 Mhz clock output 3.3V
22, 23	output	2	48 MHz	48 Mhz Universal Serial Bus / SIO clock outputs 3.3V
42, 41, 39, 38	output	4	CPUCLK	CPU and Host clock outputs 2.5V outputs.
45	output	1	IOAPIC	IOAPIC / CPU clock output 2.5V
27, 26	input	2	SEL0, SEL1	Clock select inputs
4	input	1	XTAL_IN	Crystal input
5	output	1	XTAL_OUT	Crystal output
29	input	1	CPUCLK_EN	CPUCLK_EN active high, Asynchronous, stops all CPU clock outputs in low state. On/Off latency of 4 clocks max.
6	input	1	PCICLK_EN	PCICLK_EN active high, Asynchronous, stops all the PCI clocks in a low state. On/Off latency of 4 PCI clocks max.
28	input	1	PWR_DWN#	PWR_DWN# active low, Asynchronous, stops all clocks in a low state and puts the part into static leakage (e.g. all VCOs stopped, Crystal oscillation stopped. Clock re-enable latency of </= 3mS required.
21, 25, 34, 48	Power	4	Vdd	Core Power supply
7, 15	Power	2	Vddq3	3.3V I/O Power Supply
40, 46	Power	2	Vddq2	2.5V I/O Power Supply
3, 10, 18, 24, 30, 32, 37, 43, 44	Ground	9	Vss	Ground
19, 20, 31, 35, 36	reserved	5	reserved	reserved

Table 16. Function Table

Inputs			Outputs					
Sel1	**Sel0**	**X1**	**Host**	**PCI**	**Ref**	**IOAPIC**	**24 MHz**	**48 MHz**
0	0	14.318[2]	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	14.318[2]	60	HCLK/2	14.318[2]	14.3182	24	48[3]
1	0	14.318[2]	66	HCLK/2	14.318[2]	14.3182	24	48[3]
1	1	TCLK[1]	TCLK/2	TCLK/4	TCLK	TCLK	TCLK/4	TCLK/2

NOTES:

1. TCLK is a test clock over driven on the X1 inputs during test mode.
2. Range of reference frequency allowed is min = 14.316 nominal = 14.31818 Mhz, max = 14.32 Mhz.
3. 48 and 24 Mhz outputs required to be +167 PPM to conform with USB default. Failure to comply with requirement requires a BIOS change which is determined to be unacceptable.

Table 17. Clock Enable Configuration

PWR_DWN#	CPUCLK_EN	PCICLK_EN	CPUCLK	PCICLK	Other Clocks	Crystal	VCO's
0	X	X	low	low	low	off	off
1	0	0	low	low	running	running	running
1	0	1	low	33/30 MHz	running	running	running
1	1	0	66/60 MHz	low	running	running	running
1	1	1	66/60 MHz	33/30 MHz	running	running	running

Clock sequencing must always guarantee full clock timing parameters at all times after the system has initially powered up except where noted. During power up and power down operations using the PWR_DWN# select pin, partial clocks are not allowed and all clock timing parameters must be met except for the following: It is understood that the first clock pulse coming out of a stoped clock condition could be slightly distorted due to clock network charging requirements. It is also understood that board routing and signal loading have a large impact on the initial clock distortion.

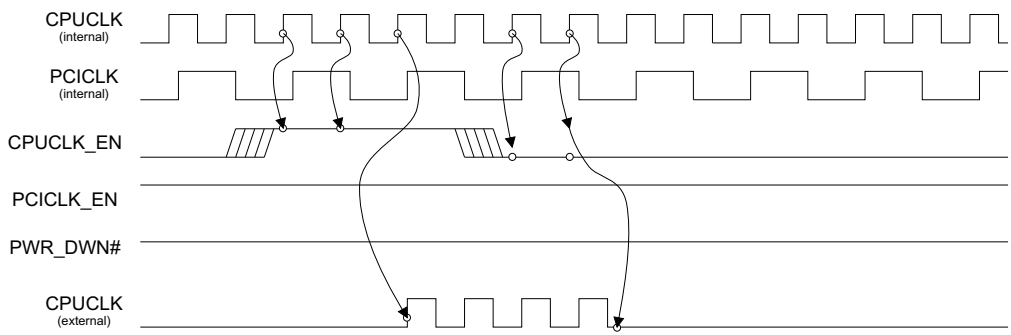
Table 18. Power Management Requirements

Signal	Signal State	Latency
		No. of rising edges of free running PCICLK
CPUCLK_EN	0 (disabled)	1
	1 (enabled)	1
PCICLK_EN	0 (disabled)	1
	1 (enabled)	1
PWR_DWN#	1 (normal operation)	3 mS
	0 (power down)	2 max.

NOTES:

1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high) to when the first valid clocks are driven from the device.

CPUCLK_EN is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPUCLK_EN is required to be synchronized by the clock synthesizer. The minimum that the CPU clock is enabled (CPUCLK_EN high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. CPU clock on latency needs to be less than 4 CPU clocks and CPU clock off latency needs to be less than 4 CPU clocks.

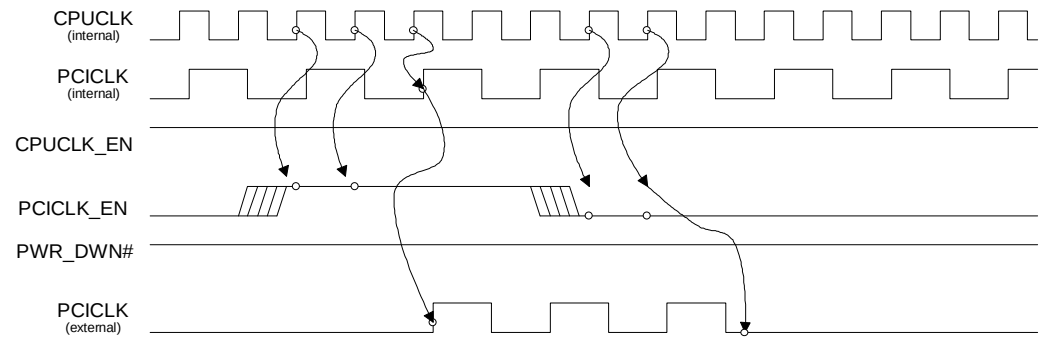


NOTES:

1. All timing is referenced to the CPUCLK
2. The Internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. CPUCLK_EN is an asynchronous input and metastable conditions could exist. This signal is required to be synchronized inside the part.
4. All other clocks continue to run undisturbed.
5. PWR_DWN# and PCICLK_EN are shown in a high state.

Figure 17. CPUCLK_EN# Timing Diagram

PCICLK_EN is an asynchronous input to the clock synthesizer. It is used to turn off the PCI clocks for low power operation. PCICLK_EN is required to be synchronized by the clock synthesizer. The minimum that the PCICLKs are enabled (PCICLK_EN high pulse) is at least 10 PCI clocks. PCI clocks are required to be stopped in a low state and started such that a full high pulse width is guaranteed. PCI clock on latency needs to be less than 4 CPU clocks and PCI clock off latency needs to be less than 4 clocks.

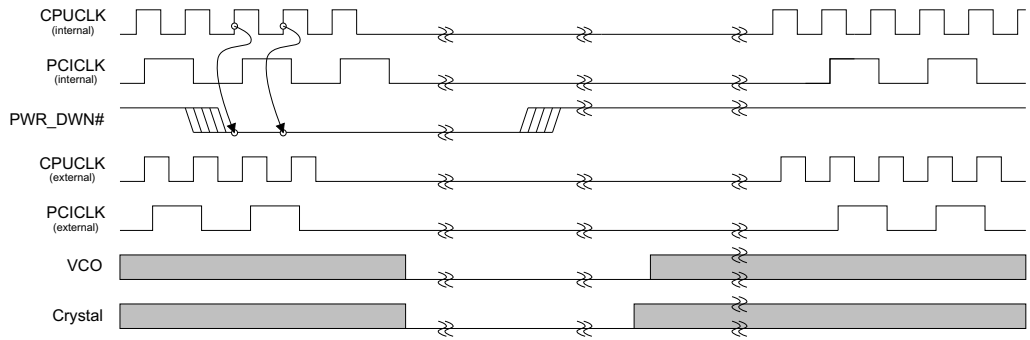


NOTES:

1. All timing is referenced to the CPUCLK
2. Internal means inside the chip
3. PCICLK_EN is an asynchronous input and metastable conditions could exist. This signal is required to be synchronized inside the part.
4. All other clocks continue to run undisturbed.
5. PWR_DWN# and CPUCLK_EN are shown in a high state.

Figure 18. PCICLK_EN# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PWR_DWN# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PWR_DWN# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PWR_DWN# is active low all clocks need to be driven to a low value and held prior to turning off the VCO's and the Crystal. The power on latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCICLK_EN and CPUCLK_EN are considered to be don't cares during the power down operations.



NOTES:

1. All timing is referenced to the CPUCLK
2. Internal means inside the chip
3. PWR_DWN is an asynchronous input and metastable conditions could exist. This signal is required to be synchronized inside the part.
4. The Shaded sections on the VCO and the Crystal signals indicate an active clock

Figure 19. PWR_DWN# Timing Diagram

7.2. Appendix B: 48 pin SSOP Package Data

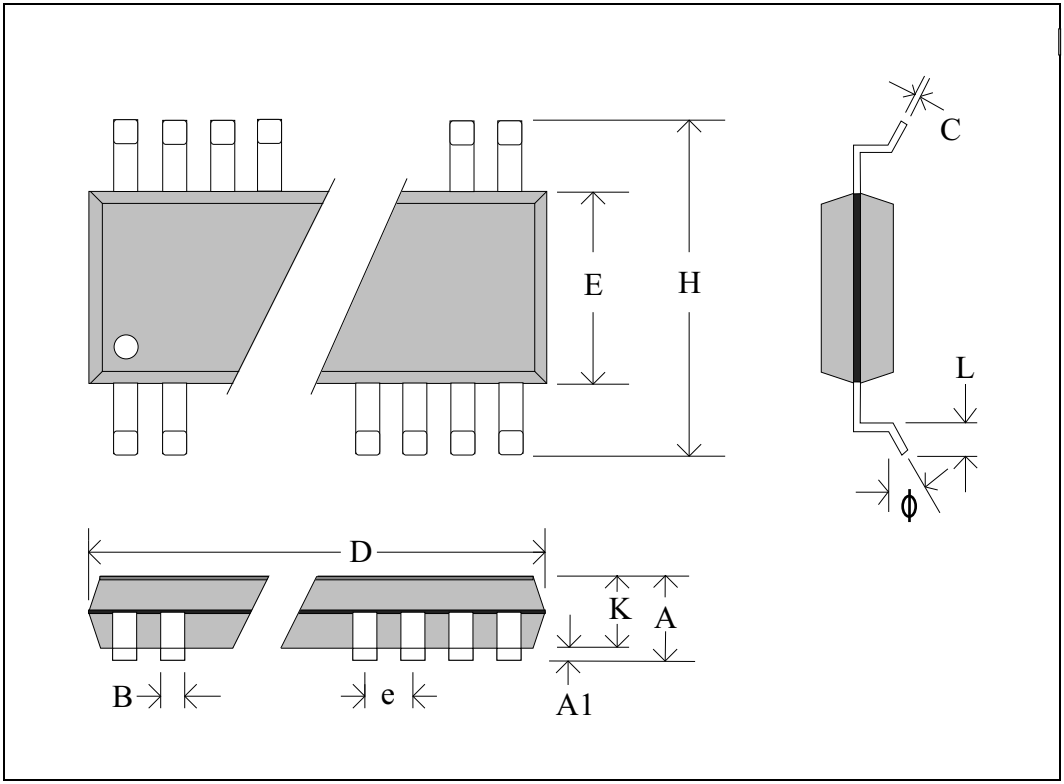


Table 19. Table of Dimensions (inches, unless otherwise specified)

Body		Symbol										
		E	**H**	**C**	**L**	**ϕ**	**D**	**K**	**A**	**A1**	**e**	**B**
48	Min	0.290	0.394	0.009	0.020	0°	0.620	-	0.092	0.004	0.025	0.008
(300mil)	Max	0.300	0.420	0.013	0.040	8°	0.630	-	0.110	0.012		0.012